SYNCFLASH® MEMORY

MT28S4M16LC
1 Meg x 16 x 4 banks

FEATURES

- 100 MHz SDRAM-compatible read timing
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access
- Programmable burst lengths: 1, 2, 4, 8, or full page (READ)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
  – Additional V_{HH} hardware protect mode (RP#)
- Four-bank architecture supports true concurrent operations with zero latency:
  Read from any bank while performing a PROGRAM or ERASE operation to any other bank
- Deep power-down mode: 300µA maximum
- Cross-compatible Flash memory command set
- Industry-standard, SDRAM-compatible pinouts
  – Pins 36 and 40 are no connects for SDRAM

OPTIONS — MARKING

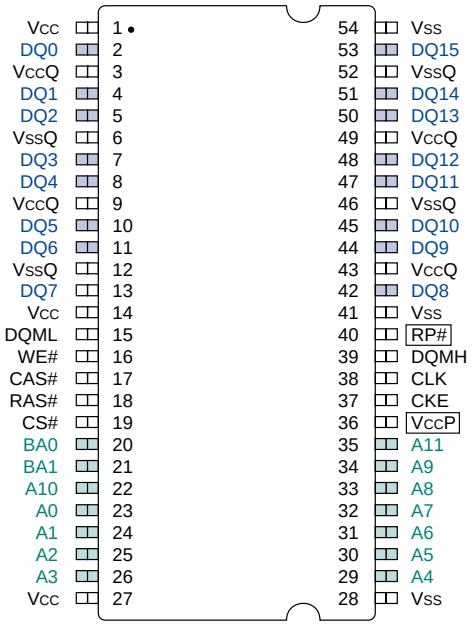
- Configuration
  4 Meg x 16 (1 Meg x 16 x 4 banks) — 4M16
- Read Timing (Cycle Time)
  10ns (100 MHz) — -10
  12ns (83 MHz) — -12
- Package
  54-pin OCPL[1] TSOP II (400 mil) — TG
- Operating Temperature Range
  Commercial Temperature (0°C to +70°C) — None

NOTE: 1. Off-center parting line

Part Number Example:
MT28S4M16LCTG-10

PIN ASSIGNMENT (Top View)

54-Pin TSOP II



NOTE: The # symbol indicates signal is active LOW.

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 2*	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-10	100 MHz	–	7ns	3ns	2ns
-10	66 MHz	9ns	–	3ns	2ns
-12	83 MHz	–	9ns	3ns	2ns
-12	66 MHz	10ns	–	3ns	2ns

*CL = CAS (READ) latency

GENERAL DESCRIPTION

This SyncFlash® data sheet is divided into two major sections. The SDRAM Interface Functional Description details compatibility with the SDRAM memory, and the Flash Memory Functional Description specifies the symmetrical-sectored flash architecture functional commands.

The MT28S4M16LC is a nonvolatile, electrically sector-erasable (Flash), programmable memory containing 67,108,864 bits organized as 4,194,304 words (16 bits). SyncFlash memory is ideal for 3.3V-only platforms that require both hardware and software protection modes. Additional hardware protection modes are

GENERAL DESCRIPTION (continued)

also available when V_{HH} is applied to the RP# pin. Programming or erasing the device is done with a 3.3V $V_{CC}P$ voltage, while all other operations are performed with a 3.3V V_{CC}. The device is fabricated with Micron's advanced CMOS floating-gate process.

The MT28S4M16LC is organized into 16 independently erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28S4M16LC features sixteen 256K-word hardware- and software-lockable blocks.

The MT28S4M16LC four-bank architecture supports true concurrent operations. A read access to any bank can occur simultaneously with a background PROGRAM or ERASE operation to any other bank.

The SyncFlash memory has a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read accesses to the memory are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ command are used to select the starting column location for the burst access.

The SyncFlash memory provides for programmable read burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option.

The 4 Meg x 16 SyncFlash memory uses an internal pipelined architecture to achieve high-speed operation.

The 4 Meg x 16 SyncFlash memory is designed to operate in 3.3V, low-power memory systems. A deep power-down mode is provided, along with a power-saving standby mode. All inputs and outputs are LVTTL-compatible.

SyncFlash memory offers substantial advances in Flash operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation and the capability to randomly change column addresses on each clock cycle during a burst access.

Please refer to Micron's Web site (www.micron.com/flash) for the latest data sheet.

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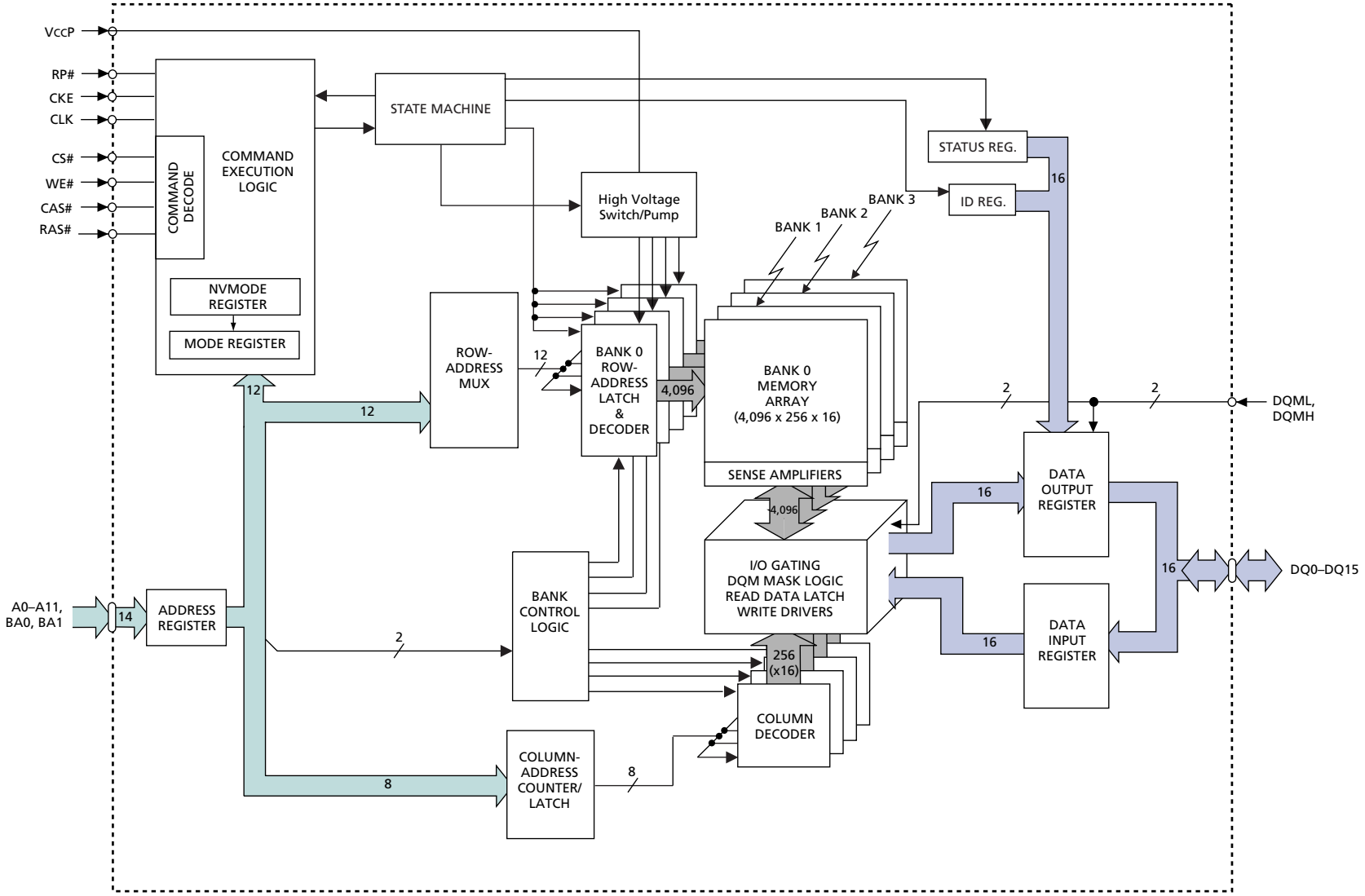
FUNCTIONAL BLOCK DIAGRAM
4 Meg x 16



PIN DESCRIPTIONS

54-PIN TSOP NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	CLK	Input	Clock: CLK is driven by the system clock. All SyncFlash memory input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides STANDBY operation or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down modes, providing low standby power. CKE may be tied HIGH in systems where power-down modes (other than RP# deep power-down) are not required.
19	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
18, 17, 16	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
15, 39	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0–DQ7 and DQMH corresponds to DQ8–DQ15. DQML and DQMH are considered same state when referenced as DQM.
23-26, 29-34, 22, 35	A0–A11	Input	Address Inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A7) to select one location in the respective bank. The address inputs provide the Op-Code during LOAD MODE REGISTER command and the operation code during a LOAD COMMAND REGISTER command.
40	RP#	Input	Initialize/Power-Down: Upon initial device power-up, a 100µs delay after RP# has transitioned from LOW to HIGH is required for internal device initialization, prior to issuing an executable command. RP# clears the status register, sets the internal state machine (ISM) to the array read mode, and places the device in the deep power-down mode when LOW. All inputs, including CS#, are "Don't Care" and all outputs are High-Z. When RP# = V_{HH}, all protection modes are ignored during PROGRAM and ERASE. Also allows the device protect bit to be set to "1" (protected) and allows the block protect bits at locations 0 and 15 to be set to "0" (unprotected) when brought to V_{HH}. RP# must be held HIGH during all other modes of operation.

(continued on next page)

PIN DESCRIPTIONS (continued)

54-PIN TSOP NUMBERS	SYMBOL	TYPE	DESCRIPTION
20, 21	BA0, BA1	Input	Bank Address Input(s): BA0, BA1 define to which bank the command is being applied. See Truth Tables 1 and 2.
2, 4, 5, 7, 8, 10, 11,13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0-DQ15	I/O	Data I/O: Data bus.
3, 9, 43, 49	VccQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
6, 12, 46, 52	VssQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 14, 27	Vcc	Supply	Power Supply: 3.3V ±0.3V.
28, 41, 54	Vss	Supply	Ground.
36	VccP	Supply	Program/Erase Supply Voltage: VccP must be tied externally to Vcc. The VccP pin sources current during device initialization, PROGRAM and ERASE operations.

SDRAM INTERFACE FUNCTIONAL DESCRIPTION

In general, the 64Mb SyncFlash memory (1 Meg x 16 x 4 banks) is configured as a quad-bank, nonvolatile SDRAM that operates at 3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits.

Read accesses to the SyncFlash memory are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A11 select the row). The address bits registered coincident with the READ command are used to select the starting column location for the burst access (BA0 and BA1 select the bank, A0–A7 select the column).

Prior to normal operation, the SyncFlash memory must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

SyncFlash memory must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. After power is applied to V_{CC}, $V_{CC}Q$, and $V_{CC}P$ (simultaneously), and the clock is stable, RP# must be brought from LOW to HIGH. A 100µs delay is required after RP# transitions HIGH in order to complete internal device initialization.

The SyncFlash memory is now in the array read mode and ready for mode register programming or an executable command. After initial programming of the nvmode register, the contents are automatically loaded into the mode register during initialization and the device will power up in the programmed state.

Register Definition

MODE REGISTER

The mode register is used to define the specific mode of operation of the SyncFlash memory. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 1. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is reprogrammed. The contents of the mode register may be copied into the nvmode register; the mode register settings automatically load the mode register during initialization. Details on erase nvmode register and program nvmode register command sequences are found in the Command Execution section of the Flash Memory Functional Description.

Mode register bits M0–M2 specify the burst length, M3 specifies the burst type (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode in an SDRAM (M9 = 1 by default), and M10 and M11 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

BURST LENGTH

Read accesses to the SyncFlash memory are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ command. Burst lengths of 1, 2, 4, or 8 locations are available for both sequential and interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A7 when the burst length is set to two, by A2–A7 when the burst length is set to four, and by A3–A7 when the burst length is set to eight. The remaining (least significant) address bit(s) are used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 1.

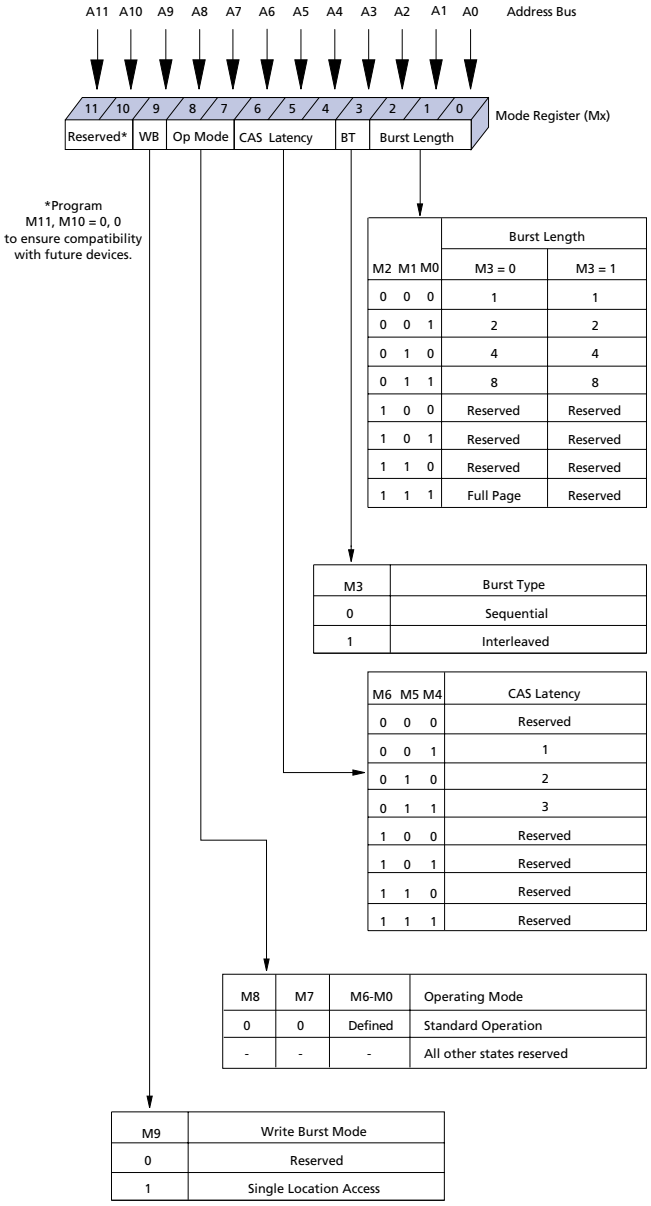


Figure 1
Mode Register Definition

Table 1
Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type=Sequential	Type=Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page 256	n = A0–A7 (location 0-255)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... …Cn-1, Cn...	Not supported

NOTE:
1. For a burst length of two, A1–A7 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2–A7 select the block-of-four burst; A0–A1 select the starting column within the block.
3. For a burst length of eight, A3–A7 select the block-of-eight burst; A0–A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0–A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0–A7 select the unique column to be accessed, and mode register bit M3 is ignored.

SDRAM

CAS LATENCY

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1) and, provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0, and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

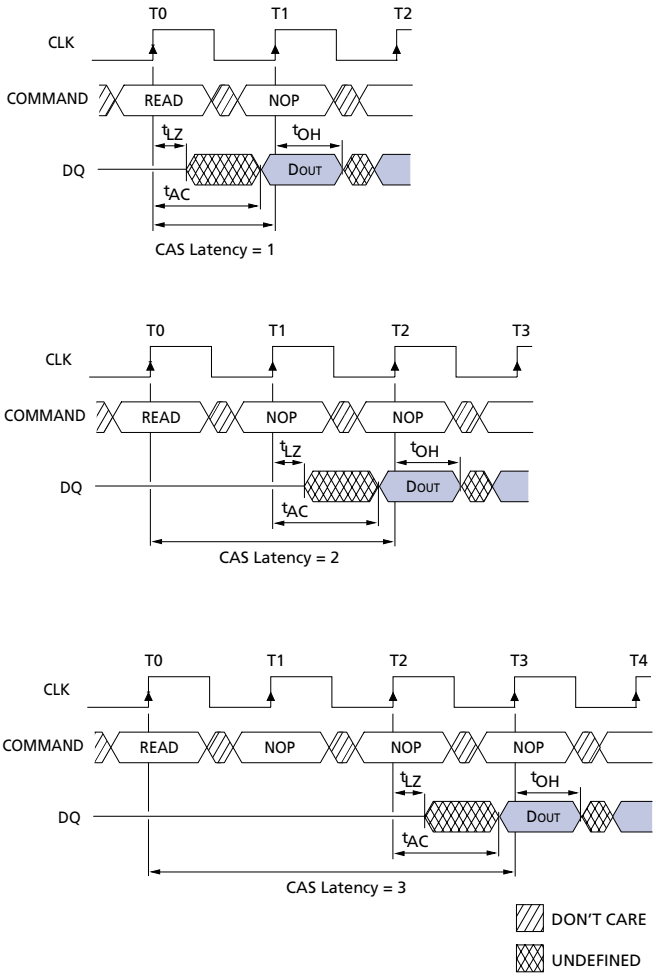


Figure 2
CAS Latency

OPERATING MODE

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to READ bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

WRITE BURST MODE

WRITE bursts are not supported with the MT28S4M16LC. By default, M9 is set to "1" and write accesses are single-location (nonburst) accesses.

Table 2
CAS Latency

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)		
	CAS LATENCY = 1	CAS LATENCY = 2	CAS LATENCY = 3
-10	≤33	≤66	≤100
-12	≤33	≤66	≤83

COMMANDS

Truth Table 1 provides a quick reference of available commands for SDRAM-compatible operation. This is followed by a written description of each command. Additional truth tables appear later.

TRUTH TABLE 1
SDRAM-COMPATIBLE INTERFACE COMMANDS AND DQM OPERATION

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	2
READ (Select bank, column and start READ burst)	L	H	L	H	X	Bank/Col	X	3
WRITE (Select bank, column and start WRITE)	L	H	L	L	X	Bank/Col	Valid	3, 4
BURST TERMINATE	L	H	H	L	X	X	Active	
ACTIVE TERMINATE	L	L	H	L	X	X	X	5
LOAD COMMAND REGISTER	L	L	L	H	X	ComCode	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	OpCode	X	8
Write Enable/Output Enable	–	–	–	–	L	–	Active	9
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	9

NOTE:
1. CKE is HIGH for all commands shown.
2. A0–A11 provide row address, and BA0 and BA1 determine which bank is made active.
3. A0–A7 provide column address, and BA0 and BA1 determine which bank is being read from or written to.
4. A program setup command sequence (see Truth Table 2) must be completed prior to executing a WRITE.
5. ACTIVE TERMINATE is functionally equivalent to the SDRAM PRECHARGE command, however PRECHARGE (deactivate row in bank or banks) is not required for SyncFlash memory. A10 LOW: BA0 and BA1 determine the bank being active terminated. A10 HIGH: All banks active terminated and BA0 and BA1 are "Don't Care."
6. A0–A7 define the ComCode, and A8–A11 are "Don't Care" for this operation. See Truth Table 2.
7. LOAD COMMAND REGISTER (LCR) replaces the SDRAM AUTO REFRESH or SELF REFRESH command, which is not required for SyncFlash memory. LCR is the first cycle for Flash memory command sequences. See Truth Table 2.
8. A0–A11 define the OpCode written to the mode register. The mode register can be dynamically loaded each cycle, provided ^{t}MRD is satisfied. The contents of the nvmode register are automatically loaded into the mode register during device initialization.
9. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMANDS

Truth Table 2 provides a quick reference of available commands for flash memory interface operation. A written description of each command is found in the Flash Memory Functional Description section.

TRUTH TABLE 2
FLASH MEMORY COMMAND SEQUENCES

(Notes: 1, 2, 3, 4, 5; see notes on the next page.)

	FIRST CYCLE					SECOND CYCLE					THIRD CYCLE					
OPERATION	CMD	ADDR[6]	BANK ADDR	DQ	RP#	CMD[7]	ADDR	BANK ADDR	DQ	RP#	CMD	ADDR	BANK ADDR	DQ[8]	RP#	NOTES
READ DEVICE CONFIGURATION	LCR	90h	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H	9, 10
READ STATUS REGISTER	LCR	70h	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H	
CLEAR STATUS REGISTER	LCR	50h	X	X	H											
ERASE SETUP/CONFIRM	LCR	20h	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	D0h	H/V_{HH}	11, 12, 13
PROGRAM SETUP/PROGRAM	LCR	40h	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	D_{IN}	H/V_{HH}	11, 12, 13
PROTECT BLOCK/CONFIRM	LCR	60h	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	01h	H/V_{HH}	11, 12, 13, 14
PROTECT DEVICE/CONFIRM	LCR	60h	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	F1h	V_{HH}	11, 12
UNPROTECT BLOCKS/CONFIRM	LCR	60h	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	D0h	H/V_{HH}	11, 12, 13, 15
ERASE NVMODE REGISTER	LCR	30h	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	C0h	H	11, 12
PROGRAM NVMODE REGISTER	LCR	A0h	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	X	H	11, 12

NOTE:
1. CMD = Command: Decoded from CS#, RAS#, CAS#, and WE# inputs.
2. NOP/COMMAND INHIBIT commands may be issued throughout any operation command sequence.
3. After a PROGRAM or ERASE operation is registered to the ISM and prior to completion of the ISM operation, a READ to any location in the bank under ISM control will output the contents of the row activated prior to the LCR/active/write sequence (see Note 7).
4. In order to meet the ^{t}RCD specification, the appropriate number of NOP/COMMAND INHIBIT commands must be issued between ACTIVE and READ/WRITE commands.
5. The ERASE, PROGRAM, PROTECT, UNPROTECT operations are self-timed. The status register may be polled to monitor these operations.
6. A8–A11 are "Don't Care."
7. A row will not be opened when ACTIVE is preceded by LCR. ACTIVE is considered a NOP.
8. Data Inputs: DQ8–DQ15 are "Don't Care."
   Data Outputs: All unused bits are driven LOW.
9. The block address is required during ACTIVE and READ cycles for the block protect bit location. The first row in a block should be specified, acceptable values include 000h, 400h, 800h, and C00h. Bank address is "Don't Care" for manufacturer compatibility ID, device ID, and device protect bit location.
10. CA = Configuration Address:
    000h – Manufacturer compatibility ID (2Ch)
    001h – Device ID (D3h)
    x02h – Block protect bit, where x = 0, 4, 8, or Ch
    003h – Device protect bit
11. The proper command sequence (LCR/active/write) is needed to initiate an ERASE, PROGRAM, PROTECT, UNPROTECT operation.
12. The bank address must match for the three command cycles (LCR/ACTIVE/WRITE) to initiate an ERASE, PROGRAM, PROTECT, UNPROTECT operation.
13. If the device protect bit is set, then an ERASE, PROGRAM, PROTECT, UNPROTECT operation can still be initiated by bringing RP# to V_{HH} prior to the WRITE command cycle and holding it at V_{HH} until the operation is completed.
14. The A10, A11 row address and BA0, BA1 bank address select the block to be protected; A0–A9 are "Don't Care."
15. If the device protect bit is not set, RP# = V_{IH} unprotects all sixteen 256K-word erasable blocks, except for blocks 0 and 15. When RP# = V_{HH}, all sixteen 256K-word erasable blocks (including block 0 and 15) will be unprotected, and the device protect bit will be ignored. If the device protect bit is set and RP# = V_{IH}, the block protect bits cannot be modified.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SyncFlash memory, regardless of whether the CLK signal is enabled. The SyncFlash memory is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to a SyncFlash memory that is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0–A11 and BA0 and BA1. See mode register heading in Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met. The data in the nvmode register is automatically loaded into the mode register upon power-up initialization and is the default mode setting unless dynamically changed with the LOAD MODE REGISTER command.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active for accesses until the next ACTIVE command, power-down or RESET.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A7 selects the starting column location. Read data appears on the DQs subject to the logic level on the DQM input two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE

The WRITE command is used to initiate a single-location write access. A WRITE command must be preceded by LRC/ACTIVE. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A7 selects the column location.

Input data appearing on the DQs is written to the memory array, subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that word/column location. A WRITE command with DQM HIGH is considered a NOP.

ACTIVE TERMINATE

ACTIVE TERMINATE, which replaces the SDRAM PRECHARGE command, is not required for SyncFlash memory, but is functionally equivalent to the SDRAM PRECHARGE command. ACTIVE TERMINATE can be issued to terminate a BURST READ in progress and may or may not be bank specific.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ command prior to the BURST TERMINATE command will be truncated as shown in the Operation section of this data sheet. BURST TERMINATE is not bank specific.

LOAD COMMAND REGISTER (LCR)

The LOAD COMMAND REGISTER (LCR) command is used to initiate flash memory control commands to the command execution logic (CEL). The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e., memory array, ID register, or status register). However, there are restrictions on what commands are allowed in this condition. See the Command Execution section of Flash Memory Functional Description for more details.

Operation

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SyncFlash memory, a row in that bank must be "opened." (Note: A row will not be activated for LCR/active/read or LCR/active write command sequences, see the Flash Memory Architecture section for additional information). This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 30ns with a 90 MHz clock (11.11ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 4, which covers any case where 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3 . (The same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can be issued without having to close a previous active row, provided the minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

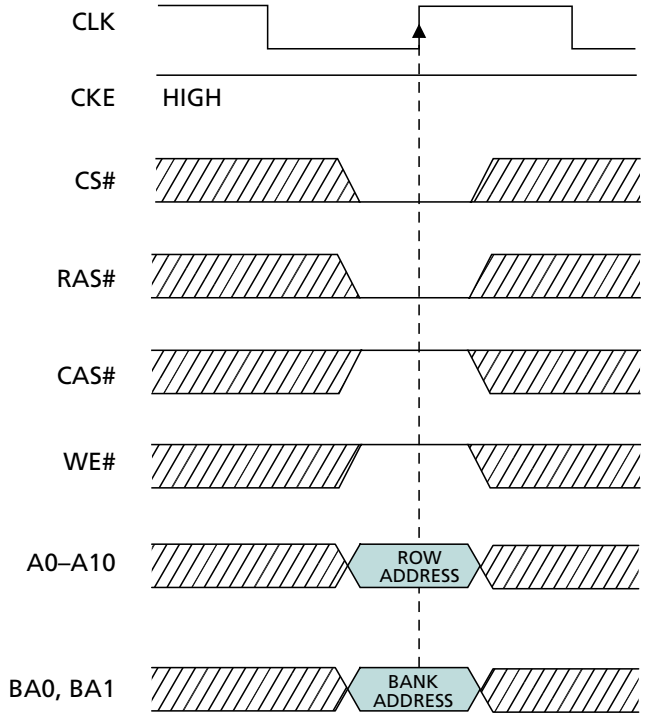


Figure 3
Activating a Specific Row in a Specific Bank

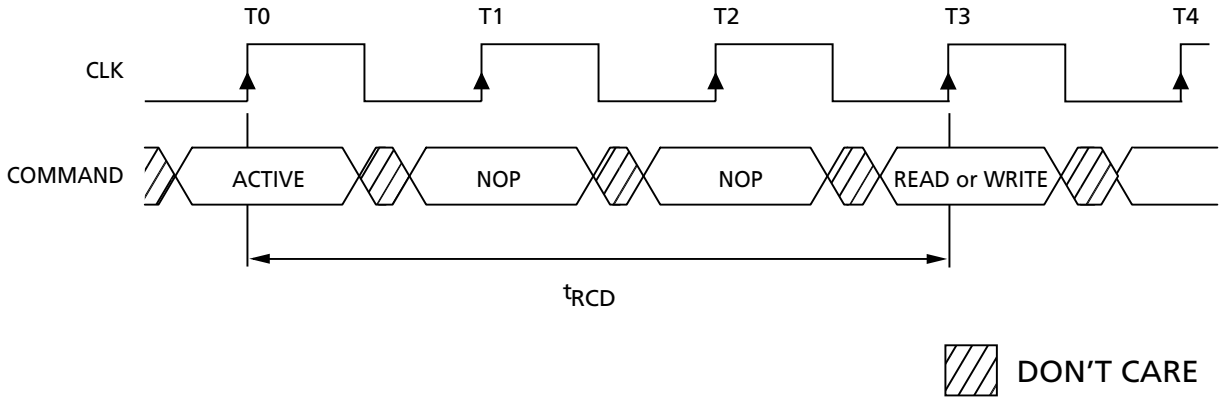


Figure 4
Example: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3

READs

READ bursts are initiated with a READ command, as shown in Figure 5.

The starting column and bank addresses are provided with the READ command.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 6 shows general timing for one, two, and three CAS latency settings.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst, or the last desired data element of a longer burst that is being truncated.

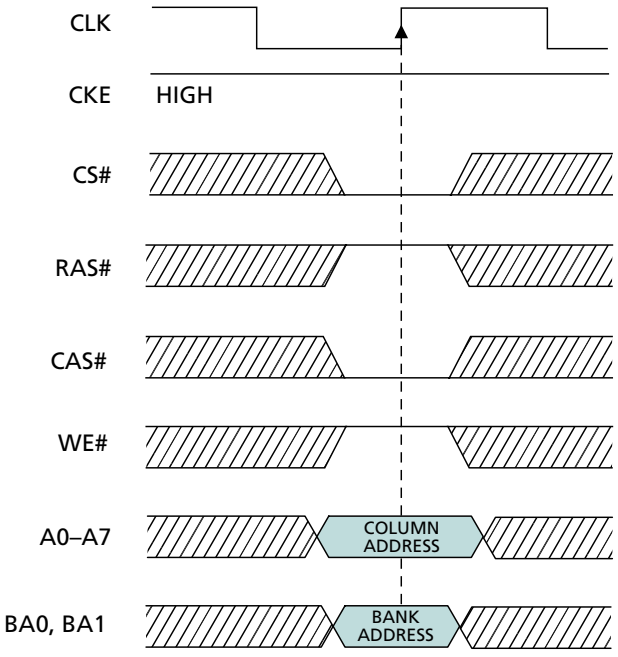


Figure 5
READ Command

The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 7 for CAS latencies of one, two, and three; data element *n* + *3* is either the last of a burst of four, or the last desired of a longer burst. The SyncFlash memory uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed, random read accesses within a page can be performed as shown in Figure 8, or each subsequent READ may be performed to a different bank.

Data from any READ burst may be truncated with a

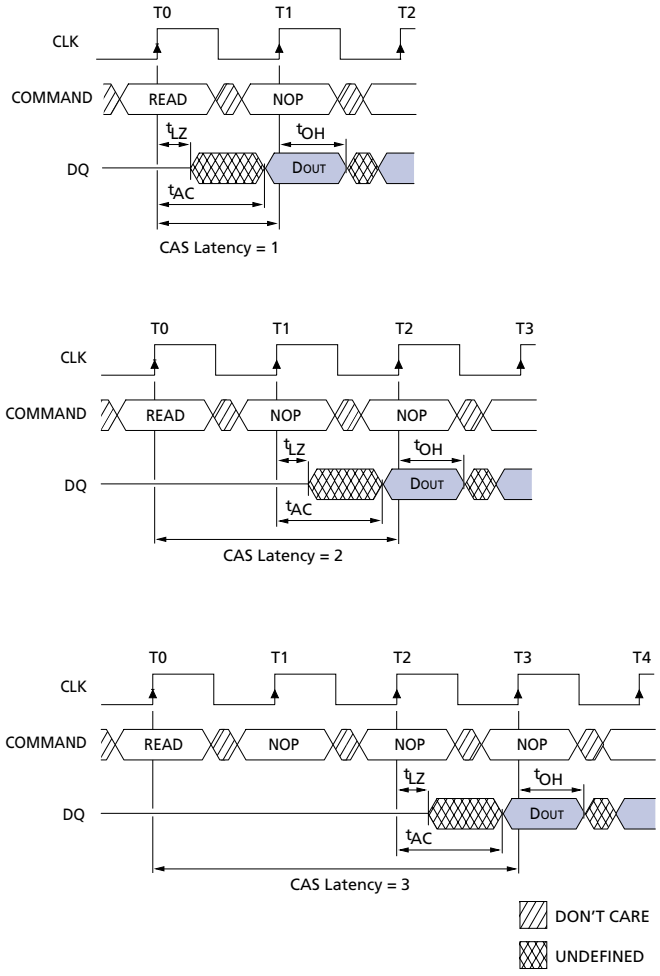
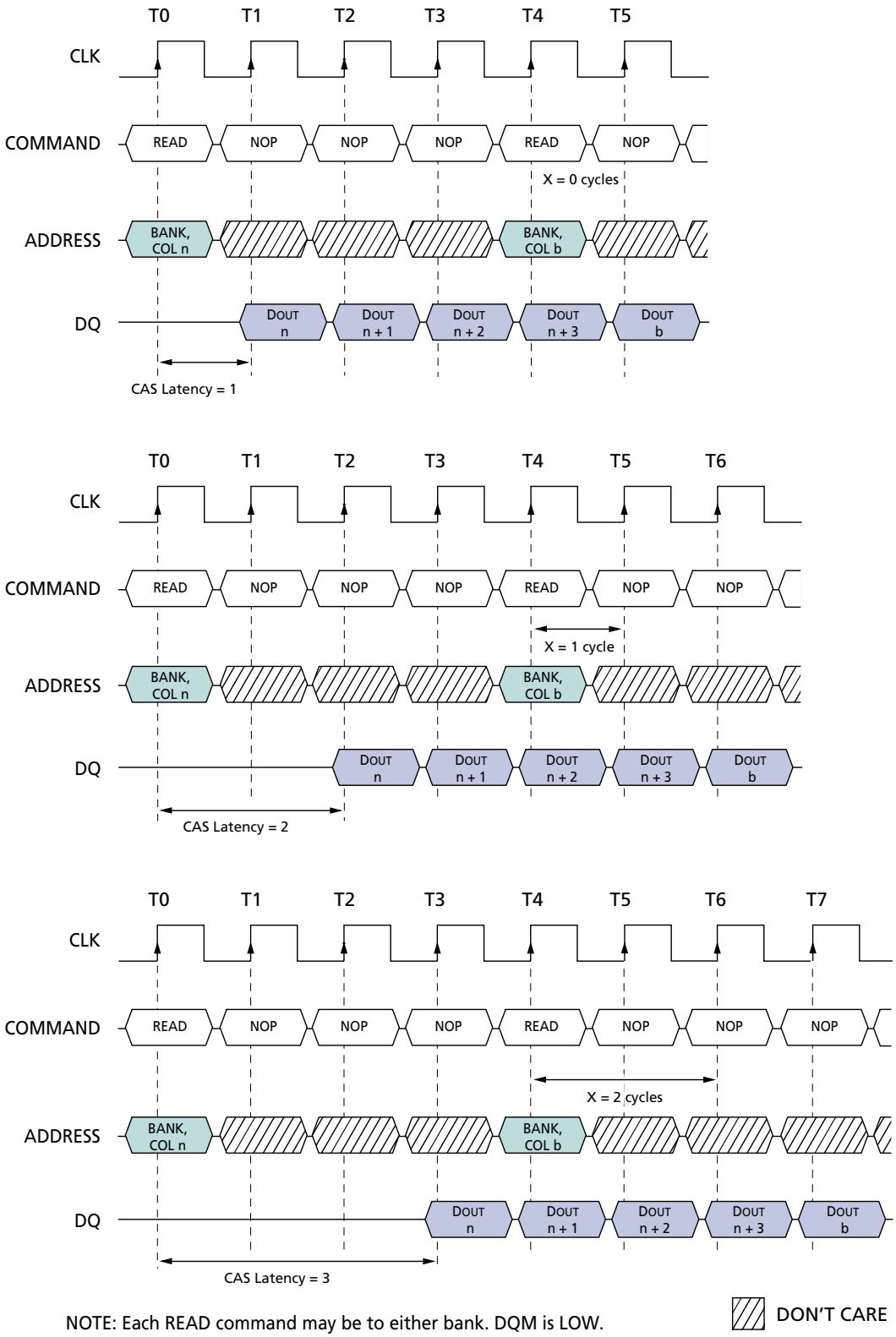
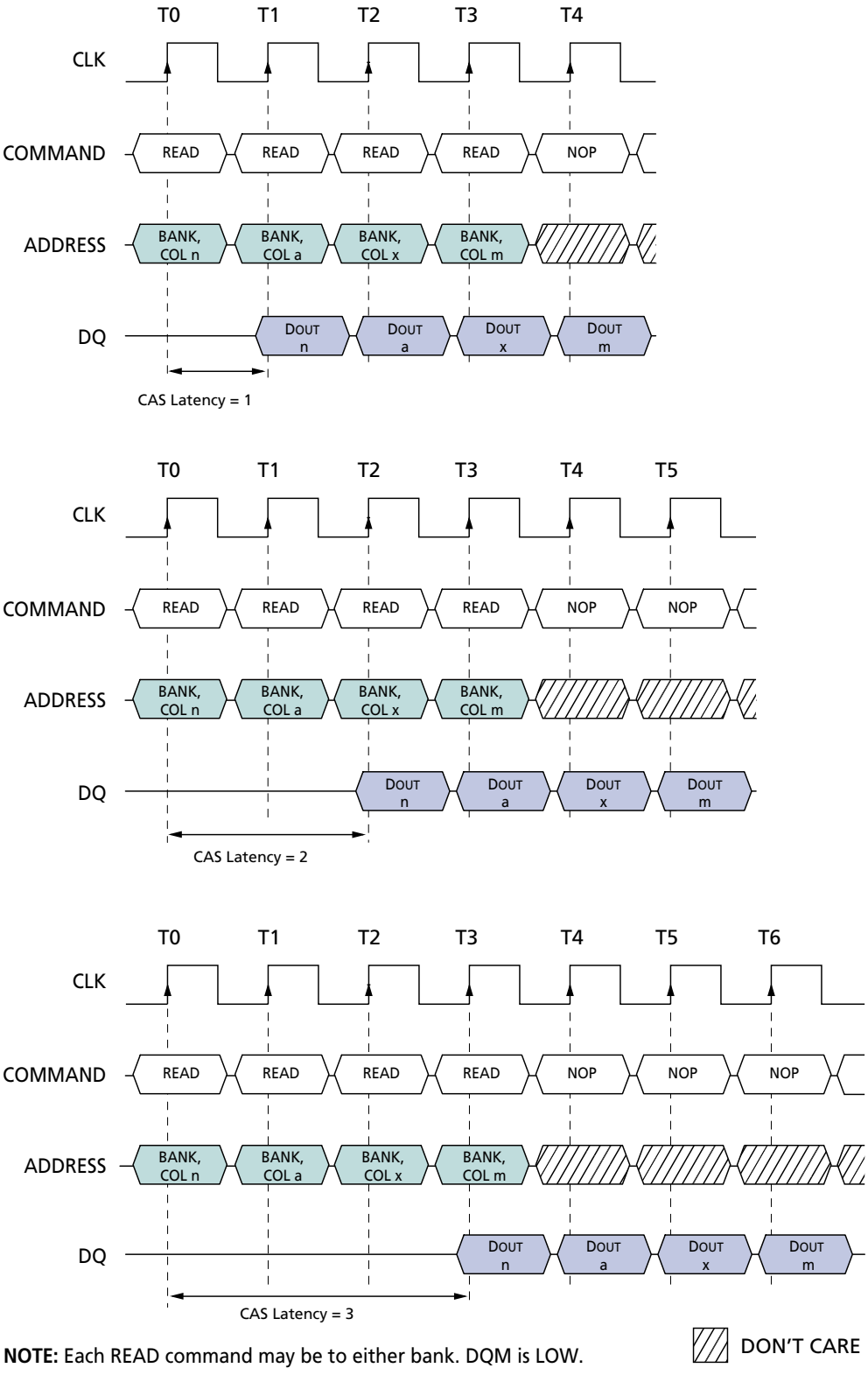


Figure 6
CAS Latency



NOTE: Each READ command may be to either bank. DQM is LOW.

Figure 7
Consecutive READ Bursts



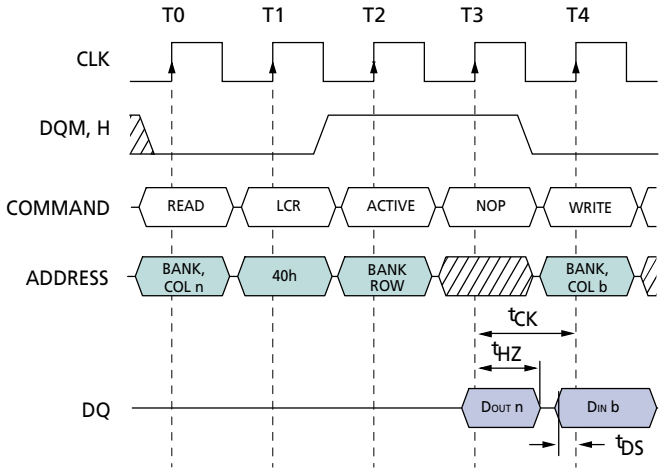
NOTE: Each READ command may be to either bank. DQM is LOW.

Figure 8
Random Read Accesses Within a Page

subsequent WRITE command (WRITE commands must be preceded by LCR/ACTIVE), and data from a fixed-length READ burst may be immediately followed by data from a subsequent WRITE command (subject to bus turnaround limitations). The WRITE may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be the possibility that the device driving the input data would go Low-Z before the SyncFlash memory DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

The DQM input is used to avoid I/O contention as shown in Figure 9. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z) regardless of the state of the DQM signal. The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 9 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle.

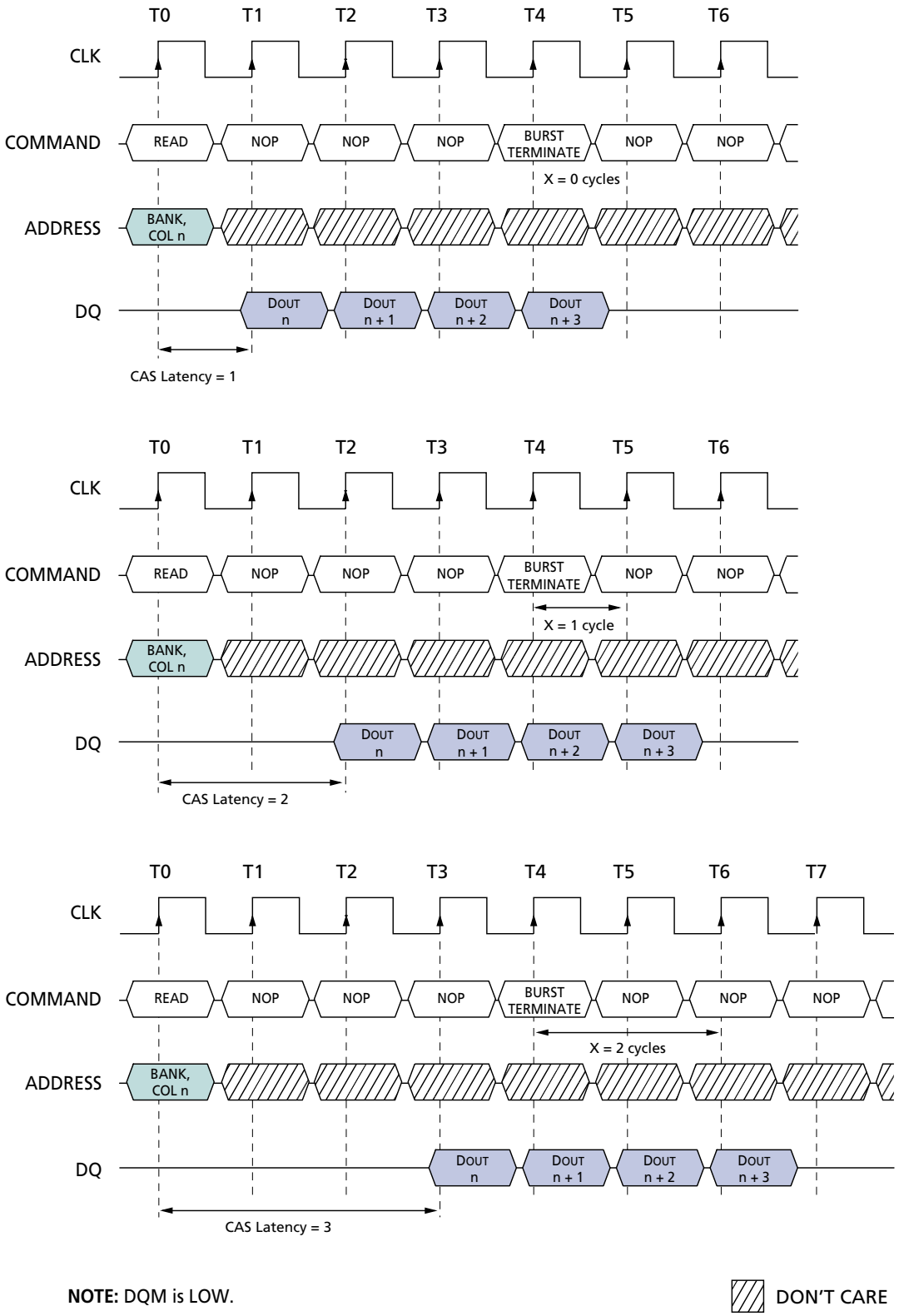
A fixed-length or full-page READ burst can be truncated with ACTIVE TERMINATE (may or may not be bank specific) or BURST TERMINATE (not bank specific). The ACTIVE TERMINATE or BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 10 for each possible CAS latency; data element *n* + *3* is the last desired data element of a burst of four or the last desired of a longer burst.



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

DON'T CARE

Figure 9
READ to WRITE



NOTE: DQM is LOW.

DON'T CARE

Figure 10
Terminating a READ Burst

WRITEs

A single-location WRITE is initiated with a WRITE command (preceded by LCR/ACTIVE, see Truth Table 2), as shown in Figure 11. The starting column and bank addresses are provided with the WRITE command. Once a WRITE command is registered, a READ command can be executed as defined by Truth Tables 4 and 5. An example is shown in Figure 12.

During a WRITE, the valid data-in element will be registered coincident with the WRITE command. Additional details on write sequence operations are found in the Command Execution section.

ACTIVE TERMINATE

The ACTIVE TERMINATE command is functionally equivalent to the SDRAM PRECHARGE command. Unlike SDRAM, SyncFlash does not require a PRECHARGE command to deactivate the open row in a particular bank or the open rows in all banks. Asserting input A10 HIGH during an ACTIVE TERMINATE command will terminate a BURST READ in any bank. When A10 is LOW during an ACTIVE TERMINATE command, BA0 and BA1 will determine which bank will undergo a terminate operation. ACTIVE TERMINATE is considered a NOP for banks not addresssed by A10, BA0, BA1.

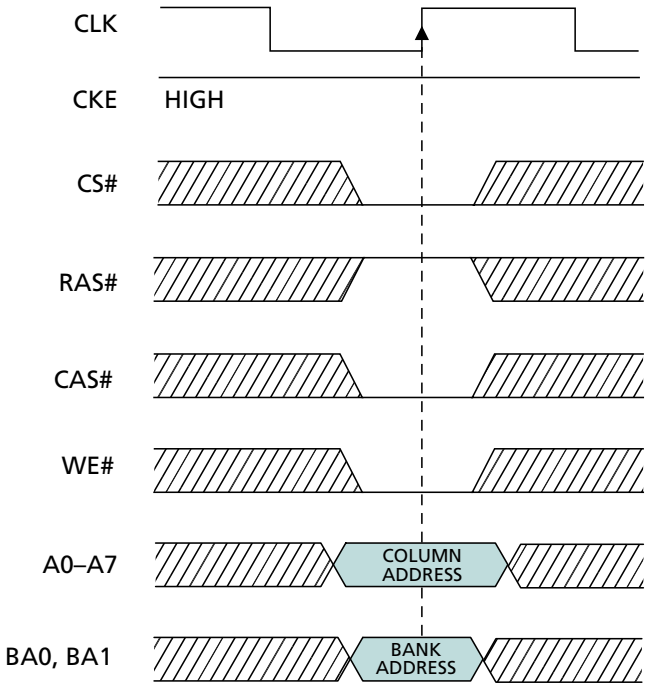
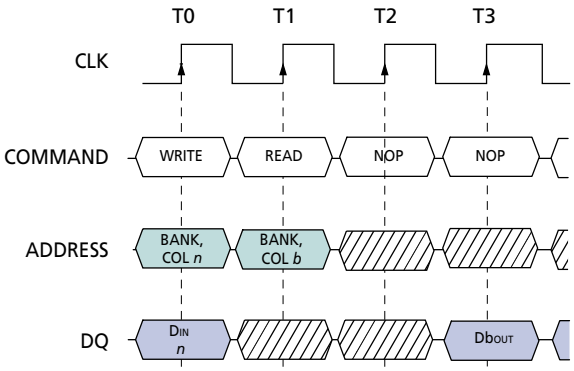


Figure 11
WRITE Command



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. For more details, refer to Truth Tables 4 and 5.

DON'T CARE

Figure 12
WRITE to READ

BURST READ/SINGLE WRITE

The burst read/single write mode is the default mode for the MT28S4M16LC; the write burst mode bit (M9) in the mode register is set to a logic 1. All WRITE commands result in the access of a single column location (burst of one). READ commands access columns according to the programmed burst length and sequence.

POWER-DOWN

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT, when no accesses are in progress. Entering power-down deactivates the input and output buffers (excluding CKE) after ISM operations (including WRITE operations) are completed, for power savings while in standby.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ^{t}CKS).

See the Reset/Deep Power-Down description in the Flash Memory Functional Description for maximum power savings mode.

CLOCK SUSPEND

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored, any data present on the DQ pins remains driven, and burst counters are not incremented, as long as the clock is suspended (see example in Figure 14).

Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

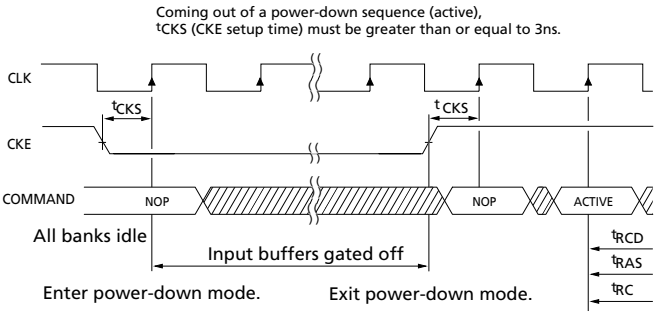
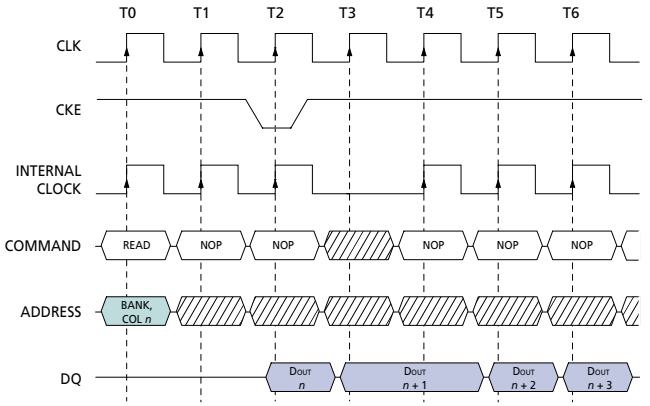


Figure 13
Power-Down



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, and DM is LOW.

Figure 14
Clock Suspend During READ Burst

TRUTH TABLE 3 – CKE

(Notes: 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMMAND_n$	$ACTION_n$	NOTES
L	L	Clock Standby	X	Maintain Clock Standby	
		Clock Suspend	X	Maintain Clock Suspend	
L	H	Clock Standby	COMMAND INHIBIT or NOP	Exit Clock Standby	5
		Clock Suspend	X	Exit Clock Suspend	6
H	L	No Burst in Progress	COMMAND INHIBIT or NOP	Clock Standby	
		Reading	VALID	Clock Suspend	
H	H		See Truth Table 4		

NOTE:
1. "CKE_n" is the logic state of CKE at clock edge *n*; "CKE_{n-1}" was the state of CKE at the previous clock edge.
2. "Current State" is the state of the SyncFlash memory immediately prior to clock edge *n*.
3. "$Command_n$" is the command registered at clock edge *n* and "$Action_n$" is a result of $Command_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting POWER-DOWN at clock edge *n* will put the device in the idle state in time for clock edge *n + 1* (provided that tCKS is met).
6. After exiting CLOCK SUSPEND at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n + 1*.

TRUTH TABLE 4 – CURRENT STATE BANK *n*; COMMAND TO BANK *n*

(Notes: 1-6)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	LOAD COMMAND REGISTER	
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	ACTIVE TERMINATE	8
Row Active	L	H	L	H	READ (Select column and start READ burst)	
	L	H	L	L	WRITE (Select column and start WRITE)	
	L	L	H	L	ACTIVE TERMINATE	8
	L	L	L	H	LOAD COMMAND REGISTER	
Read	L	H	L	H	READ (Select column and start new READ burst)	
	L	L	H	L	ACTIVE TERMINATE	8
	L	H	H	L	BURST TERMINATE	9
	L	L	L	H	LOAD COMMAND REGISTER	
Write	L	H	L	H	READ (Select column and start new READ burst)	10
	L	L	L	H	LOAD COMMAND REGISTER	

NOTE:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 3).
2. This table is bank specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank, when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank is not in read or write mode.
   - Row Active: A row in the bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated and has not yet terminated or been terminated.
   - Write: A WRITE operation has been initiated to the SyncFlash ISM and has not yet completed.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 4, and according to Truth Table 5.
   - Active Terminate: Starts with registration of an ACTIVE TERMINATE command and ends on the next clock cycle. The bank will then be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the row active state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   - Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the SyncFlash memory will be in the all banks idle state.
   - Initialize Mode: Starts with RP# transitioning from LOW to HIGH and ends after 100µs delay.
6. All states and sequences not shown are illegal or reserved.
7. Not bank specific; requires that all banks are idle.
8. May or may not be bank specific.
9. Not bank specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. A READ operation to the bank under ISM control will output the contents of the row activated prior to the LCR/active/write sequence (see Truth Table 2).

TRUTH TABLE 5 – CURRENT STATE BANK *n;* COMMAND TO BANK *m*

(Notes: 1-6)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank *m*	
Row Activating, Active, or Active Terminate	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	
	L	H	L	L	WRITE (Select column and start WRITE)	
	L	L	H	L	ACTIVE TERMINATE	
	L	L	L	H	LOAD COMMAND REGISTER	
Read	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	
	L	L	H	L	ACTIVE TERMINATE	
	L	L	L	H	LOAD COMMAND REGISTER	
Write	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	
	L	L	H	L	ACTIVE TERMINATE	
	L	H	H	L	BURST TERMINATE	
	L	L	L	H	LOAD COMMAND REGISTER	

NOTE:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 3).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank is not in initialize, read, write mode.
   - Row Active: A row in the bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated and has not yet terminated or been terminated.
   - Write: A WRITE operation has been initiated to the SyncFlash ISM and has not yet completed.
4. LOAD MODE REGISTER command may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.

FLASH MEMORY FUNCTIONAL DESCRIPTION

The SyncFlash memory incorporates a number of features that make it ideally suited for code storage and execute-in-place applications on an SDRAM bus. The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, programmed, and erased by issuing commands to the command execution logic (CEL). The CEL controls the operation of the internal state machine (ISM), which completely controls all ERASE NVMODE REGISTER, PROGRAM NVMODE REGISTER, PROGRAM, BLOCK ERASE, BLOCK PROTECT, DEVICE PROTECT, UNPROTECT ALL BLOCKS, and VERIFY operations. The ISM protects each memory location from overerasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for programming the device in-system or in an external programmer.

The Flash Memory Functional Description provides detailed information on the operation of the SyncFlash memory and is organized into these sections:

- Command Interface
- Memory Architecture
- Output (READ) Operations
- Input Operations
- Command Execution
- RESET/Power-Down Mode
- Error Handling
- PROGRAM/ERASE Cycle Endurance

COMMAND INTERFACE

All Flash operations are executed with LCR (LOAD COMMAND REGISTER), LCR/ACTIVE/READ, or LCR/ACTIVE/WRITE commands and command sequences as defined in Truth Tables 1 and 2. See the SDRAM Interface Functional Description for information on reading the memory array.

Address pins A0–A7 are used to input 8-bit commands during the LCR command cycle. This command will identify which flash operation is initiated.

Certain LCR/active/write command sequences require an 8-bit confirmation code on the WRITE cycle. The confirmation code is input on DQ0–DQ7.

All input commands are latched on the positive clock edge.

MEMORY ARCHITECTURE

The 64Mb SyncFlash is a four-bank architecture with four erasable "blocks" per bank. By erasing blocks rather than the entire array, the total device endurance is enhanced, as is system flexibility. Only the ERASE and BLOCK PROTECT functions are block oriented. The four banks have simultaneous read-while-write functionality. An ISM PROGRAM or ERASE operation to any bank can occur simultaneously with a READ to any other bank.

The SyncFlash memory has a single background operation ISM to control power-up initialization, ERASE, PROGRAM, and PROTECT operations. ISM operations are initiated with an LCR/ACTIVE/WRITE command sequence. Only one ISM operation can occur at any time; however, certain other commands, including READ operations, can be performed while an ISM operation is taking place. A new LCR/active/write command sequence will not be permitted until the current ISM operation is complete. An operational command controlled by the ISM is defined as either a bank-level operation or a device-level operation.

PROGRAM and ERASE are bank-level ISM operations. After an ISM bank-level operation has been initiated, a READ may be issued to any bank; however, a READ to the bank under ISM control will output the contents of the row activated prior to the LCR/active/write command sequence.

ERASE NVMODE REGISTER, PROGRAM NVMODE REGISTER, BLOCK PROTECT, DEVICE PROTECT, and UNPROTECT ALL BLOCKS are device-level ISM operations. Once an ISM device-level operation has been initiated, a READ to any bank will output the contents of the array.

A read status register command sequence may be issued to determine completion of the ISM operation. When SR7 = 1, the ISM operation is complete and a new ISM operation may be initiated.

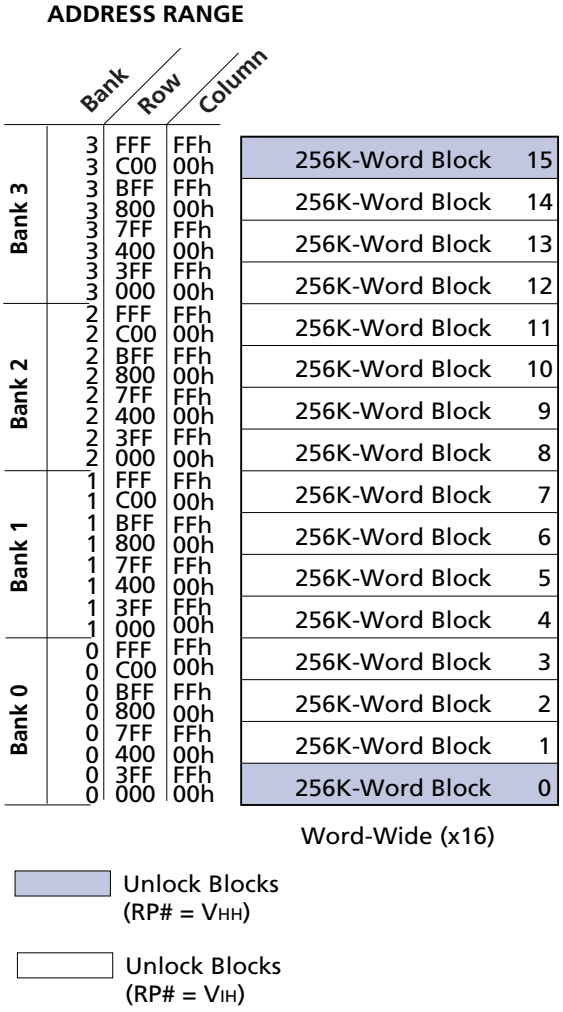
PROTECTED BLOCKS

The 64Mb SyncFlash memory is organized into 16 erasable memory blocks. Each block may be software protected by issuing the appropriate LCR/active/write sequence for a BLOCK PROTECT operation.

The blocks at locations 0 and 15 have additional protection to prevent inadvertent PROGRAM or ERASE operations in 3.3V-only platforms. Once a PROTECT BLOCK operation has been executed to these blocks, an UNPROTECT ALL BLOCKS operation will unlock all blocks except the blocks at locations 0 and 15 unless RP# = V_{HH}. This provides additional security for critical code during in-system firmware updates should an unintentional power disruption or system reset occur.

A second level of block protection is possible by completing a hardware DEVICE PROTECT operation. DEVICE PROTECT prevents block protect bit modification.

The protection status of any block may be checked by reading the protect bits with a read device configuration command sequence.



NOTE: See Block Lock and Unlock Flowchart Sequences for additional information

Figure 15
Memory Address Map

COMMAND EXECUTION LOGIC (CEL)

SyncFlash operations are executed by issuing the appropriate commands to the CEL. The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e., memory array, device configuration, or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more details.

INTERNAL STATE MACHINE (ISM)

Power-up initialization, erase, program, and protect timings are simplified by using an ISM to control all programming algorithms in the memory array. The ISM ensures protection against overerasure and optimizes programming margin to each cell.

During PROGRAM operations, the ISM automatically increments and monitors PROGRAM attempts, verifies programming margin on each memory cell, and updates the ISM status register. When BLOCK ERASE is performed, the ISM automatically overwrites the entire addressed block (eliminates overerasure), increments and monitors ERASE attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The 16-bit ISM status register allows an external processor to monitor the status of the ISM during device initialization, ERASE NVMODE REGISTER, PROGRAM NVMODE REGISTER, PROGRAM, ERASE, BLOCK PROTECT, DEVICE PROTECT or UNPROTECT ALL BLOCKS, and any related errors. ISM operations and related errors can be monitored by reading status register bits on DQ0–DQ8.

All of the defined bits are set by the ISM, but only the ISM status bits (SR0, SR1, SR2, SR7) are cleared by the ISM. The erase/unprotect block, program/protect block, and device protection bits must be cleared by the host system using the CLEAR STATUS REGISTER command. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple PROGRAM operations before checking the status register instead of checking after each individual PROGRAM.

A V_{CC} power sequence error is cleared by re-initializing the device.

Asserting the RP# signal or powering down the device will also clear the status register.

FLASH

OUTPUT (READ) OPERATIONS

SyncFlash memory features three different types of READs. Depending on the mode, a READ operation will produce data from the memory array, status register, or one of the device configuration registers. SyncFlash memory is in the array read mode unless a status register or device register read is initiated or in progress.

A READ to the device configuration register or the status register must be preceded by LCR/ACTIVE. The burst length of data-out is defined by the mode register settings. Reading the device configuration register or status register will not disrupt data in a previously opened (or "activated") page. When the burst is complete, a subsequent READ will read the array. However, several differences exist and are described in the following section. Moving between modes to perform a specific READ will be covered in the Command Execution section.

MEMORY ARRAY

A READ command to any bank will output the contents of the memory array. While a PROGRAM or ERASE ISM operation is in progress, a READ to any location in the bank under ISM control will output the contents of the row activated prior to the LCR/active/write command sequence; a READ to any other bank will output the contents of the array. All commands and their operations are covered in the SDRAM Interface Functional Description section.

STATUS REGISTER

Reading the status register requires an LCR/active/read command sequence. The status register contents are latched on the next positive clock edge subject to CAS latencies. The burst length of the status register data-out is defined by the mode register.

All commands and their operations are covered in the Command Execution section.

DEVICE CONFIGURATION REGISTERS

Reading the device ID, manufacturer compatibility ID, device protection status, and block protect status requires the same input sequencing as when reading the status register except that specific addresses must be issued.

All commands and their operations are covered in the Command Execution section.

INPUT OPERATIONS

An LCR/active/write command sequence is required to program the array, or to perform an ERASE, PROTECT, or UNPROTECT operation. The first cycle of an input operation is LCR where inputs A0–A7 determine the input command being executed to the CEL. An input operation will not disrupt data in a previously opened page.

The DQ pins are used either to input data to the array or to input a command to the command execution logic (CEL) during the WRITE cycle.

More information describing how to program, erase, protect, or unprotect the device is provided in the Command Execution section.

MEMORY ARRAY

Programming or erasing the memory array sets the desired bits to logic 0s but cannot change a given bit to a logic 1 from a logic 0. Setting any bit to a logic 1 requires that the entire block be erased. Programming a protected block requires that the RP# pin be brought to V_{HH}. A0–A11 provide the address to be programmed, while the data to be programmed in the array is input on the DQ pins. The data and addresses are latched on the rising edge of the clock. Details on how to input data to the array is covered in the Command Execution section.

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode has specific operations that can be performed while in that mode. All modes require that an LCR/active/read or LCR/active/write sequence be issued, except CLEAR STATUS REGISTER which is a single LCR command. Inputs A0–A7 during the LCR command determine the command being executed. The following section describes the properties of each mode, and Truth Tables 1 and 2 list all commands and command sequences required to perform the desired operation. Read-while-write functionality allows a background operation program or erase to any bank while simultanously reading any other bank.

The LCR/active/write command sequences in Truth Table 2 must be completed on consecutive clock cycles. However, in order to reduce bus contention issues, an unlimited number of NOPs or COMMAND INHIBITs can be issued throughout the LCR/active/write command sequence. For additional protection, these command sequences must have the same bank address for the three command cycles.

If the bank address changes during the LCR/active/write command sequence or if the command sequences are not consecutive (other than NOPs and COMMAND INHIBITs), the program and erase status bits (SR4 and SR5) will be set and the desired operation will be aborted.

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STATUS REGISTER

Reading the status register requires an LCR/active/read command sequence. The status register contents are latched on the next positive clock edge subject to CAS latencies for a burst length defined by the mode register.

DEVICE CONFIGURATION

To read the device ID, manufacturer compatibility ID, device protect bit, and each of the block protect bits, the appropriate LCR/active/read command sequence for READ DEVICE CONFIGURATION must be issued. Specific configuration addresses must be issued to read the desired information. The manufacturer compatibility ID is read at 000h; the device ID is read at 001h. The manufacturer compatibility ID and device ID are output on DQ0–DQ7. The device protect bit is read at 003h; and each of the block protect bits is read on the third address location within each block (x02h). The device and block protect bits are output on DQ0.

The device configuration register contents are output subject to CAS latencies for a burst length defined by the mode register.

PROGRAM SEQUENCE

Three commands on consecutive clock edges are required to input data to the array (NOPs and COMMAND INHIBITS are permitted between cycles). In the first cycle, LOAD COMMAND REGISTER is issued with PROGRAM SETUP (40h) on A0–A7, and the bank address is issued on BA0, BA1. The next command is ACTIVE, which identifies the row address and confirms the bank address. The third cycle is WRITE, during which the column address, the bank address, and data are issued. The ISM status bit will be set on the following clock edge (subject to CAS latencies).

While the ISM is programming the array, the ISM status bit (SR7) will be at "0." When the ISM status bit (SR7) is set to a logic 1, programming is complete, and the bank will be in the array read mode and ready for a new ISM operation.

Programming hardware-protected blocks requires that the RP# pin be set to V_{HH} prior to the third cycle (WRITE), and RP# must be held at V_{HH} until the ISM PROGRAM operation is complete. The program and erase status bits (SR4 and SR5) will be set and the operation aborted if the LCR/active/write command sequence is not completed on consecutive cycles or the bank address changes for any of the three cycles. After the ISM has initiated programming, it cannot be aborted except by a RESET or by powering down the device. Doing either while programming the array will corrupt the data being written.

ERASE SEQUENCE

Executing an erase sequence will set all bits within a block to logic 1. The command sequence necessary to execute an ERASE is similar to that of a PROGRAM. To provide added security against accidental block erasure, three consecutive command sequences on consecutive clock edges are required to initiate an ERASE of a block. In the first cycle, LOAD COMMAND REGISTER is issued with ERASE SETUP (20h) on A0–A7, and the bank address of the block to be erased is issued on BA0, BA1. The next command is ACTIVE, where A10, A11, BA0, and BA1 provide the address of the block to be erased. The third cycle is WRITE, during which ERASE CONFRIM (D0h) is issued on DQ0–DQ7 and the bank address is reissued. The ISM status bit will be set on the following clock edge (subject to CAS latencies).

After ERASE CONFIRM (D0h) is issued, the ISM will start erasing the addressed block. When the ERASE operation is complete, the bank will be in the array read mode and ready for an executable command. Erasing hardware-protected blocks also requires that the RP# pin be set to V_{HH} prior to the third cycle (WRITE), and RP# must be held at V_{HH} until the erase operation is complete (SR7 = 1). If the LCR/active/write command sequence is not completed on consecutive cycles (NOPs and COMMAND INHIBITs are permitted between cycles), or the bank address changes for one or more of the command cycles, the program and erase status bits (SR4 and SR5) will be set.

PROGRAM AND ERASE NVMODE REGISTER

The contents of the mode register may be copied into the nvmode register with a PROGRAM NVMODE REGISTER command. Prior to programming the nvmode register, an erase nvmode register command sequence must be completed to set all bits in the nvmode register to logic 1. The command sequence necessary to execute an ERASE NVMODE REGISTER and PROGRAM NVMODE REGISTER is similar to that of a PROGRAM. See Truth Table 2 for more information on the LCR/ACTIVE/WRITE commands necessary to complete ERASE NVMODE REGISTER and PROGRAM NVMODE REGISTER.

BLOCK PROTECT/UNPROTECT SEQUENCE

Executing a block protect sequence will enable the first level of software/hardware protection for a given block. The command sequence necessary to execute a BLOCK PROTECT is similar to that of a PROGRAM. To provide added security against accidental block protection, three consecutive command cycles are required to initiate a BLOCK PROTECT. In the first cycle, LOAD COMMAND REGISTER is issued with PROTECT SETUP (60h) on A0–A7, and the bank address of the

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block to be protected is issued on BA0, BA1. The next command is ACTIVE, which identifies a row in the block to be protected and confirms the bank address. The third cycle is WRITE, during which BLOCK PROTECT CONFIRM (01h) is issued on DQ0–DQ7, and the bank address is reissued. The ISM status bit will be set on the following clock edge (subject to CAS latencies) indicating the PROTECT operation is in progress.

If the LCR/ACTIVE/WRITE is not completed on consecutive cycles (NOPs and COMMAND INHIBITs are permitted between cycles), or the bank address changes, the write and erase status bits (SR4 and SR5) will be set and the operation will be aborted. When the ISM status bit (SR7) is set to a logic 1, the PROTECT opertation is complete.

Once a block protect bit has been set to a "1" (protected), it can only be reset to a "0" if the UNPROTECT ALL BLOCKS command is executed. The unprotect all blocks command sequence is similar to the block protect sequence; however, in the third cycle, a WRITE is issued with UNPROTECT ALL BLOCKS CONFIRM (D0h) and addresses are "Don't Care." For additional information, refer to Truth Table 2.

The blocks at locations 0 and 15 have additional security. Once the block protect bits at locations 0 and 15 have been set to a "1" (protected), each bit can only be reset to a "0" if RP# is brought to V_{HH} prior to the third cycle (WRITE) of the UNPROTECT operation, and held at V_{HH} until the operation is complete (SR7 = 1).

If the device protect bit is set, RP# must be brought to V_{HH} prior to the third cycle and held at V_{HH} until the BLOCK PROTECT or UNPROTECT ALL BLOCKS operation is complete.

To check a block's protect status, a read device configuration command sequence may be issued.

DEVICE PROTECT SEQUENCE

Executing a device protect sequence will set the device protect bit to a "1" and prevent block protect bit modification. The command sequence necessary to execute a DEVICE PROTECT is similar to that of a PROGRAM. Three consecutive command cycles are required to initiate a DEVICE PROTECT. In the first cycle, LOAD COMMAND REGISTER is issued with PROTECT SETUP (60h) on A0–A7, and a bank address is issued on BA0, BA1. The bank address is "Don't Care," but the same bank address must be used for all three cycles. The next command is ACTIVE. The third cycle is WRITE, during which DEVICE PROTECT (F1h) is issued on DQ0–DQ7. RP# must be brought to V_{HH} prior to registration of the WRITE command. The ISM status bit will be set on the following clock edge (subject to CAS latencies). RP# must be held at V_{HH} until the PROTECT operation is complete (SR7 = 1).

Once the device protect bit is set, it can only be reset to a "0" by issuing a BLOCK UNPROTECT command with RP# at V_{HH} during the operation. With the device protect bit set to a "1," BLOCK PROTECT or BLOCK UNPROTECT is prevented unless RP# is at V_{HH} during either operation. The device protect bit does not affect PROGRAM or ERASE operations.

RESET/DEEP POWER-DOWN MODE

To allow for maximum power conservation, the device features a very low current, deep power-down mode.

To enter this mode, the RP# pin (reset/power-down) is taken to V_{SS} ±0.2V. To prevent an inadvertent RESET, RP# must be held at V_{SS} for 50ns prior to the device entering the reset mode. With RP# held at V_{SS}, the device will enter the deep power-down mode. After the device enters the deep power-down mode, a transition from LOW to HIGH on RP# will result in a device power-up initialization sequence as outlined in the Device Initialization section. Transitioning RP# from LOW to HIGH after entering the reset mode but prior to entering deep power-down mode (i.e., less than 100ns) will require a 1µs delay prior to issuing an executable command.

When the device enters the deep power-down mode, all buffers excluding the RP# buffer are disabled and the current draw is a maximum of 100µA at 3.6V V_{CC}. The input to RP# must remain at V_{SS} during deep power-down. Entering the RESET mode clears the Status Register.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the device protect (SR3), write/protect block (SR4) and erase/unprotect (SR5) status bits may be checked. If one or a combination of SR3, SR4, SR5 status bits has been set, an error has occurred. SR8 is set when an inadvertent power failure occurs during device initialization. The device should be reinitialized to ensure proper device operation. The ISM cannot reset SR3, SR4, SR5 or SR8. To clear these bits, CLEAR STATUS REGISTER (50h) must be given. Table 5 lists the combination of errors.

PROGRAM/ERASE CYCLE ENDURANCE

SyncFlash memory is designed and fabricated to meet advanced code and data storage requirements. Operation outside specification limits may reduce the number of PROGRAM and ERASE cycles that may be performed on the device. Each block is designed and processed for a minimum of 100,000-PROGRAM/ERASE-cycle endurance.

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Table 3
Status Register Bit Definition[1]

R	VPS	ISMS	R	ES	WS	DPS	BISMS	DBS
15-9	8	7	6	5	4	3	2-1	0

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR15-SR9	RESERVED	Reserved for future use.
SR8	V_{CC} POWER SEQUENCE STATUS (VPS) 1 = Power-up incomplete error 0 = Power-up complete	VPS is set if there has been a power disruption that may result in undefined device operation. A VPS error is only cleared by re-initializing the device.
SR7	ISM STATUS (ISMS) 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine when performing PROGRAM or BLOCK ERASE. The controlling logic polls this bit to determine when the erase and program status bits are valid.
SR6	RESERVED	Reserved for future use.
SR5	ERASE/UNPROTECT BLOCK STATUS (ES) 1 = BLOCK ERASE or BLOCK UNPROTECT error 0 = Successful BLOCK ERASE or UNPROTECT	ES is set to "1" after the maximum number of ERASE cycles is executed by the ISM without a successful verify. This bit is also set to "1" if a BLOCK UNPROTECT operation is unsuccessful. ES is only cleared by a CLEAR STATUS REGISTER command or by a RESET.
SR4	PROGRAM/PROTECT BLOCK STATUS (WS) 1 = PROGRAM or BLOCK PROTECT error 0 = Successful BLOCK ERASE or UNPROTECT	WS is set to "1" after the maximum number of PROGRAM cycles is executed by the ISM without a successful verify. This bit is also set to "1" if a BLOCK or DEVICE PROTECT operation is unsuccessful. WS is only cleared by a CLEAR STATUS REGISTER command or by a RESET.
SR3	DEVICE PROTECT STATUS (DPS) 1 = Device protected, invalid operation attempted 0 = Device unprotected or RP# condition met	DPS is set to "1" if an invalid PROGRAM, ERASE, PROTECT BLOCK, PROTECT DEVICE, or UNPROTECT ALL BLOCKS is met. After one of these commands is issued, the condition of RP#, the block protect bit, and the device protect bit is compared to determine if the desired operation is allowed. Must be cleared by CLEAR STATUS REGISTER or by a RESET.
SR2 SR1	BANK ISM STATUS (BISMS) BANKA1 ISM STATUS BANKA0 ISM STATUS	When SR0 = 0, the bank under ISM control can be decoded from SR1, SR2: [0,0] Bank0; [1,0] Bank1; [0,1] Bank2; [1,1] Bank3. SR1, SR2 is valid when SR7 = 0. When SR7 = 1, SR1, SR2 is reset to "0."
SR0	DEVICE/BANK ISM STATUS (DBS) 1 = Device-level ISM operation 0 = Bank-level ISM operation	DBS is set to "1" if the ISM operation is a device-level operation. A valid READ to any bank can immediately follow the registration of an ISM PROGRAM operation. When DBS is set to "0," the ISM operation is a bank-level operation. A READ to the bank under ISM control will output the contents of the row activated prior to the LCR/ACTIVE/WRITE command sequence. SR1 and SR2 can be decoded to determine which bank is under ISM control. SR0 is used in conjuction with SR7, and is valid when SR7 = 0. When SR7 = 1, SR0 is reset to "0."

NOTE: 1. SR3-SR5 must be cleared with CLEAR STATUS REGISTER prior to initiating an ISM WRITE operation for the status bits to be valid.

Table 4
Device Configuration

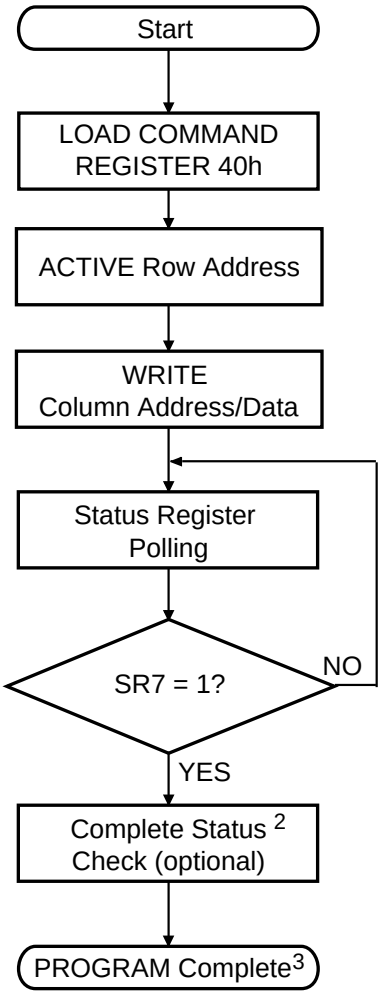
DEVICE CONFIGURATION	CONFIGURATION ADDRESS	DATA	CONDITION	NOTES
Manufacturer Compatibility ID	000h	2Ch	Manufacturer compatibility ID read	1
Device ID	001h	D3h	Device ID read	1
Block Protect Bit	x02h x02h	DQ0 = 1 DQ0 = 0	Block protected Block unprotected	2, 3
Device Protect Bit	003h 003h	DQ0 = 1 DQ0 = 0	Block protect modification prevented Block protect modification enabled	3

Table 5
Status Register Error Decode[4]

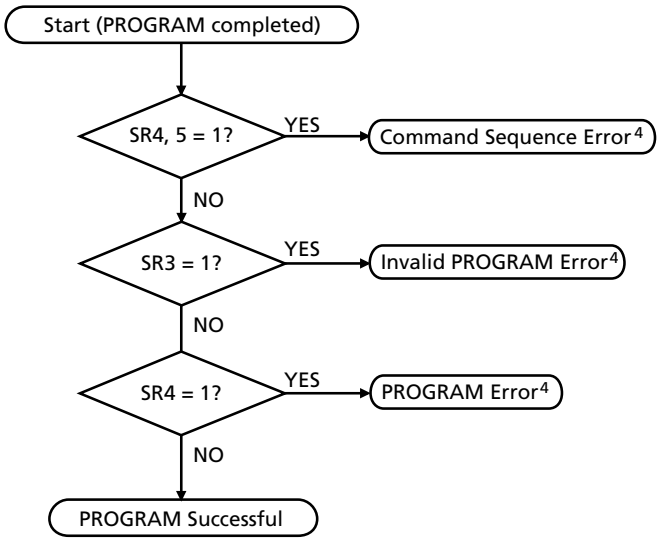
STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION[5]
0	0	0	No errors
0	1	0	PROGRAM, BLOCK PROTECT or DEVICE PROTECT error
0	1	1	Invalid BLOCK PROTECT or DEVICE PROTECT, RP# not valid (V_{HH})
0	1	1	Invalid BLOCK or DEVICE PROTECT, RP# not valid
1	0	0	ERASE or ALL BLOCK UNPROTECT error
1	0	1	Invalid ALL BLOCK UNPROTECT, RP# not valid (V_{HH})
1	1	0	Command sequencing error

NOTE: 1. DQ8–DQ15 are "Don't Care."
2. Address to read block protect bit is always the third location within each block.
x = 0, 4, 8, C; BA0, BA1 required.
3. DQ1–DQ7 are reserved, DQ8–DQ15 are "Don't Care."
4. SR3–SR5 must be cleared using CLEAR STATUS REGISTER.
5. Assumes that SR4 and SR5 reflect noncumulative results.

SELF-TIMED PROGRAM SEQUENCE[1]



COMPLETE PROGRAM STATUS-CHECK SEQUENCE



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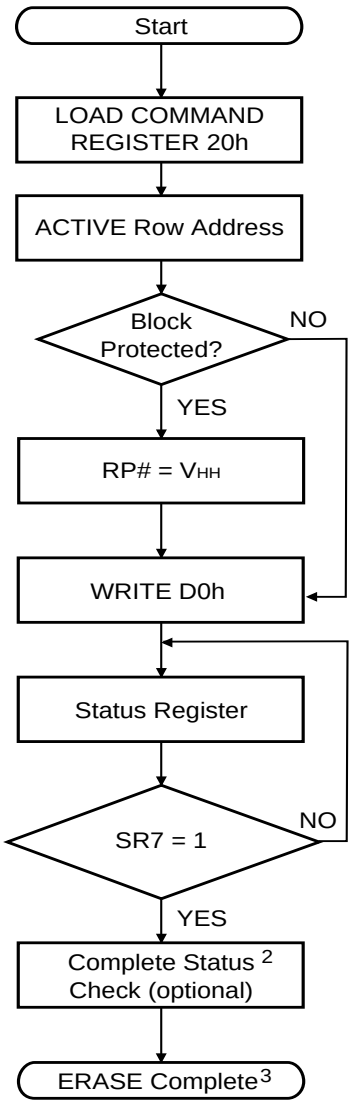
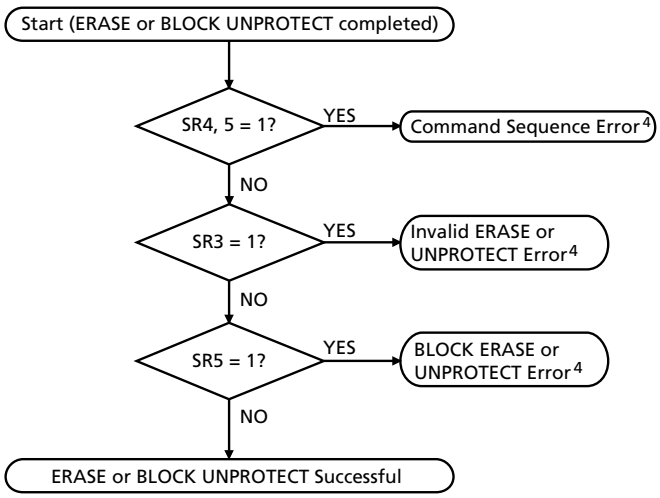
NOTE: 1. Sequence may be repeated for multiple PROGRAMs.
2. Complete status check is not required.
3. The bank will be in array read mode.
4. Status register bits 3–5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]



COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



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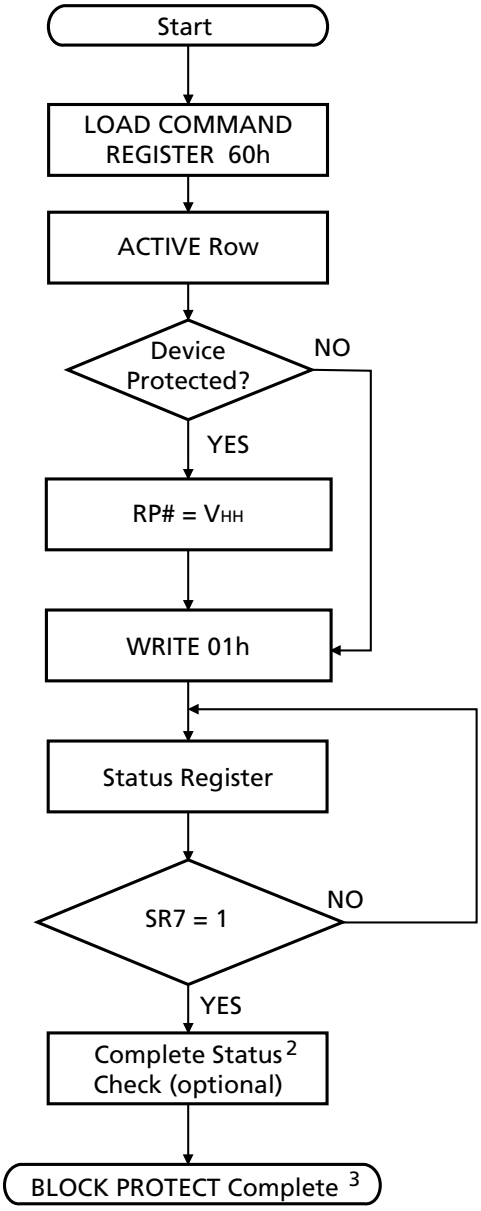
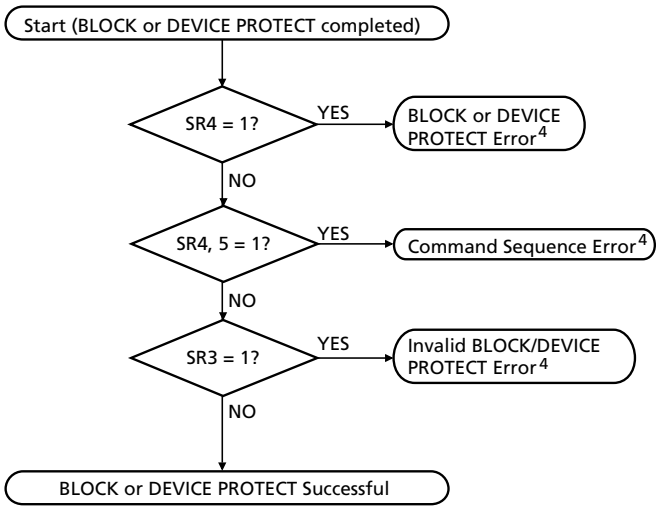
NOTE: 1. Sequence may be repeated to erase multiple blocks.
2. Complete status check is not required.
3. The bank will be in the array read mode.
4. Status register bits 3–5 must be cleared using CLEAR STATUS REGISTER.

BLOCK PROTECT SEQUENCE[1]



COMPLETE BLOCK STATUS-CHECK SEQUENCE



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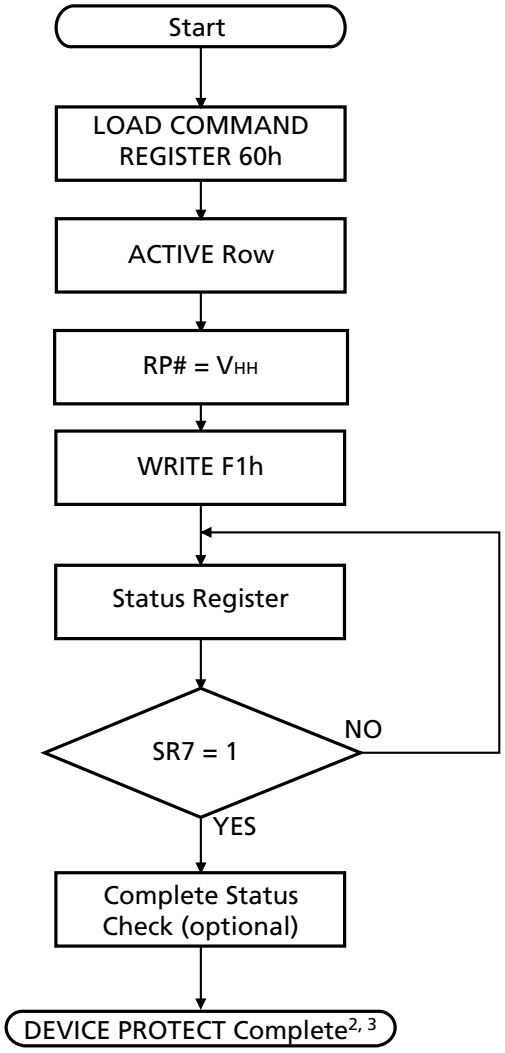
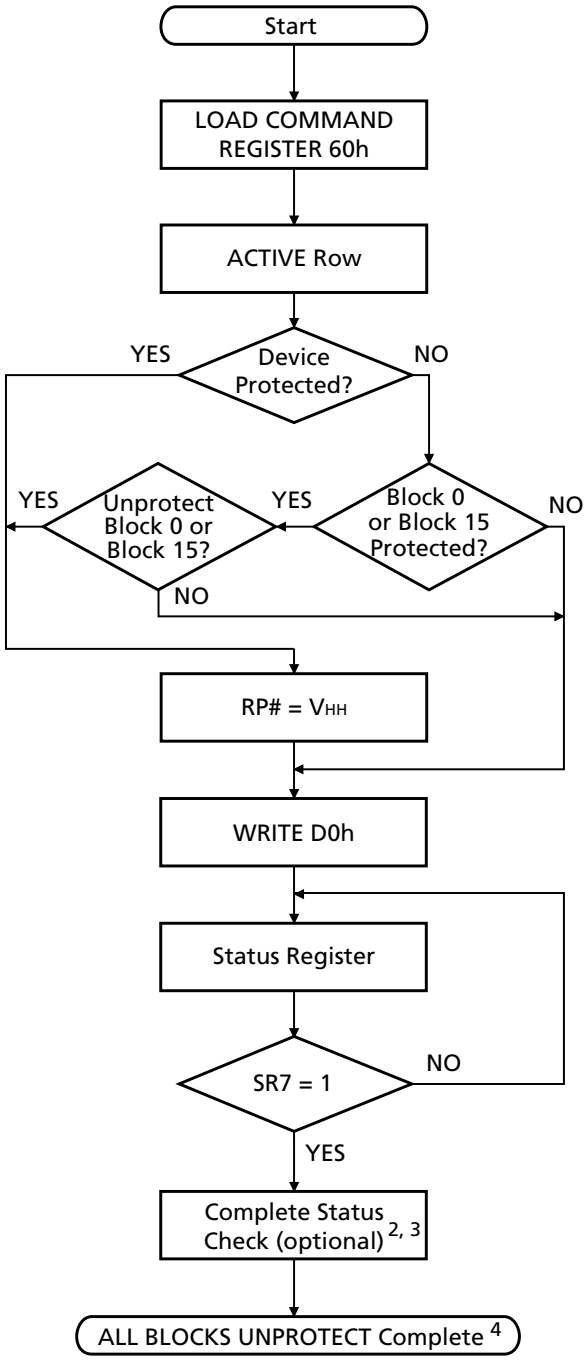
NOTE: 1. Sequence may be repeated for multiple BLOCK PROTECTs.
2. Complete status check is not required.
3. The bank will be in array read mode.
4. Status register bits 3–5 must be cleared using CLEAR STATUS REGISTER.

DEVICE PROTECT SEQUENCE[1]



BLOCK UNPROTECT SEQUENCE



NOTE: 1. Once the device protect bit is set, it cannot be reset.
2. Complete status check is not required.
3. For complete details, see Complete Block Status Check Sequence.
4. The device will remain in the array read mode; a READ may be issued to any bank after the WRITE (D0h) is registered.

ABSOLUTE MAXIMUM RATINGS*

Voltage on RP# Relative to V_{SS} ..... -1V to +10V
Voltage on V_{CC}, $V_{CC}P$ or $V_{CC}Q$ Supply or Inputs,
Relative to V_{SS} ..... -1V to +3.6V
Voltage on I/O Pins Relative to V_{SS} ..... $V_{CC}Q$ ±0.3V
Operating Temperature,
T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2); Commercial Temperature ($0°C \le T_A \le +70°C$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} SUPPLY VOLTAGE		V_{CC}	3.0	3.6	V	
$V_{CC}Q$ SUPPLY VOLTAGE		$V_{CC}Q$	3.0	3.6	V	
HARDWARE PROTECTION VOLTAGE (RP# only)		V_{HH}	8.5	10	V	
INPUT HIGH VOLTAGE: Logic 1; All Inputs		V_{IH}	2	$V_{CC}Q$ + 0.3	V	
INPUT LOW VOLTAGE: Logic 0; All Inputs		V_{IL}	- 0.3	0.8	V	
INPUT LEAKAGE CURRENT: Any input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V)		I_L	-5	5	µA	
OUPUT LEAKAGE CURRENT: DQs are disabled; $0V \le V_{OUT} \le V_{CC}Q$		I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage	(I_{OUT} = -4mA)	V_{OH}	2.4		V	
	(I_{OUT} = -100mA)	V_{OH}			V	
Output Low Voltage	(I_{OUT} = -4mA)	V_{OL}		0.4	V	
	(I_{OUT} = 100mA)	V_{OL}			V	

NOTE: 1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up. (V_{CC}, $V_{CC}P$ and $V_{CC}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.)

I_{CC} SPECIFICATIONS AND CONDITIONS

(Notes: 1, 2, 3); Commercial Temperature ($0°C \le T_A \le +70°C$)

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-10	-12		
V_{CC} OPERATING CURRENT: Active Mode; Burst = 2; READ; ^tCK = 15ns; ^tRC = ^tRC (MIN); CAS latency = 3	I_{CCR1}	125	120	mA	4,5,6
V_{CC} OPERATING CURRENT: Burst Mode; Continuous Burst; All banks active; READ; ^tCK = 15ns; CAS latency = 3	I_{CCR2}	100	95	mA	4, 5, 6
V_{CC} STANDBY CURRENT: Active Mode; CKE = LOW; Burst in progress	I_{CCS1}	10	10	mA	
V_{CC} STANDBY CURRENT: Power-Down Mode; CKE = LOW; No burst in progress	I_{CCS2}	2	2	mA	
V_{CC} DEEP POWER-DOWN CURRENT: RP# = V_{SS} ±0.2V	I_{CCDP}	300	300	µA	
PROGRAM CURRENT	I_{CCW} + I_{PPW}	60	60	mA	
$V_{CC}P$ OPERATING CURRENT: Active Mode; Burst = 2; READ; ^tRC = ^tRC (MIN); CAS latency = 3	I_{PPR1}	250	125	µA	
$V_{CC}P$ OPERATING CURRENT: ERASE CURRENT	I_{CCE}+I_{PPE}	80	80	mA	
$V_{CC}P$ DEEP POWER-DOWN CURRENT: RP# = V_{SS} ±0.2V	I_{PPDP}	1	1	µA	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CLK	C_{I1}	2.5	6.5	pF	7
Input Capacitance: All other input-only pins	C_{I2}	2.5	6.5	pF	7
Input/Output Capacitance: DQs	C_{IO}	4.0	7.0	pF	7

NOTE:
1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up. (V_{CC}, $V_{CC}P$, and $V_{CC}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.)
3. I_{CC} specifications are tested after the device is properly initialized.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. The I_{CC} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
6. Address transitions average one transition every 30ns.
7. This parameter is sampled. V_{CC} = $V_{CC}Q$; f = 1 MHz, T_A = +25°C.

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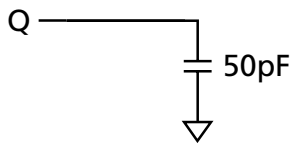
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 5); Commercial Temperature ($0°C \le T_A \le +70°C$)

AC CHARACTERISTICS			-10		-12			
PARAMETER		**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from CLK (pos. edge)	CL = 3	^tAC		7		9	ns	
	CL = 2	^tAC		9		10	ns	
	CL = 1	^tAC		27		27	ns	
Address hold time		^tAH	2		2		ns	
Address setup time		^tAS	3		3		ns	
CLK high level width		^tCH	3.5		4		ns	
CLK low level width		^tCL	3.5		4		ns	
Clock cycle time	CL = 3	^tCK	10		12		ns	
	CL = 2	^tCK	15		15		ns	
	CL = 1	^tCK	30		30		ns	
CKE hold time		^tCKH	2		2		ns	
CKE setup time		^tCKS	3		3		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	2		2		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	3		3		ns	
Data-in hold time		^tDH	2		2		ns	
Data-in setup time		^tDS	3		3		ns	
Data-out high-impedance time	CL = 3	^tHZ		8		9	ns	6
	CL = 2	^tHZ		10		10	ns	6
	CL = 1	^tHZ		15		15	ns	6
Data-out low-impedance time		^tLZ	2		2		ns	
Data-out hold time		^tOH	3		3		ns	
ACTIVE command period		^tRC	90		100		ns	
ACTIVE to READ or WRITE delay		^tRCD	30		30		ns	
ACTIVE bank A to ACTIVE bank B command		^tRRD	20		20		ns	
Transition time		^tT	0.3	1.2	1	1.2	ns	7

NOTE:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
2. An initial pause of 100µs is required after power-up. (V_{CC}, $V_{CC}P$, and $V_{CC}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.)
3. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. Outputs measured at 1.5V with equivalent load:



5. AC timing and I_{CC} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
6. ^tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^tOH before going High-Z.
7. AC characteristics assume ^tT = 1ns.

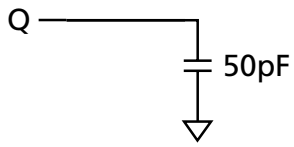
FLASH

AC FUNCTIONAL CHARACTERISTICS

(Notes: 1-6); Commercial Temperature (0°C ≤ T_A ≤ +70°C)

PARAMETER		SYMBOL	-10	-12	UNITS	NOTES
READ/WRITE command to READ/LOAD COMMAND REGISTER command		^tCCD	1	1	^tCK	7
CKE to clock disable or power-down entry mode		^tCKED	1	1	^tCK	8
CKE to clock enable or power-down exit setup mode		^tPED	1	1	^tCK	8
DQM to input data delay		^tDQD	0	0	^tCK	7
DQM to data mask during WRITEs		^tDQM	0	0	^tCK	7
DQM to data high-impedance during READs		^tDQZ	2	2	^tCK	7
WRITE command to input data delay		^tDWD	0	0	^tCK	7
Data-in to ACTIVE command		^tDAL	4	4	^tCK	
Data-in to ACTIVE TERMINATE command		^tDPL	1	1	^tCK	
LOAD MODE REGISTER command to ACTIVE command		^tMRD	2	2	^tCK	7
Data-out to High-Z from ACTIVE TERMINATE command	CL = 3	^tROH	3	3	^tCK	7
	CL = 2	^tROH	2	2	^tCK	7
	CL = 1	^tROH	1	1	^tCK	7

NOTE:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
2. An initial pause of 100µs is required after power-up. (V_{CC}, $V_{CC}P$, and $V_{CC}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.)
3. AC characteristics assume ^tT = 1ns.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. Outputs measured at 1.5V with equivalent load:



6. AC timing and I_{CC} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
7. Required clocks specified by JEDEC functionality and not dependent on any timing parameter.
8. Timing actually specified by ^tCKS; clock(s) specified as a reference only at minimum cycle rate.

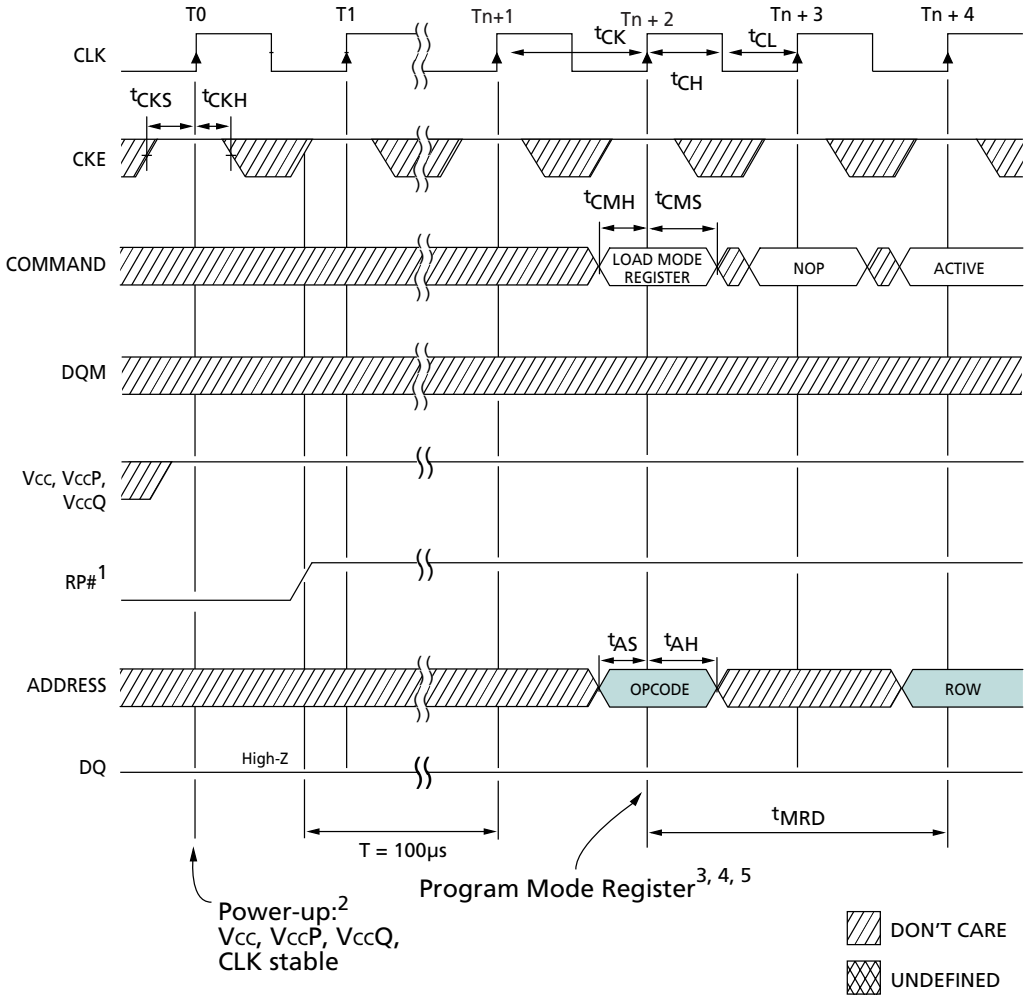
ERASE AND PROGRAM TIMING CHARACTERISTICS

Commercial Temperature (0°C ≤ T_A ≤ +70°C)

PARAMETER	-10/-12 MIN	-10/-12 MAX	UNITS
Word program time	5	5,000	µs
Block erase time	1.1	13	s

FLASH

INITIALIZE AND LOAD MODE REGISTER



TIMING PARAMETERS

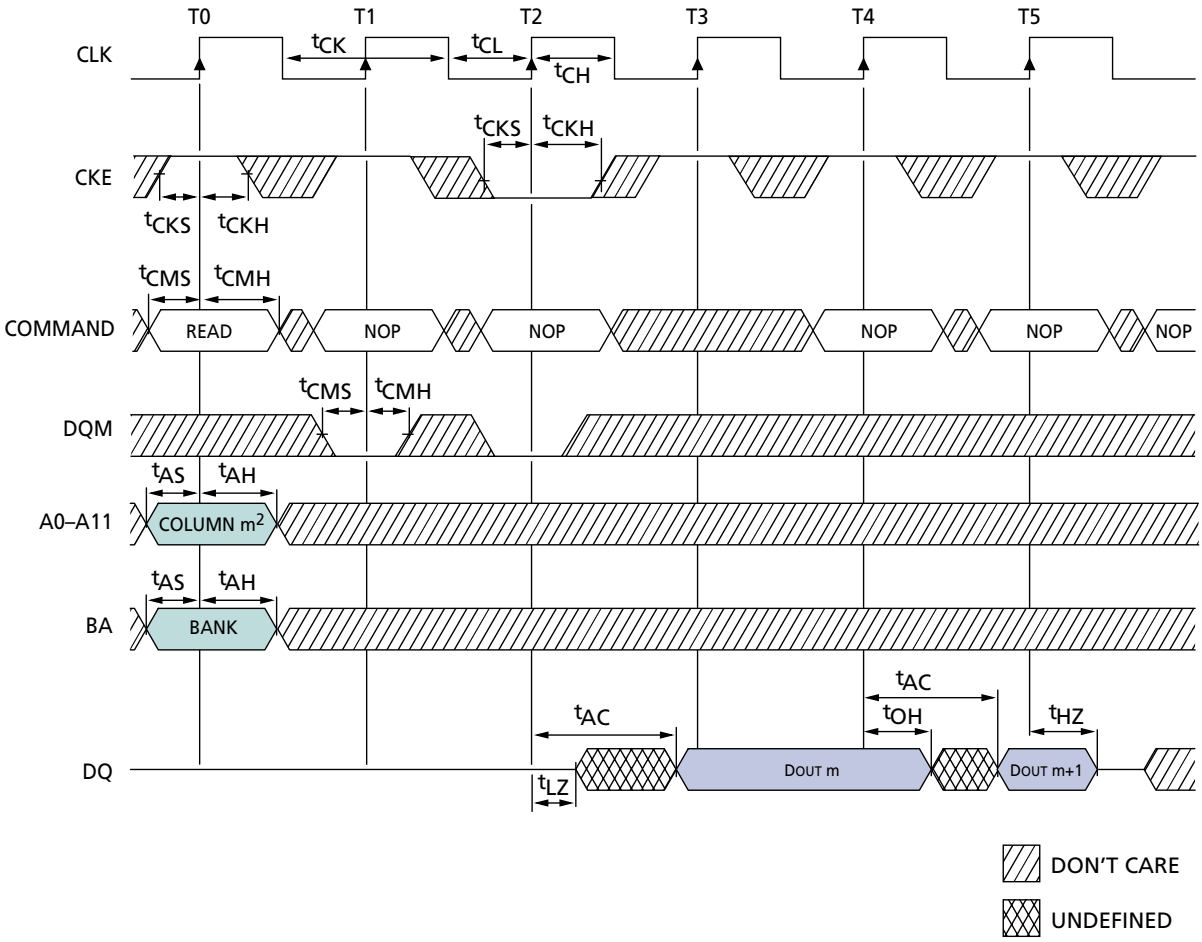
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCK (1)	30		30		ns
tCKH	2		2		ns
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tMRD	2		2		tCK

*CAS latency indicated in parentheses.

NOTE:
1. RP# = VHH or VIH
2. VCC, VCCP, VCCQ = 3.3V
3. The nvmode register contents are automatically loaded into the mode register upon power-up initialization, LOAD MODE REGISTER cycle is required to enter new mode register values.
4. JEDEC and PC100 specify three clocks.
5. If CS is HIGH at clock time, all commands applied are NOP, with CKE a "Don't Care."

CLOCK SUSPEND MODE[1]



TIMING PARAMETERS

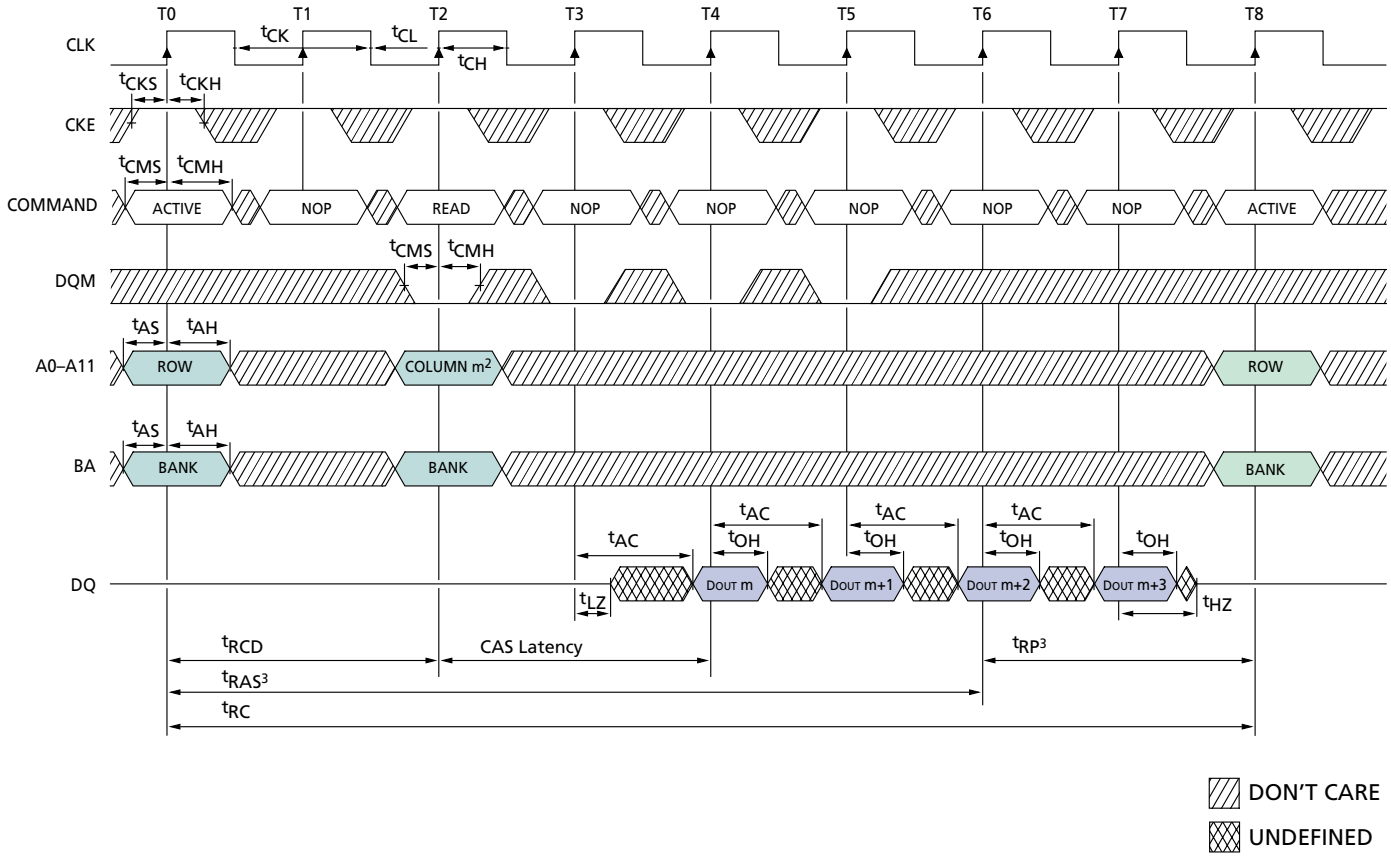
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAC (3)		7		9	ns
tAC (2)		9		10	ns
tAC (1)		27		27	ns
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns
tCKH	2		2		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tDH	2		2		ns
tDS	3		3		ns
tHZ (3)		8		9	ns
tHZ (2)		10		10	ns
tHZ (1)		15		15	ns
tLZ	2		2		ns
tOH	3		3		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 2, CAS latency = 3.
2. x16: A0–A7.

READ[1]



TIMING PARAMETERS

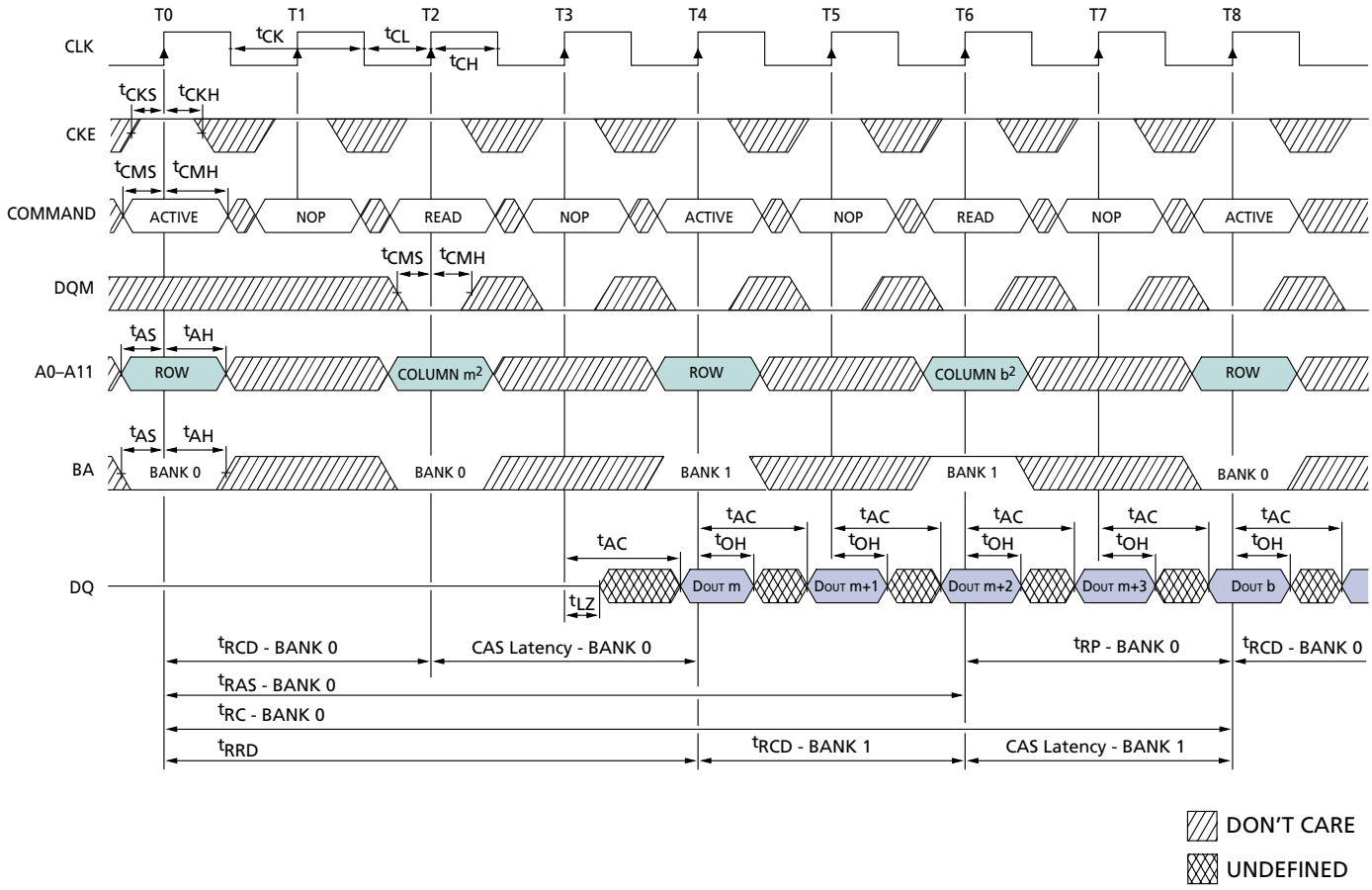
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAC (3)		7		9	ns
tAC (2)		9		10	ns
tAC (1)		27		27	ns
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns
tCKH	2		2		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tHZ (3)		8		9	ns
tHZ (2)		10		10	ns
tHZ (1)		15		15	ns
tLZ	2		2		ns
tOH	3		3		ns
tRC	90		100		ns
tRCD	30		30		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 4, CAS latency = 2.
2. x16: A0–A7.
3. tRAS and tRP are referenced to show compatibility with SDRAM timings; no values are given.

ALTERNATING BANK READ ACCESSES[1]



TIMING PARAMETERS

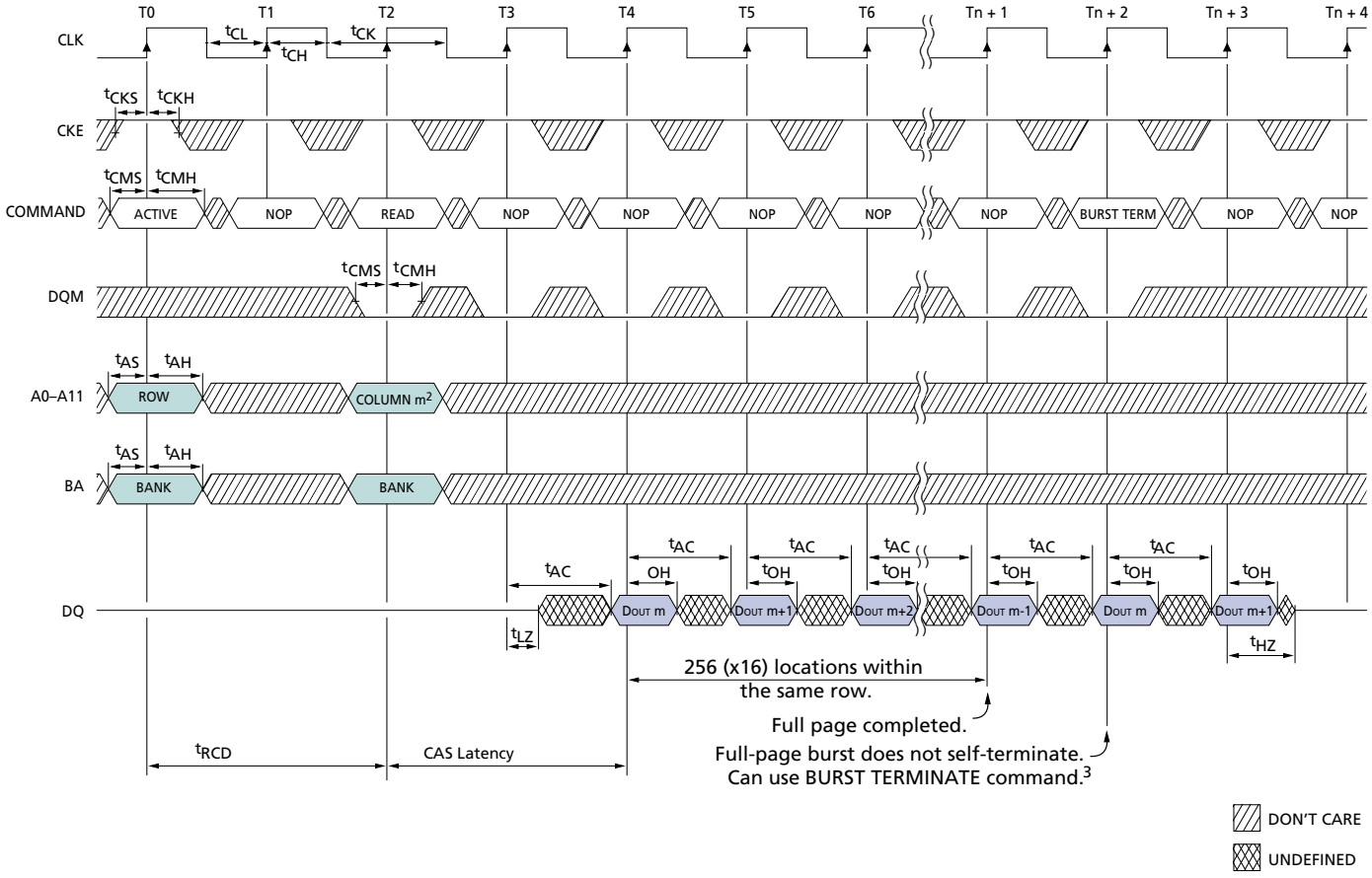
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAC (3)		7		9	ns
tAC (2)		9		10	ns
tAC (1)		27		27	ns
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKH	2		2		ns
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tLZ	2		2		ns
tOH	3		3		ns
tRC	90		100		ns
tRCD	30		30		ns
tRRD	20		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, CAS latency = 2.
2. x16: A0–A7.

READ – FULL-PAGE BURST[1]



TIMING PARAMETERS

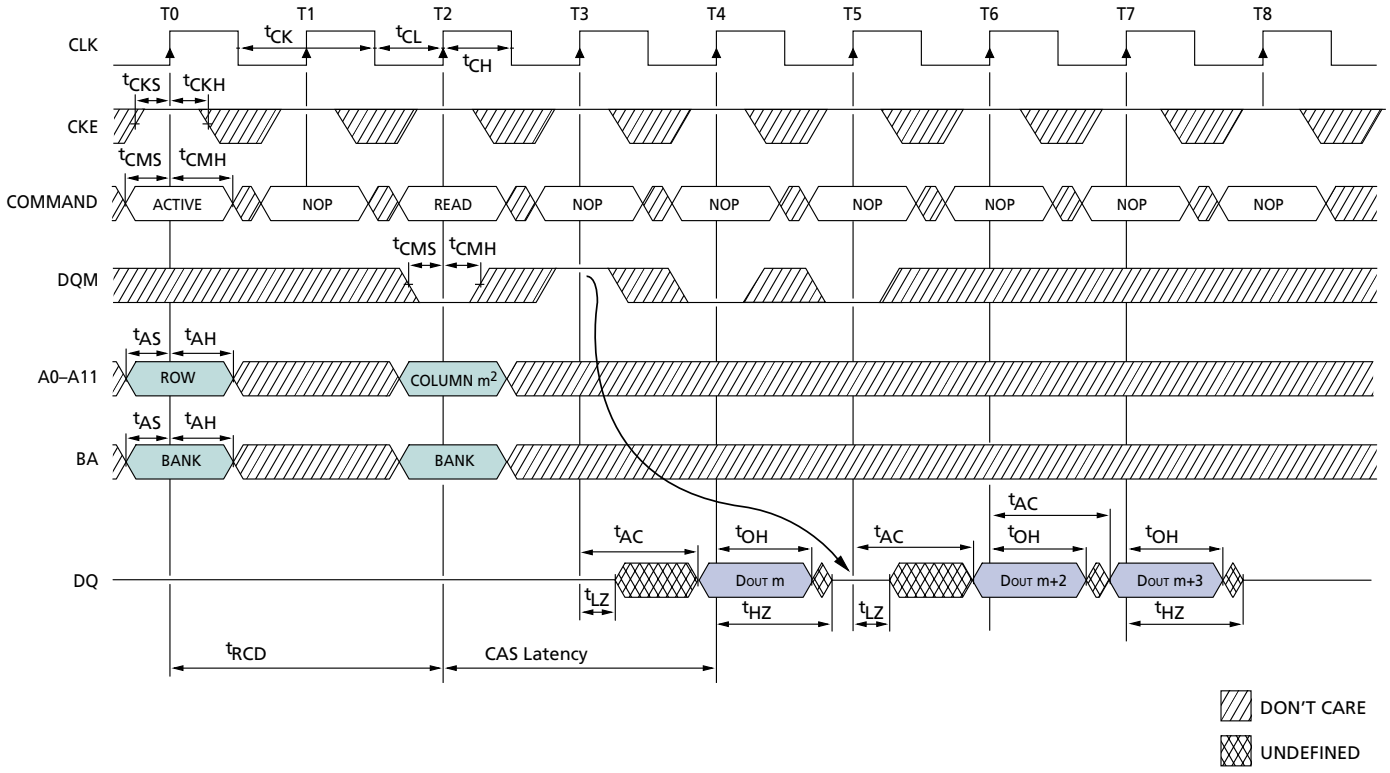
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAC (3)		7		9	ns
tAC (2)		9		10	ns
tAC (1)		27		27	ns
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKH	2		2		ns
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tHZ (3)		8		9	ns
tHZ (2)		10		10	ns
tHZ (1)		15		15	ns
tLZ	2		2		ns
tOH	3		3		ns
tRCD	30		30		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the CAS latency = 2.
2. x16: A0–A7.

READ – DQM OPERATION[1]



TIMING PARAMETERS

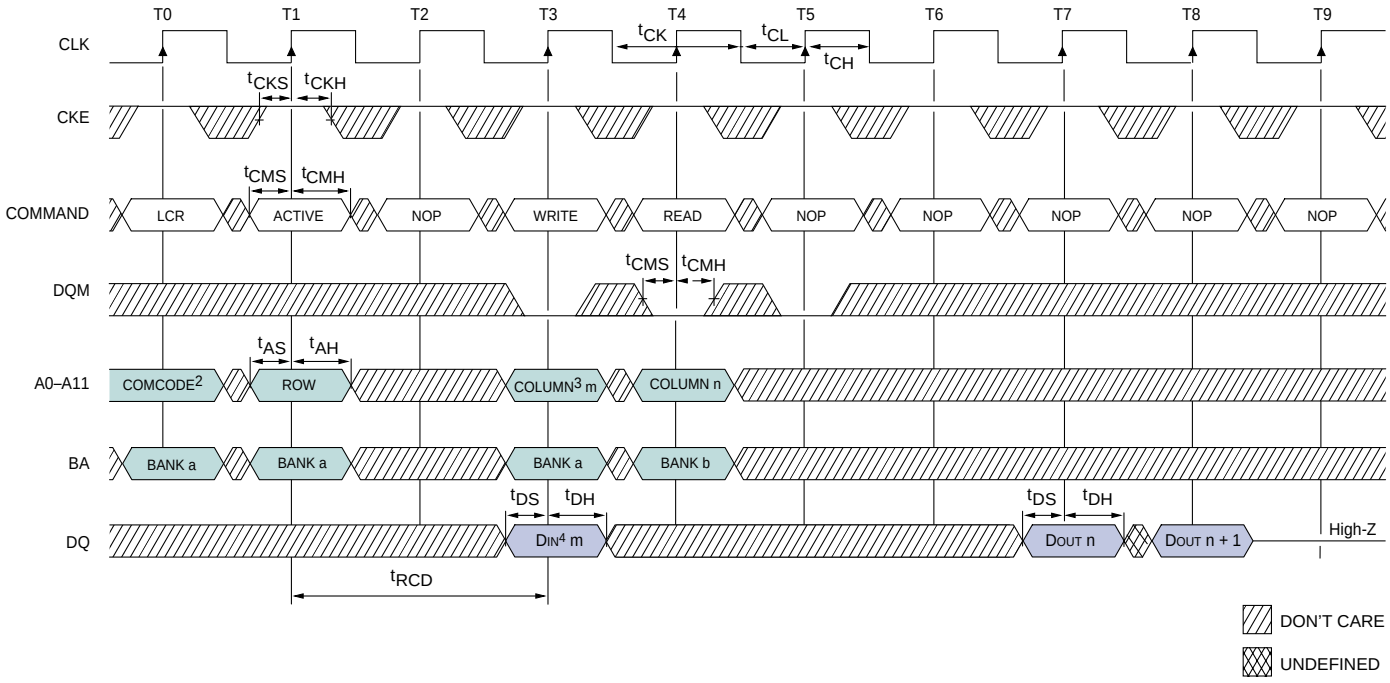
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAC (3)		7		9	ns
tAC (2)		9		10	ns
tAC (1)		27		27	ns
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKH	2		2		ns
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tHZ (3)		8		9	ns
tHZ (2)		10		10	ns
tHZ (1)		15		15	ns
tLZ	2		2		ns
tOH	3		3		ns
tRCD	30		30		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 4, CAS latency = 2.
2. x16: A0–A7.

PROGRAM/ERASE[1]
(BANK *a* FOLLOWED BY READ TO BANK *b*)



TIMING PARAMETERS

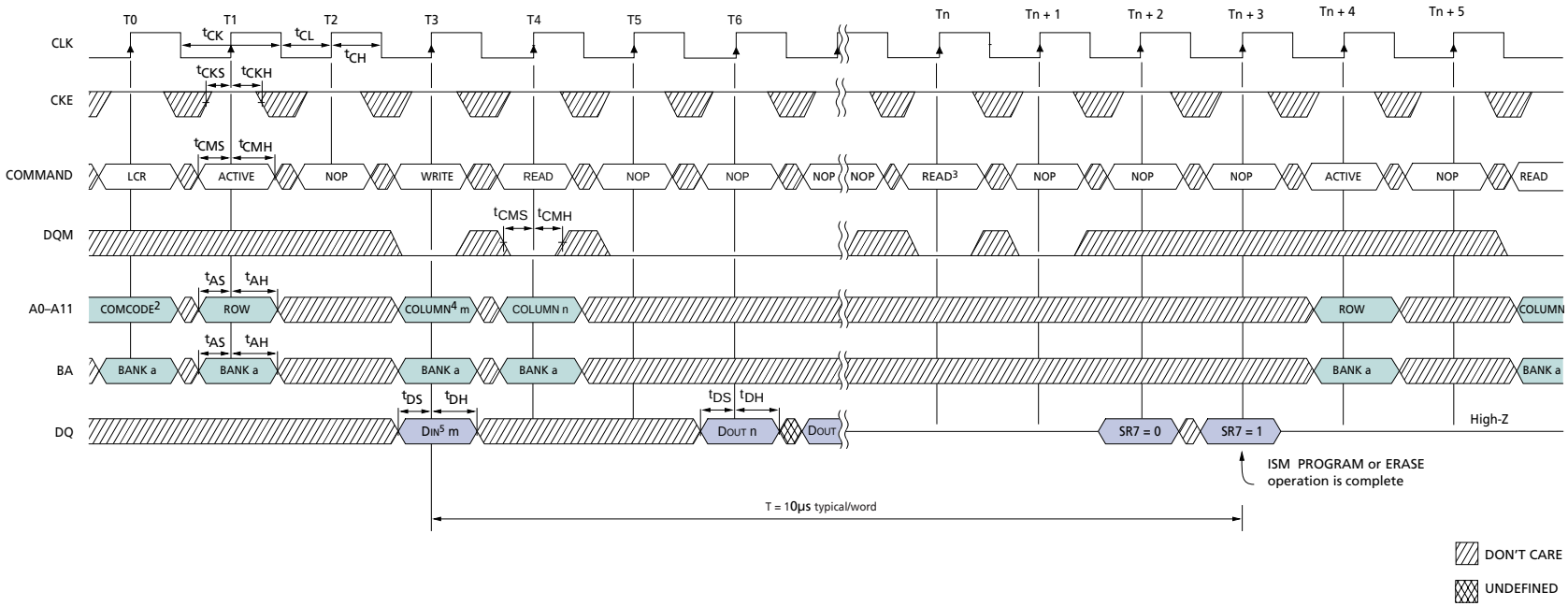
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKH	2		2		ns
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tDH	2		1.5		ns
tDS	3		3		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, READ burst length = 2, CAS = 3.
2. Com-code = 40h for WRITE, 20h for ERASE (see Truth Table 2).
3. Column address is "Don't Care" for ERASE operation.
4. DIN = D0h (erase confirm) for ERASE operation.

PROGRAM/ERASE[1]
(BANK *a* FOLLOWED BY READ TO BANK *a*)



TIMING PARAMETERS

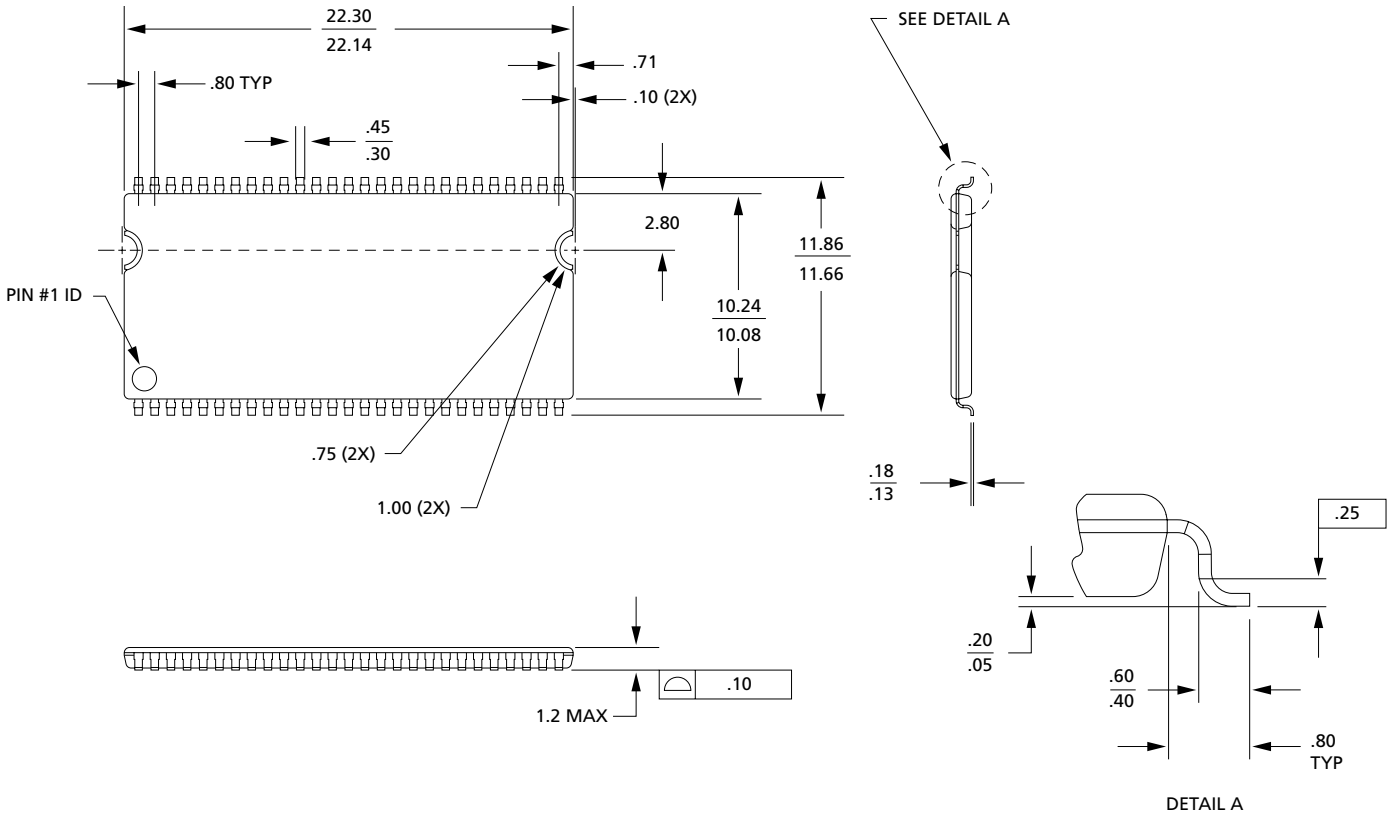
SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tAH	2		2		ns
tAS	3		3		ns
tCH	3.5		4		ns
tCL	3.5		4		ns
tCK (3)	10		12		ns
tCK (2)	15		15		ns
tCK (1)	30		30		ns

SYMBOL*	-10 MIN	-10 MAX	-12 MIN	-12 MAX	UNITS
tCKH	2		2		ns
tCKS	3		3		ns
tCMH	2		2		ns
tCMS	3		3		ns
tDH	2		2		ns
tDS	3		3		ns

*CAS latency indicated in parentheses.

NOTE:
1. ACTIVE/READ or READ will output the contents of the row activated prior to the LCR/active/write command sequence. This example illustrates the timing for activating a new row in bank *a*. For this example, READ burst length = 2, CAS latency = 2.
2. Com-code = 40h for PROGRAM, 20h for ERASE (see Truth Table 2).
3. LCR/ACTIVE cycles must be initiated prior to READ according to Truth Table 2 for a status register read command sequence.
4. Column address is "Don't Care" for ERASE operation.
5. DIN = D0h (erase confirm) for ERASE operation.

54-PIN TSOP TYPE II
(400 MIL)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

DATA SHEET DESIGNATION

This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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REVISION HISTORY

Rev. 6 ..... 9/01
- Added erase and program timing characteristics
- Updated the device protect sequence
- Removed the "Preliminary" designation

Rev. 5, PRELIMINARY 7/01
Changed ^{t}AH, ^{t}CKH, ^{t}CMH, ^{t}DH from 1ns to 2ns

Rev. 4, ADVANCE 5/01
Changed deep power-down current from 100µA to 300µA

Rev. 3, ADVANCE 4/01
Changes to V_{CC}P Operating Current
Changes to MAX Capacitance Parameters

Rev. 2, ADVANCE 2/01
Changes to Absolute Maximum Ratings
Changes to I_{CC} Specifications and Conditions

Original document, Rev. 11/00, ADVANCE 11/00