

**CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion**

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V<sub>P-P</sub> can be achieved by digital signal amplitudes of 4.5V to 20V (if V<sub>DD</sub>-V<sub>SS</sub> = 3V, a V<sub>DD</sub>-V<sub>EE</sub> of up to 13V can be controlled; for V<sub>DD</sub>-V<sub>DD</sub> level differences above 13V, a V<sub>DD</sub>-V<sub>DD</sub> of at least 4.5V is required). For example, if V<sub>DD</sub> = +4.5V, V<sub>DD</sub> = 0V, and V<sub>DD</sub> = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V<sub>DD</sub>-V<sub>DD</sub> and V<sub>DD</sub>-V<sub>DD</sub> supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERDIP	F16.3
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP	E16.3
CD4051BM, CD4052BM, CD4053BM	-55 to 125	16 Ld SOIC	M16.15

**Features**

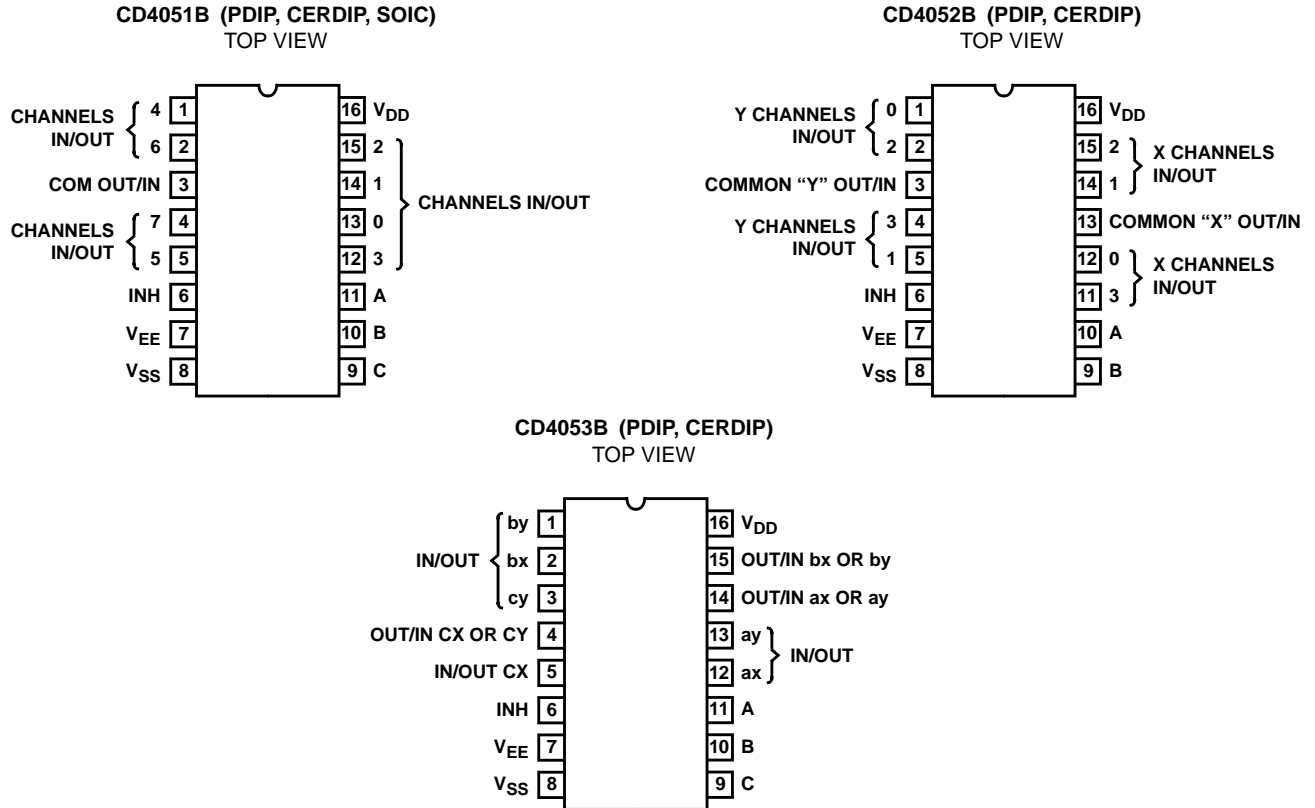
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog . . . . . ≤20V<sub>P-P</sub>
- Low ON Resistance, 125Ω (Typ) Over 15V<sub>P-P</sub> Signal Input Range for V<sub>DD</sub>-V<sub>EE</sub> = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V<sub>DD</sub>-V<sub>EE</sub> = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V<sub>DD</sub>-V<sub>SS</sub> = 3V to 20V) to Switch Analog Signals to 20V<sub>P-P</sub> (V<sub>DD</sub>-V<sub>EE</sub> = 20V)
- Matched Switch Characteristics, r<sub>ON</sub> = 5Ω (Typ) for V<sub>DD</sub>-V<sub>EE</sub> = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V<sub>DD</sub>-V<sub>SS</sub> = V<sub>DD</sub>-V<sub>EE</sub> = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

**Applications**

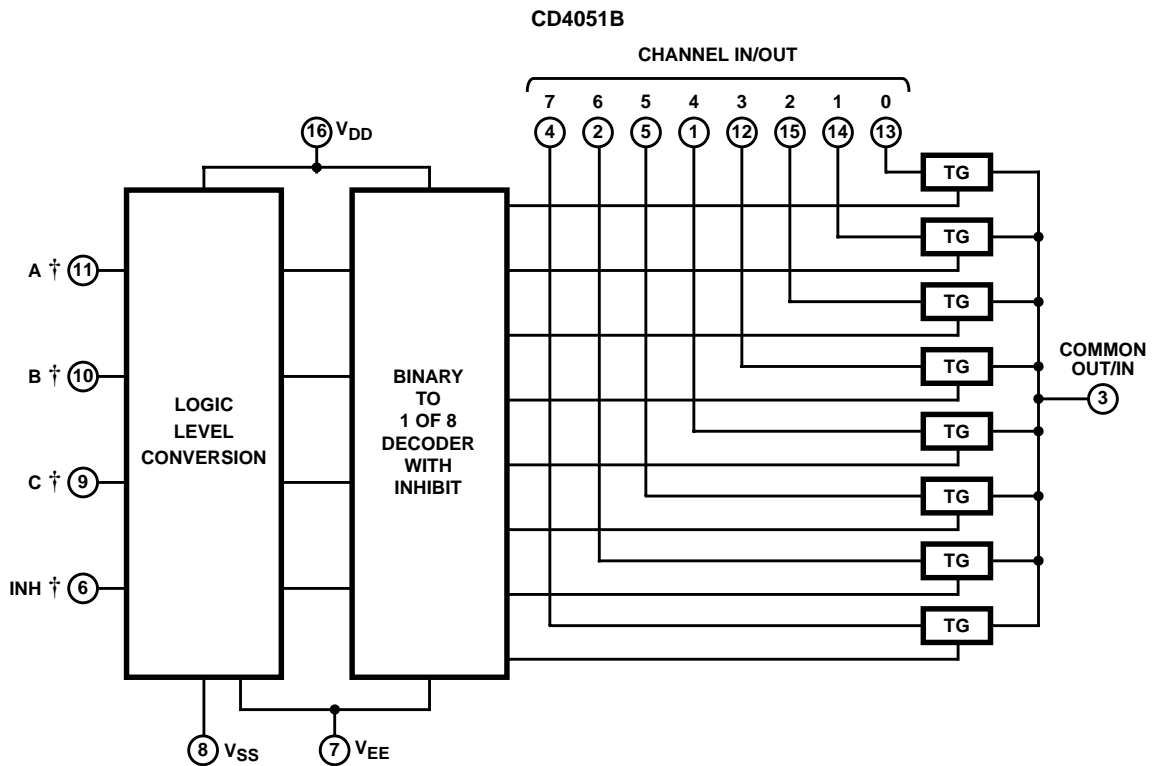
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

# CD4051B, CD4052B, CD4053B

## Pinouts

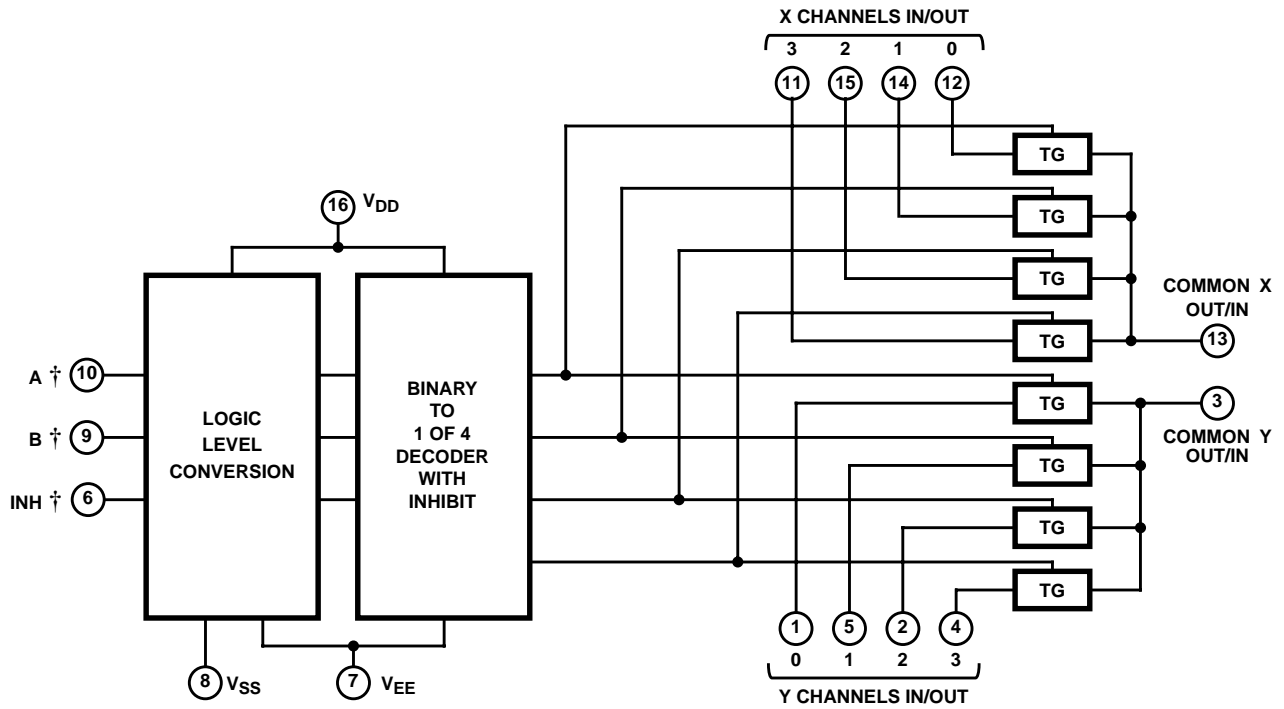


## Functional Block Diagrams

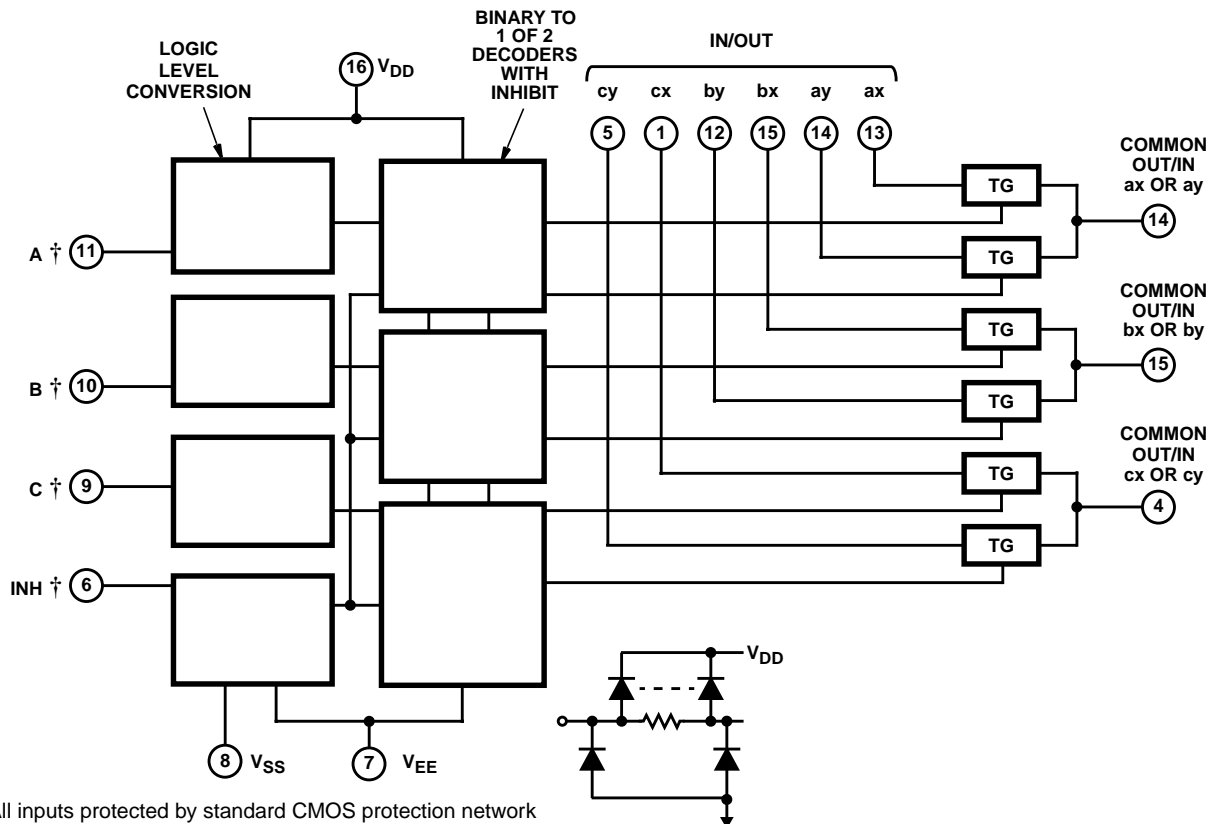


Functional Block Diagrams (Continued)

CD4052B



CD4053B



† All inputs protected by standard CMOS protection network

**CD4051B, CD4052B, CD4053B**

**TRUTH TABLES**

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
<b>CD4051B</b>				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
<b>CD4052B</b>				
INHIBIT	B		A	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
<b>CD4053B</b>				
INHIBIT	A OR B OR C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

X = Don't Care



## CD4051B, CD4052B, CD4053B

**Electrical Specifications** Common Conditions Here: If Whole Table is For the Full Temp. Range,  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_L = 100\Omega$ , Unless Otherwise Specified **(Continued)** (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	-55	-40	85	125	25			
									MIN	TYP	MAX	
<b>CONTROL (ADDRESS OR INHIBIT), <math>V_C</math></b>												
Input Low Voltage, $V_{IL}$ , Max	$V_{IL} = V_{DD}$ through 1k $\Omega$ ; $V_{IH} = V_{DD}$ through 1k $\Omega$	$V_{EE} = V_{SS}$ , $R_L = 1k\Omega$ to $V_{SS}$ , $I_{IS} < 2\mu A$ on All OFF Channels	5	1.5	1.5	1.5	1.5	-	-	1.5	V	
			10	3	3	3	3	-	-	3	V	
			15	4	4	4	4	-	-	4	V	
Input High Voltage, $V_{IH}$ , Min	$V_{IL} = V_{DD}$ through 1k $\Omega$ ; $V_{IH} = V_{DD}$ through 1k $\Omega$	$V_{EE} = V_{SS}$ , $R_L = 1k\Omega$ to $V_{SS}$ , $I_{IS} < 2\mu A$ on All OFF Channels	5	3.5	3.5	3.5	3.5	3.5	-	-	V	
			10	7	7	7	7	7	-	-	V	
			15	11	11	11	11	11	-	-	V	
Input Current, $I_{IN}$ (Max)	$V_{IN} = 0, 18$		18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$	
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figures 10, 11, 14	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	450	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-5	0	5	-	-	-	-	-	225	450	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 1k\Omega$	0	0	5	-	-	-	-	-	400	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-10	0	5	-	-	-	-	-	200	400	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	200	450	ns
		0	0	10	-	-	-	-	-	90	210	ns
		0	0	15	-	-	-	-	-	70	160	ns
		-10	0	5	-	-	-	-	-	130	300	ns
Input Capacitance, $C_{IN}$ (Any Address or Inhibit Input)				-	-	-	-	-	5	7.5	pF	

NOTE:

- Determined by minimum feasible leakage measurement for automatic testing.

### Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS		UNITS	
	$V_{IS}$ (V)	$V_{DD}$ (V)	$R_L$ (k $\Omega$ )	TYP			
Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)	5 (Note 3)	10	1	$V_{OS}$ at Common OUT/IN	CD4053	30	MHz
					CD4052	25	MHz
					CD4051	20	MHz
				$V_{EE} = V_{SS}$ , $20\text{Log} \frac{V_{OS}}{V_{IS}} = -3\text{dB}$	$V_{OS}$ at Any Channel	60	MHz

Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS		UNITS	
	V <sub>IS</sub> (V)	V <sub>DD</sub> (V)	R <sub>L</sub> (kΩ)	TYP			
Total Harmonic Distortion, THD	2 (Note 3)	5	10		0.3	%	
	3 (Note 3)	10			0.2	%	
	5 (Note 3)	15			0.12	%	
	V <sub>EE</sub> = V <sub>SS</sub> , f <sub>IS</sub> = 1kHz Sine Wave						%
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V <sub>OS</sub> at Common OUT/IN	CD4053	8	MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$					CD4052	10
				V <sub>OS</sub> at Any Channel		8	MHz
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels		3	MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$			Between Sections, CD4052 Only	Measured on Common	6	MHz
					Measured on Any Channel	10	MHz
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	MHz
						In Pin 15, Out Pin 14	6
Address-or-Inhibit-to-Signal Crosstalk	-	10	10 (Note 4)			65	mV <sub>PEAK</sub>
	V <sub>EE</sub> = 0, V <sub>SS</sub> = 0, t <sub>r</sub> , t <sub>f</sub> = 20ns, V <sub>CC</sub> = V <sub>DD</sub> - V <sub>SS</sub> (Square Wave)					65	mV <sub>PEAK</sub>

NOTES:

- Peak-to-Peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$
- Both ends of channel.

Typical Performance Curves

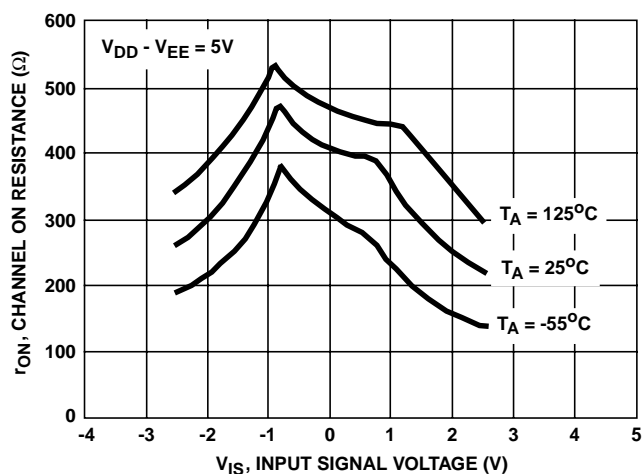


FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

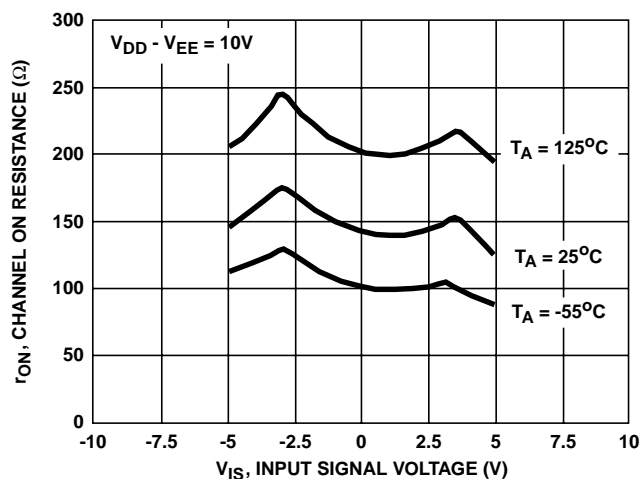


FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Curves (Continued)

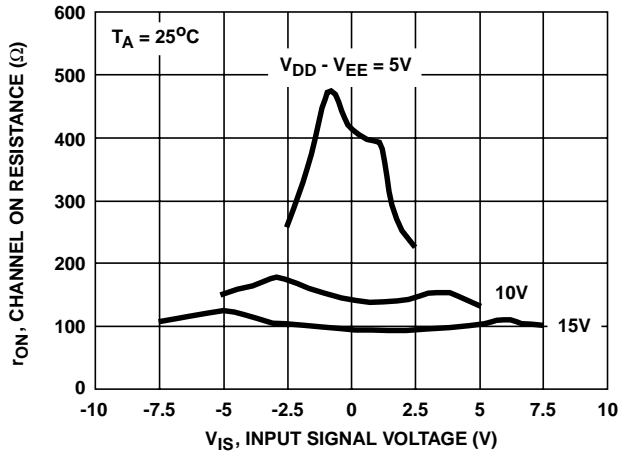


FIGURE 3. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

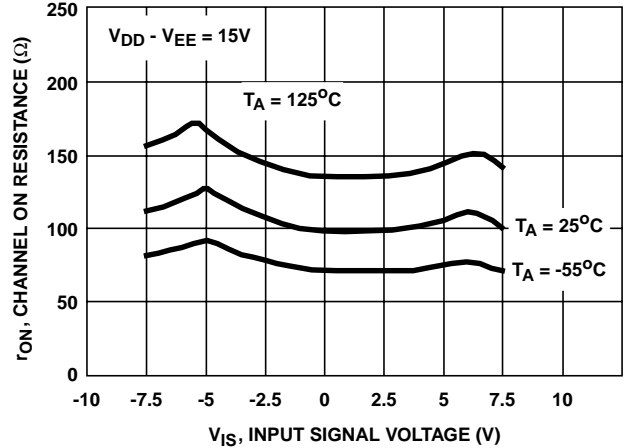


FIGURE 4. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

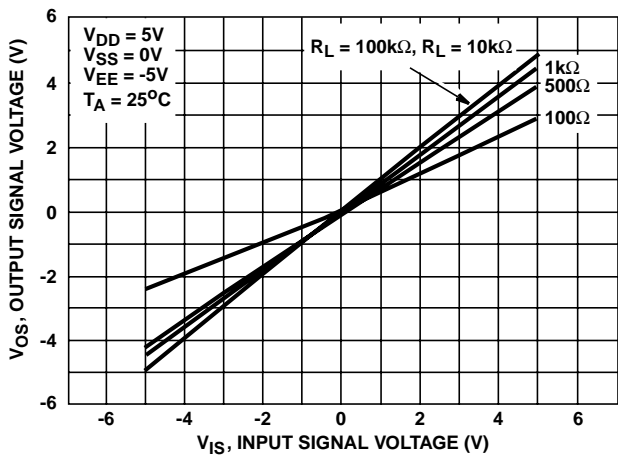


FIGURE 5. ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051B)

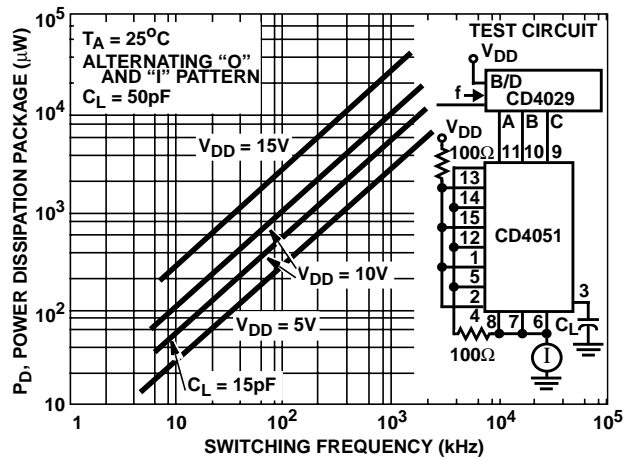


FIGURE 6. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051B)

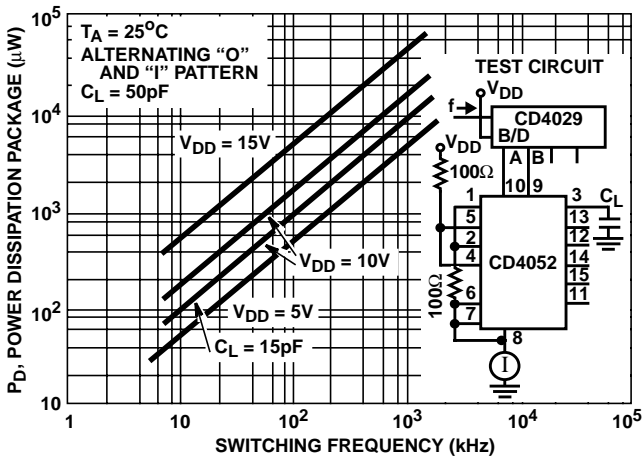


FIGURE 7. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052B)

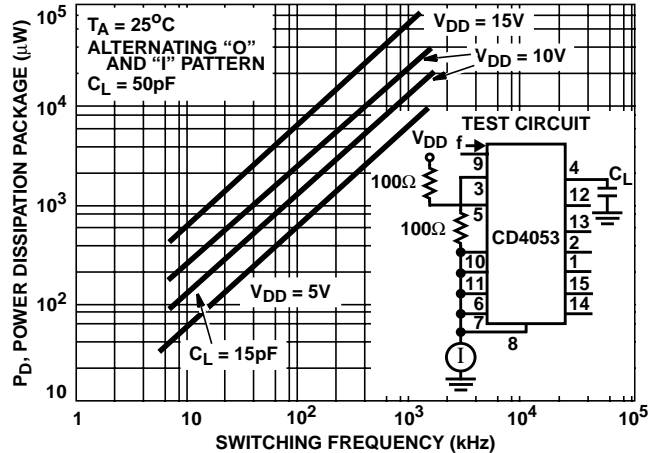
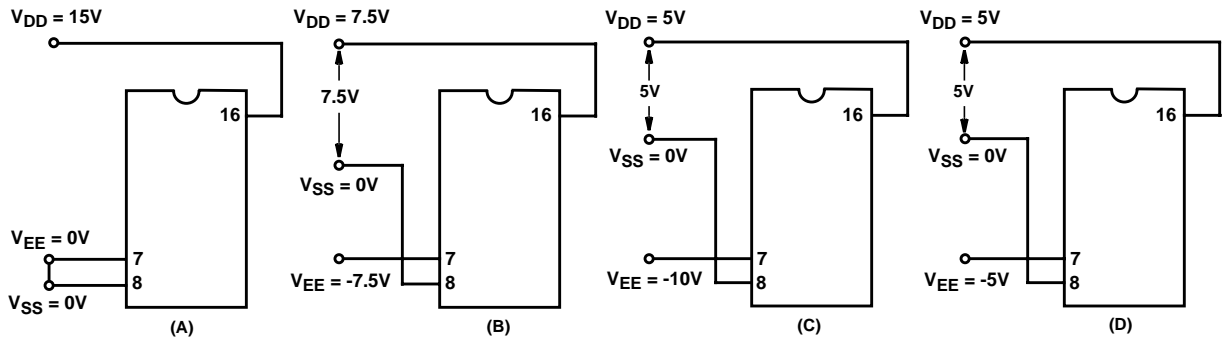


FIGURE 8. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053B)



Test Circuits and Waveforms



NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" =  $V_{SS}$  and "1" =  $V_{DD}$ . The analog signal (through the TG) may swing from  $V_{EE}$  to  $V_{DD}$ .

FIGURE 9. TYPICAL BIAS VOLTAGES

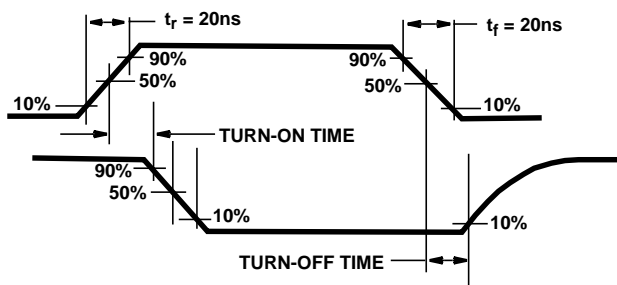


FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON ( $R_L = 1k\Omega$ )

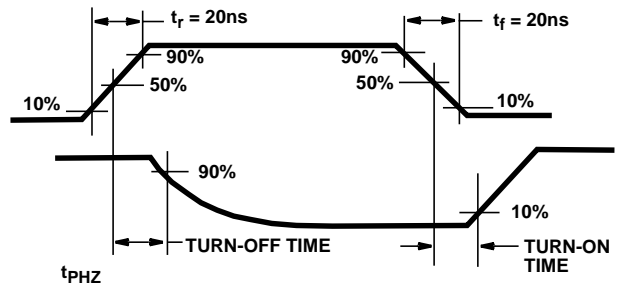


FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF ( $R_L = 1k\Omega$ )

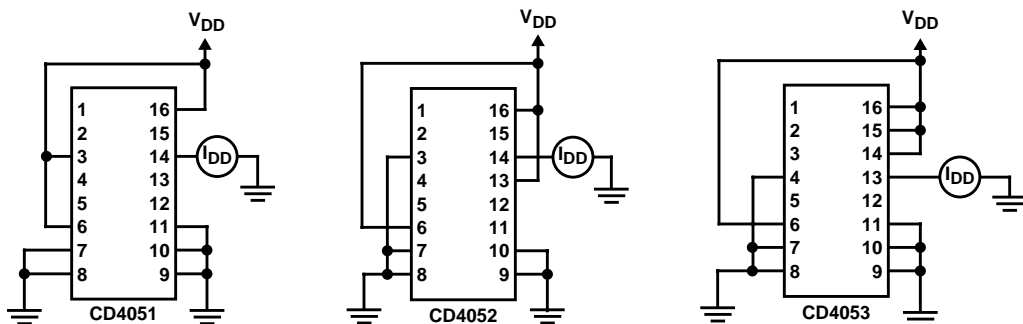


FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

Test Circuits and Waveforms (Continued)

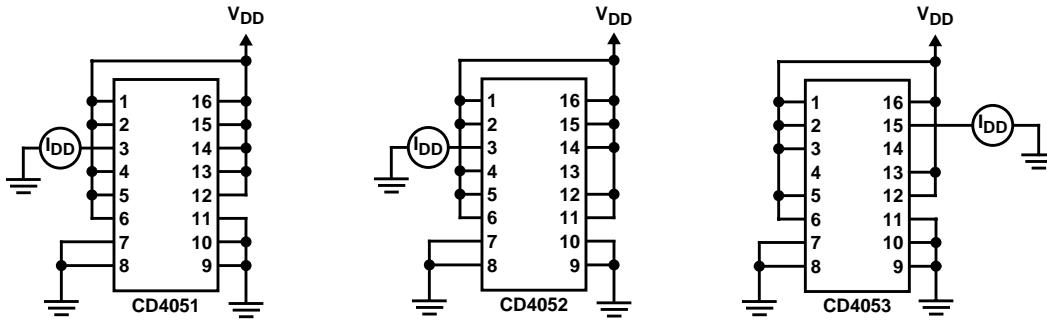


FIGURE 13. OFF CHANNEL LEAKAGE CURRENT - ALL CHANNELS OFF

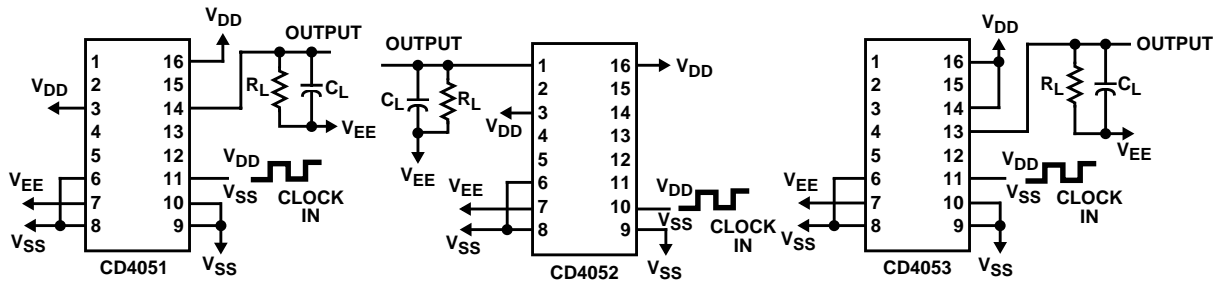


FIGURE 14. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

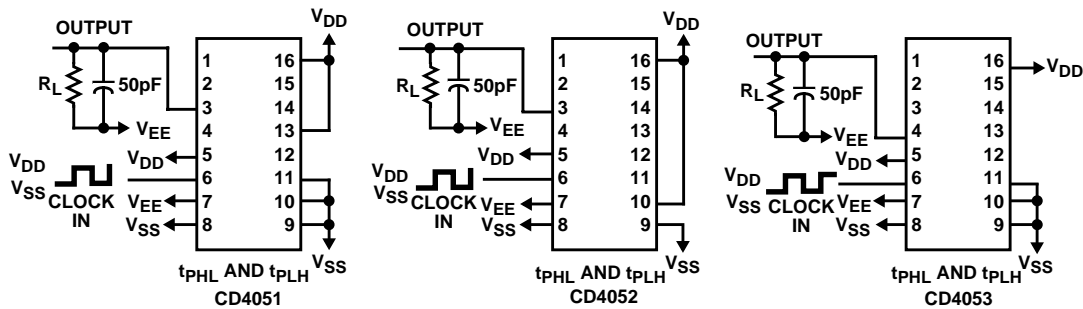
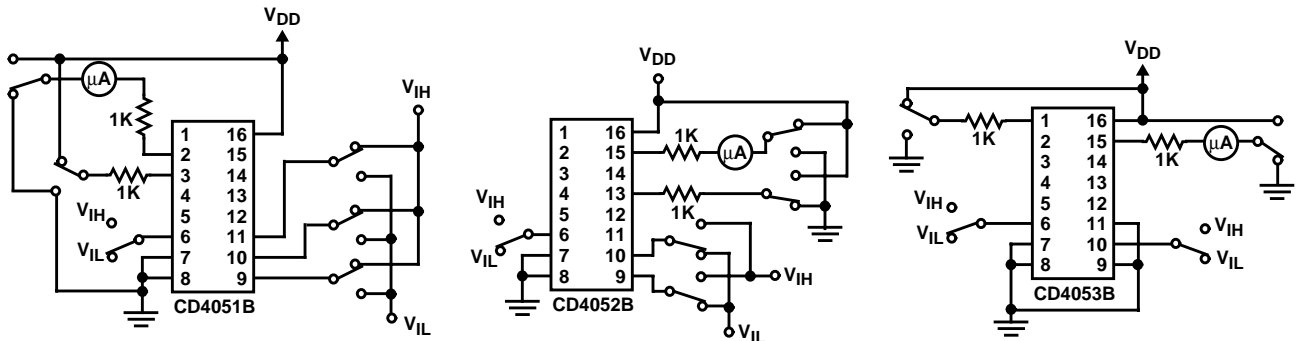


FIGURE 15. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT



MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 6)

MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 2x)

MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL by)

FIGURE 16. INPUT VOLTAGE TEST CIRCUITS (NOISE IMMUNITY)

Test Circuits and Waveforms (Continued)

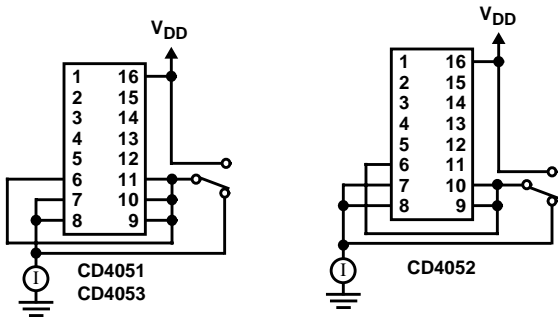


FIGURE 17. QUIESCENT DEVICE CURRENT

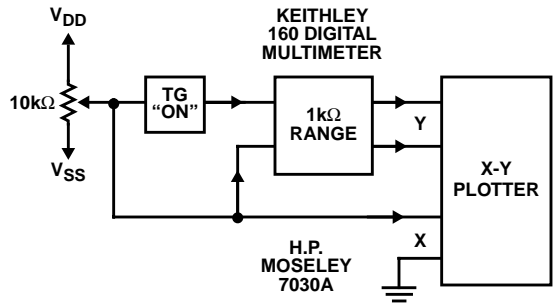


FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT

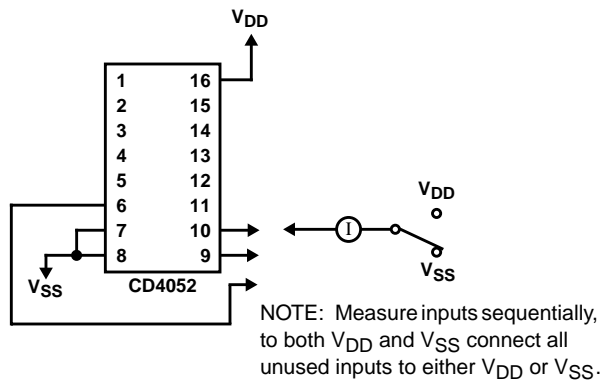
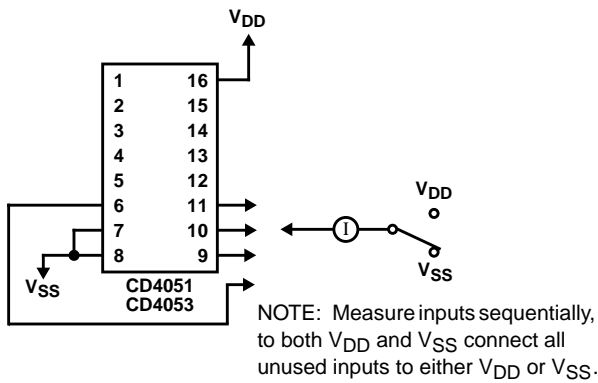


FIGURE 19. INPUT CURRENT

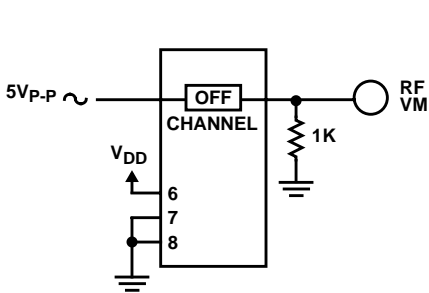


FIGURE 20. FEEDTHROUGH (ALL TYPES)

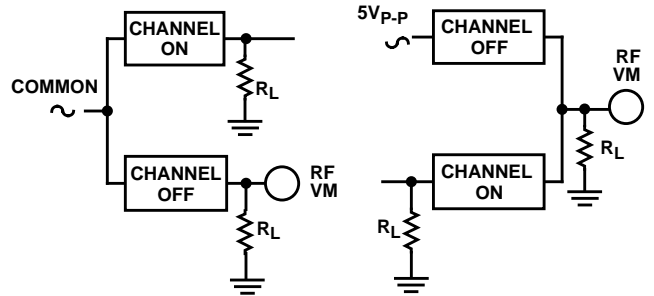


FIGURE 21. CROSSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)

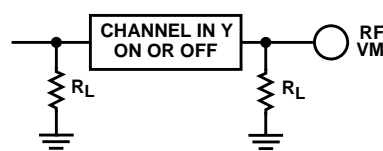
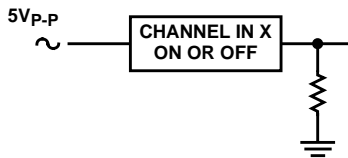


FIGURE 22. CROSSTALK BETWEEN DUALS OR TRIPLETS (CD4052B, CD4053B)

Test Circuits and Waveforms (Continued)

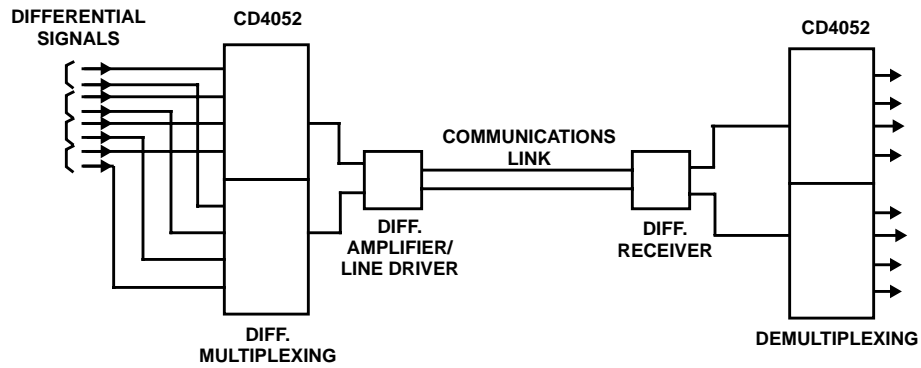


FIGURE 23. TYPICAL TIME-DIVISION APPLICATION OF THE CD4052B

**Special Considerations**

In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

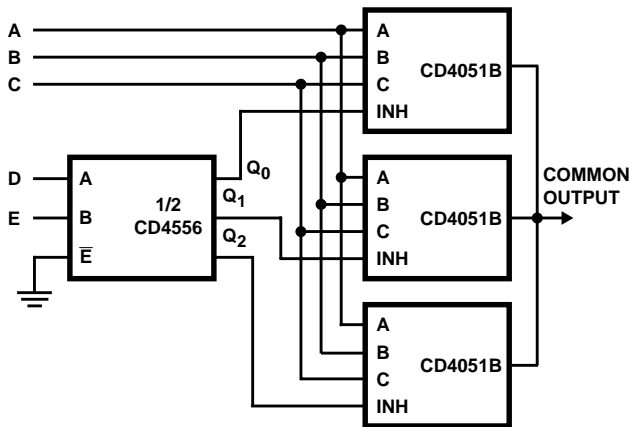
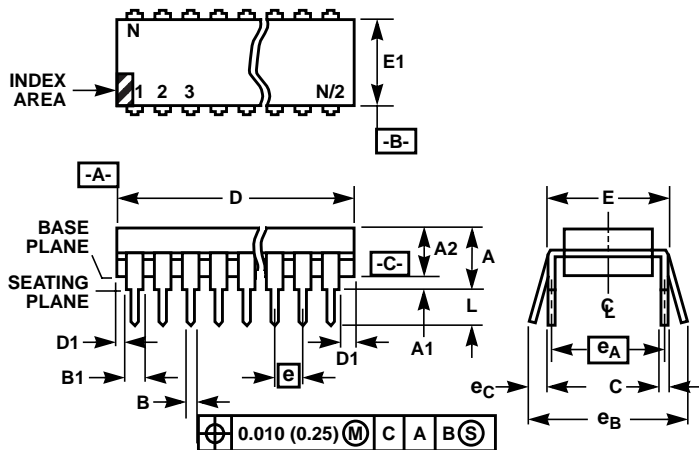


FIGURE 24. 24-TO-1 MUX ADDRESSING

Dual-In-Line Plastic Packages (PDIP)



NOTES:

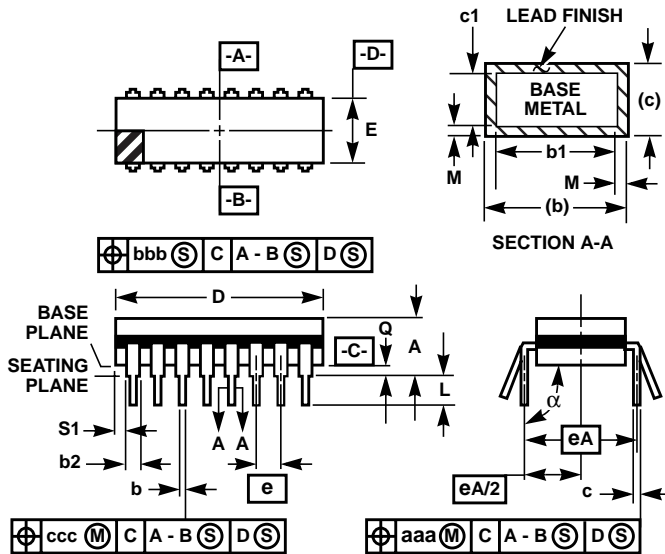
- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
- $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)  
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

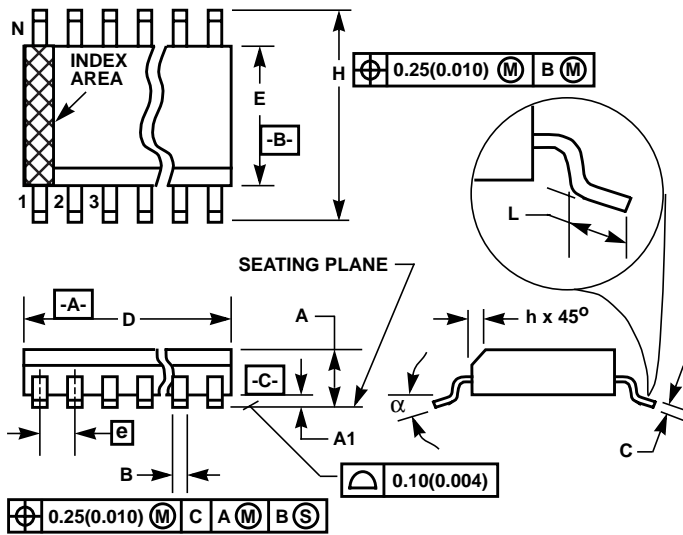
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
$\alpha$	90 <sup>o</sup>	105 <sup>o</sup>	90 <sup>o</sup>	105 <sup>o</sup>	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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Small Outline Plastic Packages (SOIC)



**M16.15** (JEDEC MS-012-AC ISSUE C)  
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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