FAIRCHILD

SEMICONDUCTOR®

August 2005

FDS8874
N-Channel PowerTrench® MOSFET
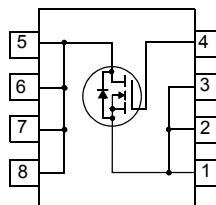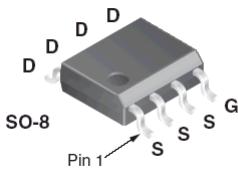
30V, 16A, 5.5mΩ

Features

- $r_{DS(ON)}$ = 5.5mΩ, V_{GS} = 10V, I_D = 16A

- $r_{DS(ON)}$ = 7.0mΩ, V_{GS} = 4.5V, I_D = 15A

- High performance trench technology for extremely low $r_{DS(ON)}$

- Low gate charge

- High power and current handling capability

- 100% Rg tested

- RoHS Compliant

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 50°C/W)	16	A
	Continuous (T_A = 25°C, V_{GS} = 4.5V, $R_{\theta JA}$ = 50°C/W)	15	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	265	mJ
P_D	Power dissipation	2.5	W
	Derate above 25°C	20	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8874	FDS8874	SO-8	330mm	12mm	2500 units

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$		30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24V$		-	-	1	μA
		$V_{GS} = 0V$	$T_A = 150°C$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm20V$		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 16A$, $V_{GS} = 10V$		-	0.0045	0.0055	Ω
		$I_D = 15A$, $V_{GS} = 4.5V$		-	0.0056	0.007	
		$I_D = 16A$, $V_{GS} = 10V$, $T_A = 150°C$		-	0.0078	0.0102	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	$V_{DS} = 15V$, $V_{GS} = 0V$, f = 1MHz		-	3000	3990	pF
C_{OSS}	Output Capacitance			-	600	800	pF
C_{RSS}	Reverse Transfer Capacitance			-	350	525	pF
R_G	Gate Resistance	f = 1MHz		0.4	1.6	4.0	Ω
Q_g	Total Gate Charge	$V_{GS} = 10V$	$V_{DD} = 15V$ $I_D = 16A$	-	56	72	nC
	Total Gate Charge	$V_{GS} = 5V$		-	30	38	nC
Q_{gs}	Gate to Source Gate Charge			-	8.0	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	5.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	10	-	nC
Switching Characteristics $(V_{GS} = 10V)$							
t_{ON}	Turn-On Time	$V_{DD} = 15V$, $I_D = 16A$ $V_{GS} = 10V$, $R_{GS} = 4.7\Omega$		-	-	81	ns
$t_{d(ON)}$	Turn-On Delay Time			-	9	-	ns
t_r	Rise Time			-	45	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	54	-	ns
t_f	Fall Time			-	20	-	ns
t_{OFF}	Turn-Off Time			-	-	111	ns
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 16A$		-	-	1.25	V
		$I_{SD} = 2.1A$		-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$		-	-	28	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$		-	-	13	nC

Notes:
1: Starting $T_J = 25°C$, L = 1mH, $I_{AS} = 23A$, $V_{DD} = 30V$, $V_{GS} = 10V$.
2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
3: $R_{\theta JA}$ is measured with 1.0 in^2 copper on FR-4 board

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## Typical Characteristics $T_A = 25°C$ unless otherwise noted
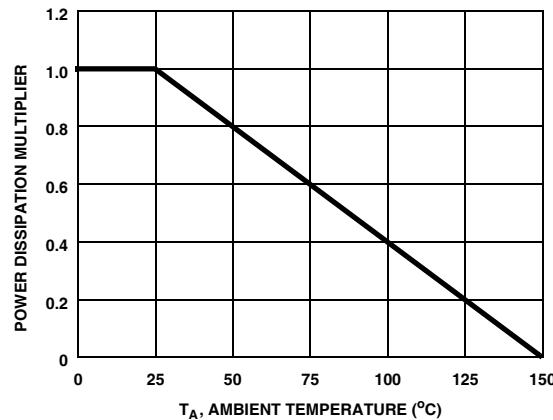
Figure 1. Normalized Power Dissipation vs Ambient Temperature
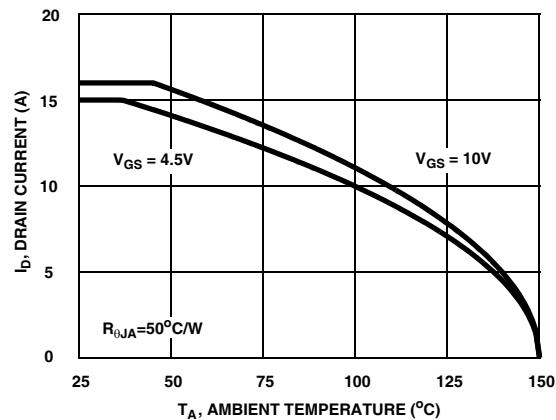
**Figure 2. Maximum Continuous Drain Current vs Ambient Temperature**

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_A$
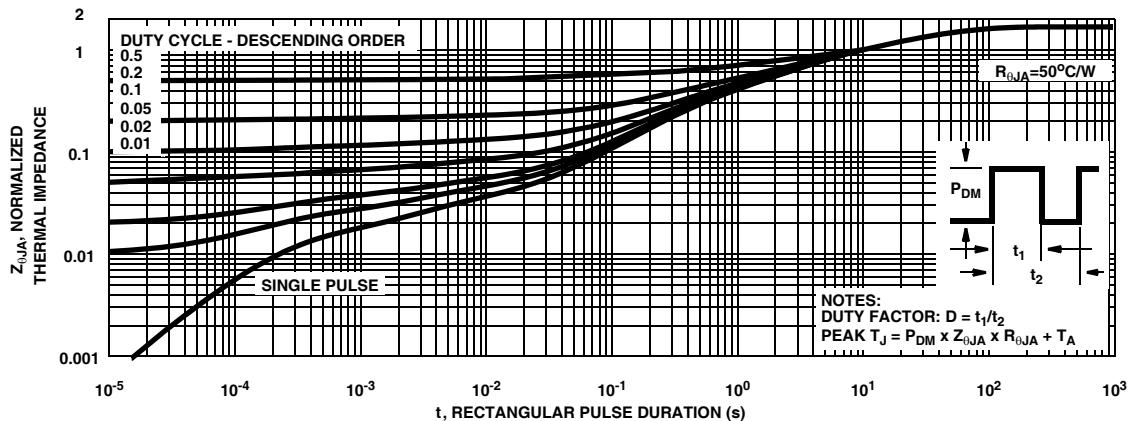
Figure 3. Normalized Maximum Transient Thermal Impedance

$T_A = 25°C$
FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_{25} \left[\sqrt{\frac{150 - T_A}{125}} \right]$$
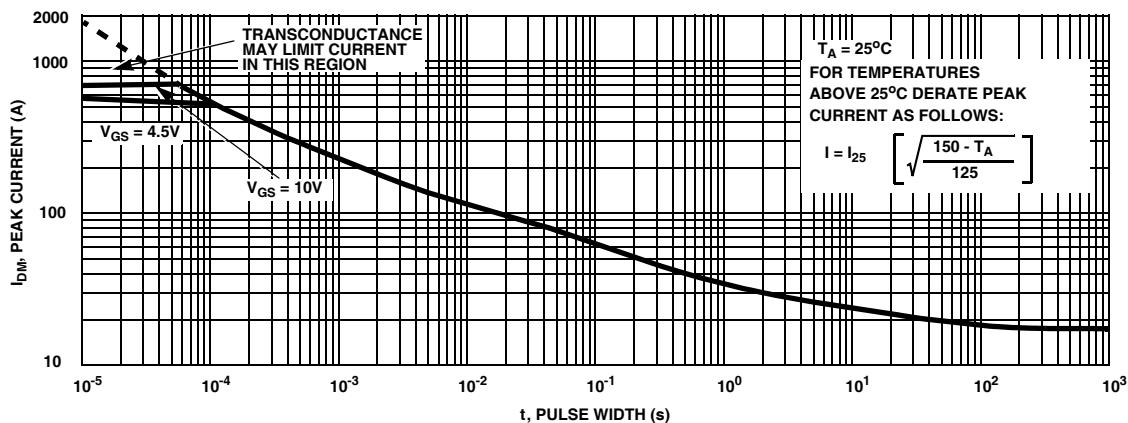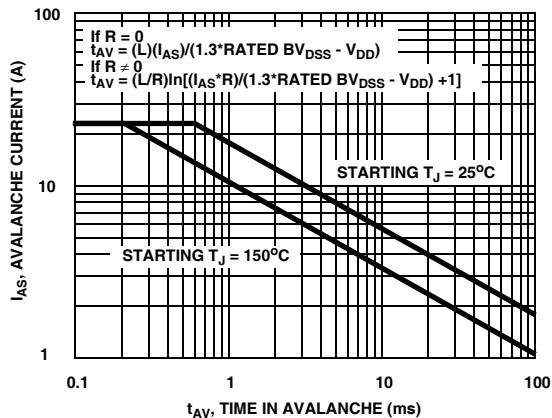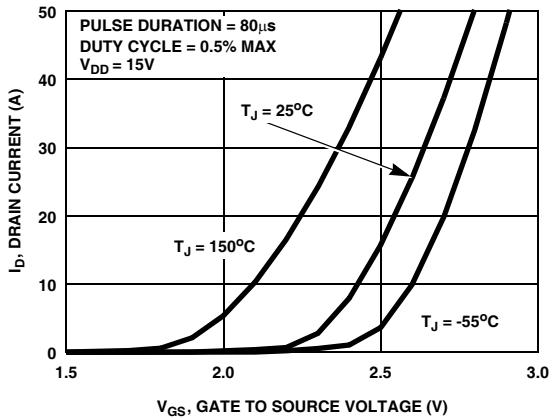
Figure 4. Peak Current Capability

Typical Characteristics T_A = 25°C unless otherwise noted

If R = 0
$t_{AV} = (L)(I_{AS})/(1.3*RATED\ BV_{DSS} - V_{DD})$
If R ≠ 0
$t_{AV} = (L/R)ln[(I_{AS}*R)/(1.3*RATED\ BV_{DSS} - V_{DD}) +1]$

STARTING T_J = 25°C

STARTING T_J = 150°C
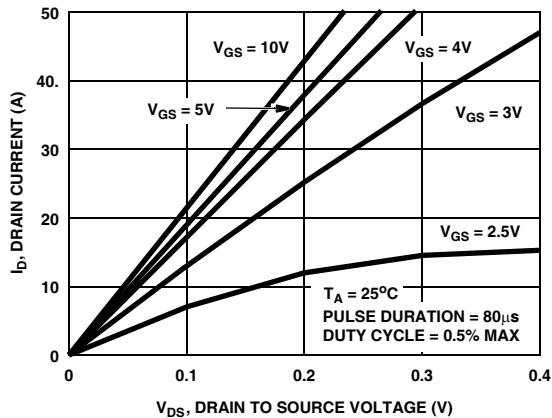
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
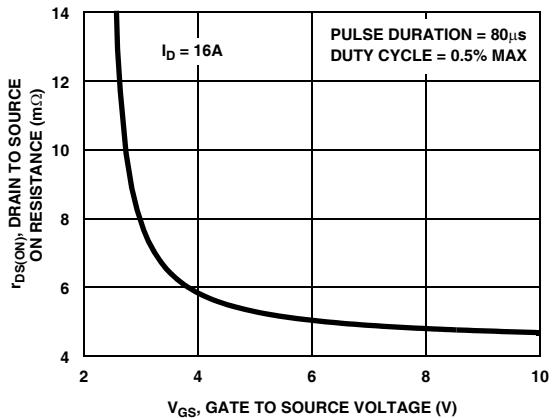
Figure 5. Unclamped Inductive Switching Capability

PULSE DURATION = 80μs
DUTY CYCLE = 0.5% MAX
V_{DD} = 15V

T_J = 25°C

T_J = 150°C

T_J = -55°C
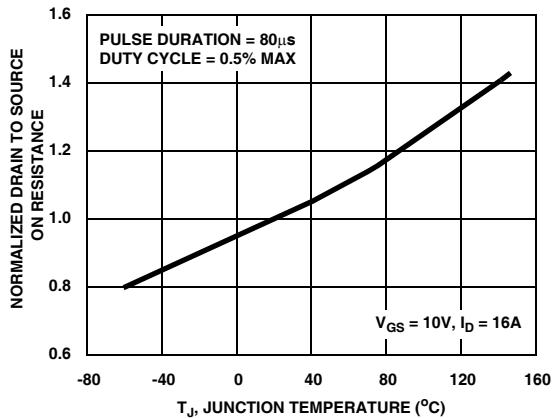
Figure 6. Transfer Characteristics

V_{GS} = 10V
V_{GS} = 4V
V_{GS} = 5V
V_{GS} = 3V
V_{GS} = 2.5V

T_A = 25°C
PULSE DURATION = 80μs
DUTY CYCLE = 0.5% MAX
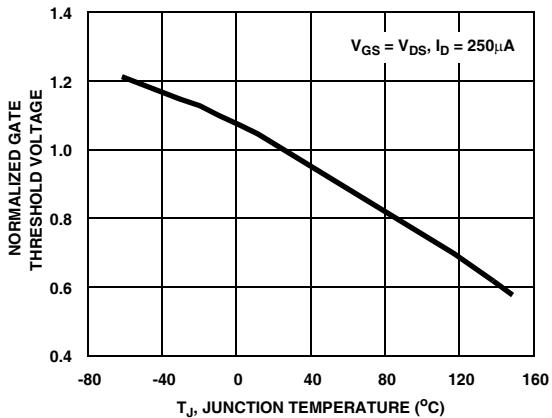
Figure 7. Saturation Characteristics

I_D = 16A

PULSE DURATION = 80μs
DUTY CYCLE = 0.5% MAX

Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

PULSE DURATION = 80μs
DUTY CYCLE = 0.5% MAX

V_{GS} = 10V, I_D = 16A

Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

V_{GS} = V_{DS}, I_D = 250μA

Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

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Typical Characteristics T_A = 25°C unless otherwise noted
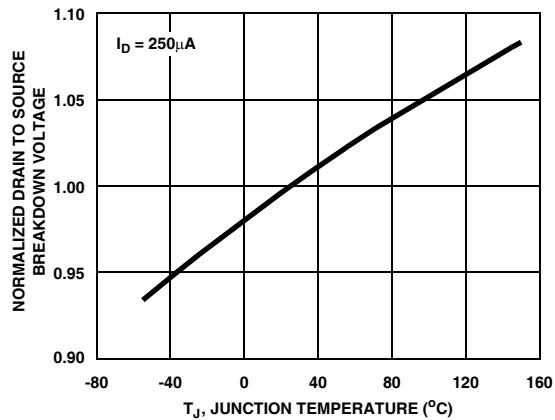
Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

$I_D = 250\mu A$
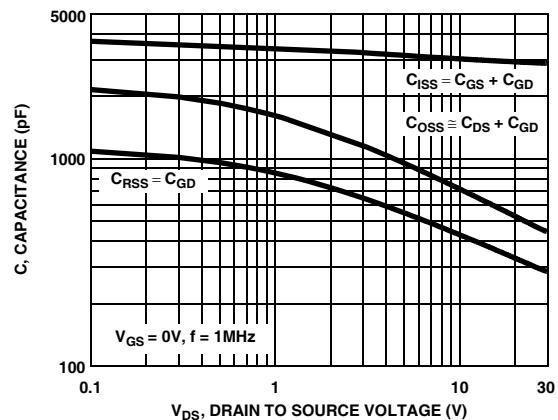
Figure 12. Capacitance vs Drain to Source Voltage

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} \cong C_{DS} + C_{GD}$

$C_{RSS} = C_{GD}$

$V_{GS} = 0V, f = 1MHz$
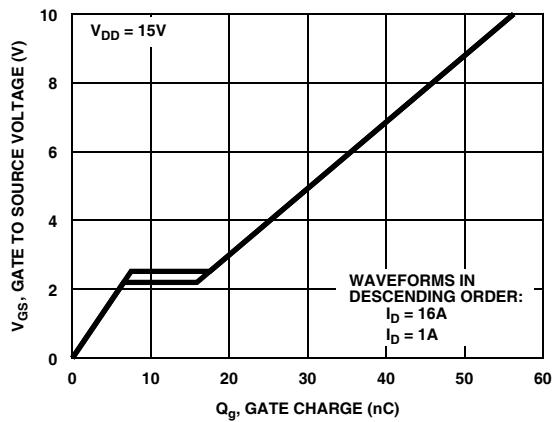
Figure 13. Gate Charge Waveforms for Constant Gate Currents

V_{DD} = 15V

WAVEFORMS IN DESCENDING ORDER:
I_D = 16A
I_D = 1A

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Test Circuits and Waveforms
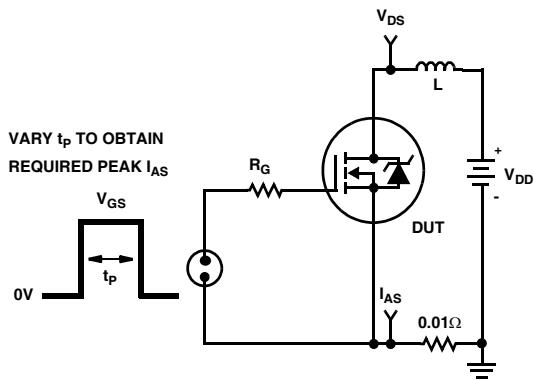
Figure 14. Unclamped Energy Test Circuit
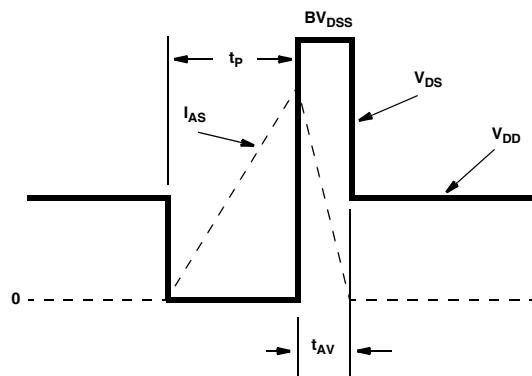
Figure 15. Unclamped Energy Waveforms
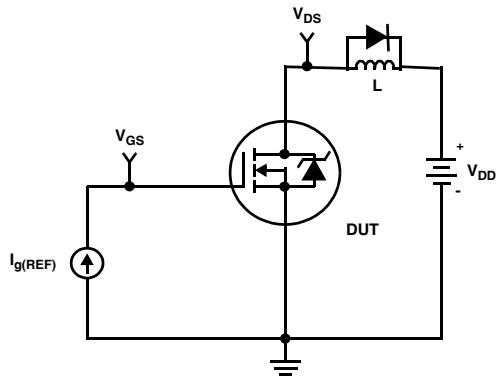
Figure 16. Gate Charge Test Circuit
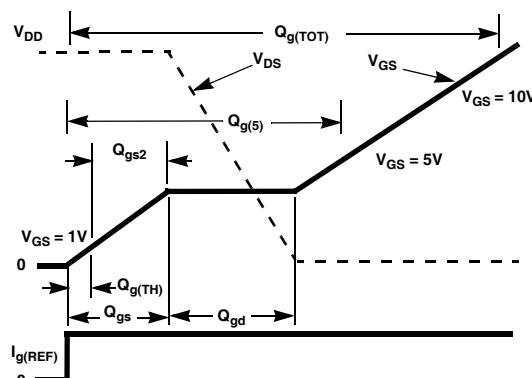
Figure 17. Gate Charge Waveforms
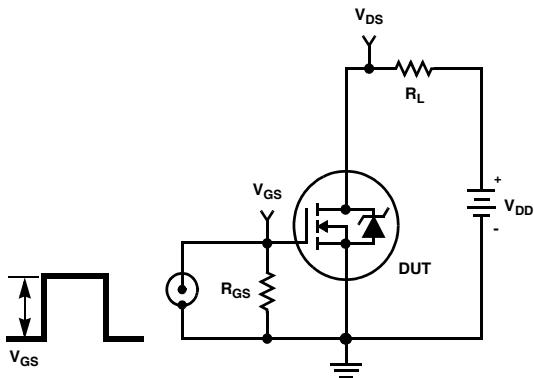
Figure 18. Switching Time Test Circuit
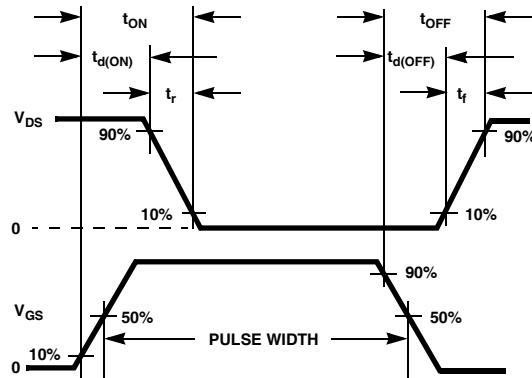
Figure 19. Switching Time Waveforms

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Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^{o}C), and thermal resistance $R_{\theta JA}$ (^{o}C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.

2. The number of copper layers and the thickness of the board.

3. The use of external heat sinks.

4. The use of thermal vias.

5. Air flow and board orientation.

6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + Area} \qquad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.
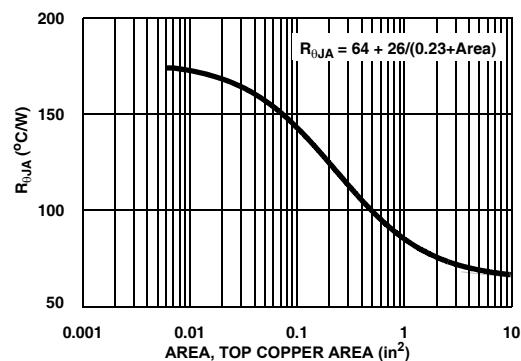

**Figure 21. Thermal Resistance vs Mounting Pad Area**
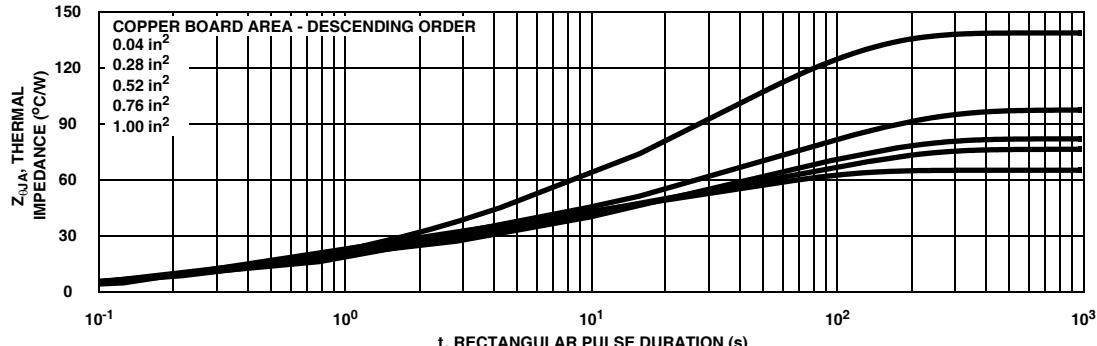
Figure 22. Thermal Impedance vs Mounting Pad Area

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PSPICE Electrical Model

```
.SUBCKT FDS8874 2 1 3 ;      rev May 2004
Ca 12 8 2.4e-9
Cb 15 14 2.4e-9
Cin 6 8 2.6e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 33.5
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 4e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 1e-10

RLgate 1 9 40
RLdrain 2 5 10
RLsource 3 7 1

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 2.35e-3
Rgate 9 20 1.9
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 2e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*500),10))}

.MODEL DbodyMOD D (IS=7E-12 IKF=10 N=1.01 RS=2.5e-3 TRS1=8e-4 TRS2=2e-7
+ CJO=1.13e-9 M=0.57 TT=1e-15 XTI=1.2)
.MODEL DbreakMOD D (RS=8e-2 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=1.13e-9 IS=1e-30 N=10 M=0.4)

.MODEL MmedMOD NMOS (VTO=1.8 KP=9 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.9)
.MODEL MstroMOD NMOS (VTO=2.2 KP=380 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=1.49 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=19 RS=0.1)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-8e-7)
.MODEL RdrainMOD RES (TC1=5e-3 TC2=1e-5)
.MODEL RSLCMOD RES (TC1=1e-4 TC2=1e-6)
.MODEL RsourceMOD RES (TC1=1e-4 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-2.1e-3 TC2=-8e-6)
.MODEL RvtempMOD RES (TC1=-1.8e-3 TC2=2e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2.0)

.ENDS
```
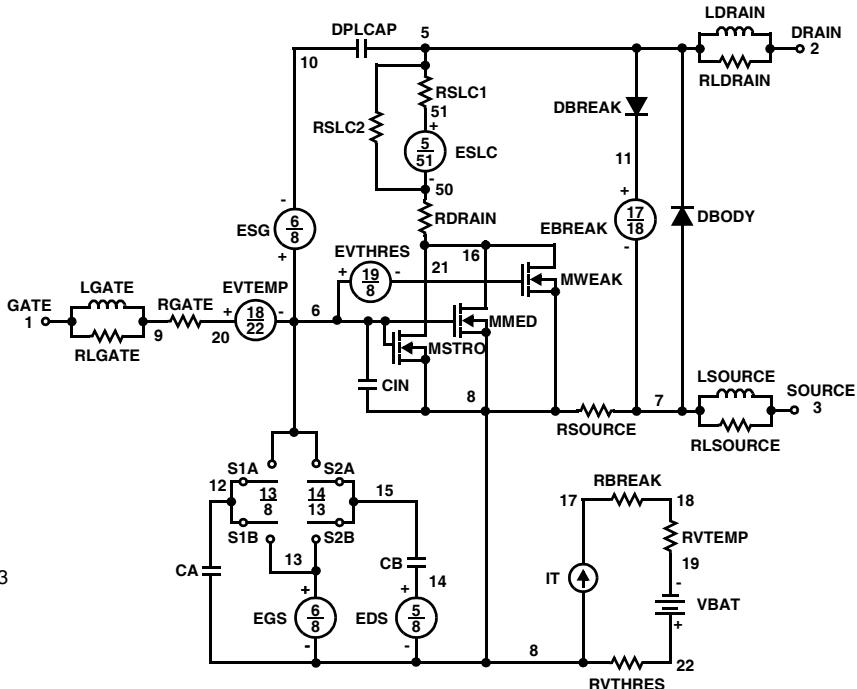
Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

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SABER Electrical Model

```
REV May 2004
template FDS8874 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=7e-12,ikf=10,nl=1.01,rs=2.5e-3,trs1=8e-4,trs2=2e-7,cjo=1.13e-9,m=0.57,tt=1e-15,xti=1.2)
dp..model dbreakmod = (rs=8e-2,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=1.13e-9,isl=10e-30,nl=10,m=0.4)
m..model mmedmod = (type=_n,vto=1.8,kp=9,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=2.2,kp=380,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=1.49,kp=0.05,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2.0,voff=-0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2.0)
c.ca n12 n8 = 2.4e-9
c.cb n15 n14 = 2.4e-9
c.cin n6 n8 = 2.6e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 33.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 4e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 1e-10

res.rlgate n1 n9 = 40
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 1

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=8.3e-4,tc2=-8e-7
res.rdrain n50 n16  = 2.35e-3, tc1=5e-3,tc2=1e-5
res.rgate n9 n20 = 1.9
res.rslc1 n5 n51  = 1e-6, tc1=1e-4,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 2e-3, tc1=1e-4,tc2=1e-6
res.rvthres n22 n8  = 1, tc1=-2.1e-3,tc2=-8e-6
res.rvtemp n18 n19  = 1, tc1=-1.8e-3,tc2=2e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/500))** 10))

}
}
```
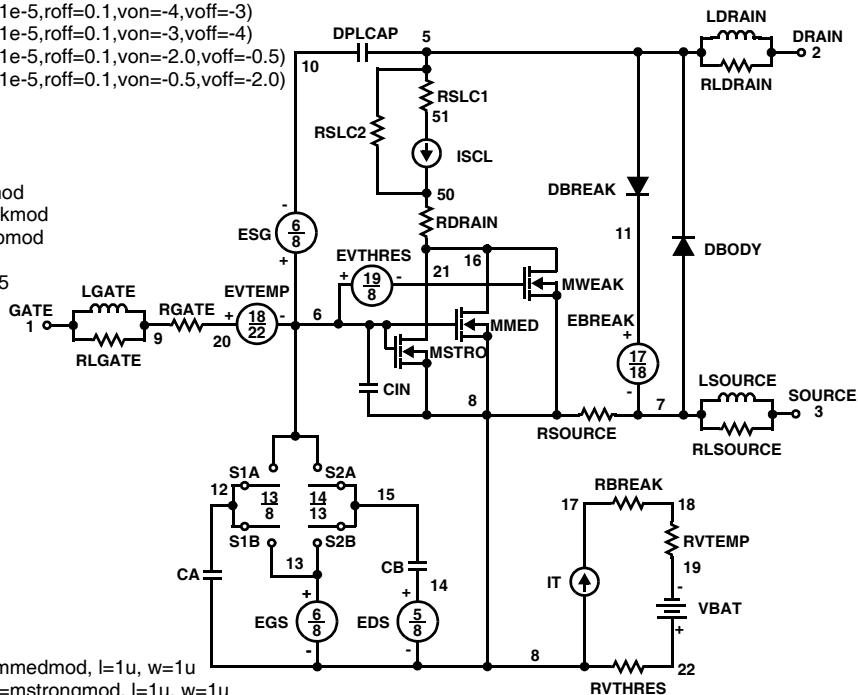
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SPICE Thermal Model

REV May 2004
FDS8874T
Copper Area =1.0 in^2
CTHERM1 TH 8 2.0e-3
CTHERM2 8 7 5.0e-3
CTHERM3 7 6 1.0e-2
CTHERM4 6 5 4.0e-2
CTHERM5 5 4 9.0e-2
CTHERM6 4 3 2e-1
CTHERM7 3 2 1
CTHERM8 2 TL 3

RTHERM1 TH 8 1e-1
RTHERM2 8 7 5e-1
RTHERM3 7 6 1
RTHERM4 6 5 5
RTHERM5 5 4 8
RTHERM6 4 3 12
RTHERM7 3 2 18
RTHERM8 2 TL 25

SABER Thermal Model

Copper Area = 1.0 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 =2.0e-3
ctherm.ctherm2 8 7 =5.0e-3
ctherm.ctherm3 7 6 =1.0e-2
ctherm.ctherm4 6 5 =4.0e-2
ctherm.ctherm5 5 4 =9.0e-2
ctherm.ctherm6 4 3 =2e-1
ctherm.ctherm7 3 2 1
ctherm.ctherm8 2 tl 3

rtherm.rtherm1 th 8 =1e-1
rtherm.rtherm2 8 7 =5e-1
rtherm.rtherm3 7 6 =1
rtherm.rtherm4 6 5 =5
rtherm.rtherm5 5 4 =8
rtherm.rtherm6 4 3 =12
rtherm.rtherm7 3 2 =18
rtherm.rtherm8 2 tl =25
}

th   JUNCTION

RTHERM1   CTHERM1
8
RTHERM2   CTHERM2
7
RTHERM3   CTHERM3
6
RTHERM4   CTHERM4
5
RTHERM5   CTHERM5
4
RTHERM6   CTHERM6
3
RTHERM7   CTHERM7
2
RTHERM8   CTHERM8

tl   CASE
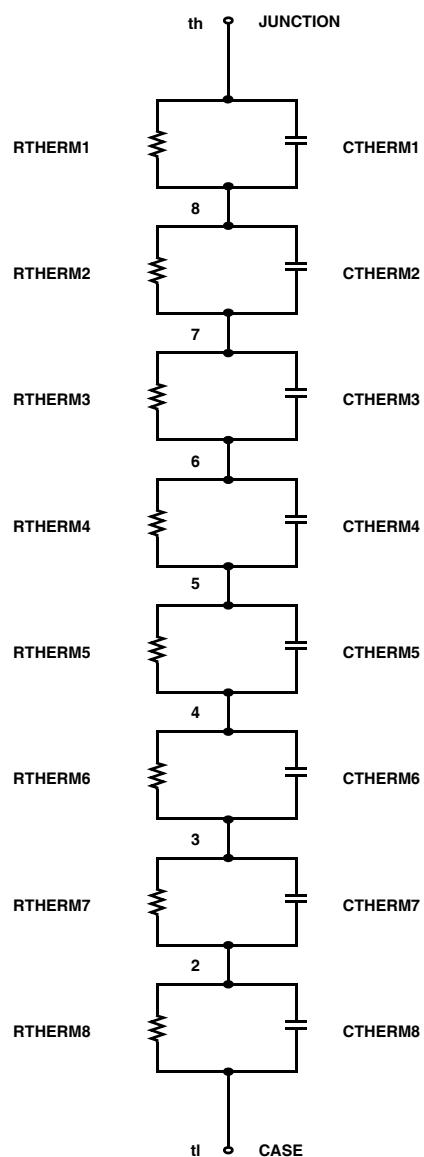
TABLE 1. THERMAL MODELS

COMPONANT	0.04 in^2	0.28 in^2	0.52 in^2	0.76 in^2	1.0 in^2
CTHERM6	1.2e-1	1.5e-1	2.0e-1	2.0e-1	2.0e-1
CTHERM7	0.5	1.0	1.0	1.0	1.0
CTHERM8	1.3	2.8	3.0	3.0	3.0
RTHERM6	26	20	15	13	12
RTHERM7	39	24	21	19	18
RTHERM8	55	38.7	31.3	29.7	25

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|				
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Bottomless™	FASTr™	ISOPLANAR™	PowerEdge™	SuperSOT™-3
CoolFET™	FPS™	LittleFET™	PowerSaver™	SuperSOT™-6
CROSSVOLT™	FRFET™	MICROCOUPLER™	PowerTrench®	SuperSOT™-8
DOME™	GlobalOptoisolator™	MicroFET™	QFET®	SyncFET™
EcoSPARK™	GTO™	MicroPak™	QS™	TinyLogic®
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EnSigna™	I²C™	MSX™	Quiet Series™	TruTranslation™
FACT™	i-Lo™	MSXPro™	RapidConfigure™	UHC™
		OCX™	RapidConnect™	UltraFET®
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