

NTHS4101P

Power MOSFET

-20 V, 6.7 A, P-Channel ChipFET™

Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low $R_{DS(on)}$ at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb-Free Package is Available

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-20	V_{dc}
Gate-to-Source Voltage - Continuous	V_{GS}	± 8.0	V_{dc}
Drain Current - Continuous - 5 seconds	I_D	-4.8	A
	I_D	-6.7	A
Total Power Dissipation Continuous @ $T_A = 25^\circ\text{C}$ (5 sec) @ $T_A = 25^\circ\text{C}$ Continuous @ 85°C (5 sec) @ 85°C	P_D	1.3	W
		2.5	
		0.7	
		1.3	
Continuous Source Current	I_S	-4.8	A
Thermal Resistance (Note 1) Junction-to-Ambient, 5 sec Junction-to-Ambient, Continuous	$R_{\theta JA}$ $R_{\theta JA}$	50	$^\circ\text{C/W}$
		95	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

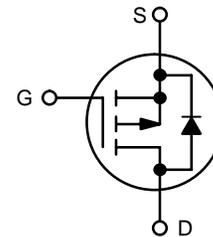
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



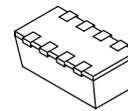
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-20 V	21 m Ω @ -4.5 V	-6.7 A
	30 m Ω @ -2.5 V	
	42 m Ω @ -1.8 V	

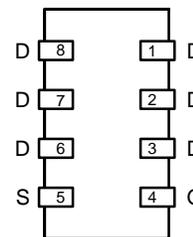


P-Channel MOSFET

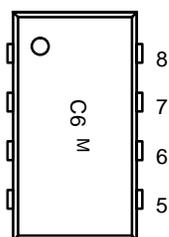


ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



MARKING DIAGRAM



C6 = Specific Device Code
M = Month Code

ORDERING INFORMATION

Device	Package	Shipping†
NTHS4101PT1	ChipFET	3000 Tape / Reel
NTHS4101PT1G	ChipFET (Pb-free)	3000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHS4101P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	V _{(Br)DSS}	V _{GS} = 0 V _{dc} , I _D = -250 μA _{dc}	-20			V _{dc}
Gate-Body Leakage Current Zero	I _{GSS}	V _{DS} = 0 V _{dc} , V _{GS} = ±8.0 V _{dc}			±100	nA _{dc}
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V _{dc} , V _{GS} = 0 V _{dc} V _{DS} = -16 V _{dc} , V _{GS} = 0 V _{dc} , T _J = 85°C			-1.0 -5.0	μA _{dc}

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA _{dc}	-0.45		-1.5	V _{dc}
Static Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5 V _{dc} , I _D = -4.8 A _{dc} V _{GS} = -2.5 V _{dc} , I _D = -4.2 A _{dc} V _{GS} = -1.8 V _{dc} , I _D = -1.0 A _{dc}		21 30 42	34 40 52	mΩ
Forward Transconductance	g _{FS}	V _{DS} = -5.0 V _{dc} , I _D = -4.8 A _{dc}		15		S
Diode Forward Voltage	V _{SD}	I _S = -4.8 A _{dc} , V _{GS} = 0 V _{dc}		-0.8	-1.2	V

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{DS} = -16 V _{dc} V _{GS} = 0 V f = 1.0 MHz		2100		pF
Output Capacitance	C _{oss}			290		
Transfer Capacitance	C _{rss}			200		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{DD} = -16 V _{dc} V _{GS} = -4.5 V _{dc} I _D = -4.5 A _{dc} R _G = 2.5 Ω		8.0		ns
Rise Time	t _r			28		
Turn-Off Delay Time	t _{d(off)}			75		
Fall Time	t _f			60		
Gate Charge	Q _g	V _{GS} = -4.5 V _{dc} I _D = -4.5 A _{dc} V _{DS} = -16 V _{dc} (Note 3)		25	35	nC
	Q _{gs}			4.0		
	Q _{gd}			7.0		

- Pulse Test: Pulse Width = 250 μs, Duty Cycle = 2%.
- Switching characteristics are independent of operating junction temperatures.

NTHS4101P

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

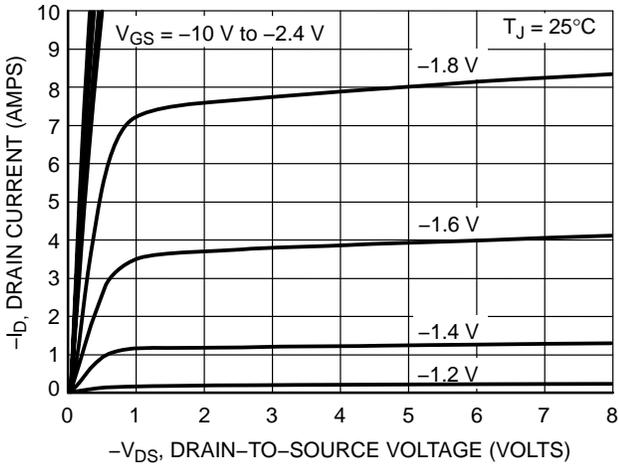


Figure 1. On-Region Characteristics

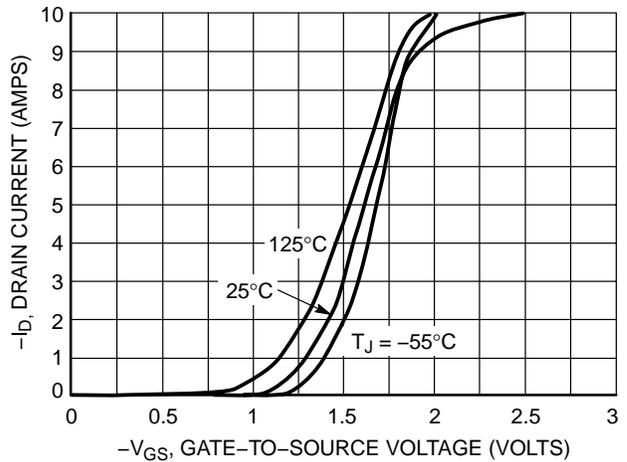


Figure 2. Transfer Characteristics

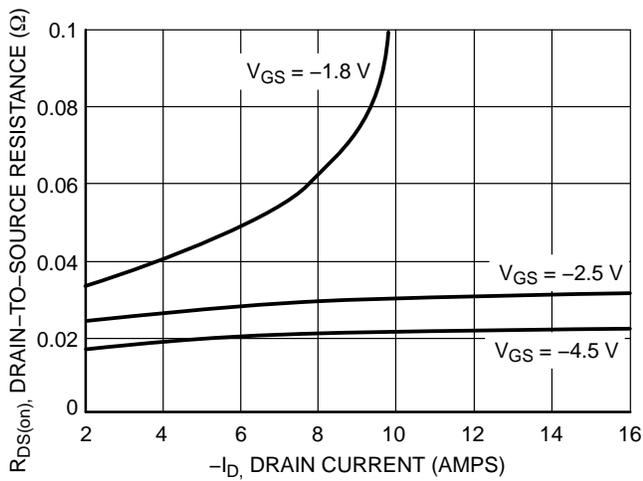


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

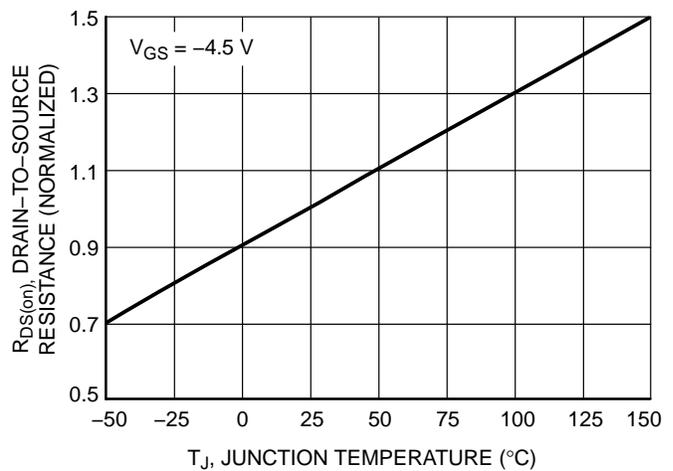


Figure 4. On-Resistance Variation with Temperature

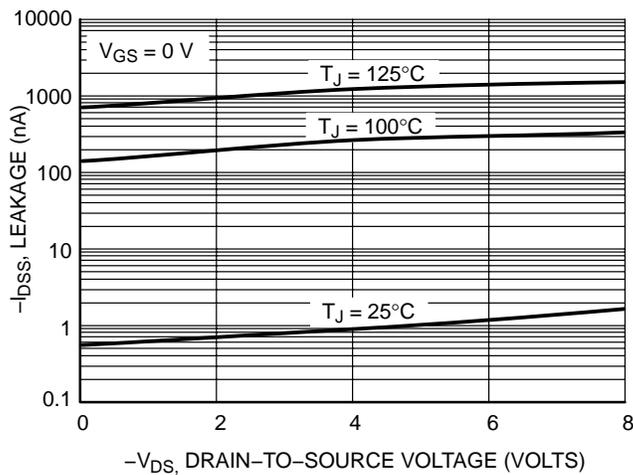


Figure 5. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

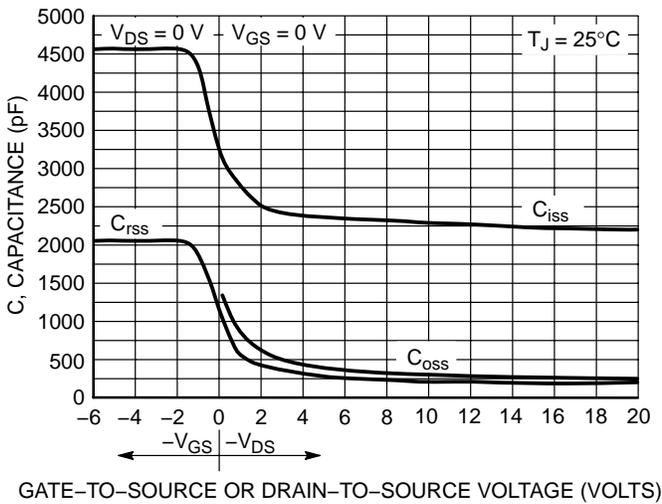


Figure 6. Capacitance Variation

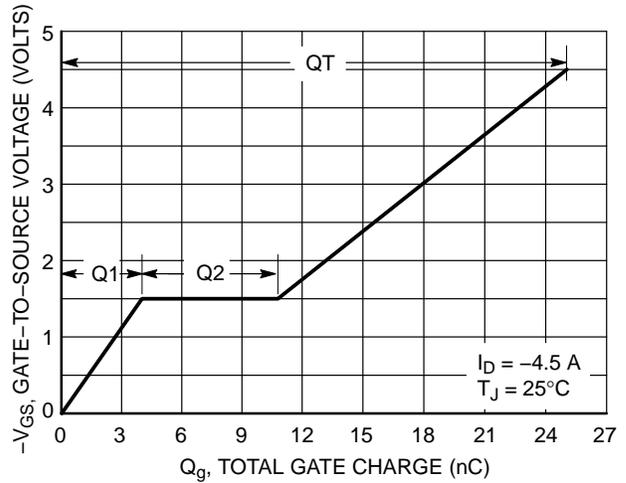


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

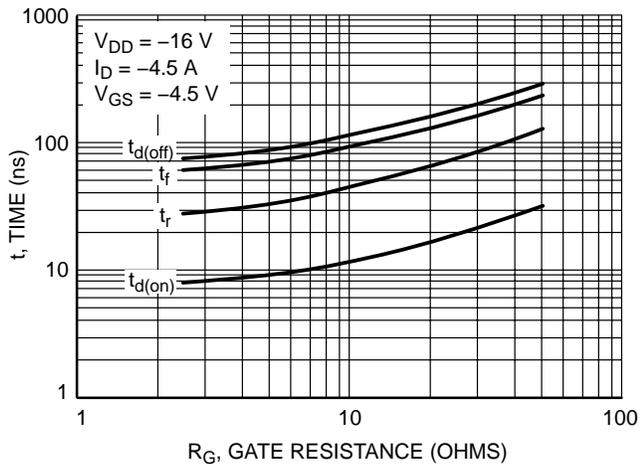


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

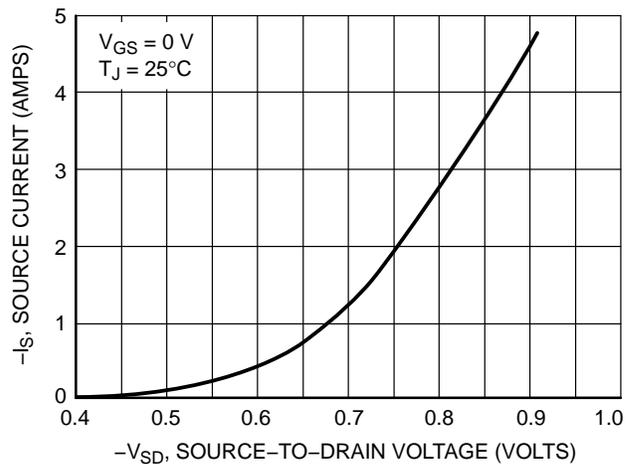


Figure 9. Diode Forward Voltage vs. Current

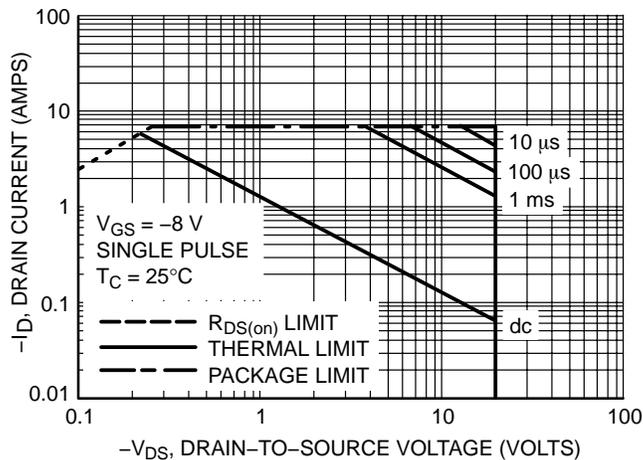
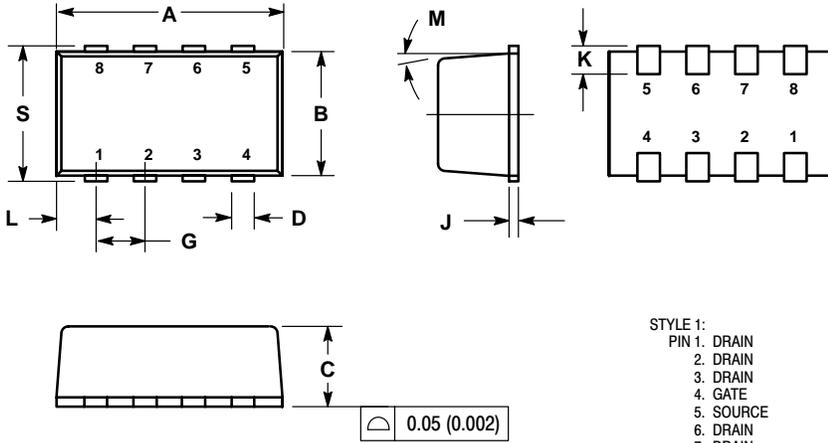


Figure 10. Maximum Rated Forward Biased Safe Operating Area

NTHS4101P

PACKAGE DIMENSIONS

ChipFET
CASE 1206A-03
ISSUE E



NOTES:

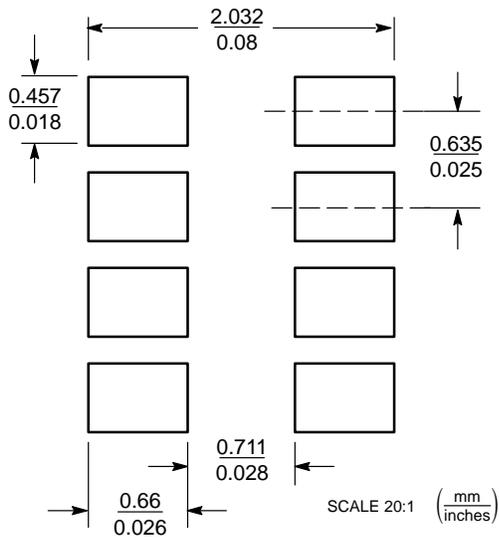
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

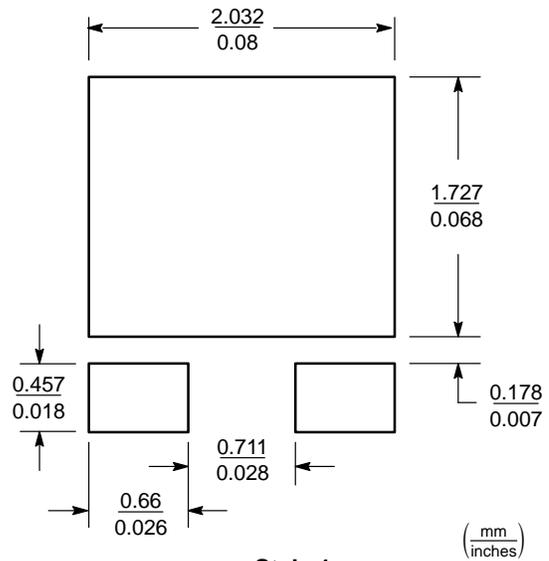
STYLE 1:

1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINTS*



Basic



Style 1

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ChipFET is a trademark of Vishay Siliconix.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.