I. General Description

The EM78861 is an 8-bit RISC type microprocessor with low power , high speed CMOS technology . Integrated onto a single chip are on chip watchdog (WDT) , RAM , ROM , programmable real time clock /counter , internal interrupt , power down mode and tri-state I/O .

II. Feature

CPU

- Operating voltage range : 2.5V～3.6V
- 32K×13 on chip Program ROM
- 2M on chip Data ROM
- 2.6K×8 on chip RAM
- Up to 32 bi-directional tri-state I/O ports
- 8 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- Two sets of 8 bit counters can be interrupt sources
- Programmable free running on chip watchdog timer
- 99.9% single instruction cycle commands
- Three modes

Mode	CPU	Main clock	Sub clock
Idle	Off	Off	On
Green	On	Off	On
Normal	On	On	On

- Power on voltage detector
- Input port wake up function
- 11 interrupt source , 8 external , 3 internal
- Sub - Clock frequency 32.768KHz crystal oscillator
- Main - Clock frequency 3MHz PLL ,1.5MHz,0.75MHZ
- 8 bit Sound generator
- Low standby current
- Die form

III. Application

1. Data Bank
2. LCD toy
3. Education computer

IV. Pin Configuration

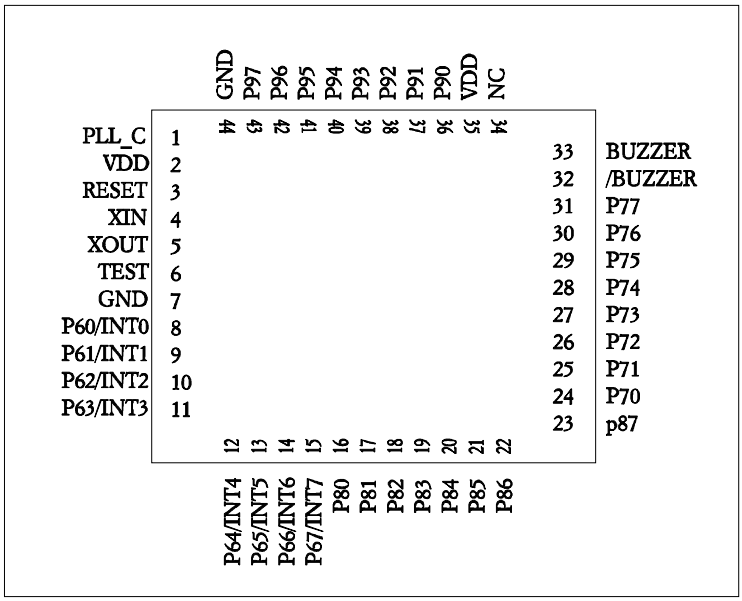


Fig1. Pin Assignment

V. Functional Block Diagram

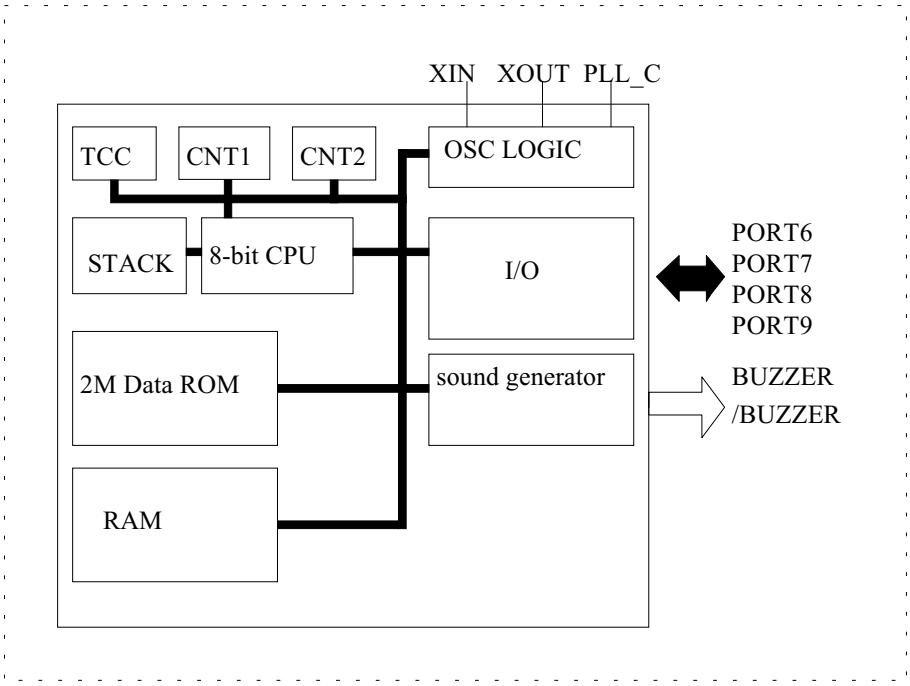


Fig2. Block diagram1

VI. Pin Descriptions

PIN	I/O	DESCRIPTION
VDD	POWER	Power
GND	POWER	Ground
PLL_C	I	Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with GND.
Xin	I	Input pin for 32.768 kHz oscillator
Xout	O	Output pin for 32.768 kHz oscillator
INT0 INT1 INT2 INT3 INT4 INT5 INT6 INT7	PORT6(0) PORT6(1) PORT6(2) PORT6(3) PORT6(4) PORT6(5) PORT6(6) PORT6(7)	PORT6(0)~PORT6(7) signal can be interrupt signals. INT2 and INT3 has the same interrupt flag. INT4 to INT7 has the same interrupt flag.
P6.0 ~P6.7	PORT6	PORT 6 can be INPUT or OUTPUT port each bit. Internal Pull high function.
P7.0 ~P7.7	PORT7	PORT 7 can be INPUT or OUTPUT port each bit.
P8.0 ~P8.7	PORT8	PORT 8 can be INPUT or OUTPUT port each bit. Internal Pull high function.
P9.0 ~P9.7	PORT9	PORT 9 can be INPUT or OUTPUT port each bit. Bit0 ,bit1 and bit2 can be set to wake up watch dog timer.
BUZZER	O	Buzzer output
/BUZZER	O	Buzzer output which is inverted from BUZZER pin.
RESET	I	Reset pin
TEST	I	TEST pin normal low

VII. Functional Descriptions

VII.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

2. R1 (TCC)

* Increased by an external signal edge applied to TCC , or by the instruction cycle clock. Written and read by the program as any other register. TCC can be a wakeup source n IDLE mode if user set IOCF bit0 “1”.

3. R2 (Program Counter)

* The structure is depicted in Fig.3 .
* Generates 32K × 13 on-chip ROM addresses to the relative programming instruction codes.
* "JMP" instruction allows the direct loading of the low 10 program counter bits.
* "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.
* "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
* "MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
* "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
* "TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change.
* The most significant bit (A10~A14) will be loaded with the content of bit PS0~PS4 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

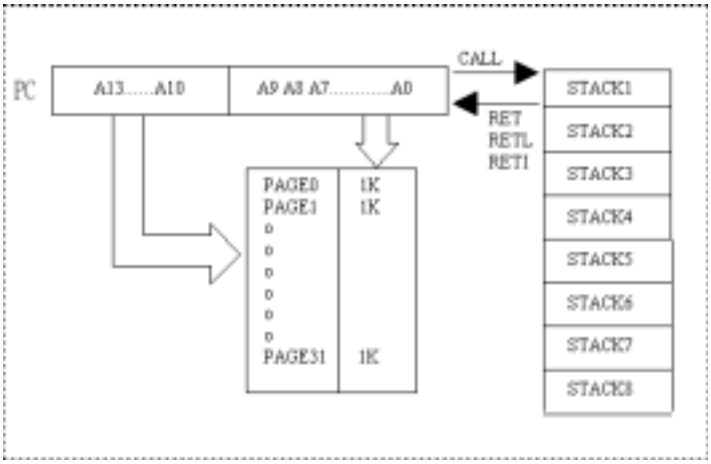


Fig.3 Program counter organization

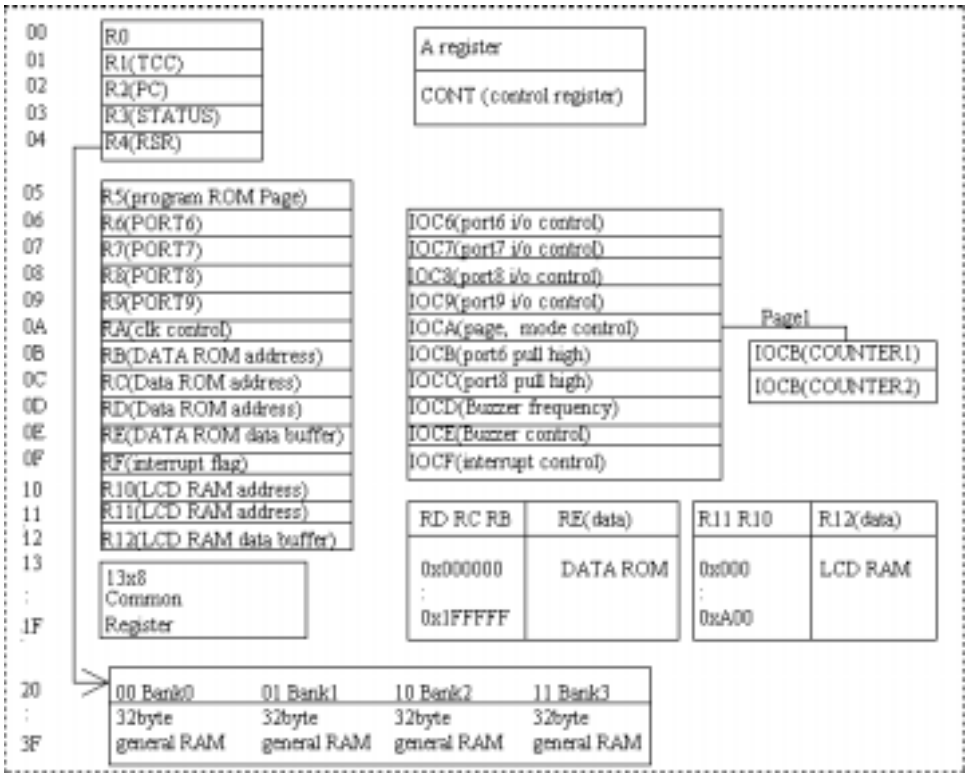


Fig.4 Data memory configuration

4. R3 (Status Register)

7	6	5	4	3	2	1	0
LPDEN	PAGE	-	T	P	Z	DC	C

* Bit 0 (C) Carry flag

* Bit 1 (DC) Auxiliary carry flag

* Bit 2 (Z) Zero flag

* Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

* Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from SLEEP mode or IDLE mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	x	x .. don't care

* Bit 5: unused

* Bit 6: PAGE : change IOCB ~ IOCE to another page , 0/1 => page0 / page1

* Bit 7: LPDEN : low power detect enable control, 0/1=>disable/enable

NOTE!! Once enable LPD circuit, it will has 12uA power consumption.

5. R4 (RAM Select Register)

* Bits 0 ~ 5 are used to select up to 64 registers in the indirect addressing mode.

* Bits 6 ~ 7 determine which bank is activated among the 4 banks.

* See the configuration of the data memory in Fig. 4

6. R5 (Program Page Select Register)

7	6	5	4	3	2	1	0
-	-	-	PS4	PS3	PS2	PS1	PS0

* Bit 0 (PS0) ~ 3 (PS4) Page select bits

Page select bits. User can select up to 32 pages.

Before " CALL " or " JMP " instruction , should set correct page where will going to.

Refer to fig.3

*User can use PAGE instruction to change page. To maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. And the program page is maintained by EMC's complier. It will change user's program by inserting instructions within program.

*Bit4~7 : unused

7. R6 ~ R9 (Port 6 ~ Port 9)

* Four 8-bit I/O registers.

8. RA

7	6	5	4	3	2	1	0
LPD	CLOCK	MS1	MS0	/WDT	P92_W	P91_W	P90_W

* Bit0 : PORT9 bit0 wake up option. 0/1= disable/enable

* Bit1 : PORT9 bit1 wake up option. 0/1= disable/enable

* Bit2 : PORT9 bit2 wake up option. 0/1= disable/enable

* Bit3 : WATCH DOG enable control bit. 0/1= disable/enable

* Bit4,5 : Main clock scalar.

MS1	MS0	Main clock
0	0	0.75MHz
0	1	1.5MHz
1	0	3MHz

* Bit6: Green mode and Normal mode switch bit. 0/1= Green mode/Normal mode

Cpu use 32.768 KHz at Green Mode. Cpu use PLL clock at Normal mode.

*Bit7: LPD:low power detect signal. 0/1=>normal power/ low power voltage

The voltage of VDD is lower than 2.2 V, it will be set ‘1’. Or it will be cleared if the voltage is higher than 2.4V.

9. RB(Data ROM address)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

* Bit 0 - Bit 7 are DATA ROM address Bit0 to Bit7.

10. RC(Data ROM address)

7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8

* Bit 0 - Bit 7 are DATA ROM address Bit8 to Bit15.

11. RD(Data ROM address)

7	6	5	4	3	2	1	0
0	0	0	A20	A19	A18	A17	A16

* Bit 0 - Bit 4 are DATA ROM address Bit16 to Bit20.

* Bit 5 ~ Bit7 always zero.

12. RE(Data ROM data)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

* Bit 0 - Bit 7 are DATA ROM data Bit0 to Bit7. User can read data from this buffer.

13. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
0	C8_2	C8_1	INT4	INT2	INT1	INT0	TCIF

* "1" means interrupt request, "0" means non-interrupt
* Bit 0 (TCIF) TCC timer overflow interrupt flag. It will be set at TCC timer overflow . And it can be a wakeup source in IDLE mode. After wakeup , bit0 will set to '1' if IOCF enable. But program will run the next insturction from "SLEP" .
* Bit 1 (INT0) external INT0 pin interrupt flag .
* Bit 2 (INT1) external INT1 pin interrupt flag .
* Bit 3 (INT2) external INT2 pin and INT3 pin interrupt flag .
* Bit 4 (INT4) external INT4 , INT5, INT6, INT7 pin interrupt flag . Any one can set this flag whenever it has a interruption.
* Bit 5 (C8_1) internal 8 bit up counter (CNT1) interrupt flag .
* Bit 6 (C8_2) internal 8 bit up counter (CNT2) interrupt flag .
* Bit 7 unused. And set to zero.

* High to low edge trigger , Refer to the Interrupt subsection.
* IOCF is the interrupt mask register. User can read and clear.

14. R10(LCD RAM address)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

* Bit 0 - Bit 7 are LCD RAM address Bit0 to Bit7.

15. R11(LCD RAM address)

7	6	5	4	3	2	1	0
0	0	0	0	A11	A10	A9	A8

* Bit 0 - Bit 3 are LCD RAM address Bit8 to Bit11.

* Bit4 – Bit7 are zero always .

16. R12(LCD RAM data)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

* Bit 0 - Bit 7 are LCD RAM data buffer Bit0 to Bit7.

17. R13~R3F (General Purpose Register)

* R13~R3F (Banks 0~3) all are general purpose registers.

VII.2 Special Purpose Registers

1. A (Accumulator)

* Internal data transfer, or instruction operand holding
* It's not an addressable register.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
-	-	TS	-	PAB	PSR2	PSR1	PSR0

* Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

* Bit 3 (PAB) Prescaler assignment bit.
  0/1 : TCC/WDT
* Bit 4 unused
* Bit 5 (TS) TCC signal source (NOTE!! If TS set to '0' then TCC will has no wakeup function)
  0: internal instruction cycle clock
  1: 16.38KHz
* Bit 6 : unused
* Bit 7 : unused

* CONT register is readable and writable.

3. IOC6 ~ IOC9 (I/O Port Control Register)

* Five I/O direction control registers.
* "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.

* User can see IOCB register how to switch to normal I/O port.

4. IOCA

7	6	5	4	3	2	1	0
C2S	C1S	PSC1	PSC0	0	0	0	0

* Bit0 unused

* Bit1~3: set to '0 ' always.

* Bit5~Bit4: counter1 prescaler

(PSC1,PSC0) = (0,0)=>1:1 , (0,1)=>1:2 , (1,0)=>1:4 , (1,1)=>1:8

* Bit6:counter1 source , (0/1)=(32768Hz/main clock if enable)

* Bit7:counter2 source , (0/1)=(32768Hz/main clock if enable)

5. IOCB (Port6 pull high control register)

PAGE0

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

*Bit0: Port6 bit0 pull high control register. (0/1 = disable/ enable)

*Bit1: Port6 bit1 pull high control register. (0/1 = disable/ enable)

*Bit2: Port6 bit2 pull high control register. (0/1 = disable/ enable)

*Bit3: Port6 bit3 pull high control register. (0/1 = disable/ enable)

*Bit4: Port6 bit4 pull high control register. (0/1 = disable/ enable)

*Bit5: Port6 bit5 pull high control register. (0/1 = disable/ enable)

*Bit6: Port6 bit6 pull high control register. (0/1 = disable/ enable)

*Bit7: Port6 bit7 pull high control register. (0/1 = disable/ enable)

PAGE1 : 8 bit up-counter (COUNTER1) preset and read out register . (write = preset) . After a interruption , it will count from "00".

6. IOCC (Port8 pull high control register)

PAGE0

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80

*Bit0: Port8 bit0 pull high control register. (0/1 = disable/ enable)

*Bit1: Port8 bit1 pull high control register. (0/1 = disable/ enable)

*Bit2: Port8 bit2 pull high control register. (0/1 = disable/ enable)

*Bit3: Port8 bit3 pull high control register. (0/1 = disable/ enable)

*Bit4: Port8 bit4 pull high control register. (0/1 = disable/ enable)

*Bit5: Port8 bit5 pull high control register. (0/1 = disable/ enable)

*Bit6: Port8 bit6 pull high control register. (0/1 = disable/ enable)

*Bit7: Port8 bit7 pull high control register. (0/1 = disable/ enable)

PAGE1 : 8 bit up-counter (COUNTER2) preset and read out register . (write = preset) After a interruption , it will count from “00”.

7. IOCD

7	6	5	4	3	2	1	0
F7	F6	F5	F4	F3	F2	F1	F0

Bit0~ Bit7: Buzzer output frequency selection control register.

Buzzer output frequency = Buzzer clock source / (F7~F0)

Ex: BCLK =32.768KHz , F7~F0=0x4A

Buzzer output= 32768 / 74 = 442 Hz

Ex: BCLK =1MHz , F7~F0=0x4A

Buzzer output= 1000000 / 74 = 13513 Hz

8. IOCE

7	6	5	4	3	2	1	0
0	0	0	0	0	0	BCLK	BEN

Bit0: Buzzer output enable. 0/1=disable/enable

Bit1: Buzzer frequency clock source. 0/1=32.768KHz/ 1MHz

Bit0~ Bit2: Bit2 ~ Bit3 unused. Set to "0" always.

9. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
0	C8_2	C8_1	INT4	INT2	INT1	INT0	TCIF

* Bit 0 ~ 6 interrupt enable bit.

0: disable interrupt

1: enable interrupt

*Bit7 always set to '0'.

* IOCF Register is readable and writable.

TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 5 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

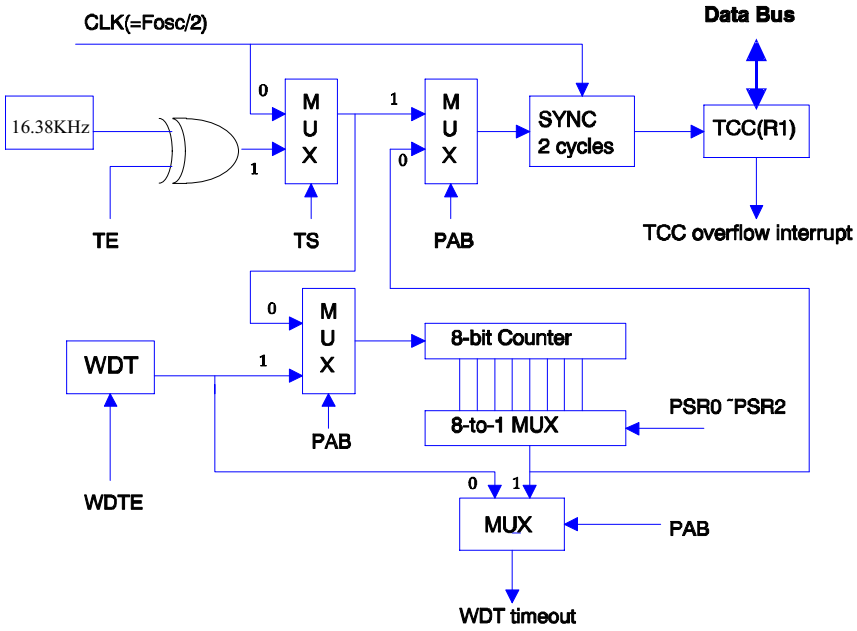


Fig. 5 Block diagram of TCC WDT

I/O Ports

The I/O registers, Port 6 ~ Port 9, are bi-directional tri-state I/O ports. Port 6,8 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.6.

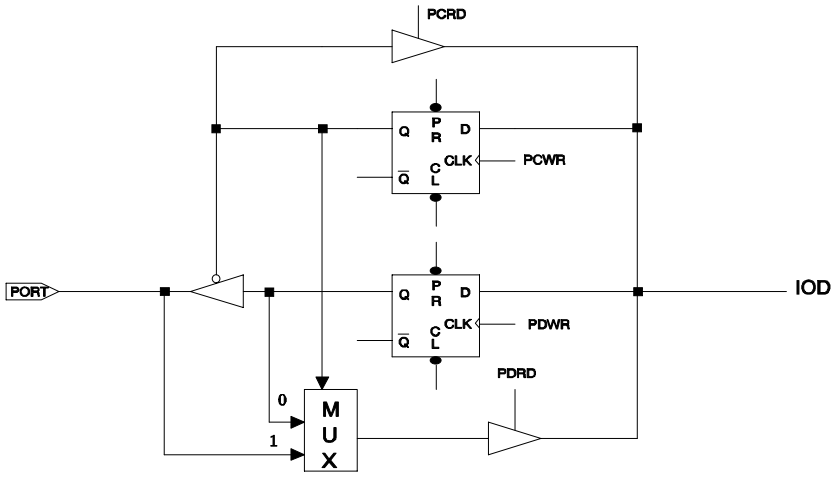


Fig. 6 The circuit of I/O port and I/O control register

RESET and Wake-up

The RESET can be caused by

(1) Power on reset, or Voltage detector

(2) WDT timeout. (if enabled and in GREEN mode)

Note that only Power on reset, or only Voltage detector in Case(1) is enabled in the system by CODE Option bit. If Voltage detector is disabled, Power on reset is selected in Case (1). Refer to Fig. 7.

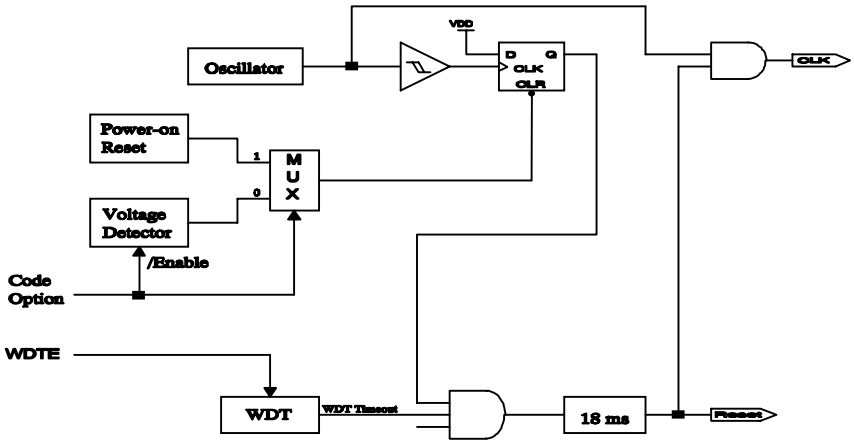


Fig. 7 Block diagram of Reset of controller

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"

- The other register (bit7..bit0)

R5 = “00000000”		
R6 = PORT	IOC6 = "11111111"	
R7 = PORT	IOC7 = "11111111"	
R8 = PORT	IOC8 = "11111111"	
R9 = PORT	IOC9 = "11111111"	
RA = "00000000”	IOCA = "00000000"	
RB = "00000000”	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000”	Page0 IOCC = "00000000"	Page1 IOCC = "00000000"
RD = "00000000"	Page0 IOCD = "00000000"	
RE = "xxxxxxxx"	Page0 IOCE = "00000000"	
RF = "00000000"	IOCF = "00000000"	
R10 = “00000000”		
R11 = “00000000”		
R12 = “xxxxxxxx”		

WAKEUP from IDLE mode

The controller can be awakened from IDLE mode (execution of "SLEP" instruction) by (1) TCC time-out (2) WDT time-out (if enable) or, (3) external input. The three cases will not cause the controller reset. And run next instruction from “SLEP” instruction. These last two cases should ebable RA register before into sleep mode.

The WAKEUP can be caused by

(1) TCC time out

(2) WDT time out. (if enabled and in IDLE MODE)

(3) PORT 9 high to low transient

Case (1), case (2) and case(3) all will run next instruction from “SLEP” instruction in IDLE mode. And all of the control register will not reset.

Case (1) will set a RF flag and run next instruction.

After wakeup, CPU will check RA bit6 to decide CPU clock is 32.768KHz or main clock.

NOTE!! If wakeup in case(2) or case(3), please take care WDT’s control or it will make a reset in GREEN mode or NORMAL mode.

Interrupt

This IC has internal interrupts which are falling edge triggered, as followed : TCC timer overflow interrupt (internal) , two 8-bit counters overflow interrupt . (COUNTER1,COUNTER2)

If these interrupt sources change signal from high to low , then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are eight external interrupt pins including INT0 , INT1 , INT2 , INT3, INT4, INT5, INT6, INT7 .The INT2 and INT3 sent to the same interrupt flag. And INT4 to INT7 is a interrupt vector, too.

External interrupt INT0 to INT7 signals are from PORT6 bit0 to bit7. If IOCF is enable then these signal will cause external interrupt , or these signals will be treated as general input data .

After reset, the next instruction will be fetched from address 000H and the instruction interrupt (INT) is 001H and the hardware inturrept is 008H.

It is very important to save ACC,R3 and R5 when processing a interruption.

Address	Instruction	Note
0x08	DISI	;Disable interrupt
0x09	MOV A_BUFFER,A	;Save ACC
0x0A	SWAP A_BUFFER	
0x0B	SWAPA 0x03	;Save R3 status
0x0C	MOV R3_BUFFER,A	
0x0D	MOV A,0x05	;Save ROM page register
0x0E	MOV R5_BUFFER,A	
:	:	
:	:	
:	MOV A,R5_BUFFER	;Return R5
:	MOV 0X05,A	
:	SWAPA R3_BUFFER	;Return R3
:	MOV 0X03,A	
:	SWAPA A_BUFFER	;Return ACC
:	RETI	

Instruction Set

Instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z

0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1	1110	1000	kkkk	1E8k	PAGE k	K->R5(3:0)	None
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

Absolute Operation Maximum Ratings

Items	Sym.	Condition	Rating	Unit
Temperature under bias	V_{DD}		-0.3 to 3.6	V
Input voltage	V_{IN}		-0.5 to V_{DD}+0.5	V
Operating temperature range	T_A		0 to 70	℃

DC Electrical Characteristic

(T_A=0°C ~ 70°C, V_{DD}=3V±5%, V_{SS}=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current for input pins	I_{IL1}	V_{IN} = V_{DD}, V_{SS}			±1	μA
Input Leakage Current for bi-directional pins	I_{IL2}	V_{IN} = V_{DD}, V_{SS}			±1	μA
Input High Voltage	V_{IH}		2.5			V
Input Low Voltage	V_{IL}				0.8	V
Clock Input High Voltage	V_{IHX}	OSCI	2.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.5	V
Output High Voltage (port6,7,8,9)	V_{OH1}	I_{OH} = -0.9mA	2.4			V
Output Low Voltage (port6,7,8,9)	V_{OL1}	I_{OL} = 0.9mA			0.4	V
Pull-high current	I_{PH}	Pull-high active input pin at V_{SS}	-100	-200	-240	μA
Power down current	I_{SB1}	CLK=32.768KHz, All input and I/O pin at V_{DD},output pin floating, WDT disabled, BUZZER disable		8 (LPD disable) 15 (enable)	11 (LPD disable) 18 (enable)	μA
Low clock current	I_{SB2}	CLK=32.768KHz,All input and I/O pin at VDD, output pin floating, WDT disabled, BUZZER disable		15 (LPD disable) 22 (enable)	20 (LPD disable) 27 (enable)	μA
Operating supply current (NORMAL mode)	I_{CC}	/RESET=High, CLK=1MHz, All input and I/O pin at VDD,output pin floating, BUZZER disable		350	400	μA

AC Electrical Characteristic

(T_A=0°C ~ 70°C, V_{DD}=3V, V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768K		60		us
		4M		500		us
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tin+20)/N			ns
Watchdog timer period	Twdt	T_A = 25°C		16		ms

Note 1: N= selected prescaler ratio.

Timing Diagrams

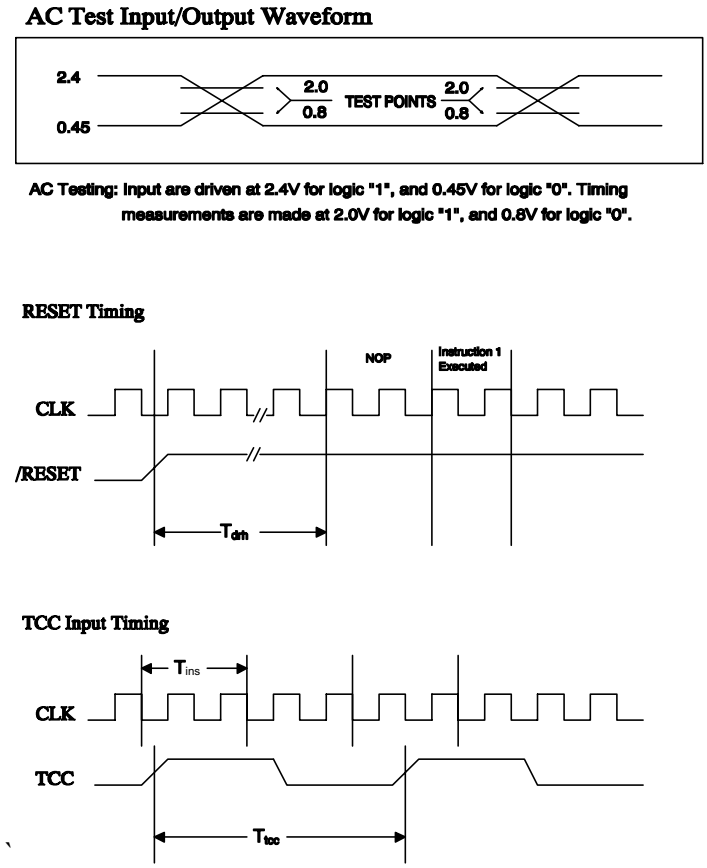
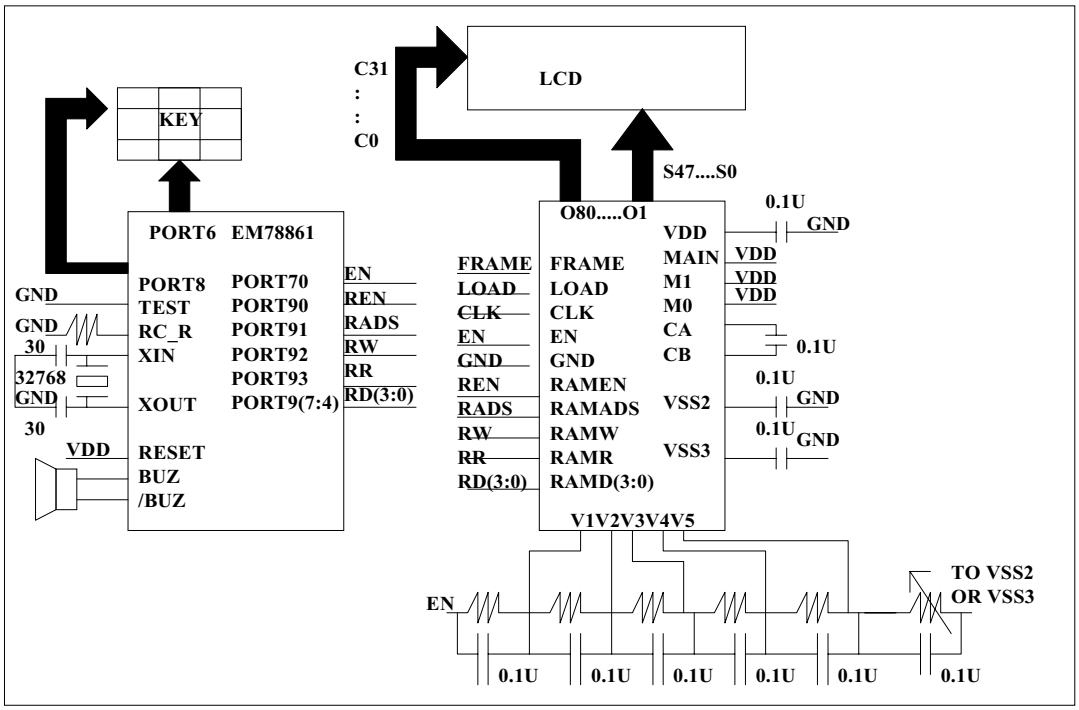


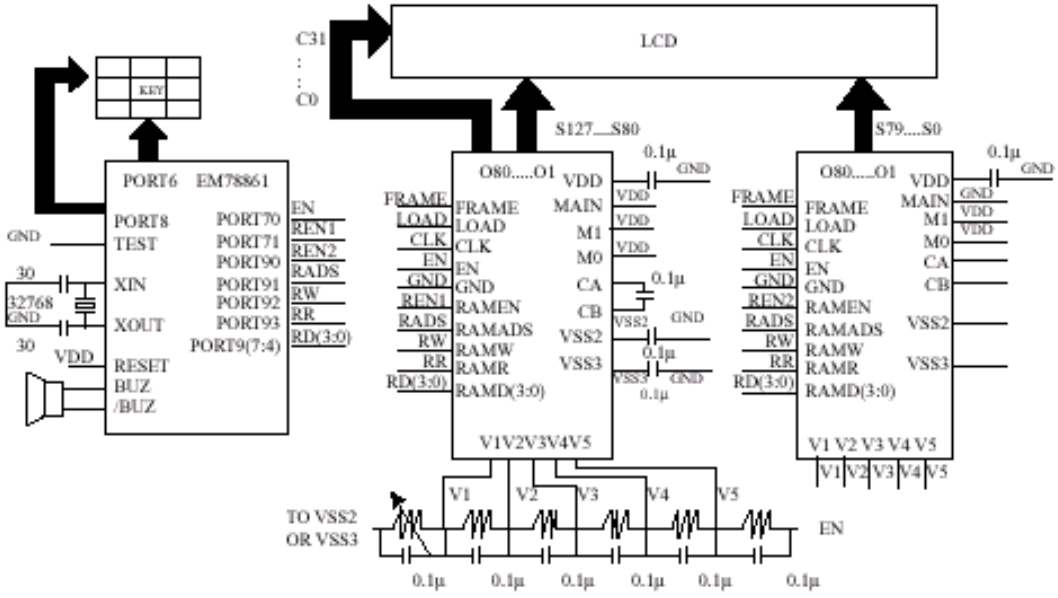
Fig.8 AC timing

Application Circuit

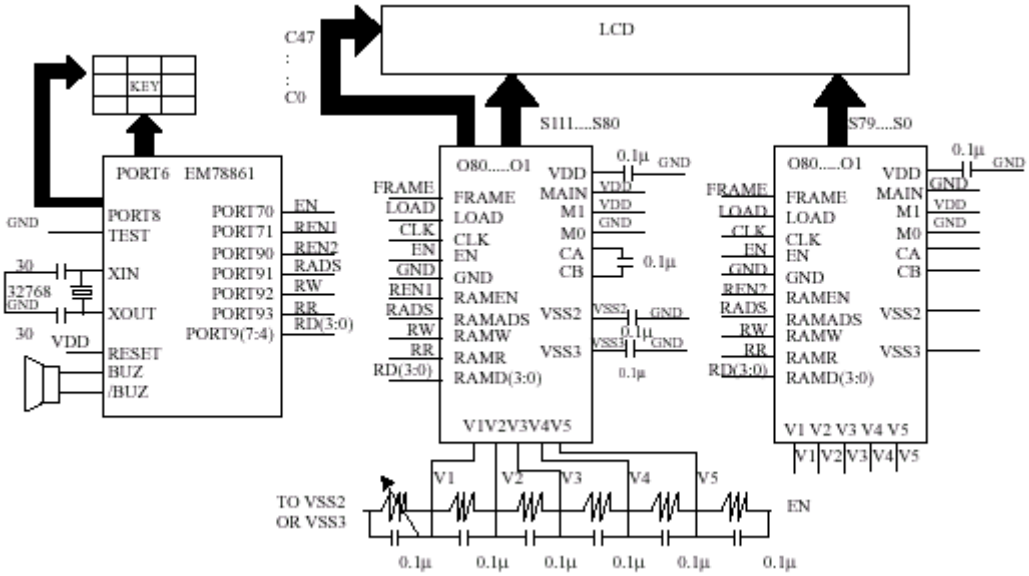
(1) C32 x S48, 78861+83040 ,fig9



(2) C32 x S48, 78861+83040+83040



(3) C48 x S112, 78861+83040+83040



(4) C80 x S160, 78861+83040+83040+83040