GENERAL DESCRIPTION

The XRT79L71 is a single channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controller and Line Interface Unit with Jitter Attenuator that is designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT79L71 includes DS3/E3 Framing, Line Interface Unit with Jitter Attenuator that supports mapping of ATM or HDLC framed data. A flexible parallel microprocessor interface is provided for configuration and control. Industry standard UTOPIA II and POS-PHY interface are also provided.

GENERAL FEATURES:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- Flexible integrated Clock Multiplier that takes single frequency clock and generates either DS3 or E3 frequency.
- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- HDLC Controller that provides the mapping/ extraction of either bit or byte mapped encapsulated packet from DS3/E3 Frame.
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola, PowerPC, and Mips µPs
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 208 STBGA Package
- JTAG Interface

LINE INTERFACE UNIT

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled
- Typical power consumption 1.3W

DS3/E3 FRAMER

- DS3 framer supports both M13 and C-bit parity.
- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF,LOF,AIS,RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832,G.751 standards.
- Framers can be bypassed.

ATM/PPP PROTOCOL PROCESSOR

TRANSMIT CELL PROCESSING

- Extracts ATM cells

- Supports ATM cell payload scrambling
- Maps ATM cells into E3 or DS3 frame
- PLCP frame and mapping of ATM cell streams

RECEIVE CELL PROCESSING

- Extraction of ATM cells from PLCP frame or directly from E3 or DS3 frame
- Termination of PLCP frame
- Supports payload cell de-scrambling

TRANSMIT PACKET PROCESSING

- Inserts PPP packets into data stream
- Maps HDLC data stream directly into DS3 or E3 frame
- Extracts in-band messaging packets
- Supports CRC-16/32, HDLC flag and Idle sequence generation

RECEIVE PACKET PROCESSING

- Extracts HDLC data stream from DS3 or E3 frame
- Inserts in-band messaging packets
- Detects and removes HDLC flags

UTOPIA/ SYSTEM INTERFACE

- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- Compliant with ATM Forum UTOPIA II interface
- Programmable FIFO size for both Transmit and Receive direction
- Compliant to POS-PHY Level 2 interface

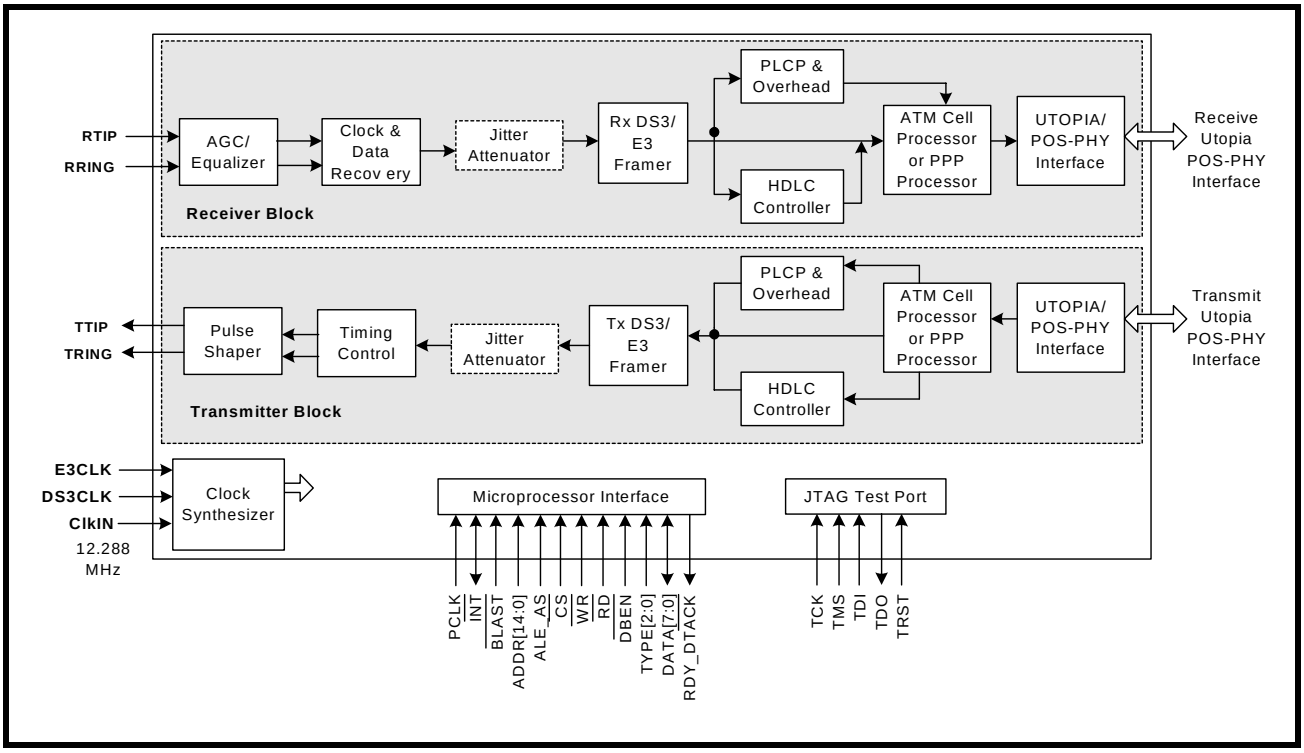
SERIAL INTERFACE

- Serial clock and data interface for accessing DS3/ E3 framer
- Serial clock and data interface for accessing cell/ packet processor

APPLICATIONS

- Digital Access and Cross Connect Systems
- 3G Base Stations
- DSLAMs
- Digital, ATM, WAN and LAN Switches

FIGURE 1. BLOCK DIAGRAM OF THE XRT79L71



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L71IB	17X17 mm 208 Ball Shrink Thin Ball Grid Array	-40°C to +85°C

TABLE 1: PIN OUT OF THE XRT79L71 (TOP VIEW)

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	TXUADDR_1	TXUADDR_3	TXUCLKO	TXPEOP	TXUCLK	RXMOD	RXUADDR_4	RXUADDR_0	RXUCLAV	RXUDATA_1	RXUDATA_2	RXUDATA_5	RXUDATA_9	RXUDATA_13	RXGFCMSB	RXGFCCLK
2	TXUADDR_0	TXUADDR_2	TXUADDR_4	RXPDVAL	TXPER	RXPERR	RXUCLKO	RXUADDR_1	RXUSOC	RXUDATA_0	RXUDATA_4	RXUDATA_8	RXUDATA_12	TXGFCCLK	RXPRED	RXPLOF
3	TXUDATA_0	TXUPRTY	TXUSOC	TXUCLAV	TXMOD	RXUCLK	RXPEOP	RXUADDR_2	RXUPRTY	RXUDATA_3	RXUDATA_7	RXUDATA_11	RXUDATA_15	RXGFC	TXPOHCLK	TXPOHFRAME
4	TXUDAT_3	TXUDATA_2	TXUDATA_1	TXUDATA_10	TXUEN_L	TSX_TSOF	RSX_RSOF	RXUADDR_3	RXUEN_L	RXUDATA_6	RXUDATA_10	RXUDATA_14	RXCP	RXPOHFRAME	RXNIB_3	RXNIB_2
5	TXUDATA_7	TXUDATA_6	TXUDATA_5	TXUDATA_4									RXPOOF	RXNIB_0	RXOUTCLK	RXSER
6	TXUDATA_12	TXUDATA_11	TXUDATA_9	TXUDATA_8									RXNIB_1	RXOHIND	RXFRAME	RXCLK
7	GPIO_0	TXUDATA_15	TXUDATA_14	TXUDATA_13									RXLOS	RXOH	RXOHENABLE	RXOHCLK
8	DMO_0	GPIO_3	GPIO_2	GPIO_1									TXNIB_1	TXNOB_2	TXNOB_3	RXOHFRAME
9	TCK	TMS	TDI	TDO									TXNIBCLK	TXSER	TXOHIND	TXNIB_0
10	TRING	TRST	MTIP	TXDGND									TXOHINS	TXINCLK	TXFRAME	TXNIBFRAME
11	TTIP	NC	MRING	TXDVDD									PDATA	TXOH	TXOHFRAME	TXFRAMEREF
12	TXAVDD	REFAVDD	REFAGND	TXAGND									PDATA_4	PDATA_1	TXOHCLK	TXOHENABLE
13	RXAVDD	RRING	ANAIO1	OVDD	OGND	GPI_2	GPO_2	PDBEN_L	DA_SEL	DPADDR_7	DPADDR_3	PADDR_6	PINT_L	PDATA_5	PDATA_2	TXAISEN
14	RXAGND	RTIP	ANAIO2	VDD	RESET_L	GPI_1	GPO_1	PTYPE_2	VDD	DPADDR_6	DPADDR_2	PADDR_5	PCS_L	PRDY_L	PDATA_6	PDATA_3
15	JAGND	TXON	ICTB	GND	TESTMODE	GPI_0	GPO_0	PTYPE_1	GND	DPADDR_5	DPADDR_1	PADDR_4	PADDR_1	PRD_L	PBLAST_L	PDATA_7
16	JAAVDD	CLKVDD	DS3CLK	CLKGND	E3CLK	NIBBLEINTF	CLKOUT	PTYPE_0	PCLK	DPADDR_4	DPADDR_0	PADDR_3	PADDR_2	PADDR_0	PWR_L	PAS_L

VDD	GND	GND	VDD	VDD
VDD	GND	GND	VDD	VDD
VDD	GND	GND	VDD	VDD
VDD	GND	GND	VDD	VDD

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2.0 PIN DESCRIPTIONS

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
MICROPROCESSOR INTERFACE			
F16 F15 F14 F13 G16 G15 G14 G13 C16 D15 D16 E16 E15 E14 E13	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14	I	**Address Bus Input pins Microprocessor Interface:** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations within the XRT79L71 whenever it performs READ and WRITE operations with the XRT79L71.
D11 C12 B13 A14 D12 C13 B14 A15	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Bi-Directional Data Bus pins Microprocessor Interface:** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT79L71.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
A16	ALE/$\overline{AS}$	I	**Address Latch Enable/Address Strobe:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - ALE** If the Microprocessor Interface of the XRT79L71 has been configured to operate in the Intel-Asynchronous Mode, then this active-"High" input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[14:0]) into the XRT79L71 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "High" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT79L71 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - $\overline{AS}$** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this active-"Low" input pin is used to latch the data (residing on the Address Bus, A[14:0]) into the Microprocessor Interface circuitry of the XRT79L71. Pulling this input pin "Low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **Power PC 403 Mode - No Function - Tie to GND:** If the Microprocessor Interface has been configured to operate in the Power PC 403 Mode, then this input pin has no role nor function and should be tied to GND.
D14	$\overline{CS}$	I	**Chip Select Input:** The user must assert this active "Low" signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT79L71 on-chip registers and buffer/memory locations.
D13	$\overline{INT}$	O	**Interrupt Request Output:** This active-"Low" output signal will be asserted when the XRT79L71 is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
C15	$\overline{RD}$/$\overline{DS}$/$\overline{WE}$	I	**READ Strobe/Data Strobe:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - $\overline{RD}$ - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin functions as the $\overline{RD}$ (Active "Low" Read Strobe) input signal from the Microprocessor. Once this active-"Low" signal is asserted, then the XRT79L71 places the contents of the addressed register or buffer location on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus is tri-stated. **Motorola-Asynchronous (68K) Mode - $\overline{DS}$ - Data Strobe:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this input pin functions as the $\overline{DS}$ (Data Strobe) input signal. **Power PC 403 Mode - $\overline{WE}$ - Write Enable Input:** If the Microprocessor Interface is operating in the Power PC 403 Mode, then this input pin functions as the $\overline{WE}$ (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-"Low" input signal (along with $\overline{CS}$ and WR/R/W) also being asserted at a logic "Low" level upon the rising edge of mPCLK, then the Microprocessor Interface will (upon the very same rising edge of mPCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the target on-chip register or buffer location within the XRT79L71.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
C14	$\overline{\text{RDY}}$/$\overline{\text{DTACK}}$/ RDY	O	**READY or DTACK Output:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - $\overline{\text{RDY}}$ - Ready Output:** If the Microprocessor Interface has been configured to operate in the Intel-Asynchronous Mode, then this output pin functions as the active-"Low" READY output. During a READ or WRITE cycle, the Microprocessor Interface block toggles this output pin to the logic "Low" level ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic "Low" level. **Motorola-Asynchronous Mode - $\overline{\text{DTACK}}$ - Data Transfer Acknowledge Output** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the active-"Low" DTACK output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "Low" level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic "Low" level. **Power PC 403 Mode - RDY - Ready Output:** If the Microprocessor Interface has been configured to operate in the Power PC 403 Mode, then this output pin will function as the active-"High" READY output. During a READ or WRITE cycle, the Microprocessor Interface block toggles this output pin to the logic "High" level ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic "High" level (upon the rising edge of PCLK), then it is now safe for it to move on and execute the next READ or WRITE cycle. If during a READ or WRITE cycle the Microprocessor Interface block is holding this output pin at a logic "Low" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic "Low" level. ***NOTE:*** *The Microprocessor Interface updates the state of this output pin upon the rising edge of mPCLK.*
M14	$\overline{\text{RESET}}$	I	**Hardware Reset Input:** When this active-"Low" signal is asserted, the XRT79L71 will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
H16	µPCLK	I	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it uses this clock signal to do the following. • To sample the $\overline{CS}$, $\overline{WR}$/$\overline{R/W}$, A[14:0], D[7:0], $\overline{RD}$/$\overline{DS}$ and DBEN input pins, and • To update the state of the D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. The Microprocessor Interface can work with µPCLK frequencies ranging up to 33MHz.* *2. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, the user should tie this pin to GND.*
B16	$\overline{WR}$/$\overline{R/W}$	I	**Write Strobe/Read-Write Operation Identifier:** The exact function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - $\overline{WR}$ - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the $\overline{WR}$ (Active "Low" WRITE Strobe) input signal from the Microprocessor. Once this active-"Low" signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the target register or address location, within the XRT79L71) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - $\overline{R/W}$ - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this pin is functionally equivalent to the $\overline{R/W}$ input pin. In the Motorola Mode, a READ operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin. **Power PC 403 Mode - $\overline{R/W}$ - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the Power PC 403 Mode, then this input pin will function as the Read/Write Operation Identification Input pin. Anytime the Microprocessor Interface samples this input signal at a logic "Low" (while also sampling the $\overline{CS}$ input pin "Low") upon the rising edge of mPCLK, then the Microprocessor Interface will (upon the very same rising edge of mPCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the $\overline{DBEN}$/$\overline{OE}$ input pin, and the Microprocessor Interface will then place the contents of the target register (or address location within the XRT79L71) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic "High" (while also sampling the $\overline{CS}$ input pin a logic "Low") upon the rising edge of µPCLK, then the Microprocessor Interface will (upon the very same rising edge of µPCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the $\overline{RD}$/$\overline{DS}$/$\overline{WE}$ input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the target register or buffer location within the XRT79L71.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
J16 J15 J14	PTYPE_0 PTYPE_1 PTYPE_2	I	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. **PTYPE[2:0]** / **Microprocessor Interface Mode** 000 — Intel-Asynchronous Mode 001 — Motorola-Asynchronous Mode (Motorola 68K) 010 — Intel X86 011 — Intel i960 100 — IDT3051/52 (MIPS) 101 — Power PC 403 Mode
J13	$\overline{\text{DBEN}}$	I	**Bi-directional Data Bus Enable Input pin:** This input pin permits the user to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]). Setting this input pin "Low" enables the Bi-directional Data bus. Setting this input "High" tri-states the Bi-directional Data Bus.
B15	$\overline{\text{BLAST}}$	I	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate to the Microprocessor Interface block that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin by toggling it "Low" in order to denote that the current READ or WRITE operation within a BURST operation is the last operation of this BURST operation. ***NOTE:*** *If the user has configured the Microprocessor Interface to operate in the Intel Asynchronous, the Motorola-Asynchronous or the Power PC 403 Mode, then tie this input pin to GND.*
H13	Direct_Ad	I	**Direct Address Select pin:** The user should pull this input pin to the logic "High" level for normal operation.

PIN #	NAME	TYPE	DESCRIPTION
TEST AND DIAGNOSTIC			
T9	TCK	I	**Test Clock input, Boundary Scan Clock input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
P9	TDI	I	**Test Data input, Boundary Scan Test Data Input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*

PIN #	NAME	TYPE	DESCRIPTION
N9	TDO	O	**Test Data output:** Boundary Scan Test Data Output:
R9	TMS	I	**Test Mode Select, Boundary Scan Test Mode Select input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
R10	TRST	I	**Test Mode Reset, Boundary Scan Mode Reset Input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
M15	TESTMODE	***	**Factory Test Mode Pin:** Tie this pin to Ground.
P15	$\overline{\text{ICT}}$	I	**In-Circuit Test Input Pin:** For normal operation, the user should pull this pin "High". ***NOTE:*** *This input pin is internally pulled "High".*
P13 P14	AnaIO1 AnaIO2	I/O	**Analog Input/Output Test Pin:** These pins should be pulled "Low" for normal operation.
L15 L14 L13	GPI_0 GPI_1 GPI_2	I	**General Purpose Input Test Pin:** These pins should be pulled "Low" for normal operation.
K15 K14 K13	GPO_0 GPO_1 GPO_2	O	**General Purpose Output Test Pin:** These pins should be left unconnected for normal operation.

PIN #	NAME	TYPE	DESCRIPTION
GENERAL PURPOSE INPUT AND OUTPUT PINS			
T8	DMO	O	**Drive Monitor Output Output Pin:** If this input signal is "High", then it means that the drive monitor circuitry within the XRT79L71 has not detected any bipolar signals at the MTIP and MRING inputs (or via the Internal Drive Monitor circuit) within the last 128 ± 32 bit periods. If this input signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT79L71.
T7 N8 P8 R8	GPIO_0 GPIO_1 GPIO_2 GPIO_3	I/O	**General Purpose Input/Output Pins:** Each of these pins can be configured to function as either a general purpose input or output pin. If a given pin (GPIO_X) is configured to function as an input pin, then the state of this input pin can be monitored by reading Bit X within the Operation General Purpose Pin Data Register (Address Location = 0x0147). If a given pin is configured to function as an output pin, then the state of this output pin (GPIO_X) can be controlled by writing the appropriate value into Bit X within the Operation General Purpose Pin Data Register. Finally, the user can configure a given GPIO_X pin to be an input pin by setting Bit X, within the Operation General Purpose Pin Direction Control Register (Address = 0x014B) to "0". Conversely, the user can configure the GPIO_X pin to be an output pin by setting Bit X, within the Operation General Purpose Pin Direction Control Register (Address = 0x014B) to "1".

PIN #	NAME	TYPE	DESCRIPTION
TRANSMIT SYSTEM SIDE INTERFACE PINS			
A13	TxAISEn	I	**Transmit AIS Pattern Input pin:** This input pin is used to command the Transmit DS3/E3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "High" configures the Transmit DS3/E3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "Low" configures the Transmit DS3/E3 Framer block to NOT transmit an AIS pattern to the remote terminal equipment. ***NOTE:*** *For normal operation, or if the user wishes to control the Transmit AIS function, via Software Control; the user should tie this input pin to GND.*

PIN #	NAME	TYPE	DESCRIPTION
L16	NibbleIntf	I	**Nibble Interface Select Input pin:** This input pin is used to configure the Transmit Payload Data Input Interface and the Receive Payload Data Output Interface blocks to operate in either the Serial or the Nibble-Parallel Mode. **Setting this input pin "High" configures each of these blocks to operate in the Nibble-Parallel Mode.** In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data from the System-Side terminal equipment in a nibble-parallel manner via the TxNib[3:0] input pins. Further, the Receive Payload Data Output Interface block will output inbound payload data to the System-Side terminal equipment in a nibble-parallel via the RxNib[3:0] output pins. **Setting this input pin "Low" configures each of these blocks to operate in the Serial Mode.** In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data from the System-Side terminal equipment in a serial manner via the TxSer input pin. Further, the Receive Payload Data Output Interface block will output the inbound payload data to the System-Side terminal equipment in a serial manner, via the RxSer output pin. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode. The user is advised to tie this input pin to GND if the user intends to configure the XRT79L71 to operate in the ATM UNI or PPP Modes.*
B10	TxFrame	O	**Transmit End of DS3/E3 Frame Indicator:** This output pin is pulse "High" for one DS3 or E3 clock period, when the Transmit Section of the XRT79L71 is processing the last bit of a given DS3 or E3 frame. The implications of this output pin, for each mode of operation, are described below. **ATM UNI/PPP/High-Speed HDLC Controller Mode:** This output pin serves as an end-of-frame indication to the System-Side terminal equipment. **Clear-Channel Framer Mode:** If the XRT79L71 is configured to operate in the Clear-Channel Framer mode, then this output pin serves to alert the System-Side Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame. Hence, the System-Side Terminal Equipment uses this output signal to maintain Framing Alignment with the XRT79L71.
A11	TxFrameRef	I	**Transmit DS3/E3 Framer - Framing Alignment Input pin:** If the the Transmit Section of the XRT79L71 is configured to operate in the Local-Timing/Frame-Slave Mode, then the Transmit DS3/E3 Framer block will use this input signal as the Framing Reference. When the XRT79L71 is configured to operate in this mode any rising edge at this input pin will cause the Transmit DS3/E3 Framer block to begin its creation of a new DS3 or E3 frame. Consequently, the user must supply a clock signal that is equivalent to the DS3 or E3 frame rates to this input pin. Further, it is imperative that this clock signal be synchronized with the 44.736MHz or 34.368MHz clock signal applied to the TxInClk input pin. ***NOTE:*** *This input pin should be tied to GND if it is not to be used as the Transmit DS3/E3 Framer block - Framing Reference input signal.*

PIN #	NAME	TYPE	DESCRIPTION
C10	TxInClk	I	**Transmit DS3/E3 Framer Block - Timing Reference Signal:** If the Transmit Section of the XRT79L71 is configured to operate in the Local-Timing Mode, then it will use this signal as the Timing Reference. If the XRT79L71 is being operating in the DS3 Mode, then the user is expected to apply a high-quality 44.736MHz clock signal to this input pin. Likewise, if the XRT79L71 is being operated in the E3 Mode, then the user is expected to apply a high-quality 34.368MHz clock signal to this input pin. **Note for Clear-Channel Framer Operation:** both the Clear-Channel Framer and Local-Timing modes, then the user should design or configure the System-Side terminal equipment circuitry, such that out-bound DS3 or E3 data will be output, upon the falling edge of TxInClk. The Transmit Payload Data Input Interface within the Transmit Section of the XRT79L71 will sample the data, applied to the TxSer input pin, upon the rising edge of TxInClk. ***NOTE:*** *For Revision A silicon, the user must supply at least a 20MHz clock signal to this input pin even if the XRT79L71 is configured to operate in the Loop-Timing Mode. If the user fails to do this, you will not be able to perform READ or WRITE operations with the on-chip Register or Buffer Space via the Microprocessor Interface block.*
C11	TxOH/ TxHDLCDat_5	I	**Transmit Overhead Data Input/Transmit High Speed HDLC Controller Input Interface - Data Bus Input pin 0 Bit 5:** The function of This input pin depends upon whether or not the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOH - Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface block accepts overhead via this input pin, and insert this data into the appropriateoverhead bit positions within the very next outbound DS3 or E3 frames. If the TxOHIns input pin is pulled "High", then the Transmit Overhead Data Input Interface will sample the over-head data residing on this input pin, upon either the rising edge TxInClk or the falling edge of the TxOHCLK output clock signal depending upon the Insertion Method used. Conversely, if the TxOHIns input pin is NOT pulled "High", then the Transmit Overhead Data Input Interface block will be inactive and will not accept any over-head data via the TxOH input pin. **High Speed HDLC Controller Mode - TxHDLCDat_5 - Transmit High-Speed HDLC Controller Input Interface - Data Bus Input pin - Bit 5:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDL-CData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side terminal equipment with a byte-wide Transmit High-Speed HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal.

PIN #	NAME	TYPE	DESCRIPTION
D10	TxOHIns/ TxHDLCDat_4	I	**Transmit Overhead Data Insert Enable Input pin/Transmit High-Speed HDLC Controller Input Interface - Data Bus Input pin - Bit 4:** The function of this input pin depends upon whether or not the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOHIns - Transmit Overhead Data Insert Input pin:** This input pin is used to either enable or disable the Transmit Overhead Data Input Interface block. If the Transmit Overhead Data Input Interface block is enabled, then it will accept overhead data from the System-Side terminal equipment via the TxOH input pin; and insert this data into the overhead bit positions within the outbound DS3 or E3 data stream. Conversely, if the Transmit Overhead Data Input Interface block is disabled, then it will NOT accept overhead data from the System-Side terminal equipment. Pulling this input pin "High" enables the Transmit Overhead Data Input Interface block. Pulling this input pin "Low" disables the Transmit Overhead Data Input Interface block. **High-Speed HDLC Controller Mode - TxHDLCDat_4 Transmit High-Speed HDLC Controller Input Interface - Data Bus Input pin - Bit 4:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 4 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDL-CData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block samples the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal.
B12	TxOHClk	O	**Transmit Overhead Clock Output:** This output pin functions as the Transmit Overhead Data Input Interface clock signal. If the user enables the Transmit Overhead Data Input Interface block by asserting the TxOHIns input pin, then the Transmit Overhead Data Input Inter-face block will sample and latch the data residing on the TxOH input pin upon the falling edge of this signal. ***NOTE:*** *The Transmit Overhead Data Input Interface block is disabled if the user has configured the XRT79L71 to operate in the High-Speed HDLC Controller Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B11	TxOHFrame/ TxHDLCClk	O	**Transmit Overhead Framing Pulse/Transmit HDLC Controller Clock Output pin:** The function of this output pin depends upon whether or not the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High-Speed HDLC Controller Mode - TxOHFrame:** This output pin pulses "High" for one TxOHClk period coincident with the instant the Transmit Overhead Data Input Interface would be accepting the first overhead bit within an outbound DS3 or E3 frame. **High Speed HDLC Controller Mode - TxHDLCClk:** This output pin functions as the demand clock output signal for the Transmit HDLC Controller byte-wide input interface. This clock signal is ultimately derived from either the TxInClk or the RxOutClk clock signal (for Local-Timing Applications) or from the RxOutClk clock signal (for Loop-Timing Applications). Hence, the frequency of this clock signal is nominally one-eight of that of the TxInClk or the RxOutClk signals. The Transmit HDLC Controller block will sample the contents of the Transmit HDLC Controller byte-wide input interface, upon the rising edge of this clock output signal. Therefore, the System-Side terminal equipment should be designed to output data onto the TxHDLCDat[7:0] bus upon the falling edge of this clock output signal.
A12	TxOHEnable/ TxHDLCDat_7	I/O	**Transmit Overhead Enable Output indicator/Transmit HDLC Controller Data Bit 7 Input:** The function of this input pin depends upon whether or not the XRT79L71 is configured to operate in the High Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOHEnable:** The XRT79L71 will assert this output pin, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the System-Side terminal equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 data stream, then it is expected to sample the state of this signal, upon the falling edge of TxInClk. Upon sampling the TxOHEnable signal "High", the System-Side terminal equipment should; (1) place the desired value of the overhead bit onto the TxOH input pin and (2) assert the TxOHIns input pin. The Transmit Overhead Data Input Interface block will sample and latch the data on the TxOH signal, upon the rising edge of the very next TxInClk input signal. **High-Speed HDLC Controller Mode - TxHDLCDat_7:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin functions as Bit 7 (the MSB) within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit High-Speed HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block samples the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal.

PIN #	NAME	TYPE	DESCRIPTION
C9	TxSer TxPOH SendMSG	I	**Transmit Payload Data Input Interface - Serial Input/Transmit PLCP Path Overhead Input/Send HDLC Message Request Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxSer - Transmit Payload Data Input Interface - Serial Input pin:** If the XRT79L71 is configured to operate in the Clear-Channel Framer mode, then this input pin functions as the Transmit Payload Data Serial Input pin. In this case, the System-Side terminal equipment is expected to apply all outbound data which is intended to be carried via the DS3 or E3 payload bits to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxSer input pin, upon the rising edge of TxInClk. **ATM/PLCP Mode - TxPOH - Transmit PLCP Path Overhead Input Port - Input pin:** If the XRT79L71 is configured to operate in the ATM Mode, and if within the ATM Mode, the chip is also configured to operate in the PLCP Mode, then this input pin functions as the Transmit PLCP Path Overhead Input Pin. In this mode, the user can externally insert desired path overhead byte values into the outbound PLCP frames. The Transmit PLCP Path Overhead Input Pin (and Port) become active whenever the user asserts the TxPOHIns input pin by pulling it "High". In this case, the data, residing upon the TxPOH input pin will be sampled upon the rising edge of the TxPOHClk signal. ***NOTE:*** *This input pin is inactive and should be tied to GND if the XRT79L71 is configured to operate in either the PPP or in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - SendMSG - Transmit High-Speed HDLC Controller Input Interface - Send Message Indicator Input:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller Mode, then this input pin functions as the Transmit HDLC Controller Input Interface enable input pin. If the user asserts this input pin by pulling it "High" then the Transmit HDLC Controller Input Interface will proceed to latch the data, residing on the TxHDLCDat[7:0] input pins, upon each rising edge of the TxHDLCClk signal. All data that is latched into the Transmit HDLC Controller Input Interface for the duration that the SendMSG input pin is "High" will be encapsulated into an HDLC frame and ultimately transported via the payload bits of the outbound DS3 or E3 data stream. If the user pulling this input pin "Low", then the Transmit HDLC Controller Input Interface will cease latching the data, residing on the TxHDLCDat[7:0] bus. ***NOTE:*** *This input pin is inactive and should be tied to GND if the XRT79L71 has been configured to operate in the PPP Mode.*
A3	TxPOHFrame	O	**Transmit PLCP Frame Path Overhead Byte Serial Input Port - Beginning of Frame indicator:** This output pin, along with the TxPOH, TxPOHClk, and the TxPOHIns pins comprise the Transmit PLCP Frame POH Byte Insertion serial input port. This particular pin pulses "High" when the Transmit PLCP POH Byte Insertion serial input port is expecting the first bit of the Z6 byte at the TxPOH input pin. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B3	TxPOHClk	O	**Transmit PLCP Frame POH Byte Insertion Clock:** This pin, along with the TxPOH and the TxPOHMSB input pins, function as the Transmit PLCP Frame POH Byte serial input port. This output pin functions as a clock output signal that is be used to sample the user's POH data at the TxPOH input pin. This output pin is always active, independent of the state of the TxPOHIns pin. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*
B9	TxOHInd/ TxPFrame/ TxHDLCDat_6/	I/O	**Transmit Overhead Data Indicator Output/Transmit PLCP Frame Boundary Indicator Output/Transmit HDLC Controller Data Bit 6 input pin:** The function of these input/output pins depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, the ATM/PLCP Mode or the High-Speed HDLC Mode. **Clear-Channel Framer Mode - TxOHInd - Transmit Overhead Data Indicator Output pin:** In the Clear-Channel Framer Mode, this output pin can be configured to function as the transmit overhead data indicator for the System-Side terminal equipment, or as a Gapped-Clock output for the Transmit Payload Data Input Interface. This output pin is pulsed "High" for one DS3 or E3 bit period in order to indicate to the System-Side terminal equipment that the Transmit Section of the Framer is going to be processing an overhead bit, upon the next rising edge of TxInClk., and will NOT latch the data that is applied to the TxSer input pin. Therefore, when the System-Side terminal equipment samples the TxOHInd output pin "High", then it must not apply the next payload bit to TxSer input pin. This output pin serves as a warning that this particular payload bit is going to be ignored by the Transmit Section of the Framer, and will not be inserted into payload bits, within the outbound DS3 or E3 data stream. **ATM/PLCP Mode - TxPFrame:** If the XRT79L71 is configured to operate in the ATM UNI/PLCP Mode, then this output pin will denote the boundaries of outbound PLCP frames, as they are being processed by the Transmit PLCP Processor block. This output pulses "High" when the last nibble of a given PLCP frame is being routed to the Transmit DS3/E3 Framer block. This output pin is inactive if the XRT79L71 is operating in the Direct-Mapped ATM Mode. **High-Speed HDLC Controller Mode - TxHDLCDat_6 - Transmit High-Speed HDLC Controller Bit 6 Input pin:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 6 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit High-Speed HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block sample the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal.

PIN #	NAME	TYPE	DESCRIPTION
D9	TxNibClk/ TxGFCMSB/ SendFCS	I/O	**Transmit Nibble Clock Output pin/Transmit GFC Byte - MSB Indicator Output/Send FCS Value Request Input:** The function of this input/output pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM Mode. **Clear-Channel Framer Mode - TxNibClk - Transmit Nibble Clock Output pin:** When operating in the Nibble-Parallel Mode the XRT79L71 will derive this clock signal from either the TxInClk or the RxLineClk signal depending upon whether the chip is operating in the Local-Timing or Loop-Timing Mode. The user is advised to configure the Terminal Equipment to output the outbound payload data to the XRT79L71 onto the TxNib_[3:0] input pins, upon the rising edge of this clock signal. The Transmit Payload Data Input Interface block will sample the data, residing on the TxNib_[3:0] line, upon the falling edge this clock signal. ***NOTES:*** 1. *For DS3 applications, the XRT79L71 will output 1176 clock pulses to the System-Side terminal equipment for each outbound DS3 frame.* 2. *For E3, ITU-T G.832 applications, the XRT79L71 will output 1074 clock pulses to the System-Side terminal equipment for each outbound E3 frame.* 3. *For E3, ITU-T G.751 applications, the XRT79L71 will output 384 clock pulses to the System-Side terminal equipment for each outbound E3 frame.* **ATM Mode - TxGFCMSB - Transmit GFC Input Port - MSB Indicator Output:** This signal, along with TxGFC and TxGFCClk combine to function as the Transmit GFC Nibble Field serial input port. This output signal will pulse "High" when the MSB (most significant bit) of the GFC nibble for a given outbound cell is expected at the TxGFC input pin. **High-Speed HDLC Controller Mode - SendFCS - Transmit High-Speed HDLC Controller - Send FCS Command Input pin:** The System-Side terminal equipment is expected to control both this input pin, along with the SendMSG input pin, during the construction and transmission of each outbound HDLC frame. This input pin is used to command the Transmit HDLC Controller block to compute and insert the computed FCS (Frame-Check Sequence) value into the back-end of the outbound HDLC frame, as a trailer. If the user has configured the Transmit HDLC Controller block to compute and insert a CRC-16 value into the outbound HDLC frame, then the System-Side terminal equipment is expected to hold this input pin "High" for two periods of TxHDLCClk.Conversely, if the user has configured the Transmit HDLC Controller block to compute and insert a CRC-32 value into the outbound HDLC frame, then the System-Side terminal equipment is expected to hold this input pin "High" for four (4) periods of TxHDLCClk. ***NOTES:*** 1. *This input/output pin is inactive if the XRT79L71 has been configured to operate in the PPP Mode.* 2. *This input/output pin is inactive if the XRT79L71 has been configured to operate in the Clear-Channel Framer/Serial mode.*

PIN #	NAME	TYPE	DESCRIPTION
C2	TxGFCClk	O	**Transmit GFC Nibble-Field Serial Input port - Clock Output signal:** This signal, along with TxGFC and TxGFCMSB combine to function as the Transmit GFC Nibble-field serial input port. This output signal functions as the demand clock signal for this port. The user will specify the value of the GFC field, within a given ATM cell, by serially transmitting its four bit-value into the TxGFC input pin. The Transmit GFC Nibble-Field serial input port will latch the contents of TxGFC upon the rising edge of this clock signal. Hence, the System-Side terminal equipment should be designed to place its outbound GFC bits on to the TxGFC line, upon the falling edge of this clock signal. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configure to operate in the ATM UNI Mode.*
B8	TxNib_3/ TxPOHIns/ TxHDLCDat_3	I	**Transmit Nibble Interface - Bit 3/Transmit PLCP Path Overhead Insert enable/Transmit HDLC Controller Data Bus - Bit 3 input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_3 - Transmit Nibble Interface - Bit 3:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 3 (MSB) input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_0 through TxNib_2) upon the falling edge of TxNibClk. ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - TxPOHInsTxPOHIns - Transmit PLCP Path Overhead Insert Enable Input pin:** f the XRT79L71 is configured to operate in the ATM Mode, and if (within the ATM Mode, the chip is also configured to operate in the PLCP Mode), then this input pin functions as the Transmit PLCP Path Overhead Port - Enable input pin. In this mode, the user can externally insert desired path overhead byte values into the outbound PLCP frames. The Transmit PLCP Path Overhead Input port becomes active whenever the user asserts this input pin by pulling it "High". Once this occurs, the data, residing upon the TxPOH input pin will be sampled upon the rising edge of the TxPOHClk signal. ***NOTE:*** *This input pin is inactive (and should be tied to GND) if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_3 - Transmit High-Speed HDLC Controller Data Bus - Bit 3 Input pin:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 3 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit High-Speed HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface sample the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal. ***NOTE:*** *This input pin is inactive (and should be tied to GND) if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
C8	TxNib_2/ TxStuff_Ctl/ TxHDLCDat_2	I	**Transmit Nibble Input Interface - Bit 2/Transmit PLCP Stuff Control Input/ Transmit HDLC Controller Data Bus - Bit 2 Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode, or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_2 - Transmit Nibble Interface - Bit 2:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 1 input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_0, TxNib_2 and TxNib_3) upon the falling edge of TxNibClk ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - TxStuff_Ctl - Transmit PLCP Stuff Control Input pin:** This input pin is used to externally exercise or forego trailer nibble stuffing opportunities by the Transmit PLCP Processor block. PLCP trailer nibble stuff opportunities occur in periods of three PLCP frames (375 us). The first PLCP frame (first, within a stuff opportunity period) will have 13 trailer nibbles appended to it. The second PLCP frame (second within a stuff opportunity period will have 14 trailer nibbles appended to it. The third PLCP frame (the location of the stuff opportunity) will contain 13 trailer nibbles if this input pin is pulled "Low", and 14 trailer nibbles if this input pin is pulled "High". ***NOTE:*** *This input pin is inactive (and should be tied to GND) if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_2 - Transmit High-Speed HDLC Controller Data Bus - Bit 2 Input pin:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 2 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block samples the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal. ***NOTE:*** *This input pin is inactive (and should be tied to GND) if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
D8	TxNib_1/ Tx8KREF/ TxHDLCDat_1	I	**Transmit Nibble Input Interface - Bit 1/Transmit PLCP Framing 8kHz Reference Input/Transmit HDLC Controller Data Bus - Bit 1 Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode, or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_1 - Transmit Nibble Interface -Bit 1:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 1 input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_0, TxNib_2 and TxNib_3) upon the falling edge of TxNibClk. ***NOTE:*** *This input pin is inactive (and should be tied to GND) if the XRT79L71 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - Tx8KREF - Transmit PLCP Framing 8kHz Reference Input pin:** If the XRT79L71 is configured to operate in the ATM/PLCP Mode, then the Transmit PLCP Processor can be configured to synchronize its PLCP frame generation to this input clock signal. The Transmit PLCP Processor will also use this input signal to compute the nibble-trailer stuff opportunities. ***NOTE:*** *This input pin is inactive (and should be tied to GND) if the use has configured the XRT79L71 to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_1 - Transmit HDLC Controller Data Bus - Bit 1 Input pin:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block samples the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal. ***NOTE:*** *This input pin is inactive and should be tied to GND, if the XRT79L71 has been configured to operate in either the PPP or in the Direct-Mapped ATM Mode.*

PIN #	NAME	TYPE	DESCRIPTION
A9	TxNib_0/ TxGFC/ TxHDLCDat_0	I	**Transmit Nibble Interface - Bit 0/Transmit GFC Input pin/Transmit HDLC Controller Data Bus - Bit 0 Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High Speed HDLC Controller Mode or in the ATM Mode. **Clear-Channel Framer Mode - TxNib_0 - Transmit Nibble Interface - Bit 0:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 0 (LSB) input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_1 through TxNib_3) upon the falling edge of TxNibClk. ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM Mode - TxGFC TxGFC - Transmit GFC Port Input pin:** This signal, along with TxGFCMSB, and TxGFCClk combine to function as the Transmit GFC Nibble Field serial input port. The user will specify the value of the GFC field, within a given ATM cell, by serially transmitting its four bit-value into this input pin. Each of these four bits will be clocked into the port upon the rising edge of the TxGFCClk output signal. **High-Speed HDLC Controller Mode - TxHDLCDat_0 - Transmit HDLC Controller Data Bus - Bit 0 Input pin:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then this input pin will function as Bit 0 (the LSB) within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block provides the System-Side terminal equipment with a byte-wide Transmit HDLC Controller clock output signal (TxHDLCClk). The Transmit High-Speed HDLC Controller Input Interface block samples the data residing on this input pin (along with the rest of the TxHDLCData[7:0] input pins) upon the rising edge of the TxHDLCClk clock output signal. ***NOTE:*** *This input pin is inactive and should be tied to GND if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
A10	TxCellTxed/ TxNibFrame/ ValidFCS	O	**Transmit ATM Cell Generator indicator/Transmit Nibble Frame Indicator/ Valid FCS Indicator output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM Mode, the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **ATM Mode - TxCellTxed TxCellTxed - Transmit ATM Cell Generator Indicator:** This output pin pulses "High" (for one TxInClk or RxOutClk period) each time the ATM Transmit Cell Processor block transmits an ATM cell to either the Transmit PLCP Processor or the Transmit DS3/E3 Framer block. **Clear-Channel Framer Mode - TxNibFrame - Transmit Nibble Frame Indicator Output pin:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the System-Side terminal equipment that it needs to begin the transmission of a new DS3 or E3 frame to the XRT79L71. ***NOTE:*** *This output pin is not active if the XRT79L71 is configured to operate in the Serial-Mode.* **High-Speed HDLC Controller Mode - ValidFCS:** The combination of the RxIdle and ValidFCS output signals are used to convey information about data that is being output via the Receive High-Speed HDLC Controller Output Interface - Data bus output (RxHDLCDat_[7:0]). ***If RxIdle = "High":*** The Receive High-Speed HDLC Controller Output Interface block with drive this output pin "High" anytime the flag sequence octet (0x7E) is present on the RxHDLCDat[7:0] output data bus. ***If RxIdle and ValidFCS are both "High":*** The Receive High-Speed HDLC Controller Output Interface block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame are valid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive High-Speed HDLC Controller Output Interface block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame is invalid. ***If RxIdle is "Low" and ValidFCS is "High":*** The Receive High-Speed HDLC Controller Output Interface block has received an ABORT sequence. ***NOTE:*** *This input pin is active if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
M2	TxPERR	I	**Transmit POS-PHY Interface - Transmit Packet Error Indicator from Link Layer:** The Link Layer Processor is expected to assert this input signal (e.g., toggle it "High") anytime it is routing a packet to the Transmit POS-PHY Interface that is erred and needs to be ABORTED. The Link Layer Processor should only assert this input pin coincident to when the last byte, or 16-bit word, of a given packet is being written onto the Transmit POS-PHY Data Bus (e.g., the TxPData[15:0]) input pins. If the Link Layer Processor identifies a given outbound PPP Packet as being erred, then the Transmit PPP Packet Processor block transmits this particular packet to the remote terminal equipment as an Aborted Packet. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the PPP Mode. The user should tie this input pin to GND if the user intends to operate the XRT79L71 in some mode other than the PPP Mode.*
N1	TxPEOP	I	**Transmit POS-PHY Interface - End of Packet:** The link layer processor toggles this output pin "High" whenever the Link Layer Processor is writing the last byte (or 16-bit word) of a given Packet into the Transmit POS-PHY Data Bus (e.g., the TxPData[15:0] input pins). ***NOTES:*** 1. *This input pin is only valid when the XRT79L71 is configured to operate in the PPP Mode. The user should tie this input pin to GND if the user intends to operate the XRT79L71 in some mode other than the PPP Mode.* 2. *This input pin is only valid when the Transmit POS-PHY Interface - Write Enable Input pin ($\overline{TxPEn}$) is asserted.*

PIN #	NAME	TYPE	DESCRIPTION
R3	TxUPrty/ TxPPrty	I	**Transmit UTOPIA Data Bus - Parity Input/Transmit POS-PHY Interface - Parity Input:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - TxUPrty - Transmit UTOPIA Interface - Parity Input pin:** The ATM Layer processor will apply the parity value of the byte or word which is being applied to the Transmit UTOPIA Data Bus (e.g., TxUData[15:8] or TxUData[15:0]) inputs of the XRT79L71, respectively. ***NOTE:*** *This parity value can be computed based upon either the even or odd-parity of the data applied at the Transmit UTOPIA Data Bus. The Transmit UTOPIA Interface block (within the XRT79L71) will independently compute either the even or odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin.* The Transmit UTOPIA Interface block within the XRT79L71 will independently compute an odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin. **PPP Mode - TxPPrty - Transmit POS-PHY Interface - Parity Input pin:** The Link Layer Processor will apply the parity value of the byte or word which is being applied to the Transmit POS-PHY Data Bus (e.g., TxPData[15:8] or TxPData[15:0]) inputs of the XRT79L71, respectively. ***NOTES:*** 1. *This parity value can be computed based upon either the even or odd-parity of the data applied to the Transmit POS-PHY Data Bus. The Transmit POS-PHY Interface block (within the XRT79L71) will independently compute either the even or odd-parity value of each byte (or word) that it receives from the Link Layer processor and will compare it will the logic level of this input pin.* 2. *This input pin is only active if the user has configured the XRT79L71 to operate in either the ATM UNI or the PPP Mode. The user should tie this input pin to GND to operate the XRT79L71 in either the Clear-Channel Framer or High-Speed HDLC Controller Modes.*

PIN #	NAME	TYPE	DESCRIPTION
M4	$\overline{\text{TxUEN}}$/ $\overline{\text{TxPEN}}$	I	**Transmit UTOPIA Interface Block - Write Enable/Transmit POS-PHY Interface - Write Enable:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode Operation - $\overline{\text{TxUEN}}$ - Transmit UTOPIA Interface - Write Enable Input pin:** This active-"Low" signal, from the ATM Layer processor enables the data on the Transmit UTOPIA Data Bus to be latched and written into the TxFIFO on the rising edge of TxUClk. When this signal is asserted (e.g., pulled to a logic "Low" level), then the contents of the byte or word that is present, on the Transmit UTOPIA Data Bus (TxUData[15:0]), will be latched into the Transmit UTOPIA Interface block, on the rising edge of TxUClk. When this signal is negated, then the Transmit UTOPIA Data bus inputs will be tri-stated. **PPP Mode Operation - $\overline{\text{TxPEN}}$ - Transmit POS-PHY Interface - Write Enable Input pin:** This active-"Low" signal, from the Link Layer processor enables the data on the Transmit POS-PHY Data Bus to latched and be written into the TxFIFO on the rising edge of TxPClk. When this signal is asserted (e.g., pulled to a logic "Low" level), then the contents of the byte or word that is present, on the Transmit POS-PHY Data Bus (TxPData[15:0]), will be latched into the Transmit POS-PHY Interface block, on the rising edge of TxPClk. When this signal is negated, then the Transmit POS-PHY Data bus inputs will be tri-stated. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. The user should tie this input pin to GND to operate the XRT79L71 in either the Clear-Channel Framer or High-Speed HDLC Controller Mode.*

PIN #	NAME	TYPE	DESCRIPTION
N3	TxUClav/ TxPPA	O	**Transmit UTOPIA Interface - Cell Available Output Pin/Transmit POS-PHY Interface - Packet Data Available Output pin:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - TxUClav - Transmit UTOPIA Interface - Cell Space Available Indicator Output pin:** This output pin supports data flow control between the ATM Layer Processor and the Transmit UTOPIA Interface block. This signal is asserted (e.g., driven "High") whenever the TxFIFO is capable of receiving at least one more full ATM cell of data from the ATM Layer processor. This signal is negated (e.g., driven "Low"), if the TxFIFO is not capable of receiving one more full ATM cell of data from the ATM Layer processor. The exact behavior of the TxUClav output pin, as a function of UTOPIA Level is presented below. **Multi-PHY Operation - UTOPIA Level 2:** When the XRT79L71 is operating in a Multi-PHY Application and is configured to operate in the UTOPIA Level 2 Mode, then this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins, TxUAddr[4:0], match that which have been assigned to this particular Transmit UTOPIA Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the TxFIFO. **Multi-PHY Operation - UTOPIA Level 3** When the XRT79L71 is operating in a Multi-PHY Application and is configured to operate in the UTOPIA Level 2 Mode, then this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins, TxUAddr[4:0], match that which have been assigned to this particular Transmit UTOPIA Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the TxFIFO. **PPP Mode - TxPPA TxPPA - Transmit POS-PHY Interface Packet Space Available Indicator Output:** The XRT79L71 will drive this output pin "High" whenever a (programmable) number of bytes of empty space is available (for writing more PPP packet data) into the TxFIFO. The exact behavior of the TxPPA output pin, as a function of POS-PHY Level is presented below. **POS-PHY Level 2:** When the XRT79L71 is configured to operate in the POS-PHY Level 2 Mode, then this signal will be tri-stated until the TxPClk cycle following the assertion of a valid address on the Transmit POS-PHY Address bus input pins (e.g., if the contents on the Transmit POS-PHY Address bus pins, TxPAddr[4:0], match that which have been assigned to this particular Transmit POS-PHY Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the TxFIFO. **POS-PHY Level 3:** When the XRT79L71 is configured to operate in the POS-PHY Level 3 Mode, then this signal will be tri-stated until two TxPClk cycles following the assertion of a valid address on the Transmit POS-PHY Address Bus input pins (e.g., if the contents on the Transmit POS-PHY Address bus pins, TxPAddr[4:0], match that which have been assigned to this particular Transmit POS-PHY Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the TxFIFO.

PIN #	NAME	TYPE	DESCRIPTION
P3	TxUSoC/ TxPSoP/ TxPSoC	I	**Transmit UTOPIA - Start of Cell Input/Transmit POS-PHY - Start of Packet Input (Packet Mode)/Transmit POS-PHY - Start of Chunk Input (Chunk Mode):** The function of this input signal depends upon whether the XRT79L71 has been configured to operate in the ATM UNI Mode, the PPP Packet Mode, or in the PPP Chunk Mode, as described below. **ATM UNI Mode Operation - TxUSoC TxUSoC - Transmit Start of Cell Indicator Input:** This input pin is driven by the ATM Layer Processor and is used to indicate the start of an ATM cell that is being transmitted from the ATM Layer Processor. This input pin must be pulsed "High" whenever the first byte (or word) of a new cell is present on the Transmit UTOPIA Data Bus (TxUData[15:0]). This input pin must remain "Low" at all other times. **PPP Mode Operation - TxPSoP/TxPSoC** If the XRT79L71 has been configured to operate in the PPP Mode, then the role of this input pin can be further sub-divided, depending upon whether the Transmit POS-PHY Interface block has been configured to operate in the Packet Mode, or in the Chunk Mode, as described below. **PPP Packet Mode Operation - TxPSoP (Transmit POS-PHY - Start of Packet Input):** If the XRT79L71 has been configured to operate in the Packet-Mode, then the Link Layer Processor must pulse this input pin "High" coincident to whenever it places the very first byte (or 16-bit word) of a given packet onto the Transmit POS-PHY Data Bus (TxPData[15:0]) input pins. ***NOTE:*** *The Link Layer Processor must keep this input pin "Low" at all other times.* **PPP Chunk Mode Operation - TxPSoC (Transmit POS-PHY - Start of Chunk Input):** If the XRT79L71 has been configured to operate in the Chunk Mode, then the Link Layer Processor must pulse this input pin "High" coincident to whenever it places the very first byte (or 16-bit word) of a given Chunk onto the Transmit POS-PHY Data Bus (TxPData[15:0]) input pins. ***NOTES:*** 1. *The Link Layer Processor must keep this input pin "Low" at all other times.* 2. *This input pin is only valid if the XRT79L71 has been configured to operate in the ATM UNI or PPP Modes. The user should tie this input pin to GND to operate the XRT79L71 in either the Clear-Channel Framer or in the High-Speed HDLC Controller Modes.*

PIN #	NAME	TYPE	DESCRIPTION
L4	TxTSX/ TxPSOF	I	**Transmit - Change of Port Indicator Input/Transmit - Start of PPP Packet in Chunk Mode:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the Packet Mode or Cell-Chunk Mode. **Packet Mode - TxTSX TxTSX - Transmit POS-PHY Interface - Change of Port Indicator Output (POS-PHY Level 3, Packet Mode only):** The Link-Layer processor pulses this input pin "High" when an in-band port address is present on the TxPData[15:11] bus input pins. When this input pin and TxPENB are both set "High" then the value of TxPData[15:11] is the address value of the TxFIFO (Transmit POS-PHY Port) to be selected. Subsequent write operations, into TxPData[15:0] will fill the TxFIFO (within the Transmit POS-PHY Port) corresponding to this particular in-band address. **Chunk Mode - TxPSOF - Transmit Start of Packet Input Indicator:** The Link Layer processor pulses this input pin "High" in order to indicate that the first byte (or 16-bit word) of a given Packet is placed on the TxPData[15:0] pins. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the POS-PHY Level 3, Packet Mode or in the Chunk Mode. If the user intends to operate the XRT79L71 in any other mode, then the user should tie this input pin to GND.*
P1	TxUClkO/ TxPClkO	O	**Transmit UTOPIA Interface Clock/Transmit POS-PHY Interface Clock Output:** This output is derived from an internal PLL.
M1	TxUClk/ TxPClk	I	**Transmit UTOPIA Interface Clock/Transmit POS-PHY Interface Clock Input:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - TxUClk - Transmit UTOPIA Interface - Clock Input pin:** The Transmit UTOPIA Interface clock is used to latch the data on the Transmit UTOPIA Data bus, into the Transmit UTOPIA Interface block. This clock signal is also used as the timing source for circuitry used to process the ATM cell data into and through the TxFIFO. During Multi-PHY operation, the data on the Transmit UTOPIA Address bus pins is sampled on the rising edge of TxUClk. **PPP Mode - TxPClk - Transmit POS-PHY Interface - Clock Input pin:** The Transmit POS-PHY Interface clock is used to latch the data on the Transmit POS-PHY Data bus, into the Transmit POS-PHY Interface block. This clock signal is also used as the timing source for circuitry used to process the Packet data into and through the TxFIFO. ***NOTES:*** 1. *The XRT79L71 can support TxUClk or TxPClk clock frequencies of up to 50MHz.* 2. *This input pin is inactive and should be tied to GND if the user configures the XRT79L71 to operate in either the Clear-Channel Framer or in the High-Speed HDLC Controller Modes.*

PIN #	NAME	TYPE	DESCRIPTION
T2 T1 R2 R1 P2	TxUAddr_0/ TxPAddr_0 TxUAddr_1/ TxPAddr_1 TxUAddr_2 /TxPAddr_2 TxUAddr_3 /TxPAddr_3 TxUAddr_4 /TxPAddr_4	I	**Transmit UTOPIA Address Bus:/Transmit POS-PHY Address Bus:** The exact function of these input pins depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Modes. **ATM UNI Mode -TxUAddr[4:0] - Transmit UTOPIA Address Bus:** These input pins comprise the Transmit UTOPIA Address Bus input pins. The Transmit UTOPIA Address Bus is only in use when the XRT79L71 is operating in the Multi-PHY mode. Whenever the ATM Layer processor wishes to poll or write data to a particular UNI (PHY-Layer)device, it will provide the address of the target UNI on the Transmit UTOPIA Address Bus. The contents of the Transmit UTOPIA Address Bus input pins are sampled on the rising edge of the TxUClk clock signal. The Transmit UTOPIA Interface block will compare the data on the Transmit UTOPIA Address Bus with the pre-programmed UTOPIA Address value (which was loaded into the XRT79L71 by writing the appropriate data into both the Transmit UTOPIA Port Address Register (Address = 0x0593) and the Transmit UTOPIA Port Number Register (Address = 0x0597). If these two values are identical and the TxUEN input pin is asserted, then the TxUClav output pin will be driven to the appropriate state (based upon the TxFIFO fill level) for the Cell Level handshake mode of operation. If these two values do not match, then the Transmit UTOPIA Interface block will continue to tri-state the TxUClav output pin. ***NOTE:*** *These input pins are only active if the XRT79L71 has been designed into a Multi-PHY Application. If the user intends to design the XRT79L71 into a Single-PHY Application, tie these input pins to GND.* **PPP Mode - TxPAddr[4:0] - Transmit POS-PHY Interface Address Bus Input Pins:** These input pins comprise the Transmit POS-PHY Address Bus input pins. Whenever the Link Layer Processor wishes to poll or write data to a particular PHY-Layer device, it will provide the address of the target PHY-Layer device on the Transmit POS-PHY Address Bus. The contents of the Transmit POS-PHY Address Bus input pins are sampled on the rising edge of TxPClk. The XRT79L71 will compare the data on the Transmit POS-PHY Address Bus with the pre-programmed POS-PHY Address value (which was loaded into the XRT79L71 by writing the appropriate data into the Transmit POS-PHY Interface - Transmit Control Register - Byte 0 (Address = 0x0582). If these two values are identical and the TxPENB input pin is asserted, then the TxPPA output pin will be driven to the appropriate state (based upon the TxFIFO fill level). If these two values do not match, then the Transmit POS-PHY Interface block will continue to tri-state the TxPPA output pin. ***NOTE:*** *These input pins are only active if the XRT79L71 has been configured to operate in either the ATM UNI or PPP Modes. The user should tie these input pins to GND to operate the XRT79L71 in either the Clear-Channel Framer or High-Speed HDLC Controller Modes.*

PIN #	NAME	TYPE	DESCRIPTION
M3	TxPMod	I	**Transmit PPP Data Bus - Modulo Indicator:** This input pin is used to specify the number of valid packet octets are being placed on the TxPData[15:0] input pins. The Link Layer Processor is expected to set this input pin "Low" when both bytes on the TxPData[15:0] data bus contains valid packet data. Conversely, the Link Layer Processor is expected to set this input pin "High" when only the upper octet contains valid packet data. ***NOTES:*** *1. This input pin is only active if the XRT79L71 has been configured to operate in the PPP Mode and if the Transmit POS-PHY Data Bus has been configured to be 16-bits wide. In all other case, the user should tie this input pin to GND.* *2. The Link Layer Processor is expected to set this input pin to the appropriate state, as each 16-bit word is being written into the TxPData[15:0] data bus.*
T3 P4 R4 T4 N5 P5 R5 T5 N6 P6 N4 R6 T6 N7 P7 R7	TxUData_0/ TxPData_0 TxUData_1/ TxPData_1 TxUData_2/ TxPData_2 TxUData_3/ TxPData_3 TxUData_4/ TxPData_4 TxUData_5/ TxPData_5 TxUData_6/ TxPData_6 TxUData_7/ TxPData_7 TxUData_8/ TxPData_8 TxUData_9/ TxPData_9 TxUData_10/ TxPData_10 TxUData_11/ TxPData_11 TxUData_12/ TxPData_12 TxUData_13/ TxPData_13 TxUData_14/ TxPData_14 TxUData_15/ TxPData_15	I	**Transmit UTOPIA Data Bus Inputs/Transmit POS-PHY Data Bus Inputs:** The function of these input pins depends upon whether the XRT79L71 is operating in the ATM UNI Mode or in the PPP Mode as described below. **ATM UNI Operation - TxUData[15:0]] - Transmit UTOPIA Interface Data Bus Input pins:** These input pins comprise the Transmit UTOPIA Data Bus input pins. Whenever the ATM Layer Processor wishes to transmit ATM cell data through the XRT79L71 ATM UNI, it must place this data on these pins. The data, on the Transmit UTOPIA Data Bus is latched into the Transmit UTOPIA Interface block upon the rising edge of TxUClk. ***NOTES:*** *1. These input pins are only active (e.g., data will be sampled and latched into the Transmit UTOPIA Interface block) if the TxUEN input pin is asserted (e.g., pulled "Low").* *2. If the user configures the width of the Transmit UTOPIA Data Bus to be 8-bits, then only the pins TxUData[15:8] are active. In this case, the user must tie the TxUData[7:0] input pins to GND.* **PPP Operation - TxPDATA[15:0] - Transmit POS-PHY Data Bus Input pins:** These input pins comprise the Transmit POS-PHY Data Bus input pins. When a Link Layer Processor transmits PPP packet data through the XRT79L71, it must place this data on these pins. The data, on the Transmit POS-PHY Data Bus is latched into the Transmit POS-PHY Interface block upon the rising edge of TxPClk. ***NOTES:*** *1. These input pins are only active (e.g., data will be sampled and latched into the Transmit POS-PHY Interface block) if the TxPENB input pin is asserted (e.g., pulled "Low").* *2. If the user configures the width of the Transmit POS-PHY Data Bus to be 8-bits, then only the pins TxPData[15:8] are active. In this case, the user must tie the TxPData[7:0] input pins to GND.* *3. The user should tie all of these pins to GND to operate the XRT79L71 in either the Clear-Channel Framer or in the High-Speed HDLC Controller Modes.*

PIN #	NAME	TYPE	DESCRIPTION
RECEIVE SYSTEM SIDE INTERFACE PINS			
A4	RxAIS/ RxNib_2/ RxHDLCDat_2	O	**Receive AIS Pattern Indicator/Receive Nibble Output Interface - Bit 2/ Receive HDLC Controller Data Bus - Bit 2 output pin:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Interface Mode, the High-Speed HDLC Controller Mode, or in the other modes. **Other Modes - RxAIS - AIS Defect Indicator Output Pin:** This output pin is driven "High" whenever the Receive DS3/E3 Framer block has detected and is currently declaring the AIS (Alarm Indicator Signal) defect. **Clear-Channel Framer/Nibble-Parallel Interface Mode - RxNib_2:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this output pin will function as the bit 2 output from the Receive Nibble-Parallel output interface. The Receive Payload Data Output Interface block will output this signal (along with RxNib_0, RxNib_1, and RxNib_3) upon the rising edge of the RxClk output signal. **High-Speed HDLC Controller Mode - Receive High Speed HDLC Controller Output Interface Block - Data Bus Output Pin #2 - RxHDLCDat_2:** This output pin along with RxHDLCDat_[7:3] and RxHDLCDat_[1:0] functions as the Receive High-Speed HDLC Controller Output Interface byte wide output data bus. The Receive High-Speed HDLC Controller outputs the contents of all HDLC frames and flag sequence octets via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.

PIN #	NAME	TYPE	DESCRIPTION
B4	RxRED/ RxNib_3/ RxHDLCDat_3	O	**Receive Section Red Alarm Indicator/Receive Nibble Interface Output pin - Bit 3/Receive HDLC Controller Data Bus output pin - Bit 3:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Mode, the High-Speed HDLC Controller Mode, or in some other mode. **Clear-Channel Framer/Nibble-Parallel Mode - RxNib_3:** The XRT79L71 will output Received data from the remote terminal equipment to the System-Side terminal equipment via this pin, along with RxNib_0 through RxNib_2. This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's System-Side terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - Receive High-Speed HDLC Controller Output Interface Block - Data Bus Output Pin #3 - RxHDLCDat_3:** This output pin along with RxHDLCDat_[7:4] and RxHDLCDat_[2:0] functions as the Receive High-Speed HDLC Controller Output Interface byte wide output data bus. The Receive High-Speed HDLC Controller Output Interface block will output the contents of all HDLC frames and flag sequence octects via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. **Other Modes - RxRED - RED Alarm/Defect Indicator Output pin:** The XRT79L71 will assert this output pin (e.g., toggle it "High") in order to indicate that the Receive DS3/E3 Framer block is currently declaring at least one of the following defect conditions. • LOS - Loss of Signal Defect Condition • OOF - Out of Frame Defect Condition • AIS - Alarm Indication Signal Defect Condition. The XRT79L71 will negate this output pin (e.g., toggle it "Low") anytime that the Receive DS3/E3 Framer block is NOT currently declaring any of the above-mentioned defect conditions.

PIN #	NAME	TYPE	DESCRIPTION
D6	RxOOF/ RxNib_1/ RxHDLCDat_1	O	**Receive Out of Frame Defect Indicator/Receive Nibble Interface Output pin - Bit 1/Receive HDLC Controller Data Bus Output pin - Bit 1:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Mode or the High-Speed HDLC Controller Mode. **Clear-Channel Framer/Nibble-Parallel Mode - RxNib_1:** The XRT79L71 will output Received data from the remote terminal equipment to the System-Side terminal equipment via this pin, along with RxNib_0, RxNib_2 and RxNib_3: This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's System-Side terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - Receive High Speed HDLC Controller Output Interface Block - Data Bus Output Pin #1 - RxHDLCDat_1:** This output pin along with RxHDLCDat_[7:2] and RxHDLCDat_0 functions as the Receive High-Speed HDLC Controller Output Interface byte wide output data bus. The Receive High-Speed HDLC Controller will output the contents of all HDLC frames and flag sequence octets via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. **All other Modes - RxOOF - OOF Defect Indicator Output pin:** The Receive DS3/E3 Framer will assert this output signal whenever it has declared the Out of Frame (OOF) defect condition with the incoming DS3 or E3 frames. This signal is negated when the Receive DS3/E3 Framer block re-acquires DS3 or E3 frame synchronization and clears the OOF defect condition.

PIN #	NAME	TYPE	DESCRIPTION
B5	RxLCD/ RxOutClk/ RxHDLCDat_7	O	**Receive Loss of Cell Delineation Defect indicator/Receive Output Clock signal/Receive HDLC Controller Data Bus - Bit 7 Output:** The function of output pin depends upon whether the XRT79L71 has been configured to operate in the ATM, Clear-Channel Framer or High Speed HDLC Controller Mode. **ATM Mode - RxLCD:(Loss of Cell Delineation Defect Indicator)** The XRT79L71 will assert this output pin (e.g., toggle it "High") anytime (and for the duration that) the Receive ATM Cell Processor block is declaring the LCD (Loss of Cell Delineation) defect condition. The XRT79L71 will negate this output pin (e.g., toggle it "Low") whenever the Receive ATM Cell Processor block is not currently declaring the LCD defect condition. **Clear-Channel Framer Mode - RxOutClk:** This clock signal functions as the Transmit Payload Data Input Interface clock source, if the XRT79L71 has been configured to operate in the loop-timing mode. In this mode, the System-Side terminal equipment is expected to input data to the TxSer input pin, upon the rising edge of this clock signal. The XRT79L71 will use the rising edge of this signal to sample the data on the TxSer input. **High-Speed HDLC Controller Mode - Receive High-Speed HDLC Controller Output Interface Block - Data Bus Output Pin #7 - RxHDLCDat_7:** This output pin along with RxHDLCDat_[6:0] functions as the Receive High-Speed HDLC Controller Output Interface byte wide output data bus. This particular output pin functions as the MSB (Most Significant Bit) of the Receive High-Speed HDLC Controller Output Interface byte wide data bus. The Receive High-Speed HDLC Controller Output Interface block will output the contents of all HDLC frames and flag sequence octets via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
D7	RxLOS	O	**LOS (Loss of Signal) Defect Indicator:** The XRT79L71 will assert this output pin (e.g., toggle it "High") anytime (and for the duration that) the Receive DS3/E3 Framer block declares the LOS defect condition. Conversely, the XRT79L71 will negate this output pin (e.g., toggle it "Low") anytime (and for the duration that) the Receive DS3/E3 Framer block is NOT declaring the LOS defect condition.
B2	RxPRED	O	**Receiver Red Alarm Indicator - Receive PLCP Processor:** The XRT79L71 will assert this output pin (e.g., toggle it "High") anytime (and for the duration that) the Receive PLCP Processor block is currently declaring any of the following defect conditions. • PLCP OOF - PLCP Out of Frame Defect Condition • PLCP LOF - PLCP Loss of Frame Defect Condition Conversely, the XRT79L71 will negate this output pin (e.g., toggle it "Low") anytime (and for the duration that) the Receive PLCP Processor block is NOT declaring any of the above-mentioned defect conditions. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes..*

PIN #	NAME	TYPE	DESCRIPTION
D5	RxPOOF	O	**Receive PLCP Processor Block - PLCP Out of Frame Defect Indicator:** The XRT79L71 will assert this output pin (e.g., toggle it "High") anytime (and for the duration that) the Receive PLCP Processor block is currently declaring the PLCP OOF (Out of Frame) defect condition. Conversely, the XRT79L71 will negate this output pin (e.g., toggle it "Low") anytime (and for the duration that) the Receive PLCP Processor block is NOT declaring the PLCP OOF defect condition. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*
A2	RxPLOF	O	**Receive PLCP Processor Block - PLCP Loss of Frame Defect Indicator Output:** The XRT79L71 will assert this output pin (e.g., toggle it "High") anytime (and for the duration that) the Receive PLCP Processor block is currently declaring the PLCP LOF (Loss of Frame) defect condition. Conversely, the XRT79L71 will negate this output pin (e.g., toggle it "Low") anytime (and for the duration that) the Receive PLCP Processor block is NOT declaring the PLCP LOF defect condition. ***NOTE:*** *This output pin is only active is the XRT79L71 has been configured to operate in both the ATM UNI/PLCP Modes.*
C5	RxNib_0/ RxHDLCDat_0	O	**Receive Nibble Interface Output pin - Bit 0/Receive HDLC Controller Data Bus output pin - Bit 0:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel/Nibble-Parallel Mode, the High-Speed HDLC Controller Mode, or in some other mode. **Clear-Channel/Nibble-Parallel Mode - RxNib_0:** The XRT79L71 will output Received data from the remote terminal equipment to the System-Side terminal equipment via this pin, along with RxNib_1 through RxNib_3. This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's System-Side terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - Receive High-Speed HDLC Controller Output Interface Block - Data Bus Output Pin #0 - RxHDLCDat_0:** This output pin along with RxHDLCDat_[7:1] functions as the Receive High-Speed HDLC Controller Output Interface byte wide output data bus. This particular output pin functions as the LSB (Least Significant Bit) of the Receive High-Speed HDLC Controller byte wide data bus. The Receive High-Speed HDLC Controller will output the contents of all HDLC frames and flag sequence octects via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. ***NOTE:*** *This output pin is only active if the XRT79L71 is configured to operate in either the Clear-Channel/ Framer/Nibble-Parallel Mode or in the High-Speed HDLC Controller Mode. This output is inactive for all remaining modes.*

PIN #	NAME	TYPE	DESCRIPTION
B7	RxOHEnable/ RxHDLCDat_5	O	**Receive Overhead Data Output Interface - Enable Output/Receive HDLC Controller Data Bus - Bit 5 output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHEnable:** The XRT79L71 will assert this output signal for one RxOHClk period when it is safe for the System-Side terminal equipment to sample the data on the RxOH output pin. **High-Speed HDLC Controller Mode - RxHDLCDat_5:** This output pin along with RxHDLCDat_[4:0], RxHDLCDat_6 and RxHDLCDat_7 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
C7	RxOH/ RxHDLCDat_6	O	**Receive Overhead Data Output Interface - output/Receive HDLC Controller Data Bus - Bit 6 output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOH:** All overhead bits, which are received via the Receive Section of the XRT79L71 will be output via this output pin, upon the rising edge of RxOHClk. **High-Speed HDLC Controller Mode - RxHDLCDat_6:** This output pin along with RxHDLCDat_[5:0] and RxHDLCDat_7 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
A7	RxOHClk/ RxHDLCClk	O	**Receive Overhead Data Output Interface - clock/Receive HDLC Controller - Clock output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHClk:** The XRT79L71 will output the overhead bits within the incoming DS3 or E3 frames via the RxOH output pin, upon the falling edge of this clock signal. As a consequence, the user's System-Side terminal equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. ***NOTE:*** *This clock signal is always active.* **High-Speed HDLC Controller Mode - RxHDLCClk:** This output pin functions as the Receive HDLC Controller Data bus clock output. The Receive HDLC Controller block outputs the contents of all received HDLC frames via the Receive HDLC Controller Data bus (RxHDLCDat_[7:0]) upon the rising edge of this clock signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of this clock signal.

PIN #	NAME	TYPE	DESCRIPTION
A8	RxOHFrame/ RxHDLCDat_4	O	**Receive Overhead Data Interface - Framing Pulse indicator/Receive HDLC Controller Data Bus - Bit 4 output:** The function of this output pins depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHFrame:** This output pin pulses "High" whenever the Receive Overhead Data Output Interface block outputs the first overhead bit of a new DS3 or E3 frame. **High-Speed HDLC Controller Mode - RxHDLCDat_4:** This output pin along with RxHDLCDat_[3:0] and RxHDLCDat_[7:5] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's System-Side terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
B6	RxFrame	O	**Receive Boundary of DS3 or E3 Frame Output indicator:** The function of this output pin depends upon whether or not the XRT79L71 is operating in the Clear-Channel Framer/Nibble-Parallel Mode. **Clear-Channel Framer/Nibble-Parallel Mode:** The Receive Section of the XRT79L71 will pulse this output pin "High" for one nibble period, when the Receive Payload Data Output interface block is driving the very first nibble of a given DS3 or E3 frame, on the RxNib[3:0] output pins. **Clear-Channel Framer/Serial Mode:** The Receive Section of the XRT79L71 will pulse this output pin "High" for one bit period, when the Receive Payload Data Output interface block is driving the very first bit of a given DS3 or E3 frame, on the RxSer output pin. **All Other Modes:** The Receive Section of the XRT79L71 will pulse this output pin "High" when the Receive DS3/E3 Framer block is processing the first bit within a new DS3 or E3 frame.
D4	RxCellRxed	O	**Receive Cell Processor - Cell Received Indicator:** This output pin pulses "High" (for one DS3 or E3 clock period) each time the Receive ATM Cell Processor receives a new cell from the Receive PLCP Processor or the Receive DS3/E3 Framer block. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the ATM UNI Mode.*

PIN #	NAME	TYPE	DESCRIPTION
A5	RxPOH/ RxSer	O	**Receive PLCP Path Overhead Output pin/Receive Serial Output pin:** The function of this output depends upon whether the XRT79L71 has been configured to operate in the ATM/PLCP Mode or in the Clear-Channel Framer Mode. **ATM/PLCP Mode - RxPOH (Receive PLCP Path Overhead Output pin):** This output pin along with the RxPOHClk, RxPOHFrame and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. For each PLCP frame, that is received by the Receive PLCP Processor, this serial output port will output the contents of all 12 POH (Path Overhead) bytes. The data that is output via this pin, is updated on the rising edge of the RxPOHClk output clock signal. The RxPOHFrame pin will pulse "High" whenever the first bit of the Z6 byte is being output via this output pin. ***NOTE:*** *This pin is not active if the user has configured the XRT79L71 to operate in the ATM UNI/Direct Mapped Mode* **Clear-Channel Framer Mode - RxSer RxSer (Receive Serial Output pin):** If the XRT79L71 is configured to operate in the Clear-Channel Framer/Serial Mode, then the chip will output all received data, via this output pin. This output signal will be updated upon the rising edge of RxClk. ***NOTE:*** *The user should either configure the the Receive Payload Data Output Interface block to operate in the Gapped-Clock Mode, or the user must validate the sampling of each bit from the RxSer output with the state of RxOHInd' output pin, in order to prevent the System-Side terminal equipment from sampling overhead bits.* This output pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP or the Clear-Channel Framer/Serial Mode. This pin is inactive for all remaining modes of operation.

PIN #	NAME	TYPE	DESCRIPTION
A6	RxPOH_Clk/ RxClk/ RxNibClk	O	**Receive PLCP Path Overhead Serial Port Clock output/Receive Nibble-Parallel Output port clock/Receive Serial Clock output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM/PLCP Mode or the Clear-Channel Framer Mode. **ATM/PLCP Mode - RxPOH_Clk:** This output clock pin along with RxPOH, RxPOHFrame and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. All POH (Path Overhead) data that is output via the RxPOH output pin is updated on the rising edge of this clock signal. ***NOTE:*** *This output signal is inactive if the XRT79L71 has been configured to operate in the Direct-Mapped ATM Mode.* **Clear-Channel Framer Mode - RxClk:** This output pin is active whenever the XRT79L71 has been configured to operate in either the Serial or Nibble Parallel Mode, as is described below.Clear-Channel Framer/Serial Mode - RxClkIn this serial mode, this output is a 44.736MHz clock output signal (for DS3 applications) or 34.368MHz clock output signal (for E3 applications). The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the System-Side terminal equipment to sample the RxSer data, upon the falling edge of this clock signal. **Clear-Channel Framer/Nibble-Parallel Mode - RxNibClk:** In the Nibble-Parallel Mode, the XRT79L71 will derive this clock signal from the RxLineClk signal. The XRT79L71 will pulse this clock signal 1176 times for each inbound DS3 frame or 1074 times for each inbound E3/ITU-T G.832 frame or 384 times for each inbound E3/ITU-T G.751 frame. The Receive Payload Data Output Interface block will update the data on the RxNib[3:0] output upon the falling edge of this clock signal. The user is advised to design (or configure) the System-Side terminal equipment to sample the data on the RxNib[3:0] output pins, upon the rising edge of this clock signal.
C4	RxPOHFrame	O	**Receive PLCP Frame POH Serial Output Port - Frame Indicator:** This output pin along with the RxPOH RxPOHClk and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. This output pin provides framing information to external circuitry receiving and processing this POH (Path Overhead) data, by pulsing "High" whenever the first bit of the Z6 byte is being output via the RxPOH output pin. This pin is "Low" at all other times during this PLCP POH Framing cycle. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Modes.*

PIN #	NAME	TYPE	DESCRIPTION
C6	RxPFrame/ RxOHInd	O	**Receive PLCP Frame Indicator/Receive Overhead Indicator Output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM/PLCP, the Clear-Channel Framer/Serial or the Clear-Channel Framer/Nibble-Parallel Modes. **ATM/PLCP Mode - RxPFrame - Receive PLCP Frame Indicator Output:** This output pin pulses "High" when the Receive PLCP Processor is receiving the last bit of a PLCP frame. ***NOTE:*** *This output pin is inactive if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode.* **Clear-Channel Framer/Serial Mode - RxOHInd RxOHInd - Receive Overhead Indicator Output:** This output pin pulses "High" for one bit-period whenever an overhead bit is being output via the RxSer output pin, by the Receive Payload Data Output Interface block. ***NOTE:*** *If the user configures the Receive Payload Data Output Interface block to operate in the Gapped-Clock Mode, then this output pin will provide a demand clock to the System-Side terminal equipment In the Gapped-Clock Mode, this output pin will only provide a clock pulse, whenever a payload bit is being output via the RxSer output pin. This output pin will NOT generate a clock pulse, whenever an overhead is being output via the RxSer output pin.* **Clear-Channel Framer/Nibble-Parallel - RxOHInd RxOHInd - Receive Overhead Indicator Output:** This output pin pulse "High" for one nibble-period whenever an overhead nibble is being output via the RxNib[3:0] output pins by the Receive Payload Data Output Interface block. ***NOTES:*** 1. *1.If the XRT79L71 has been configured to operate in both the DS3 and the Nibble-Parallel Modes, then the RxOHInd output pin will be inactive and will pulled "Low" at all times.* 2. *If the XRT79L71 has been configured to operate in both the E3 and the Nibble-Parallel Mode, then the RxOHInd output pin will be active and will pulse "High" to denote overhead nibbles.* 3. *The purpose of this output pin is to alert the System-Side terminal equipment that an overhead bit (or nibble) is being output via the RxSer or RxNib[3:0] output pins and that this data should be ignored.*

PIN #	NAME	TYPE	DESCRIPTION
C3	RxGFC/ RxIdle	O	**Receive GFC Nibble Field - Output Pin/Receive Idle Sequence Indicator:** The function of this output pin depends upon whether the XRT79L71 is operating in the ATM Mode or in the High-Speed HDLC Controller Mode. **ATM Mode - RxGFC:** This pin, along with the RxGFCClk and the RxGFCMSB pins form the Receive GFC Nibble-Field serial output port. This pin will serially output the contents of the GFC Nibble field of each cell that is processed via the Receive Cell Processor. This data is serially clocked out of this pin on the rising edge of the RxGFCClk signal. The MSB of each GFC value is designated by a pulse at the RxGFCMSB output pin. **High-Speed HDLC Controller Mode - RxIdle:** The combination of the RxIdle and ValidFCS output signals are used to convey information about data that is being output via the Receive HDLC Controller output Data bus (RxHDLCDat_[7:0]). ***If RxIdle = "High":*** The Receive HDLC Controller block will drive this output pin "High" anytime the flag sequence octet (0x7E) is present on the RxHDLCDat[7:0] output data bus. ***If RxIdle and ValidFCS are both "High":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame are valid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame is invalid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received an ABORT sequence. ***NOTE:*** *: This output pin is in-active if the XRT79L71 has been configured to operate in either the Clear-Channel Framer or in the PPP Modes.*
A1	RxGFCClk	O	**Received GFC Nibble Serial Output Port Clock Signal:** This output pin functions as a part of the Receive GFC Nibble-Field Serial Output Port, also consisting of the RxGFC and RxGFCMSB pins. This pin provides a clock pulse which allows external circuitry to latch in the GFC Nibble-Data via the RxGFC output pin. ***NOTE:*** *This output pin is only active if the XRT79L71 is operating in the ATM UNI Mode.*
B1	RxGFCMSB	O	**Receive GFC Nibble Field - MSB Indicator:** This output pin functions as a part of the Receive GFC Nibble Field Serial Output port which also consists of the RxGFC and RxGFCClk pins. This pin pulses "High" the instant that the MSB (Most Significant Bit) of a GFC Nibble is being output on the RxGFC pin. ***NOTE:*** *This output pin is only active if the XRT79L71 is operating in the ATM UNI Mode.*

PIN #	NAME	TYPE	DESCRIPTION
H1	RxUClav/RxPPA	O	**Receive UTOPIA - Cell Available/Receive POS-PHY Interface - Packet Available:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - RxUClav - Receive UTOPIA Interface - Cell Available Indicator Output:** The Receive UTOPIA Interface block will assert this output pin in order to indicate that the RxFIFO has some ATM cell data that needs to be read out by the ATM Layer Processor. This signal will be asserted (e.g., toggles to a logic "High" level) if the RxFIFO contains at least one full ATM cell of data. This signal toggle "Low" if the RxFIFO is depleted of data, or if it contains less than one full cell of data. The exact behavior of the RxUClav output pin, as a function of UTOPIA Level is presented below. **Multi-PHY Operation - UTOPIA Level 2:** When the XRT79L71 is operating in a Multi-PHY Application and is configured to operate in the UTOPIA Level 2 Mode, then this signal will be tri-stated until the RxUClk cycle following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents on the Receive UTOPIA Address bus pins , RxUAddr[4:0], match that which have been assigned to this particular Receive UTOPIA Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the RxFIFO. **Multi-PHY Operation - UTOPIA Level 3:** When the XRT79L71 is operating in a Multi-PHY Application, then this signal will be tri-stated until two RxUClk cycles following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents of the Receive UTOPIA Address bus input pins, RxUAddr[4:0], match that which have been assigned to this particular Receive UTOPIA Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the RxFIFO. **PPP Mode - RxPPA - Receive POS-PHY Interface - Packet Available Indicator Output** The XRT79L71 will drive this output pin "High" whenever a (programmable) number of bytes of incoming PPP Packet data are available to be read from the RxFIFO by the Link Layer Processor. The exact behavior of the RxPPA output pin, as a function of POS-PHY Level is presented below. **POS-PHY Level 2:** When the XRT79L71 is configured to operate in the POS-PHY Level 2 Mode, then this signal will be tri-stated until the RxPClk cycle following the assertion of a valid address on the Receive POS-PHY Address bus input pins (e.g., if the contents on the Receive POS-PHY Address bus pins, RxPAddr[4:0], match that which have been assigned to this particular Receive POS-PHY Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the RxFIFO. **POS-PHY Level 3:** When the XRT79L71 is configured to operate in the POS-PHY Level 3 Mode, then this signal will be tri-stated until two RxPClk cycles following the assertion of a valid address on the Receive POS-PHY Address bus input pins (e.g., if the contents on the Receive POS-PHY Address bus pins, RxPAddr[4:0], match that which have been assigned to this particular Receive POS-PHY Interface block). Afterwards, this output pin will be driven either "High" or "Low" depending upon the current fill status of the RxFIFO.

PIN #	NAME	TYPE	DESCRIPTION
K2	RxUClkO/ RxPClkO	O	**Receive UTOPIA Interface Clock/Receive POS-PHY Interface Clock Output:** This clock output signal is derived from an internal PLL.
L3	RxUClk/ RxPClk	I	**Receive UTOPIA Interface Clock Input/Receive POS-PHY Interface Clock Input:** The function of this input pin depends upon whether the XRT79L71 is operating in the ATM UNI or PPP Mode. **ATM UNI Mode - RxUClk:** The byte (or word) data, on the Receive UTOPIA Data bus (RxUData[15:0]) is updated on the rising edge of this signal. The Receive UTOPIA Interface can be clocked at rates up to 50 MHz. **PPP Mode - RxPClk:** This byte (or word) data, on the Receive POS-PHY Data Bus (RxPData[15:0]) is updated on the rising edge of this signal. The Receive POS-PHY Interface can be clocked at rates up to 50MHz. ***NOTE:*** *The user should tie this pin to GND to operate the XRT79L71 in the Clear-Channel Framer or High-Speed HDLC Controller Modes.*
L2	RxPERR	O	**Receive POS-PHY Interface - Error Indicator:** This output pin indicates whether or not the Receive PPP Packet Processor block has detect any of the following types of erred packets within the incoming PPP Packet data-stream. • Packets with FCS Errors· • Aborted Packets • RUNT Packets Anytime the Receive PPP Packet Processor block detects these types of PPP Packets, then the XRT79L71 will pulse this output pin "High" coincident to whenever the Receive POS-PHY Interface block outputs the very last byte or 16-bit word of the erred packet via the RxPData[15:0] output pins.The XRT79L71 will hold this output pin "Low" at all other times. ***NOTE:*** *This output pin is only valid if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
K4	RxTSX/ RxPSOF	O	**Receive - Change of Port Indicator Output/Receive - Start of PPP Packet in Chunk Mode:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Packet Mode or Cell-Chunk Mode. **Packet Mode - RxTSX - Receive POS-PHY Interface - Change of Port Indicator Output (POS-PHY Level 3, Packet Mode Only):** The XRT79L71 pulses this output pin "High" when an in-band port address is present on the RxPData[15:11] output pins. When this output pin is "High", the value of RxPData[15:11] is the address value of the RxFIFO to be selected. This is an indication (to the Link Layer Processor) that subsequent read operations, from RxPData[15:0] will be from the RxFIFO (or Receive POS-PHY Port) corresponding to this particular in-band address. ***NOTE:*** *In order to avoid Receive POS-PHY Interface bus contentions, we advise that the user avoid configuring the XRT79L71 in the POS-PHY Level 3 Mode.* **Chunk Mode - RxPSOF - Receive Start of Packet Output Indicator:** The XRT79L71 pulses this output pin "High" in order to indicate that the first byte (or word) of a given Packet is placed on the RxPData[15:0] pins. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the POS-PHY Level 3, Packet Mode or in the Chunk Mode.*
H4	$\overline{\text{RxUEN}}$/ $\overline{\text{RxPEN}}$	I	**Receive UTOPIA Interface - Output Enable/Receive POS-PHY Interface - Output Enable:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP mode. **ATM UNI Mode - $\overline{\text{RxUEN}}$ - Receive UTOPIA Interface - Read/Output Enable Input pin:** This active-"Low" input signal is used to control the drivers of the Receive UTOPIA Data Bus. When this signal is "High" (negated) then the Receive UTOPIA Data Bus is tri-stated. When this signal is asserted (e.g., pulled to a logic "Low" level), then the contents of the byte or word that is at the front of the RxFIFO will be popped and placed on the Receive UTOPIA Data bus on the very next rising edge of RxUClk. **PPP Mode - $\overline{\text{RxPEN}}$ - Receive POS-PHY Interface - Read/Output Enable Input pin:** This active-"Low" input signal is used to control the drivers of the Receive POS-PHY Data Bus. When this signal is "High" (negated) then the Receive POS-PHY Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the front of the RxFIFO will be popped and placed on the Receive POS-PHY Data bus on the very next rising edge of RxPClk. ***NOTE:*** *The user should tie these input pins to GND, to operate the XRT79L71 in either the Clear-Channel Framer or High-Speed HDLC Controller Modes.*

PIN #	NAME	TYPE	DESCRIPTION
H2	RxUSoC/ RxPSOP RxPSOC	O	**Receive UTOPIA Interface - Start of Cell Indicator/Receive POS-PHY Interface - Start of Packet Indicator (Packet Mode)/Receive POS-PHY Interface - Start of Chunk Indicator (Chunk Mode):** The exact function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI Mode, the PPP Packet Mode, or in the PPP Chunk Mode as described below. **ATM UNI Mode - RxUSoC - Receive Start of Cell Indicator Output:** This output pin allows the ATM Layer Processor to determine the boundaries of the ATM cells that are output via the Receive UTOPIA Data bus. The Receive UTOPIA Interface block will assert this signal when the first byte (or word) of a new cell is present on the Receive UTOPIA Data Bus; RxUData[15:0]. PPP Packet Mode - RxPSOP - Receive Start of Packet Indicator Output (Packet Mode):This output pin allows the Link Layer Processor to determine the boundaries of the PPP packets that are output via the Receive POS-PHY Data Bus. The Receive POS-PHY Interface block will assert this signal when the first byte (or word) of a new packet is present on the Receive POS-PHY Data Bus, RxPData[15:0]. **PPP Chunk Mode - RxPSOC - Receive Start of Chunk Indicator Output (Chunk Mode):** If the XRT79L71 has been configured to operate in the Chunk Mode, then the Receive POS-PHY Interface block will pulse this output pin "High" coincident to whenever it outputs the very first byte (or 16-bit word) of a given Chunk onto the Receive POS-PHY Data Bus (RxPData[15:0]) output pins. The Receive POS-PHY Interface block will keep this output pin "Low" at all other times. ***NOTE:*** *In the PPP Chunk Mode, the RxPSOF output pin will function as the Start of Packet Output Indicator pin.*
H3	RxUPrty/ RxPPrty/ RxPSOC	O	**Receive UTOPIA Interface - Parity Output pin/Receive POS-PHY Interface - Parity Output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or the PPP Modes. **ATM UNI Mode - RxUPrty:** The Receive UTOPIA interface block will compute the odd-parity value of each byte (or word) that it will place in the Receive UTOPIA Data Bus. This odd-parity value will be output on this pin, while the corresponding byte (or word) is present on the Receive UTOPIA Data Bus **PPP Mode - RxPPrty:** The Receive POS-PHY Interface block will compute the odd-parity value of each byte (or word) that it will place in the Receive POS-PHY Data Bus. This odd parity value will be output on this pin, which the corresponding byte (or word) is present on the Receive POS-PHY Data Bus. ***NOTE:*** *This output pin will be in-active if the user has configured the XRT79L71 to operate in either the Clear-Channel Framer or in the High-Speed HDLC Controller Modes.*
K3	RxPEOP	O	**Receive POS-PHY Interface - End of Packet:** The XRT79L71 drives this output pin "High" whenever the last byte of a given Packet is being output via the RxPData[15:0] data bus. ***NOTES:*** 1. *This output pin is only valid when the XRT79L71 is configured to operate in the PPP Mode.* 2. *This output pin is only valid when the Receive POS-PHY Interface - Read Enable Output pin.*

PIN #	NAME	TYPE	DESCRIPTION
N2	RxPDVAL	O	**Receive POS-PHY Interface Signal Valid Indicator:** This output signal indicates whether or not the Receive POS-PHY Interface signals (e.g., RxPData[15:0], RxPSOP, RxPEOP, RxPPrty, RxPERR) are valid. This output pin will be driven "High", when these signals are valid. Conversely, this output pin will be driven "Low" when these signals are NOT valid. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
J1 J2 J3 J4 K1	RxUAddr_0/ RxPAddr_0 RxUAddr_1/ RxPAddr_1 RxUAddr_2/ RxPAddr_2 RxUAddr_3/ RxPAddr_3 RxUAddr_4/ RxPAddr_4	I	**Receive UTOPIA Interface Address Bus input MSB Receive POS-PHY Interface Address Bus Input pins:** The exact function of these input pins depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Modes. **ATM UNI Modes - RxUAddr[4:0] - Receive UTOPIA Address Bus:** These input pins functions as the Receive UTOPIA Address bus inputs. These input pins are only active when the XRT79L71 is operating in both the ATM UNI and Multi-PHY Modes. Whenever the ATM Layer Processor wishes to poll or read data from a particular UNI (PHY-Layer) device, it will provide the UTOPIA Address of the target PHY-Layer device on the Receive UTOPIA Address Bus. The Receive UTOPIA Address Bus input is sampled on the rising edge of the RxUClk signal. Each time the Receive UTOPIA Interface block samples the Receive UTOPIA Address Bus, the contents of this address bus are compared with the pre-programmed UTOPIA Address value (which was loaded into the XRT79L71 by writing the appropriate data into both the Receive UTOPIA Port Address Register (Address = 0x0513) and the Receive UTOPIA Port Number Register (Address = 0x0517). If these two values match, and the $\overline{\text{RxUEN}}$ input pin is asserted, then the RxUClav output pin will be driven to the appropriate state (based upon the RxFIFO fill level). If these two address values do not match, then the Receive UTOPIA Interface block will continue to tri-state the RxUClav output pin. ***NOTE:*** *These input pins are only active if the XRT79L71 has been designed into a Multi-PHY Application. If the user intends to design the XRT79L71 into a Single-PHY Application, then the user should tie these input pins to GND.* **PPP Mode - RxPAddr[4:0] - Receive POS-PHY Interface Address Bus Input Pins:** These input pins comprise the Receive POS-PHY Address Bus input pins. Whenever the Link Layer Processor wishes to poll or read PPP packet data from a particular PHY-Layer device, it will provide the address of the target PHY-Layer device on the Receive POS-PHY Address Bus. The contents of the Receive POS-PHY Address Bus input pins are sampled on the rising edge of RxPClk. The XRT79L71 will compare the data on the Receive POS-PHY Address Bus with the pre-programmed POS-PHY Address value (which was loaded into the XRT79L71 by writing the appropriate data into the Receive POS-PHY Interface - Receive Control Register - Byte 0 (Address = 0x0502). If these two values are identical and the $\overline{\text{RxPEN}}$ input pin is asserted, then the RxPPA output pin will be driven to the appropriate state (based upon the RxFIFO fill-level). If these two values do not match, then the Receive POS-PHY Interface block will continue to tri-state the RxPPA output pin. These input pins are only active if the XRT79L71 has been configured to operate in either the ATM UNI or PPP Modes. The user should tie these input pins to GND to operate the XRT79L71 in either the Clear-Channel Framer or High-Speed HDLC Controller Modes.

PIN #	NAME	TYPE	DESCRIPTION
G2 G1 F1 G3 F2 E1 G4 F3 E2 D1 F4 E3 D2 C1 E4 D3	RxUData_0/ RxPData_0 RxUData_1/ RxPData_1 RxUData_2/ RxPData_2 RxUData_3/ RxPData_3 RxUData_4/ RxPData_4 RxUData_5/ RxPData_5 RxUData_6/ RxPData_6 RxUData_7/ RxPData_7 RxUData_8/ RxPData_8 RxUData_9/ RxPData_9 RxUData_10/ RxPData_10 RxUData_11/ RxPData_11 RxUData_12/ RxPData_12 RxUData_13/ RxPData_13 RxUData_14/ RxPData_14 RxUData_15/ RxPData_15	O	**Receive UTOPIA Data Bus Input/Receive POS:** The function of these output pins depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - RxUData[15:0]-PHY Data Bus Output pins - Receive UTOPIA Interface Data Bus Output pins:** These output pins function as the Receive UTOPIA Data Bus output pins. Whenever the ATM Layer Processor wishes to read out ATM cell data that has been received from the Remote Terminal Equipment, the Receive UTOPIA Interface block will output this data via the Receive UTOPIA Data Bus, where it can be read and processed by the ATM Layer Processor. **PPP Mode - RxPData[15:0]:** These output pins function as the Receive POS-PHY Data Bus output pins. PPP Packet data that has been received from the Remote Terminal Equipment is output on the Receive POS-PHY Data Bus, where it can be reads and processed by the Link Layer Processor.
L1	RxMod	O	**Receive PPP Data Bus - Modulus Indicator:** The XRT79L71 will indicate the number of valid packet octets that are being read out of the RxPData[15:0] output pins. The XRT79L71 will drive this output pin "Low" when both bytes of the RxPData[15:0] data bus consists of valid packet data. Conversely, the XRT79L71 will drive this output pin "High" when only the upper byte of the RxPData[15:0] data bus consists of valid packet data. The Link Layer Processor is expected to validate all packet data that it reads out of the RxPData[15:0] output pins by also reading the state of this output pin. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
TRANSMIT LINE SIDE SIGNALS			
R15	TxON	I	**Transmit Driver ON - Channel n:** This input pin is used to either enable or disable the Transmit Output Driver within the Transmit DS3/E3 LIU Block. "Low" - Disables the Transmit Output Driver within the Transmit DS3/E3 LIU Block. In this setting, the TTIP and TRING output pins will be tri-stated. "High" - Enables the Transmit Output Driver within the Transmit DS3/E3 LIU Block. In this setting, the TTIP and TRING output pins will be enabled. ***NOTES:*** *1. Whenever the transmitters are turned off , the TTIP and TRING output pins will be tri-stated.* *2. These pins are internally pulled "High".*
P16	DS3CLK /SFMCLK	I	**Clock Recovery PLL DS3 Reference Clock Input/12.288MHz SFM Reference Clock Input:** The function of this input pin depends upon whether or not the XRT79L71 has been configured to operate in the SFM (Single Frequency Mode) Mode, as described below. **If the XRT79L71 is NOT operating in the Single-Frequency Mode** If the XRT79L71 has NOT been configured to operate in the SFM Mode, then this input pin will functions as the Reference Clock for the Clock Recovery PLL and the Jitter Attenuator PLL within the Receive DS3/E3 LIU Block, whenever the XRT79L71 has been configured to operate in the DS3 Mode. ***NOTE:*** *For DS3/Non-SFM Modes of operation, the user is expected to supply a 44.736MHz ± 20ppm clock signal to this input pin.* **If the XRT79L71 is operating in the Single-Frequency Mode** If the user has configured the XRT79L71 to operate in the SFM Mode, then the user MUST apply a clock signal with a frequency of 12.288MHz ± 20ppm to this input pin. The SFM Synthesizer block (within the Receive DS3/E3 LIU Block) will then synthesize one of the appropriate line rate frequencies (e.g., 34.368MHz for E3 and 44.736MHz for DS3) based upon this 12.288MHz Reference Clock source. ***NOTE:*** *If the user does not intend to operate the XRT79L71 in the SFM Mode, nor the DS3 Mode, tie this input pin to GND.*

PIN #	NAME	TYPE	DESCRIPTION
M16	E3CLK	I	**Clock Recovery PLL E3 Reference Clock Input:** The function of this input pin depends upon whether or not the XRT79L71 has been configured to operate in the SFM (Single-Frequency Mode) Mode, as described below. **If the XRT79L71 is NOT operating in the Single-Frequency Mode** If the XRT79L71 has NOT been configured to operate in the SFM Mode, then this input pin will function as a Reference Clock signal for the Clock Recovery PLL and the Jitter Attenuator PLL within the Receive DS3/E33 LIU Block, whenever the XRT79L71 has been configured to operate in the E3 Mode. ***NOTE:*** *For E3/Non-SFM Modes of operation, the user is expected to supply a 34.368MHz ± 20ppm clock signal to this input pin.* **If the XRT79L71 is operating in the Single-Frequency Model** f the user has configured the XRT79L71 to operate in the SFM Mode, then the user MUST apply a clock signal with a frequency of 12.288 ± 20ppm to the DS3CLK/SFMCLK input pin (Ball P16). Additionally, the user MUST tie this input pin to GND. ***NOTE:*** *If the user only intends to operate the XRT79L71 in the DS3/Non-SFM Mode, then the user should tie this input pin to GND.*
T11	TTIP	O	**Transmit Output - Positive Polarity Signal:** This output pin, along with the TRING output pin, function as the Transmit DS3/E3 output signal drivers for the XRT79L71. The user is expected to connect this signal and the TRING output signal to a 1:1 transformer. Whenever the Transmit Section of the XRT79L71 generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a higher-voltage than the TRING output pin. Conversely, whenever the Transmit Section of the XRT79L71 generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a lower-voltage than that of the TRING output pin. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the TxON input pin (or bit-field) to "0".*
T10	TRING	O	**Transmit Output - Negative Polarity Signal:** This output pin along with the TTIP output pin, functions as the Transmit DS3/E3 output signal drivers for the XRT79L71. The user is expected to connect this signal and the TTIP output signal to a 1:1 transformer. Whenever the Transmit Section of the XRT79L71 generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a lower-voltage than the TTIP output pin. Conversely, whenever the Transmit Section of the XRT79L71 generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a higher-voltage than that of the TTIP output pin. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the TxON input pin (or bit-field) to "0".*

PIN #	NAME	TYPE	DESCRIPTION
P10	MTIP	I	**Transmit Drive Monitor Input pin - Positive Polarity Input:** This input pin along with MRING functions as the Transmit Drive Monitor Output (DMO) input monitoring pins. If the user wishes to (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then the user MUST connect this particular pin to the TTIP output pin via a 274 ohm series resistor. Similarly, the user MUST also connect the MRING input pin to the TRING output pin via a 274 ohm series resistor. The MTIP and MRING input pins will continuously monitor the Transmit Output line signal via the TTIP and TRING output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the DMO output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. This input pin is inactive if the user choose to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the user is operating the XRT79L71 in the Host Mode.*
P11	MRING	I	**Transmit Drive Monitor Input pin - Negative Polarity Input:** This input pin along with MTIP functions as the Transmit Drive Monitor Output (DMO) input monitoring pins. If the user wishes to (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then the user MUST connect this particular input pin to the TRING output pin via a 274 ohm series resistor. Similarly, the user MUST also connect the MTIP input pin to the TTIP output pin via a 274 ohm series resistor. The MTIP and MRING input pins will continuously monitor the Transmit Output line signal via the TTIP and TRING output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the DMO output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. This input pin is inactive if the user chooses to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the user is operating the XRT79L71 in the Host Mode.*

PIN #	NAME	TYPE	DESCRIPTION
RECEIVE LINE SIDE SIGNALS			
R14	RTIP	I	**Receive Input - Positive Polarity Signal:** This input pin, along with the RRING input pin, functions as the Receive DS3/E3 Line Signal input for the XRT79L71. The user is expected to connect this signal and the RRING input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3 or E3 line signal, this input pin will be pulsed to a higher-voltage than that of the RRING input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3 or E3 line signal, this input pin will be pulsed to a lower-voltage than that of the RRING input pin.

PIN #	NAME	TYPE	DESCRIPTION
R13	RRING	I	**Receive Input - Negative Polarity Signal:** This input pin, along with the RTIP input pin, functions as the Receive DS3/E3 Line Signal input for the XRT79L71. The user is expected to connect this signal and the RTIP input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3 or E3 line signal, then this input pin will be pulsed to a lower-voltage than that of the RTIP input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3 or E3 line signal, then this input pin will be pulsed to a higher-voltage than that of the RTIP input pin.
K16	CLKOUT	O	**SFM Synthesizer/Clock Recovery PLL Reference Clock Output:** The exact source of this output signal depends upon whether or not the XRT79L71 has been configured to operate in the SFM (Single-Frequency Mode) Mode, as described below. **If the XRT79L71 is configured to operate in the SFM Mode** If the XRT79L71 has been configured to operate in the SFM Mode, then the CLKOUT output pin (if enabled) will output a 44.736MHz clock signal (if the XRT79L71 is configured to operate in the DS3 Mode) or a 34.368MHz clock signal (if the XRT79L71 is configured to operate in the E3 Mode. ***NOTES:*** 1. *In this case, the 44.736MHz or 33.368MHz clock (that is output via the CLKOUT signal) will ultimately be derived from the 12.288MHz clock signal that is being applied to the DS3CLK/SFMCLK input pin.2.* 2. *This output pin is only active if Bit 6 (SFM Clock Out Enable), within the LIU Channel Control Register (Address = 0x1306) has been set to "1".* **If the XRT79L71 is NOT configured to operate in the SFM Mode** If the XRT79L71 has NOT been configured to operate in the SFM Mode, then frequencies of the CLKOUT output signal will be as follows. **a.** If the XRT79L71 has been configured to operate in the DS3 Mode, then the XRT79L71 will simply output a buffered version of the signal that is being applied to the DS3CLK/SFMCLK input pin (which should be a 44.736MHz clock signal). **b.** If the XRT79L71 has been configured to operate in the E3 Mode, then the XRT79L71 will simply output a buffered version of the signal that is being applied to the E3CLK input pin (which should be a 34.368MHz clock signal). ***NOTE:*** *This output pin is only if Bit 6 (SFM Clock Out Enable), within the LIU Channel Control Register (Address = 0x1306) has been set to "1".*

PIN #	NAME	TYPE	DESCRIPTION
VDD PINS			
G7 G8 G9 G10 K7 K8 K9 K10 H14 N14			3.3V Power Supply Pins
R16	CLKVDD		3.3V Clock Power Supply Pin
T16	JAAVDD		3.3V Jitter Attenuator Analog Power Supply Pin
N13	OVDD		3.3V Output Power Supply Pin
R12	REFAVDD		3.3V Reference Analog Power Supply Pin
T13	RXAVDD		3.3V Receive Analog Power Supply Pin
N11	TXDVDD		3.3V Transmit Digital Power Supply Pin
T12	TXAVDD		3.3V Transmit Analog Power Supply Pin

PIN #	NAME	TYPE	DESCRIPTION
GND PINS			
H7 H8 H9 H10 J7 J8 J9 J10 H15 N15			Ground Pins
N16	CLKGND		3.3V Clock Ground Pin
T15	JAAGND		3.3V Jitter Attenuator Analog Ground Pin
M13	OGND		3.3V Output Ground Pin
P12	REFAGND		3.3V Reference Analog Ground Pin
T14	RXAGND		3.3V Receive Analog Ground Pin
N10	TXDGND		3.3V Transmit Digital Ground Pin
N12	TXAGND		3.3V Transmit Analog Ground Pin

PIN #	NAME	TYPE	DESCRIPTION
NOT CONNECTED PINS			
R11			No Connect Pin

3.0 1.0.0BRIEF XRT79L71 ARCHITECTURE DESCRIPTION

The XRT79L71 can be configured to operate in any of the following modes.

- The Clear-Channel DS3/E3 Framer Mode
- The High-Speed HDLC Controller over DS3/E3 Mode
- The ATM UNI over DS3/E3 Mode
- The PPP over DS3/E3 Mode

The detailed functional description of the XRT79L71, that covers these four modes of operation, can be found in various documents as presented below in Table 2.

TABLE 2: LISTING OF ARCHITECTURAL/FUNCTIONAL DESCRIPTION DOCUMENTS FOR THE XRT79L71

MODE OF OPERATION	ARCHITECTURAL/FUNCTIONAL DESCRIPTION DOCUMENT
DS3/E3 Clear-Channel Framer Mode	**79L71_Arch_Descr_CC.pdf** Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel with LIU IC - Clear-Channel AND High Speed HDLC Controller Mode Applications.Framer Applications
DS3/E3 ATM UNI Mode	**79L71_Arch_Descr_ATM.pdf** Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - ATM UNI Mode Applications.
DS3/E3 PPP Mode	**79L71_Arch_Descr_PPP.pdf** Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - ATM Mode Applications

If the user intends to operate the XRT79L71 in a particular mode, then the user should obtain the appropriate document, which is presented in Table 2. However, a brief functional/architectural description of the XRT79L71, when it is configured to operate in any of these modes will be presented below.

BRIEF FUNCTIONAL ARCHITECTURE DESCRIPTION OF THE XRT79L71 - CLEAR-CHANNEL DS3/E3 FRAMER MODE

If the XRT79L71 has been configured to operate in the Clear-Channel DS3/E3 Framer Mode, then it will have the Functional Architecture as is presented below in Figure 2.

FIGURE 2. THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT79L71 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE CLEAR-CHANNEL DS3/E3 FRAMER MODE

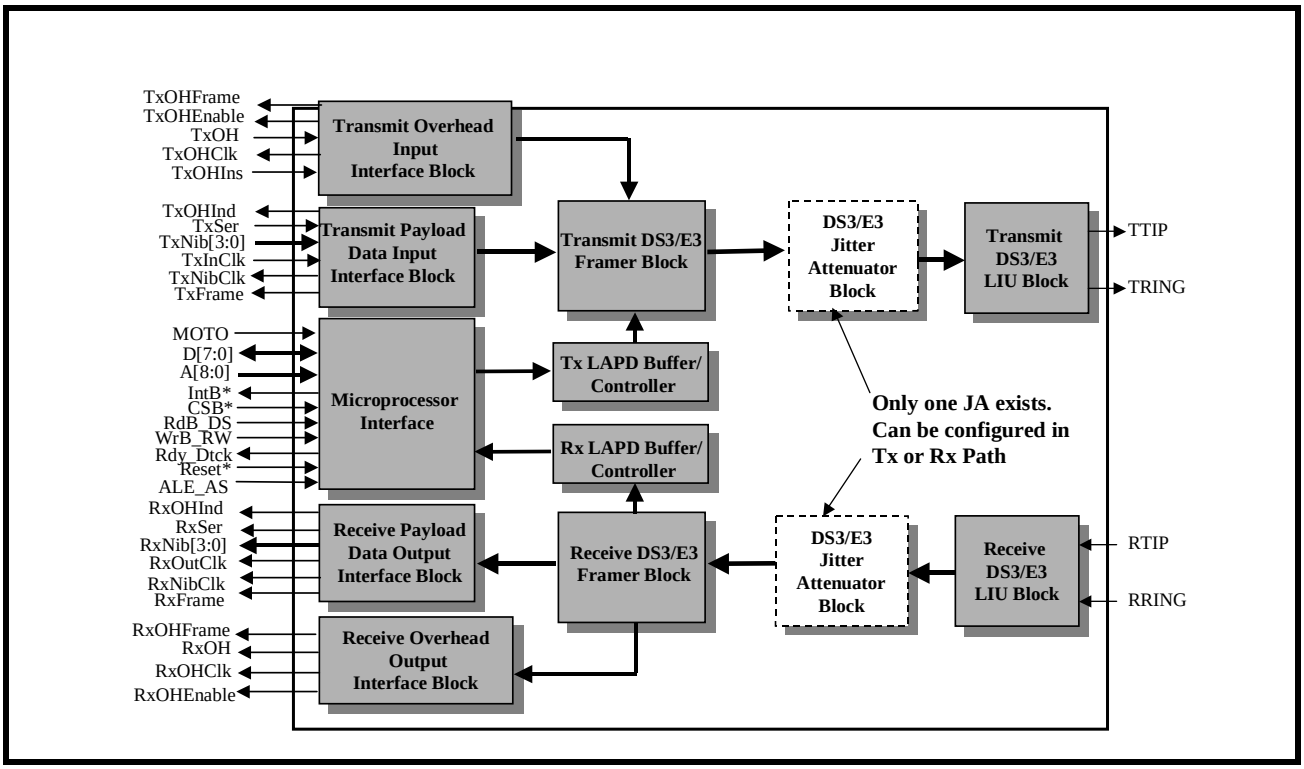

Figure 2 indicates that the XRT79L71 consists of the following functional blocks.

- The Transmit Payload Data Input Interface Block
- The Transmit Overhead Data Input Interface Block
- The Transmit LAPD Controller Block
- The Transmit FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit DS3/E3 Framer Block
- The Transmit DS3/E3 LIU Block
- The Receive DS3/E3 LIU Block
- The Receive DS3/E3 Framer Block
- The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Receive LAPD Controller Block
- The Receive Payload Data Output Interface Block
- The Receive Overhead Data Output Interface Block

Each of these functional blocks is briefly discussed below. These functional blocks will be discussed in considerable detail throughout this data sheet.

The Transmit Payload Data Input Interface Block

The purpose of the Transmit Payload Data Input Interface block is to accept outbound payload data either via a Serial or Nibble-Parallel interface, and to route this data to the Transmit DS3/E3 Framer block (where this data will ultimately be mapped into the payload bit-positions within each outbound DS3/E3 frame).

The Transmit Overhead Data Input Interface Block

The purpose of the Transmit Overhead Data Input Interface block is to permit the user to externally insert his/her own value for overhead bits into the outbound DS3/E3 data-stream.

NOTE: *This particular feature is very valuable in those applications in which the XRT79L71 is processing a Channelized DS3 signal that is of the M23-framing format (where it is imperative to preserve the contents of the C-bits within the DS3 data-stream).*

The Transmit LAPD Controller Block

The purpose of the Transmit LAPD Controller block is to permit the user to transmit LAPD/PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment. The Transmit LAPD Controller block comes with a LAPD Controller/Transmitter and 90 bytes of on-chip RAM (for storage of outbound PMDL Messages), prior to transmission.

The Transmit FEAC Controller Block (for DS3, C-Bit Parity Applications only)

The purpose of the Transmit FEAC Controller block is to permit the user to transmit FEAC (Far-End Alarm & Control) Messages to the remote terminal equipment.

NOTE: *The Transmit FEAC Controller Block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

The Transmit Trail-Trace Message Controller Block

The Transmit SSM Controller Block

The Transmit DS3/E3 Framer Block

The purpose of the Transmit DS3/E3 Framer block is to accept data from the Transmit Payload Data Input Interface block, and Transmit Overhead Data Input Interface, the Transmit LAPD Controller and the Transmit FEAC Controller block and to construct a DS3/E3 data-stream for transmission to the remote terminal equipment. Additionally, the Transmit DS3/E3 Framer block can be configured to do all of the following.

- To transmit the AIS Indicator (upon Software Control)
- To automatically transmit the FERF/RDI Indicator (in response to the Receive DS3/E3 Framer block declare the LOS, LOF/OOF or AIS defect condition).
- To transmit the FERF/RDI indicator (upon Software Control)
- To automatically transmit the FEBE/REI Indicator (in response to the Receive DS3/E3 Framer block detecting Framing bit or CP-bit errors - DS3, C-bit Parity Applications).
- To automatically transmit the FEBE/REI Indicator (in response to the Receive DS3/E3 Framer block detecting BIP-8 Error - E3, ITU-T G.832 Applications).
- To transmit the FEBE/REI indicator (upon Software Control).

The Transmit DS3/E3 LIU Block

The purpose of the Transmit DS3/E3 LIU Block is to accept the outbound DS3/E3 data-stream from the Transmit DS3/E3 Framer block, and to perform all of the following operations on this signal.

- To encode into the B3ZS Line Code (for DS3 Applications) or the HDB3 Line Code (for E3 Applications)
- To convert this outbound DS3 or E3 data into a DS3/E3 line signal and transmit this signal to the remote terminal equipment.

- To generate and transmit DS3 pulses that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE
- To generate and transmit E3 pulses that complies with the ITU-T G.703 Pulse Template requirements for E3 applications.

The Receive DS3/E3 LIU Block

The purpose of the Receive DS3/E3 LIU Block is to receive a DS3/E3 line signal from the remote terminal equipment, and to perform the following operations

- To decode this incoming signal from the B3ZS Line Code (for DS3 Applications) or the HDB3 Line Code (for E3 Applications) into a binary data-stream
- To route this binary data-stream to the Receive DS3/E3 Framer block for further processing
- To detect and flag the occurrence of LCVs (Line Code Violations) and EXZs (Excessive Zeros)
- To insure that the XRT79L71 meets all of the following Receive requirements.
  - **a.** The Receive Sensitivity requirements for DS3 Applications (e.g., able to receive a DSX-3 type of signal through at least 450 feet of cable loss)
  - **b.** The Receive Sensitivity requirements for E3 Applications (e.g., able to receive an E3 signal over 12dB of cable loss)
  - **c.** To comply with the Category I and II Jitter Tolerance Requirements per Bellcore GR-499-CORE (for DS3 Applications)
  - **d.** To comply with the Jitter Tolerance Requirements per ITU-T G.832 (for E3 Applications)
  - **e.** To comply with the Interference Margin Requirements of 20dB, per ITU-T G.703 (for E3 Applications)

The Receive DS3/E3 Framer Block

The purpose of the Receive DS3/E3 Framer block is to acquire and maintain Frame Synchronization with the incoming DS3/E3 data-stream that is receives from the Receive DS3/E3 LIU Block. As the Receive DS3/E3 Framer block performs this task, it will also do the following.

- It will declare and clear the LOS defect condition
- It will declare and clear the LOF/OOF defect condition
- It will declare and clear the AIS defect condition
- It will declare and clear the FERF/RDI defect condition
- It will detect and flag the occurrences of P-bit, CP-bit and Framing bit errors (DS3 Applications)
- It will detect and flag the occurrence of BIP-8 Errors (E3, ITU-T G.832 Applications)
- It will detect and flag the occurrence of BIP-4 Errors (E3, ITU-T G.751 Applications)
- It will detect and flag the occurrence of FEBE/REI Events
- It will route all PMDL data to the Receive LAPD Controller block for further processing
- It will route all Overhead bits/bytes to the Receive Overhead Data Output Interface block for further processing
- It will route all DS3/E3 data to the Receive Payload Data Output Interface block.

The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)

The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The Receive FEAC Controller Block (DS3 Applications Only)

The purpose of the Receive FEAC Controller block is to permit the user to receive FEAC (Far-End Alarm & Control) Messages from the remote terminal equipment.

NOTE: The Receive FEAC Controller Block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.

The Receive LAPD Controller Block

The purpose of the Receive LAPD Controller block is to permit the user to receive LAPD/PMDL (Path Maintenance Data Link) Messages from the remote terminal equipment. The Receive LAPD Controller block comes with a Receive LAPD Controller and 90 bytes of on-chip RAM (for storage of inbound PMDL Messages) after reception.

The Receive Payload Data Output Interface Block

The purpose of the Receive Payload Data Output Interface block is to output payload data (within the incoming DS3 or E3 data-stream) via either a Serial or Nibble-Parallel interface, and to route this data to the off-chip System-Side Terminal Equipment.

The Receive Overhead Data Output Interface Block

The purpose of the Receive Overhead Data Output Interface block is to permit the user to extract out the overhead bits (within the incoming DS3/E3 data-stream) and to route this data to some off-chip System-Side Terminal Equipment circuitry.

A MORE DETAILED FUNCTIONAL/ARCHITECTURAL DESCRIPTION FOR CLEAR-CHANNEL FRAMER MODE

BRIEF FUNCTIONAL ARCHITECTURE DESCRIPTION OF THE XRT79L71 - HIGH-SPEED HDLC CONTROLLER OVER DS3/E3 MODE

If the XRT79L71 has been configured to operate in the High-Speed HDLC Controller over DS3/E3 Mode, then it will have the Functional Architecture as is presented below in **Figure 3**.

FIGURE 3. THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT79L71 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE HIGH-SPEED HDLC CONTROLLER OVER DS3/E3 MODE

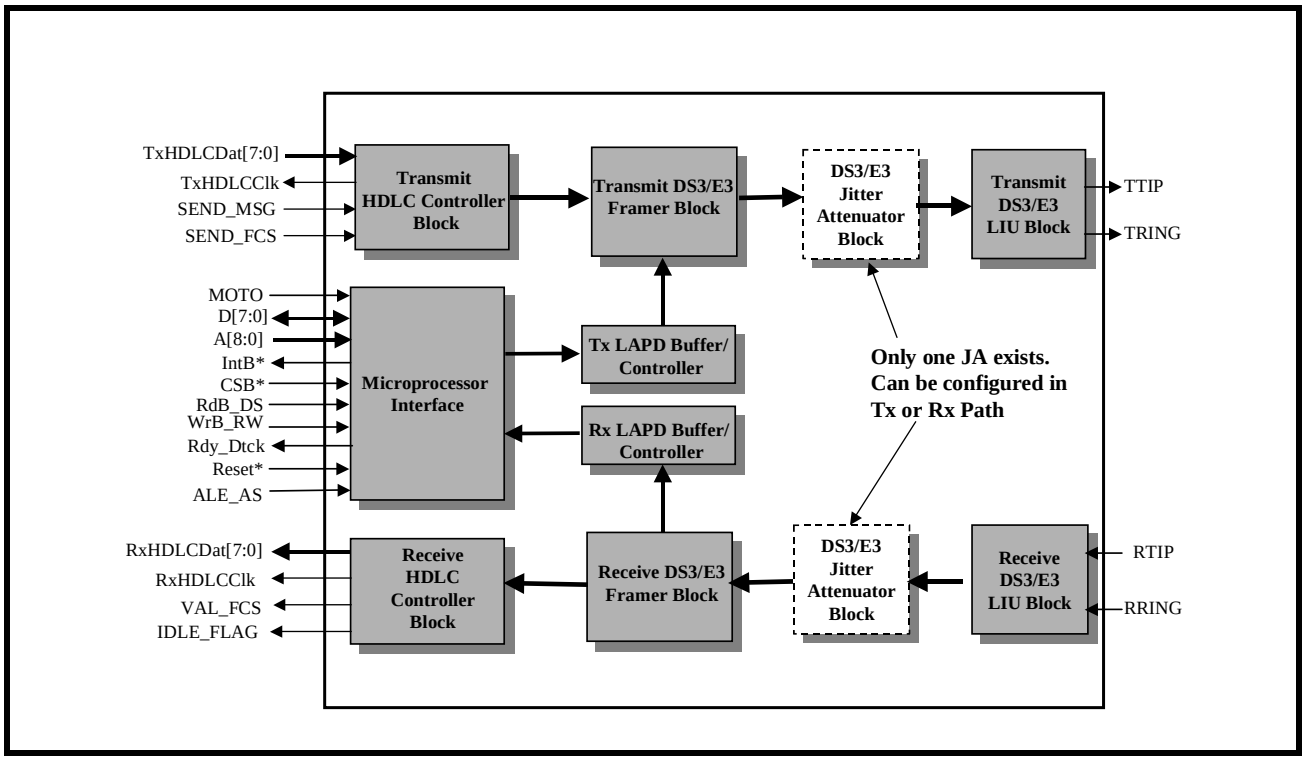

Figure 3 indicates that the XRT79L71 consists of the following functional blocks.

- The Transmit High-Speed HDLC Controller Block
- The Transmit LAPD Controller Block
- The Transmit FEAC Controller Block (DS3 Applications only)
- The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications only)
- The Transmit SSM Controller Block (E3, ITU-T G.832 Applications only)
- The Transmit DS3/E3 Framer Block
- The Transmit DS3/E3 LIU Block
- The Receive DS3/E3 LIU Block
- The Receive DS3/E3 Framer Block
- The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications only)
- The Receive SSM Controller Block (E3, ITU-T G.832 Applications only)
- The Receive FEAC Controller Block (DS3 Applications only)
- The Receive LAPD Controller Block
- The Receive High-Speed HDLC Controller Block

Each of these functional blocks is briefly discussed below. These functional blocks will also be discussed in considerable detail throughout this data sheet.

The Transmit High-Speed HDLC Controller Block

The purpose of the Transmit High-Speed HDLC Controller block is to perform the following tasks.

- To accept user payload data, in a byte-wide manner (via an 8-bit wide Input Data Bus)
- To (while accepting this user payload data, via this byte-wide interface, encapsulate this user data into an HDLC frame)
- To generate and transmit a repeating string of Flag Sequence octets (0x7E), whenever the Transmit High-Speed HDLC Controller block is not accepting nor processing user data
- To route these outbound HDLC frames and Flag Sequence octets to the Transmit DS3/E3 Framer block for further processing.

NOTES:

1. *Whenever the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode, then the role of the Transmit Payload Data Input Interface block will be replaced by the Transmit High-Speed HDLC Controller block.*
2. *The Transmit High Speed HDLC Controller block should NOT be confused with the Transmit LAPD Controller block (which also exists within the XRT79L71).*

The Transmit Overhead Data Input Interface block (not shown in Figure 3)

If the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode, then the Transmit Overhead Data Input Interface block will be disabled.

The Transmit LAPD Controller Block

The purpose of the Transmit LAPD Controller block is to permit the user to transmit LAPD/PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment. The Transmit LAPD Controller block comes with a LAPD Controller/Transmitter (not to be confused with the Transmit High-Speed HDLC Controller) and 90 bytes of on-chip RAM (for storage of outbound PMDL Messages) prior to transmission.

The Transmit FEAC Controller Block (DS3 Applications only)

The purpose of the Transmit FEAC Controller block is to permit the user to transmit FEAC (Far-End Alarm & Control) Messages to the remote terminal equipment.

NOTE: The Transmit FEAC Controller block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.

The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications only)

The Transmit SSM Controller Block (E3, ITU-T G.832 Applications only)

The Transmit DS3/E3 Framer Block

The purpose of the Transmit DS3/E3 Framer block is to accept payload data from the Transmit High-Speed HDLC Controller block, the Transmit LAPD Controller block and the Transmit FEAC Controller block and to construct a DS3/E3 data-stream for transmission to the remote terminal equipment. More specifically, in this particular application, the Transmit DS3/E3 Framer block is responsible for accepting the outbound HDLC frames and Flag Sequences octets from the Transmit High-Speed HDLC Controller block, and inserting this data into the payload bits/bytes within the outbound DS3/E3 fames. Additionally, the Transmit DS3/E3 Framer block can be configured to do all of the following.

- To transmit the AIS Indicator (upon Software Control)
- To automatically transmit the FERF/RDI Indicator (in response to the Receive DS3/E3 Framer block declaring the LOS, LOF/OOF or AIS defect condition)
- To transmit the FERF/RDI indicator (upon Software Control)
- To automatically transmit the FEBE/REI Indicator (in response to the Receive DS3/E3 Framer block detecting Frmaing bit or CP-bit errors - DS3, C-bit Parity Applications)
- To automatically transmit the FEBE/REI Indicator (response to the Receive DS3/E3 Framer block detecting BIP-8 Errors - E3, ITU-T G.832 Applications)
- To transmit the FEBE/REI Indicator (upon Software Control).

The Transmit DS3/E3 LIU Block

The purpose of the Transmit DS3/E3 LIU Block is to accept the outbound DS3/E3 data-stream from the Transmit DS3/E3 Framer block, and to perform all of the following operations on the signal.

- To encode into the B3ZS Line Code (for DS3 Applications) or the HDB3 Line Code (for E3 Applications)
- To convert this outbound DS3 or E3 data-stream into a DS3/E3 line signal and transmit this signal to the remote terminal equipment
- To generate and transmit DS3 pulses that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE
- To generate and transmit E3 pulse that complies with the ITU-T G.703 Pulse Template requirements for E3 applications.

The Receive DS3/E3 LIU Block

The purpose of the Receive DS3/E3 LIU Block is to receive a DS3/E3 line signal from the remote terminal equipment, and to perform the following operations on this incoming line signal.

- To decode this incoming signal from the B3ZS Line Code (for DS3 Applications) or from the HDB3 Line Code (for E3 Applications) into a binary data-stream
- To route this binary data-stream to the Receive DS3/E3 Framer block for further processing.
- To insure that the XRT79L71 meets all of the following Receive requirements.
  - **a.** The Receive Sensitivity requirement for DS3 Applications (e.g., able to receive a DSX-3 type of signal through at least 450 feet of cable loss).
  - **b.** The Receive Sensitivity requirement for E3 Applications (e.g., able to receive an E3 signal over 12dB of cable loss).

c. To comply with the Category I and II Jitter Tolerance Requirements per Bellcore GR-499-CORE (for DS3 Applications)

d. To comply with the Jitter Tolerance Requirements per ITU-T G.823 (for E3 Applications)

e. To comply with the Interference Margin Requirements of 20dB, per ITU-T G.703 (for E3 Applications)

The Receive DS3/E3 Framer Block

The purpose of the Receive DS3/E3 Framer block is to acquire and maintain Frame Synchronization with the incoming DS3/E3 data-stream that it receives from the Receive DS3/E3 LIU Block. As the Receive DS3/E3 Framer block performs this task, it will also do the following.

- It will declare and clear the LOS defect condition
- It will declare and clear the LOF/OOF defect condition
- It will declare and clear the AIS defect condition
- It will declare and clear the FERF/RDI defect condition
- It will detect and flag the occurrences of P-bit, CP-bit and Framing bit errors (DS3 Applications)
- It will detect and flag the occurrence of BIP-8 Errors (E3, ITU-T G.832 Applications)
- It will detect and flag the occurrence of BIP-4 Errors (E3, ITU-T G.751 Applications)
- It will detect and flag the occurrence of FEBE/REI Events
- It will route all PMDL data to the Receive LAPD Controller block for further processing
- It will route all DS3/E3 payload to the Receive High-Speed HDLC Controller block.

The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications only)

The Receive SSM Controller Block (E3, ITU-T G.832 Applications only)

The Receive FEAC Controller Block (DS3 Applications only)

The purpose of the Receive FEAC Controller block is to permit the user to receive FEAC (Far-End Alarm & Control) Messages from the remote terminal equipment.

NOTE: *The Receive FEAC Controller block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

The Receive LAPD Controller Block

The purpose of the Receive LAPD Controller block is to permit the user to receive LAPD/PMDL (Path Maintenance Data Link) Messages from the remote terminal equipment. The Receive LAPD Controller block comes with a Receive LAPD Controller (not to be confused with the Receive High-Speed HDLC Controller block) and 90 bytes of on-chip RAM (for storage of inbound PMDL Messages) after reception.

The Receive High-Speed HDLC Controller Block

The purpose of the Receive High-Speed HDLC Controller block is to receive the payload data (from the incoming DS3/E3 data-stream) and perform the following tasks.

- To identify the boundaries of incoming HDLC frames (within the incoming DS3/E3 data-stream)
- To terminate the Flag Sequence octets within the incoming data-stream
- To (optionally) compute and verify the CRC-16 or CRC-32 values that have been appended to the back-end of these incoming HDLC frames (at the remote terminal equipment) and to flag any occurrences of CRC errors
- To zero-un-stuff the contents within these incoming HDLC frames
- To output this HDLC frame data (in a byte-wide manner) via an 8-bit wide Output Data Bus.

The Receive Overhead Data Output Interface Block (not shown in Figure 3).

If the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode, then the Receive Overhead Data Output Interface block will be disabled.

A MORE DETAILED FUNCTIONAL/ARCHITECTURAL DESCRIPTION FOR THE HIGH-SPEED HDLC CONTROLLER MODE

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The Functional/Architectural Description of the XRT79L71, when configured to operate in the High-Speed HDLC Controller Mode, can be found in Section _, within the document entitled: 79L71_Arch_Descr_HDLC.pdf -Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - High-Speed HDLC Controller Applications.

BRIEF FUNCTIONAL/ARCHITECTURAL DESCRIPTION OF THE XRT79L71 - ATM UNI OVER DS3/E3 MODE

If the XRT79L71 has been configured to operate in the ATM UNI over DS3/E3 Mode, then it will have the Functional Architecture as is presented below in **Figure 4**.

FIGURE 4. THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT79L71 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE ATM UNI OVER DS3/E3 MODE

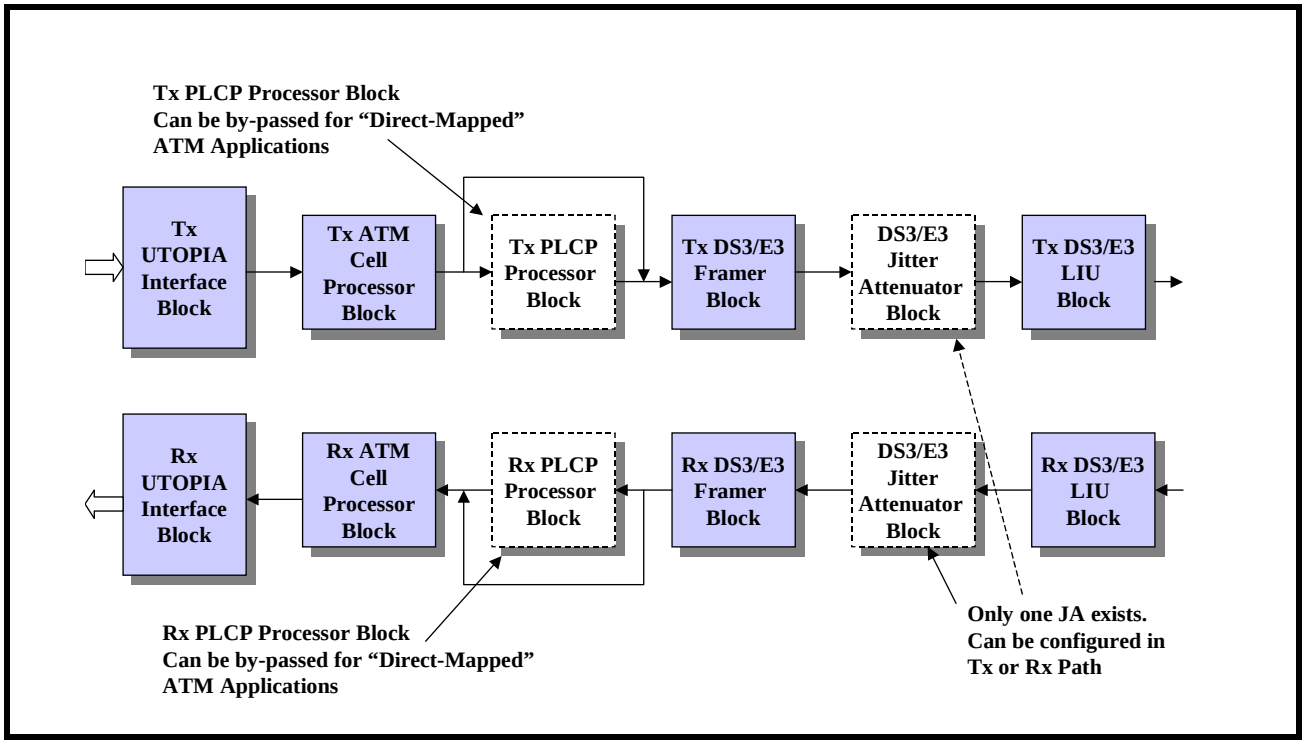

Figure 4 indicates that the XRT79L71 consists of the following functional blocks.

- The Transmit UTOPIA Interface Block
- The Transmit Overhead Data Input Interface Block
- The Transmit ATM Cell Processor Block
- The Transmit FEAC Controller Block (DS3 C-bit Parity Applications Only)
- The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit SSM Controller Block (E3, ITU-T G.832 Appications Only)
- The Transmit LAPD Controller Block

- The Transmit PLCP Processor Block
- The Transmit DS3/E3 Framer Block
- The Transmit DS3/E3 LIU Block
- The Receive DS3/E3 LIU Block
- The Receive DS3/E3 Framer Block
- The Receive PLCP Processor Block
- The Receive LAPD Controller Block
- The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive Trail-Trace Message Controller Block (ITU-T G.832 Applications Only)
- The Receive FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Receive ATM Cell Processor Block
- The Receive Overhead Data Output Interface Block
- The Receive UTOPIA Interface Block

Each of these functional blocks is briefly discussed below. These functional blocks will be discussed in considerable detail throughout this data sheet.

The Transmit UTOPIA Interface Block

The purpose of the Transmit UTOPIA Interface block is to provide a standard UTOPIA Level 1, 2 or 3 interface to the ATM Layer Processor, for writing in the contents of all Valid ATM cells, into the Transmit FIFO (TxFIFO).

The Transmit UTOPIA Interface Block can be configured to operate with either an 8 or 16-bit wide Transmit UTOPIA Data bus.

NOTE: *The Transmit UTOPIA Interface block supports UTOPIA Level 3 from a signaling stand-point. The Transmit UTOPIA Interface Block (within the XRT79L71) still only supports a 16-bit wide (not 32-bit wide) UTOPIA Bus and only operates at clock rates of up to 50MHz (not 100MHz).*

The Transmit Overhead Data Input Interface block (not shown in Figure 4)

The purpose of the Transmit Overhead Data Input Interface block is to permit the user to externally insert his/her own values for overheads bits into the outbound DS3/E3 data-stream.

The Transmit ATM Cell Processor Block

The purpose of the Transmit ATM Cell Processor block is to read out the contents of user cells that have been written into the TxFIFO (via the Transmit UTOPIA Interface block); and perform the following functions.

- Optionally Compute and Verify the HEC byte of each cell written into the TxFIFO
- To optionally discard all incoming ATM cells that contain HEC byte errors
- To optionally compute and insert the HEC byte into the fifth octet position, within each ATM cell that is written into the TxFIFO
- To optionally filter User Cells (that are read out from the TxFIFO) by either discarding these User Cells, or by replicating them and routing the copies of these cells to the Transmit Cell Extraction Buffer
- To insert cells (residing within the Transmit Cell Insertion Buffer) into the Transmit Data Path anytime the TxFIFO is depleted of user cells
- To generate Idle Cells anytime the TxFIFO and the Transmit Cell Insertion Buffer are depleted of User cells
- To route the composite stream of valid and idle cells to either the Transmit PLCP Processor or the Transmit DS3/E3 Framer Block.

The Transmit FEAC Controller Block (DS3, C-bit Parity Applications Only)

The purpose of the Transmit FEAC Controller block is to permit the user to transmit FEAC (Far-End Alarm & Control) Messages to the remote terminal equipment.

NOTE: The Transmit FEAC Controller block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.

The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The Transmit SSM Controller Block (E3, ITU-T G.832 Applications Only)

The Transmit LAPD Controller Block

The purpose of the Transmit LAPD Controller block is to permit the user to transmit LAPD/PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment. The Transmit LAPD Controller block comes with a LAPD Controller/Transmitter (not to be confused with the Transmit High-Speed HDLC Controller) and 90 bytes of on-chip RAM (for storage of outbound PMDL Messages) prior to transmission.

The Transmit PLCP Processor Block (Can be by-passed)

The purpose of the Transmit PLCP Processor block is to perform the following functionsl

- To accept ATM cells from the Transmit ATM Cell Processor Block and to pack 12 of these ATM cells into a PLCP frame
- As the Transmit PLCP Processor block creates these PLCP frames, it will also do the following
  - **a.** Automatically transmit the PLCP RAI (Remote Alarm Indicator) to the remote terminal whenever the corresponding Near-End Receive PLCP Processor block declares the PLCP LOF defect condition.
  - **b.** Automatically transmits the PLCP FEBE (Far-End Block Error) condition to the remote terminal whenever the corresponding near-end Receive PLCP Processor block detects PLCP B1 byte errors within its incoming PLCP data-stream.
- The Transmit PLCP Processor block can be commanded to transmit the PLCP RAI indicator upon Software command
- The Transmit PLCP Processor block can be commanded to transmit the PLCP FEBE indicator upon Software command
- Routes these outbound PLCP frames to the Transmit DS3/E3 Framer block
- Can be by-passed for Direct-Mapped ATM Applications.

The Transmit DS3/E3 Framer Block

The purpose of the Transmit DS3/E3 Framer block is to perform the following functions.

- To accept ATM cell data from the Transmit ATM Cell Processor block and to map this ATM cell data into the payload bits within each outbound DS3 or E3 frame (for Direct Mapped ATM Applications)
- To accept PLCP frames from the Transmit PLCP Processor block and to map these PLCP frames into the payload bits within each outbound DS3 or E3 frames (for PLCP Applications)
- To transmit this resulting framed DS3 or E3 data-stream to the Transmit DS3/E3 LIU block. In this case, the user can also configure the Transmit DS3/E3 Framer block to do the following.
  - **a.** Transmit an AIS pattern (upon software command)
  - **b.** Transmit a DS3 Idle pattern (upon software command)
  - **c.** Automatically transmit the FERF/RDI indicator whenever the Receive DS3/E3 Framer block (within this particular XRT79L71) declares the LOS, LOF/OOF or AIS defect condition.
  - **d.** Automatically transmits the FEBE/REI indicator whenever the corresponding near-end Receive DS3/E3 Framer block detects CP-bit or Framing bit errors within the incoming DS3 data-stream (for DS3 C-bit Parity Applications).
  - **e.** Automatically transmit the FEBE/REI indicator whenever the Receive DS3/E3 Framer block detects BIP-8 errors within the incoming E3 data-stream (for E3, ITU-T G.832 Applications).

f. To transmit FEAC (Far-End Alarm & Control) messages to the remote terminal equipment (DS3, C-bit Parity Applications only).

g. To transmit LAPD/PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment.

h. To transmit Trail-Trace Messages to the remote terminal equipment (E3, ITU-T G.832 Applications only).

The Transmit DS3/E3 LIU Block

The purpose of the Transmit DS3/E3 LIU Block is to accept the outbound DS3/E3 data-stream from the Transmit DS3/E3 Framer block and to perform the following functions on this data.

- Encode this data into the B3ZS/HDB3 Line code
- Convert this data-stream into a proper DS3 or E3 line code that complies with the following requirements.
  - **a.** The Isolated Pulse Template requirements per Bellcore GR-499-CORE (for DS3 Applications).
  - **b.** The ITU-T G.703 Pulse Template requirements (for E3 Applications).

The Receive DS3/E3 LIU Block

The purpose of the Receive DS3/E3 LIU Block is to receive an inbound DS3/E3 line signal from the remote terminal equipment, and to perform the following functions on this data.

- To decode this data from the B3ZS/HDB3 Line code into a binary data-stream (prior to routing this data to the Receive DS3/E3 Framer block
- To detect and flag the occurrence of LCVs (Line Code Violations) and EXZs (Excessive Zeros)
- To insure that the XRT79L71 meets all of the following Receive requirements
  - **a.** The Receive Sensitivity requirements for DS3 Applications (e.g., able to receive a DSX-3 type of signal through at least 450 feet of cable loss).
  - **b.** The Receive Sensitivity requirements for E3 Applications (e.g., able to receive an E3 signal over 12dB of cable loss).
  - **c.** To comply with the Category I and II Jitter Tolerance Requirements per Bellcore GR-499-CORE (for DS3 Applications)
  - **d.** To comply with the Jitter Tolerance Requirements per ITU-T G.823 (for E3 Applications)
  - **e.** To comply with the Interference Margin Requirements of 20dB, per ITU-T G.703 (for E3 Applications)

The Receive DS3/E3 Framer Block

The purpose of the Receive DS3/E3 Framer block is to perform the following functions.

- To receive either a DS3 or E3 data-stream from the Receive DS3/E3 LIU Block. As the Receive DS3/E3 Framer block receives this DS3/E3 data-stream, it will do the following.
  - **a.** Compute and verify P and CP-bits (for DS3 Applications)
  - **b.** Compute and verify BIP-4 bits (for E3, ITU-T G.751 Applications)
  - **c.** Compute and verify BIP-8 bits (for E3, ITU-T G.832 Applications)
  - **d.** To declare and clear the LOS, OOF, LOF, AIS and FERF/RDI defect conditions
  - **e.** To declare and clear the DS3 Idle condition (DS3 Applications)
  - **f.** To detect FEBE/REI events.

The Receive PLCP Processor Block (Can be by-passed)

The purpose of the Receive PLCP Processor block is to perform the followoing functions.

- To receive the PLCP framd data-stream from the Receive DS3/E3 Framer block, and to acquire and maintain PLCP frame synchronization with this data
- To declare and clear the PLCP OOF, PLCP LOF and PLCP RAI defect conditions

- To detect and flag B1 byte errors
- To detect and flag PLCP FEBE/REI events
- To extract out the payload data from incoming PLCP frame (which consists of ATM cells) and to route this data to the Receive ATM Cell Processor block for further processing
- Can be by-passed for Direct-Mapped ATM Applications

The Receive LAPD Controller Block

The purpose of the Receive LAPD Controller block is to permit the user to receive LAPD/PMDL (Path Maintenance Data Link) Messages from the remote terminal equipment. The Receive LAPD Controller block comes with a Receive LAPD Controller (not to be confused with the Receive High-Speed HDLC Controller block) and 90 bytes of on-chip RAM (for storage of inbound PMDL Messages) after reception.

The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)

The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The Receive FEAC Controller Block (DS3, C-bit Parity Applications Only)

The purpose of the Receive FEAC Controller block is to permit the user to receive FEAC (Far-End Alarm & Control) Messages from the remote terminal equipment.

NOTE: *The Receive FEAC Controller block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

The Receive ATM Cell Processor Block

The purpose of the Receive ATM Cell Processor block is to extract out the data (being carried by the incoming DS3/E3 frame or PLCP frame data-stream) and to perform the following operations on it.

- Cell Delineation
- HEC Byte Verification
- User and Idle Cell Filtering
- To receive cells with user-specified header bytes and to load them into the Receive Cell Extraction Memory Buffer (where they can be read out and accessed via the Microprocessor Interface)
- To read out a user-specified ATM cell (which is residing in the Receive Cell Insertion Buffer) and to insert this cell into the Receive ATM Cell traffic
- To route all filtered cells to the RxFIFO (where it will be made available to the ATM Layer Processor via the Receive UTOPIA Interface block)

The Receive Overhead Data Output Interface block

The purpose of the Receive Overhead Data Output Interface block is to permit the user to extract out the overhead bits (within the incoming DS3/E3 data-stream) and to route this data to some off-chip System-Side Terminal Equipment circuitry.

The Receive UTOPIA Interface block

The purpose of the Receive UTOPIA Interface block is to provide a standard UTOPIA Level 1, 2 or 3 interface to the ATM Layer Processor, for reading out the contents of all ATM cells that are written into the RxFIFO.

The Receive UTOPIA Interface block can be configured to operate with either an 8 or 16-bit wide Receive UTOPIA Data bus.

NOTE: *The Receive UTOPIA Interface block supports UTOPIA Level 3 from a signaling stand-point. The Receive UTOPIA Interface block (within the XRT79L71) still only supports a 16-bit wide (not 32-bit wide) UTOPIA Bus and only operates up to 50MHz (not 100MHz).*

A MORE DETAILED FUNCTIONAL/ARCHITECTURAL DESCRIPTION FOR THE ATM UNI MODE

The Functional/Architectural Description of the XRT79L71, when configured to operate in the ATM UNI Mode, can be found in Section _, within the document entitled: 79L71_Arch_Descr_ATM.pdf - Architectural/Functional Description of the XRT79L71 1-Channel DS3/E3 ATM UNI/PPP/Clear-Channel Framer with LIU IC - ATM UNI Mode Applications.

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FUNCTIONAL ARCHITECTURE/DESCRIPTION OF THE XRT79L71 - PPP OVER DS3/E3 MODE

If the XRT79L71 has been configured to operate in the PPP over DS3/E3 Mode, then it will have the Functional Architecture as is presented below in **Figure 5**.

FIGURE 5. THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT79L71 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE PPP OVER DS3/E3 MODE

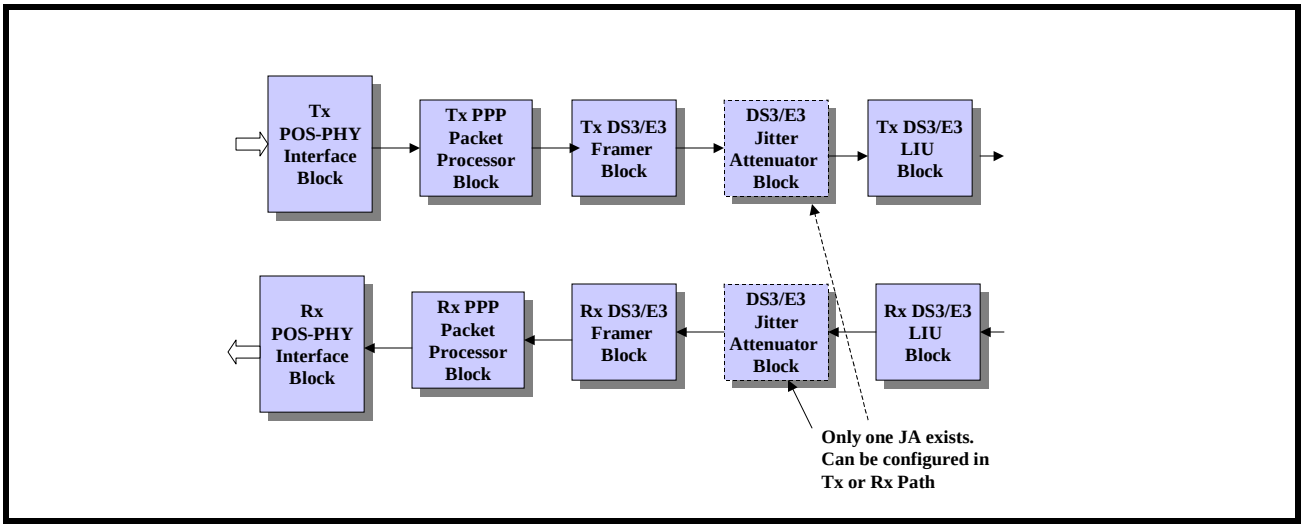

Figure 5 indicates that the XRT79L71 consists of the following functional blocks.

- The Transmit POS-PHY Interface block
- The Transmit Overhead Data Input Interface block
- The Transmit PPP Packet Processor Block
- The Transmit FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Transmit LAPD Controller Block
- The Transmit DS3/E3 Framer Block
- The Transmit DS3/E3 LIU Block
- he Receive DS3/E3 LIU Block
- The Receive DS3/E3 Framer Block
- The Receive LAPD Controller Block
- The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)
- The Receive FEAC Controller Block (DS3, C-bit Parity Applications Only)
- The Receive PPP Packet Processor Block

- The Receive Overhead Data Output Interface Block
- The Receive POS-PHY Interface Block

Each of these functional blocks is briefly discussed below. These functional blocks will be discussed in considerable detail throughout this data sheet.

The Transmit POS-PHY Interface Block

The purpose of the Transmit POS-PHY Interface block is to provide a standard Saturn POS-PHY™ Level 2 or 3 compliant interface to the Link Layer Processor, for writing in the contents of all outbound PPP packets, into the Transmit FIFO (TxFIFO).

The Transmit POS-PHY Interface block can be configured to operate with either an 8 or 16-bit wide Transmit POS-PHY Data Bus.

NOTES:

1. *The Transmit POS-PHY Interface Block supports POS-PHY Level 3 from a signaling stand-point. The Transmit POS-PHY Interface block (within the XRT79L71) still only supports a 16-bit wide (not 32-bit wide) POS-PHY Data Bus and only operates up to 50MHz (not 104MHz).*
2. *The Transmit POS-PHY Interface block can be configured to support either Out-of-Band Addressing or In-Band Addressing for Device Selection to WRITE operations. However, since the XRT79L71 is a single-channel device, we strongly recommend that the user only use Out-of-Band Addressing for Device Selection whenever it is designed into a Multi-PHY system in which multiple PHY Layer devices are sharing the same POS-PHY Bus.*

The Transmit Overhead Data Input Interface Block

The purpose of the Transmit Overhead Data Input Interface block is to permit the user to externally insert his/her own value for overhead bits into the outbound DS3/E3 data-stream.

The Transmit PPP Packet Processor Block

The purpose of the Transmit PPP Packet Processor block is to read out the contents of the PPP Packets that have been written into the TxFIFO (via the Transmit POS-PHY Interface block) and perform the following functions.

- Compute and verify the Transmit POS-PHY Interface Parity value for each byte or (16-bit) word of each incoming PPP Packet
- To Parse through the contents of each outbound packet for any occurrence of the value 0x7E and 0x7D and to character-stuff (or replace) these values with strings of values 0x7D5E and 0x7D5D, respectively
- To compute and append either a CRC-16 or CRC-32 value to the back-end of each outbound PPP Packet
- To repeatedly generate and transmit the Flag Sequence Octet, anytime the Transmit PPP Packet Processor block is NOT processing any PPP Packet data from the TxFIFO (e.g., whenever the TxFIFO is depleted)
- To route this composite stream of PPP packet and Flag Sequence octets to the Transmit DS3/E3 Framer block for further processing.

The Transmit FEAC Controller Block (DS3, C-bit Parity Applications Only)

The purpose of the Transmit FEAC Controller block is to permit the user to transmit FEAC (Far-End Alarm & Control) Messages to the remote terminal equipment.

NOTE: *The Transmit FEAC Controller block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

The Transmit Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The Transmit SSM Controller Block (E3, ITU-T G.832 Applications Only)

The Transmit LAPD Controller Block

The purpose of the Transmit LAPD Controller block is to permit the user to transmit LAPD/PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment. The Transmit LAPD Controller block

comes with a LAPD Controller/Transmitter (not to be confused with the Transmit High-Speed HDLC Controller) and 90 bytes of on-chip RAM (for storage of outbound PMDL Messages) prior to transmission.

The Transmit DS3/E3 Framer Block

The purpose of the Transmit DS3/E3 Framer block is to perform the following functions.

- To accept PPP packet and Flag Sequence octets from the Transmit PPP Packet Processor block and to map all of this data into the payload bits within each outbound DS3 or E3 frame.
- To transmit the resulting framed DS3 or E3 data-stream to the Transmit DS3/E3 LIU Block. In this case, the user can also configure the Transmit DS3/E3 Framer block to do the following.
  - **a.** Transmit an AIS Pattern (upon software command)
  - **b.** Transmit a DS3 Idle Pattern (upon software command)
  - **c.** Automatically transmit the FERF/RDI whenever the Receive DS3/E3 Framer block (within the very same XRT79L71) declares the LOS, LOF/OOF or AIS defect conditions.
  - **d.** Automatically transmit the FEBE/REI indicator whenever the Receive DS3/E3 Framer block detects CP-bit or Framing bit errors within the incoming DS3 data-stream (for DS3, C-bit Parity Applications only)
  - **e.** Automatically transmit the FEBE/REI indicator whenever the Receive DS3/E3 Framer block detects BIP-8 errors within the incoming E3 data-stream (for E3, ITU-T G.832 Applications).

The Transmit DS3/E3 LIU Block

The purpose of the Transmit DS3/E3 LIU Block is to accept the outbound DS3/E3 data-stream from the Transmit DS3/E3 Framer block and to perform the following functions on this data.

- Encode this data into the B3ZS Line Code (for DS3 Applications) or the HDB3 Line Code (for E3 Applications)
- To convert this outbound DS3 or E3 data-stream into a DS3/E3 line signal and transmit this signal to the remote terminal equipment
- To generate and transmit DS3 pulses that comply with the Isolated Pulse Template requirements per Bellcore GR-499-CORE
- To generate and transmit E3 pulses that comply with the ITU-T G.703 Pulse Template requirements for E3 Applications.

The Receive DS3/E3 LIU Block

The purpose of the Receive DS3/E3 LIU Block is to receive a DS3/E3 line signal from the remote terminal equipment, and perform the following operations on this incoming line signal.

- To decode this incoming signal from the B3ZS Line Code (for DS3 Applications) or from the HDB3 Line Code (for E3 Applications) into a binary data-stream
- To route this binary data-stream to the Receive DS3/E3 Framer block for further processing
- To insure that the XRT79L71 meets all of the following Receive requirements.
  - **a.** The Receive Sensitivity requirements for DS3 Applications (e.g., able to receive a DSX-3 type of signal through at least 450 feet of cable loss)
  - **b.** The Receive Sensitivity requirements for E3 Applications (e.g., able to receive a E3 siganl over 12dB of cable loss)
  - **c.** To comply with the Category I and II Jitter Tolerance Requirements per Bellcore GR-499-CorE (for DS3 Applications)
  - **d.** To comply with the Jitter Tolerance Requirements per ITU-T G.823 (for E3 Applications)
  - **e.** To comply with the Interference Margin Requirements of 20dB, per ITU-T G.703 (for E3 Applications).

The Receive DS3/E3 Framer Block

The purpose of the Receive DS3/E3 Framer block is to acquire and maintain Frame Synchronization with the incoming DS3/E3 data-stream that it receives from the Receive DS3/E3 LIU Block. As the Receive DS3/E3 Framer block performs this task, it will also do the following.

- It will declare and clear the LOS defect condition
- It will declare and clear the LOF/OOF defect condition
- It will declare and clear the AIS defect condition
- It will declare and clear the FERF/RDI defect condition
- It will detect and flag the occurrence of P-bit, CP-bit and Framing bit errors (DS3 Applications)
- It will detect and flag the occurrence of BIP-8 Errors (E3, ITU-T G.832 Applications)
- It will detect and flag the occurrence of BIP-4 Errors (E3, ITU-T G.751 Applications)
- It will detect and flag the occurrences of FEBE/REI Events
- It will detect and flag any occurrences of LCVs (Line Code Violations) and EXZs (Excessive Zero) events within the incoming DS3/E3 line signal
- It will extract the payload bits (out from each incoming DS3 or E3 frame) and it will route this data to the Receive PPP Packet Processor block for further processing.

The Receive LAPD Controller Block

The purpose of the Receive LAPD Controller block is to permit the user to receive LAPD/PMDL (Path Maintenance Data Link) Messages from the remote terminal equipment. The Receive LAPD Controller block comes with a Receive LAPD Controller (not to be confused with the Receive High-Speed HDLC Controller block) and 90 bytes of on-chip RAM (for storage of inbound PMDL Messages) after reception.

The Receive SSM Controller Block (E3, ITU-T G.832 Applications Only)

The Receive Trail-Trace Message Controller Block (E3, ITU-T G.832 Applications Only)

The Receive FEAC Controller Block (DS3, C-bit Parity Applications Only)

The purpose of the Receive FEAC Controller block is to permit the user to receive FEAC (Far-End Alarm & Control) Messages from the remote terminal equipment.

NOTE: *The Receive FEAC Controller block is only active if the XRT79L71 is configured to operate in the DS3, C-bit Parity Framing format.*

The Receive PPP Packet Processor Block

The purpose of the Receive PPP Packet Processor block is to extract out the payload data (being carried by the incoming DS3/E3 data-stream) and to perform the following operations on it.

- Identification/Location of boundaries of incoming PPP packets
- Computation and Verification of either the CRC-16 or CRC-32 values within the incoming PPP Packets
- To Parse through the contents of each inbound packet for any occurrences of the values 0x7D5E and 0x7D5D and to character de-stuff (or replace) these values with strings of 0x7E and 0x7D, respectively
- To terminate any incoming Flag Sequence octets
- To flag the occurrence of any incoming RUNT packets
- To flag the occurrence of any incoming Aborted Packets

The Receive Overhead Data Output Interface Block

The purpose of the Receive Overhead Data Output Interface block is to permit the user to extract out the overhead bits (within the incoming DS3/E3 data-stream) and to route this data to some off-chip System-Side Terminal Equipment circuitry.

The Receive POS-PHY Interface Block

The purpose of the Receive POS-PHY Interface block is to provide a standard Saturn POS-PHY™ Level 2 or 3 compliant interface to the Link Layer Processor, for reading in the contents of all inbound PPP Packets, from the Receive FIFO (RxFIFO).

The Receive POS-PHY Interface block can be configured to operate with either an 8 or 16-bit wide Receive POS-PHY Data Bus.

NOTES:

1. *The Receive POS-PHY Interface Block supports POS-PHY Level 3 from a signaling stand-point. The Receive POS-PHY Interface block (within the XRT79L71) still only supports a 16-bit wide (not 32-bit wide) POS-PHY Data Bus and only operates up to 50MHz (not 104MHz).*
2. *The Receive POS-PHY Interface Block can be configured to support either Out-of-Band Addressing or In-Band Addressing for Device Selection to READ. However, since the XRT79L71 is a single-channel device, we strongly recommend that the user only use Out-of-Band Addressing for Device Selection whenever it is designed into a Multi-PHY systemin which multiple PHY Layer devices are sharing the same POS-PHY Bus.*

A MORE DETAILED FUNCTIONAL/ARCHITECTURAL DESCRIPTION FOR THE PPP MODE

The Functional/Architectural Description of the XRT79L71, when configured to operate in the PPP Mode can be found in Section _, within this document.

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4.0 INTERRUPT STRUCTURE WITHIN THE XRT79L71

The XRT79L71 is equipped with a sophisticated Interrupt Servicing Structure. This Interrupt Structure includes an Interrupt Request output pin (INT*), numerous Interrupt Enable Registers and numerous Interrupt Status Registers. The Interrupt Servicing Structure, within the XRT79L71 IC contains two levels of hierarchy. The top level is at the Functional Block level (e.g., the Receive ATM Cell Processor Block, the Receive PPP Packet Processor Block, the Receive DS3/E3 Framer block, etc). The lower hierarchical level is at the individual or source level. Each hierarchical level consists of a complete set of Interrupt Status Registers/bits and Interrupt Enable Registers/bits, as will be discussed below.

Most of the functional blocks within the XRT79L71 are capable of generating Interrupt Requests to the μC/µP. The XRT79L71 Interrupt Structure has been carefully designed to allow the user to quickly determine the exact source of the interrupt (with a minimum number of read operations, and, in-turn, minimal latency) which will aid the μC/µP in determine the appropriate interrupt service routine to call up in order to either eliminate, or properly respond to the condition(s) causing the interrupt.

Table 3 lists all of the possible conditions that can generate interrupts, within each functional block of the XRT79L71.

TABLE 3: LIST OF ALL OF THE POSSIBLE CONDITIONS THAT CAN GENERATE INTERRUPTS WITHIN THE XRT79L71

FUNCTIONAL BLOCK	INTERRUPT CONDITION
DS3/E3 Framer Block (Consists of both the Transmit DS3/E3 Framer Block, the Transmit PLCP Processor Block, the Receive DS3/E3 Framer Block and the Receive PLCP Processor Block)	**Transmit DS3/E3 Framer Block Interrupts** • Completion of Transmission of FEAC Message (DS3,C-bit Parity Only) • Completion of Transmission of LAPD/PMDL Message **Transmit PLCP Processor Block Interrupts** • None **Receive DS3/E3 Framer Block Interrupts** • Change of LOS (Loss of Signal) Defect Condition • Change of OOF (Out of Frame) Defect Condition • Change of AIS Defect Condition • Change in Trail-Trace Buffer Message (E3, ITU-T G.832 only) • Change of FERF/RDI (Yellow Alarm) Defect Condition • Detection of P-Bit Errors (DS3 Applications only) • Detection of CP-Bit Errors (DS3, C-bit Parity Applications only)· Detection of BIP-4 Error (E3, ITU-T G.751 only) • Detection of BIP-8 Error (E3, ITU-T G.832 only)· Detection of FEBE (Far-End Block Error) Event • Validation of FEAC Message (DS3, C-bit Parity Only)· • Removal of FEAC Message (DS3, C-bit Parity Only) • Receipt of New LAPD/PMDL Message • One Second Interrupt **Receive PLCP Processor Block Interrupts** • Change of PLCP OOF Defect Condition • Change of PLCP LOF Defect Condition • Change of PLCP RAI Defect Condition
DS3/E3 LIU Block	• Change of FL (Jitter Attenuator FIFO Limit Alarm) Condition • Change of LOL (Receive Loss of Lock) Condition • Change of LOS (Loss of Signal) Condition • Change of DMO (Transmit Drive Monitor Output) Condition

TABLE 3: LIST OF ALL OF THE POSSIBLE CONDITIONS THAT CAN GENERATE INTERRUPTS WITHIN THE XRT79L71

FUNCTIONAL BLOCK	INTERRUPT CONDITION
Receive ATM Cell/PPP Packet Processor Block	**Receive ATM Cell Processor Block Interrupts** • Receive Cell Extraction Event • Receive Cell Insertion Event • Receive Cell Insertion Memory Overflow Condition • Receive Cell Extraction Memory Overflow Condition • RxFIFO Overflow • Detection of Correctable HEC Byte Error • Detection of Uncorrectable HEC Byte Error • Declaration of the LCD (Loss of Cell Delineation) Defect Condition • Clearances of the LCD Defect Condition **Receive PPP Packet Processor Block Interrupts** • Detection of Receive FIFO Overflow Condition • Detection of FCS (Frame Check Sequence) Error· • Detection of ABORT Sequence • Detection of RUNT Packet
Transmit ATM Cell/PPP Packet Processor Block	**Transmit ATM Cell Processor Block Interrupts** • Transmit Cell Extraction Event • Transmit Cell Insertion Event· • Transmit Cell Insertion Memory Overflow Condition • Transmit Cell Extraction Memory Overflow Condition • TxFIFO Overflow • Detection of HEC Byte Error • Detection of Transmit UTOPIA Parity Error • Transmit PPP Processor Block Interrupts • Detection of Transmit FIFO Overflow Condition· • Detection of Transmit POS-PHY Interface Parity Error

The XRT79L71 ATM UNI/PPP/Clear-Channel DS3/E3 Framer device comes equipped with the following registers to support the servicing of this wide array of potential interrupt request sources. Table 4 lists these registers and their corresponding addresses, within the XRT79L71.

TABLE 4: A LISTING OF THE XRT79L71 ATM UNI/PPP/CLEAR-CHANNEL DS3/E3 FRAMER DEVICE INTERRUPT BLOCK REGISTERS

REGISTER	ADDRESS LOCATION
Operation Control Register	0x0101
Operation Interrupt Status Register - Byte 1	0x0112
Operation Interrupt Status Register - Byte 0	0x0113
Operation Interrupt Enable Register - Byte 1	0x0116
Operation Interrupt Enable Register - Byte 0	0x0117
Framer Block Interrupt Enable Register	0x1104

TABLE 4: A LISTING OF THE XRT79L71 ATM UNI/PPP/CLEAR-CHANNEL DS3/E3 FRAMER DEVICE INTERRUPT BLOCK REGISTERS

REGISTER	ADDRESS LOCATION
Framer Block Interrupt Status Register	0x1105
RxDS3 Interrupt Enable RegisterRxE3 Interrupt Enable Register # 1 - ITU-T G.751RxE3 Interrupt Enable Register # 1 - ITU-T G.832	0x1112
RxDS3 Interrupt Status RegisterRxE3 Interrupt Enable Register # 2 - ITU-T G.751RxE3 Interrupt Enable Register # 2 - ITU-T G.832	0x1113
RxE3 Interrupt Status Register # 1 - ITU-T G.751RxE3 Interrupt Status Register # 1 - ITU-T G.832	0x1114
RxE3 Interrupt Status Register # 2 - ITU-T G.751RxE3 Interrupt Status Register # 2 - ITU-T G.832	0x1115
RxDS3 FEAC Interrupt Enable/Status Register	0x1117
RxDS3/E3 LAPD Control Register	0x1118
TxDS3 FEAC Configuration & Status Register	0x1131
TxDS3/E3 LAPD Status/Interrupt Register	0x1134
RxPLCP Interrupt Enable Register	0x1191
RxPLCP Interrupt Status Register	0x1192
LIU Interrupt Enable Register	0x1301
LIU Interrupt Status Register	0x1302
Receive ATM Cell Processor Block - Receive ATM Interrupt Status Register - Byte 1	0x170A
Receive ATM Cell Processor Block - Receive ATM Interrupt Status Register - Byte 0	0x170B
Receive ATM Cell Processor Block - Receive ATM Interrupt Enable Register - Byte 1	0x170E
Receive ATM Cell Processor Block - Receive ATM Interrupt Enable Register - Byte 0	0x170F
Transmit ATM Cell Processor Block - Transmit ATM Interrupt Status Register	0x1F0B
Transmit ATM Cell Processor Block - Transmit ATM Interrupt Enable Register	0x1F0F

General Flow of XRT79L71 ATM UNI/PPP/Clear-Channel DS3/E3 Framer Device Interrupt Servicing

Whenever any of the conditions, presented in **Table 4** occur (if their Interrupt is enabled), then the XRT79L71 will generate an interrupt request to the µC/µP by asserting the active-low interrupt request output pin, INT*. Shortly after the µC/µP has detected the activated INT* signal, it will enter into the appropriate user-supplied interrupt service routine. The first task, for the µC/µP, while running this interrupt service routine, may be to isolate the source of the interrupt request down to the device level (e.g., the XRT79L71 ATM UNI/PPP/Clear-Channel DS3/E3 Framer device), if multiple peripheral devices exist in the user's system.

However, once the interrupting peripheral device has been identified and determined to be the XRT79L71, the next task for the µC/µP is to identify the functional block (within the XRT79L71) that requested the interrupt. Finally, the µC/µP will need to proceed further and identify the exact condition(s) causing the interrupt to be generated by the XRT79L71.

The procedure for servicing the XRT79L71 Interrupts is best achieved by executing the following steps.

STEP 1 - Determine the Functional Block(s) requesting the Interrupt

If the interrupting device turns out to be the XRT79L71 ATM UNI/PPP/Clear-Channel DS3/E3 Framer IC, then the μC/µP must determine which functional block requested the interrupt. Hence, upon reaching this state, one of the very first things that the μC/µP must do within the user supplied XRT79L71 Interrupt Service Routine, is to perform a read of both of the following registers.

- Operation Interrupt Status Register - Byte 1 (Address = 0x0112)
- Operation Interrupt Status Register - Byte 0 (Address = 0x0113)

The bit-format of each of these registers is presented below.

Operation Interrupt Status Register - Byte 1 (Address = 0x0112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS3/E3 LIU/ JA Block Interrupt Status	DS3/E3 Framer Block Interrupt Status	Unused	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Operation Interrupt Status Register - Byte 0 (Address = 0x0113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive ATM Cell/ PPP Processor Block Interrupt Status	Unused			Transmit ATM Cell/ PPP Processor Block Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Each of the Operation Block Interrupt Status Register presents the interrupt-request status of each of the functional blocks within the chip. The purpose of these two registers is to help the µC/µP identify which functional block(s) has requested the interrupt. Whichever bit(s) are asserted, in this register, identifies which block(s) has requested the interrupt. Whichever bit(s) are asserted, in this register, identifies which block(s) have experienced an interrupt-generating condition as presented in **Table 5**. Once the µC/µP has read this register, it can determine which branch within the interrupt service routine that it must follow in order to properly service this interrupt.

The XRT79L71 ATM UNI/PPP/Clear-Channel DS3/E3 Framer IC further supports the Operational Block hierarchy by providing the Operation Block Interrupt Enable Register - Bytes 1 and 0. The bit format of these two registers are identical to that for the Operation Block Interrupt Status Registers - Byte 1 and 0, and are presented below for the sake of completeness.

Operation Interrupt Enable Register - Byte 1 (Address = 0x0116)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS3/E3 LIU/ JA Block Interrupt Enable	DS3/E3 Framer Block Interrupt Enable	Unused	
R/O	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

Operation Interrupt Enable Register - Byte 0 (Address = 0x0117)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive ATM Cell/ PPP Processor BlockInterrupt Enable	Unused			Transmit ATM Cell/ PPP Processor Block Interrupt Enable
R/O	R/O	R/O	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

These Operation Block Interrupt Enable registers permit the user to individually enable or disable the interrupt requesting capability of the functional blocks within the XRT79L71. If a particular bit-field, within this register contains the value "0", then the corresponding functional block has been disabled for generating any interrupt requests. Conversely, if that bit-field contains the value "1", then the corresponding functional block has been enabled for interrupt generation (e.g., those potential interrupts, within the enabled functional block that are enabled at the source level are now enabled). The user should be aware of the fact that each functional block, within the XRT79L71 contains multiple potential interrupt sources. Each of these lower lever interrupt sources contain their own set of interrupt enable bits and interrupt status bits, existing in various on-chip registers.

STEP 2 - Interrupt Service Routing Branching: After reading the Operation Block Interrupt Status Registers

The contents of the Operation Block Interrupt Status Registers permit the user to identify which of the seven (7) functional blocks (within the XRT79L71 IC) have requested interrupt service. The µC/µP should use this information in order to determine where, within the Interrupt Service Routine, program control should branch to. The following table can be viewed as an interrupt service routine guide. It lists each of the Functional Blocks that contain bit-fields in the Operation Block Interrupt Status and Enable registers. Additionally, this table also presents a list and addresses of the corresponding on-chip Registers that the Interrupt Service Routine should branch to and read, based upon the Interrupting Functional Block.

TABLE 5: INTERRUPT SERVICE ROUTINE GUIDE FOR THE XRT79L71

INTERRUPT FUNCTIONAL BLOCK	THE NEXT REGISTER TO BE READ DURING THE INTERRUPT SERVICE ROUTINE	ADDRESS LOCATION
DS3/E3 Framer Block	Framer Block Interrupt Status Register	0x1105
DS3/E3 LIU/JA Block	LIU Interrupt Status Register	0x1302

TABLE 5: INTERRUPT SERVICE ROUTINE GUIDE FOR THE XRT79L71

INTERRUPT FUNCTIONAL BLOCK	THE NEXT REGISTER TO BE READ DURING THE INTERRUPT SERVICE ROUTINE	ADDRESS LOCATION
Receive ATM Cell/PPP Packet Processor Block	Receive ATM Cell Processor Block - Receive ATM Interrupt Status Register - Byte 1	0x170A
	Receive ATM Cell Processor Block - Receive ATM Interrupt Status Register - Byte 0	0x170B
Transmit ATM Cell/PPP Packet Processor Block	Transmit ATM Cell Processor Block - Transmit ATM Interrupt Status Register - Byte 1	0x1F0B

NOTE: *Registers associated within each functional block are specified in ascending order (based upon the on-chip Address Location). No other inferences should be made regarding the order in which these registers are presented in this table.*

Once the µC/µP has read out the contents of the appropriate registers (as listed above in **Table 5**), then there may (or may not) be additional interrupt status registers to read as described below.

Interrupt Servicing for the DS3/E3 Framer Block

If, upon reading out the contents of the Operation Interrupt Status Registers that the interrupting block is the DS3/E3 Framer block then the user should execute a READ operation to the Framer Block Interrupt Status Register. The bit-format for the Framer Block Interrupt Status Register is as presented below.

Framer Block Interrupt Status Register (Address = 0x1105)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive DS3/E3 Framer Block Interrupt Status	Receive PLCP Processor Block Interrupt Status	Unused				Transmit DS3/E3 Framer Block Interrupt Status	One Second Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
X	X	0	0	0	0	X	X

Depending upon which of these bit-fields are set to "1", the µC/µP (while executing the Interrupt Service Routine) will need to branch to reading out the appropriate register as depicted below in **Table 6**.

TABLE 6: INTERRUPT SERVICE ROUTINE GUIDE FOR THE DS3/E3 FRAMER BLOCK

BIT NUMBER ASSERTED IN REGISTER	BIT-FIELD NAME	NEXT REGISTER TO READ WITHIN INTERRUPT SERVICE ROUTINE	ADDRESS LOCATION OF NEXT REGISTER
7	Receive DS3/E3 Framer Block Interrupt Status	RxDS3 Interrupt Status Register	0x1113
		RxE3 Interrupt Status Register # 1	0x1114
		RxE3 Interrupt Status Register # 2	0x1115
		RxDS3 FEAC Interrupt Enable/Status Register	0x1117
		RxDS3/E3 LAPD Control Register	0x1118
6	Receive PLCP Processor Block Interrupt Status	RxPLCP Interrupt Status Register	0x1192

TABLE 6: INTERRUPT SERVICE ROUTINE GUIDE FOR THE DS3/E3 FRAMER BLOCK

BIT NUMBER ASSERTED IN REGISTER	BIT-FIELD NAME	NEXT REGISTER TO READ WITHIN INTERRUPT SERVICE ROUTINE	ADDRESS LOCATION OF NEXT REGISTER
1	Transmit DS3/E3 Framer Block Interrupt Status	TxDS3 FEAC Configuration & Status Register	0x1131
		TxDS3/E3 LAPD Status/Interrupt Register	0x1134
0	One Second Interrupt Status	NONE - Cause of Interrupt was One Second Interrupt	****

A more detailed description of each of these registers will be presented in the corresponding sections describing the Receive DS3/E3 Framer, Transmit DS3/E3 Framer or Receive PLCP Processor Blocks.

5.0 REGISTER MAP/DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC (SEE 79L71-REGISTER/MAP-DESC.PDF)

6.0 PIN DESCRIPTIONS (SEE 79L71-HARDWARE-MANUAL.PDF)

7.0 ELECTRICAL CHARACTERISTICS (SEE 79L71-HARDWARE-MANUAL.PDF)

8.0 MICROPROCESSOR INTERFACE (SEE 79L71-HARDWARE-MANUAL.PDF)

9.0 ARCHITECTURAL/FUNCTIONAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - CLEAR CHANNEL FRAMER AND HIGH-SPEED HDLC CONTROLLER MODE APPLICATIONS (SEE 79L71-CC-ARC-DESC.PDF)

10.0 ELECTRICAL CHARACTERISTICS

10.1 DC Electrical

TABLE 7: DC ELECTRICAL CHARACTERISTICSS

APPLIES TO ALL TTL-LEVEL INPUT AND CMOS LEVEL OUTPUT PINS - AMBIENT TEMPERATURE = 25°C						
SYMBOL	**PARAMETER**	**TEST CONDITION**		**MIN**	**MAX**	**UNITS**
VDDQ	I/O Supply Voltage			3.135	3.465	V
VIH	High-Level Input Voltage	VOUT ³ VOH(min)		2.0	VDD + 0.3	V
VIL	Low-Level Input Voltage	VOUT < VOL (max)		-0.3	0.3*VDD	V
VOH	High-Level Output Voltage	VDD = MIN VIN = VIH	IOH = -2mA	1.9		V
VOL	Low-Level Output Voltage	VDD = MIN VIN = VIL	IOL = 2mA		0.6	V
II	Input Current	VDD = MAX VIN = VDD or GND			±15	mA

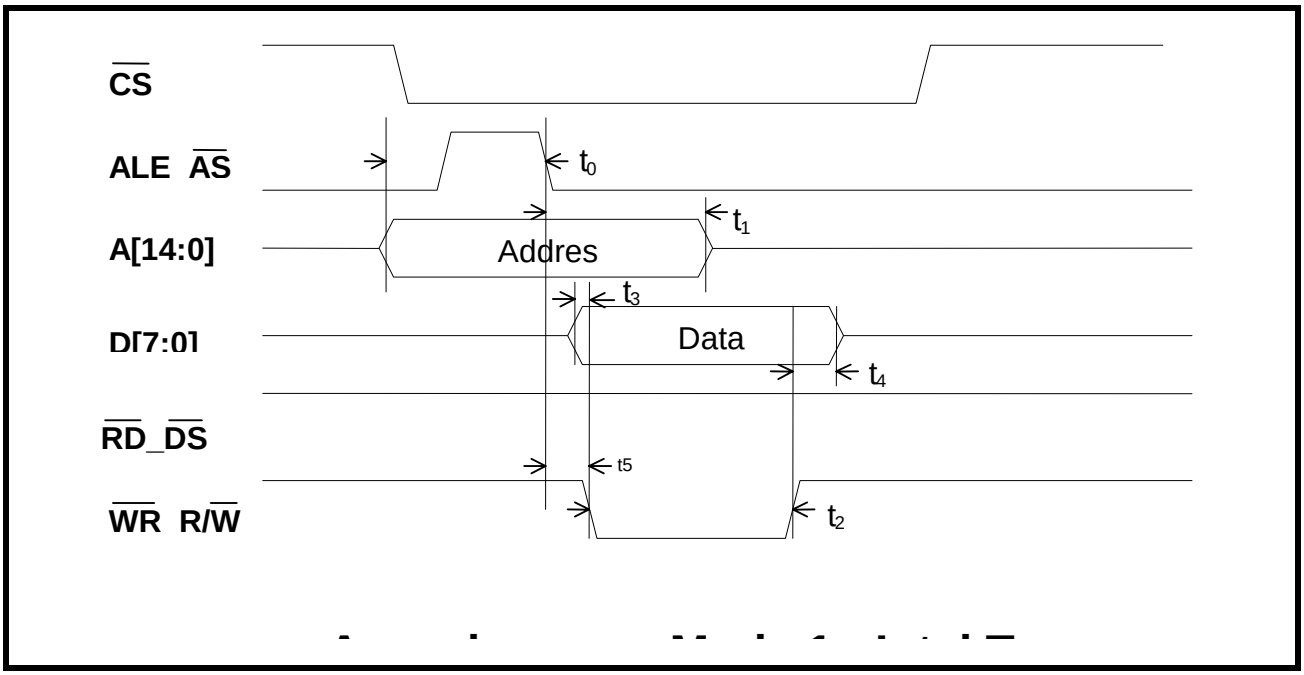
10.2 AC ELECTRICAL CHARACTERISTIC INFORMATION

11.0 MICROPROCESSOR INTERFACE

MICROPROCESSOR INTERFACE TIMING FOR REVISION A SILICON

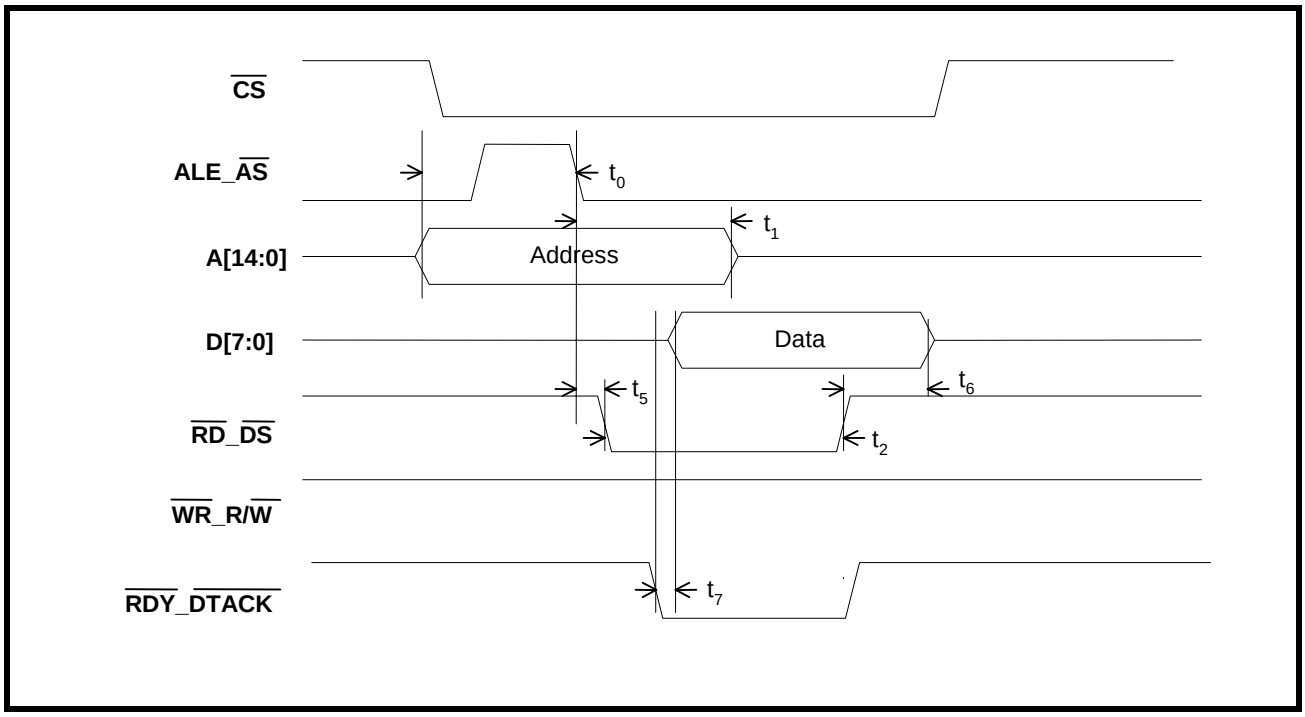
MICROPROCESSOR INTERFACE TIMING - ASYNCHRONOUS INTEL MODE

FIGURE 6. ASYNCHRONUS MODE 1 - INTEL TYPE PROGRAMMED I/O TIMING (WRITE CYCLE)



NOTE: *The values for "t0" through "t7", in this figure can be found in* **Table 8**.

FIGURE 7. ASYNCHRONUS MODE 1 - INTEL TYPE PROGRAMMED I/O TIMING (READ CYCLE)



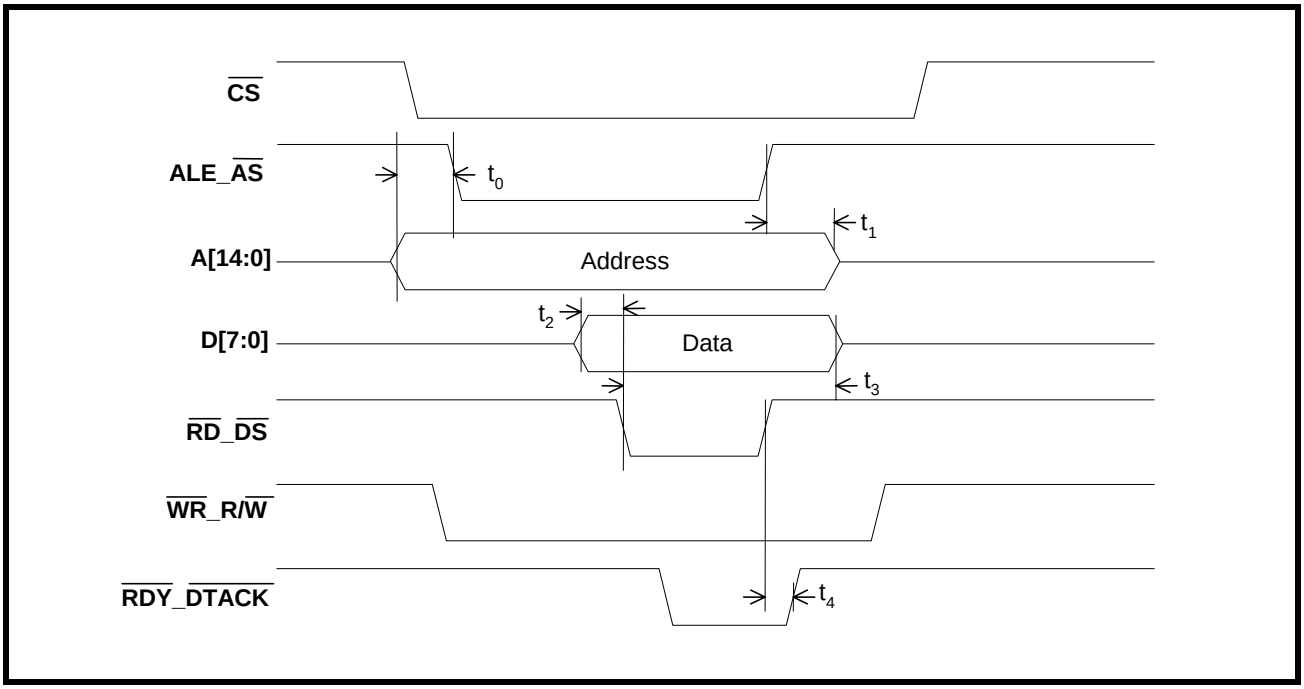
NOTE: The values for "t0" through "t7", in this figure can be found in **Table 8**.

TABLE 8: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE INTEL ASYNCHRONOUS MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t0	Address setup time to pALE low	4	-	-
t1	Address hold time from pALE low	4	-	-
t2	pRD_L, pWR_L pulse width	320	-	-
t3	Data setup time to pWR_L low	0	-	-
t4	Data hold time from pWR_L high	0	-	-
t5	pALE low to pRD_L, pWR_L low	5	-	-
t6	Data invalid from pRD_L high	4	-	-
t7	Data valid from pRDY_L low	-	-	0
t8	pRDY inactive from pRD_L inactive	3		9

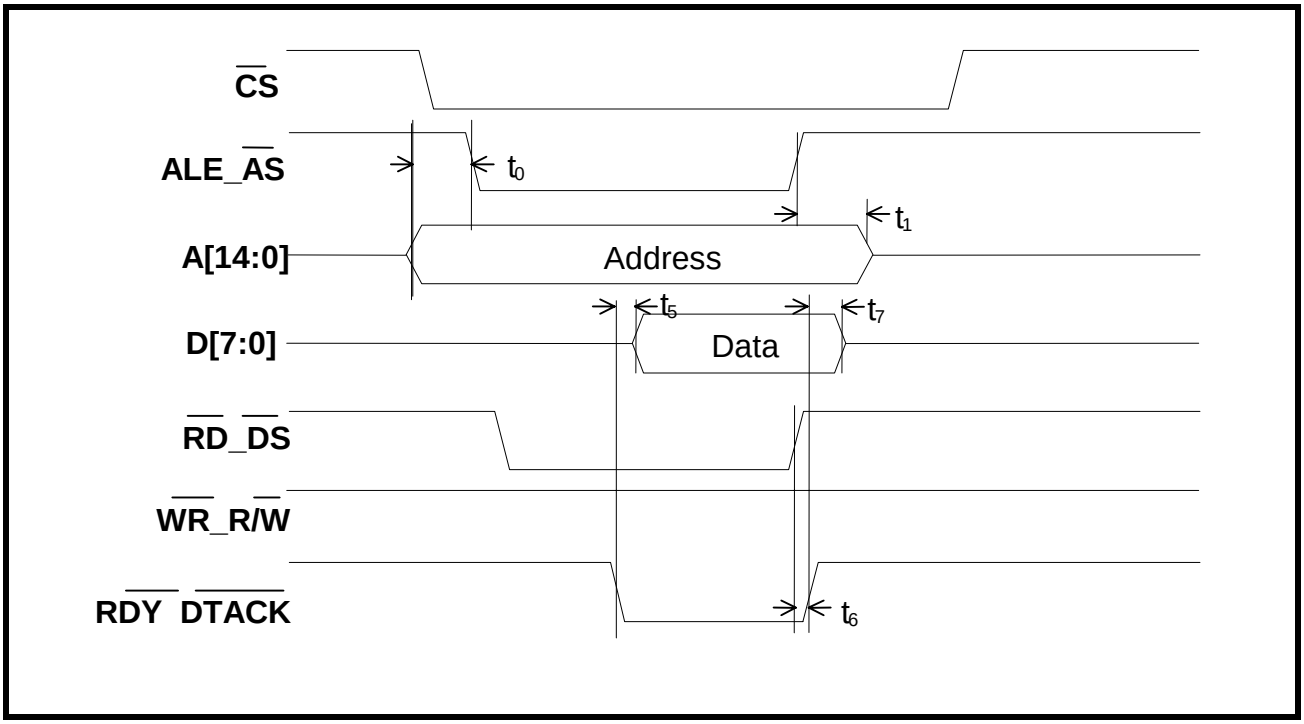
MICROPROCESSOR INTERFACE TIMING - ASYNCHRONOUS MOTOROLA (68K) MODE

FIGURE 8. ASYNCHRONUS MODE 2 - MOTOROLA 68K PROGRAMMED I/O TIMING (WRITE CYCLE)



NOTE: The values for "t0" through "t7" can be found in **Table 9**.

FIGURE 9. ASYNCHRONUS MODE 2 - MOTOROLA 68 PROGRAMMED I/O TIMING (READ CYCLE)



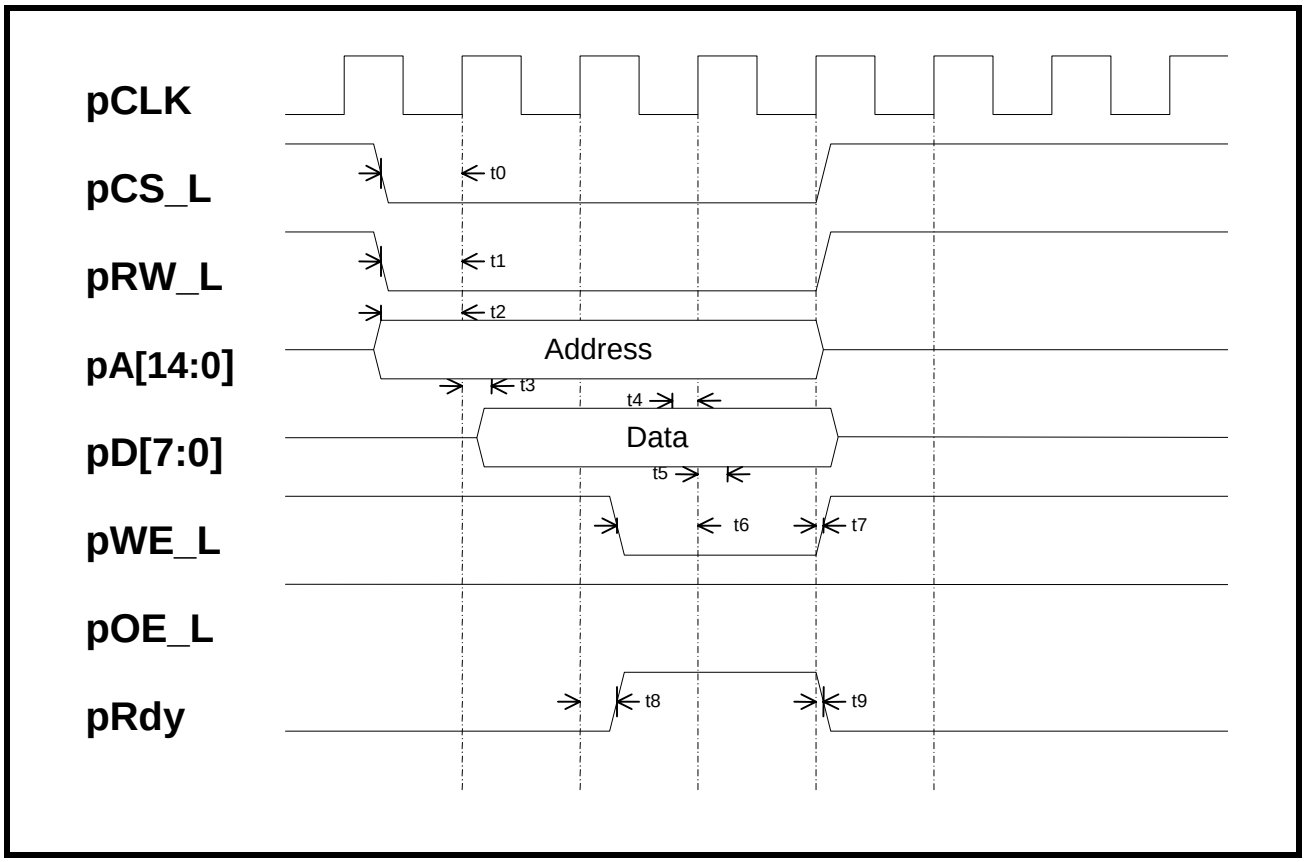
NOTE: The values for "t0" through "t7" can be found in **Table 9**.

TABLE 9: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE WHEN CONFIGURED TO OPERATE IN THE MOTOROLA (68K) ASYNCHRONOUS MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX**
t0	Address setup time to pALE low	6	-	-
t1	Address hold time to pALE high	6	-	-
t2	Data setup time to pDS_L low	0	-	-
t3	Data hold time to pDS_L low	160	-	-
t4	pDS_L high to pRDY_L high (Write Cycle)	-	-	16
t5	pRDY_L low to Data valid	-	-	15
t6	pDS_L high to pRDY_L high (Read Cycle)	-	-	16
t7	pRDY_L high to Data invalid	3	-	-

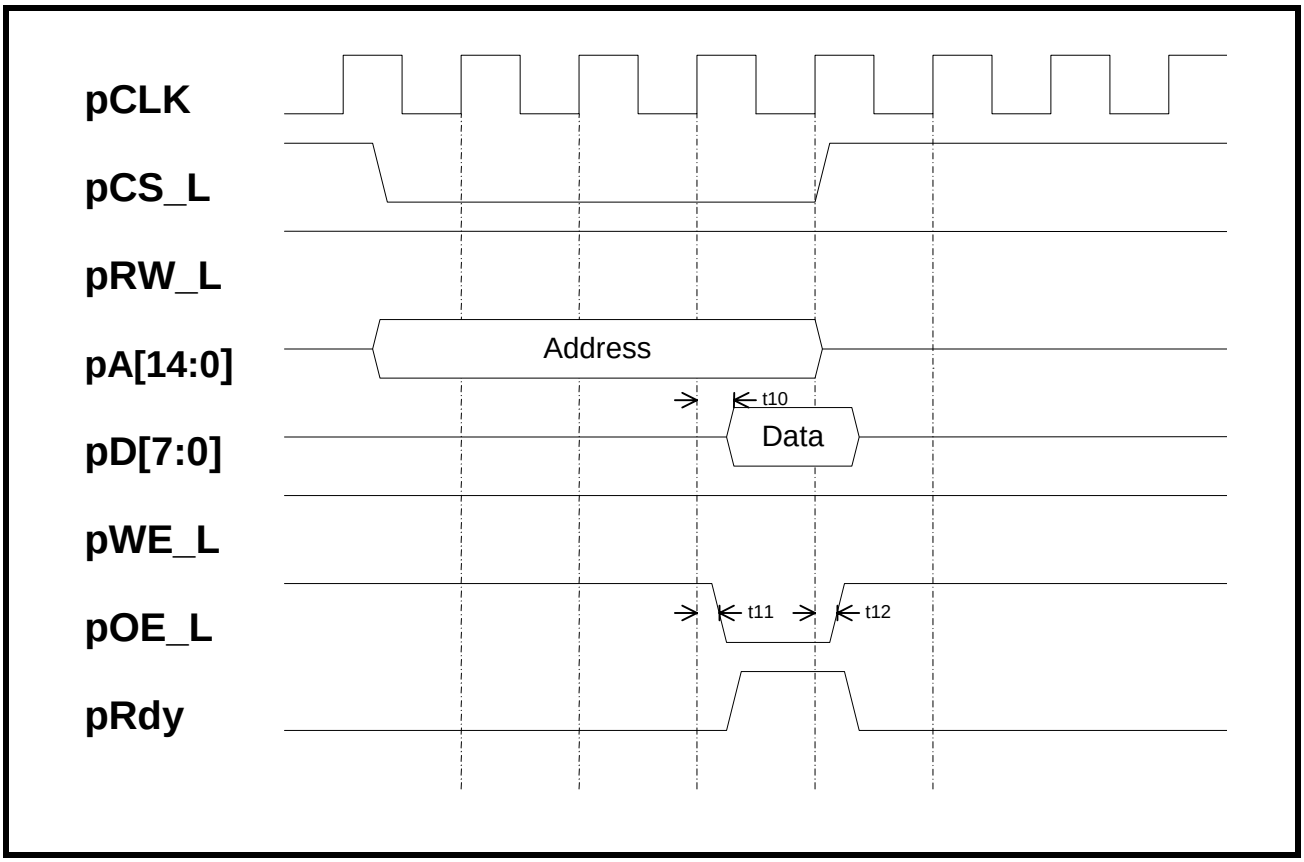
MICROPROCESSOR INTERFACE TIMING - POWER PC 403 SYNCHRONOUS MODE

FIGURE 10. SYNCHRONOUS MODE 3 - IBM POWERPC 403 INTERFACE TIMING (WRITE CYCLE)



NOTE: *The value for "t0" through "t12" can be found in* **Table 10**.

FIGURE 11. SYNCHRONOUS MODE 3 - IBM POWERPC 403 INTERFACE TIMING (READ CYCLE)



NOTE: The value for "t0" through "t12" can be found in **Table 10**.

TABLE 10: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

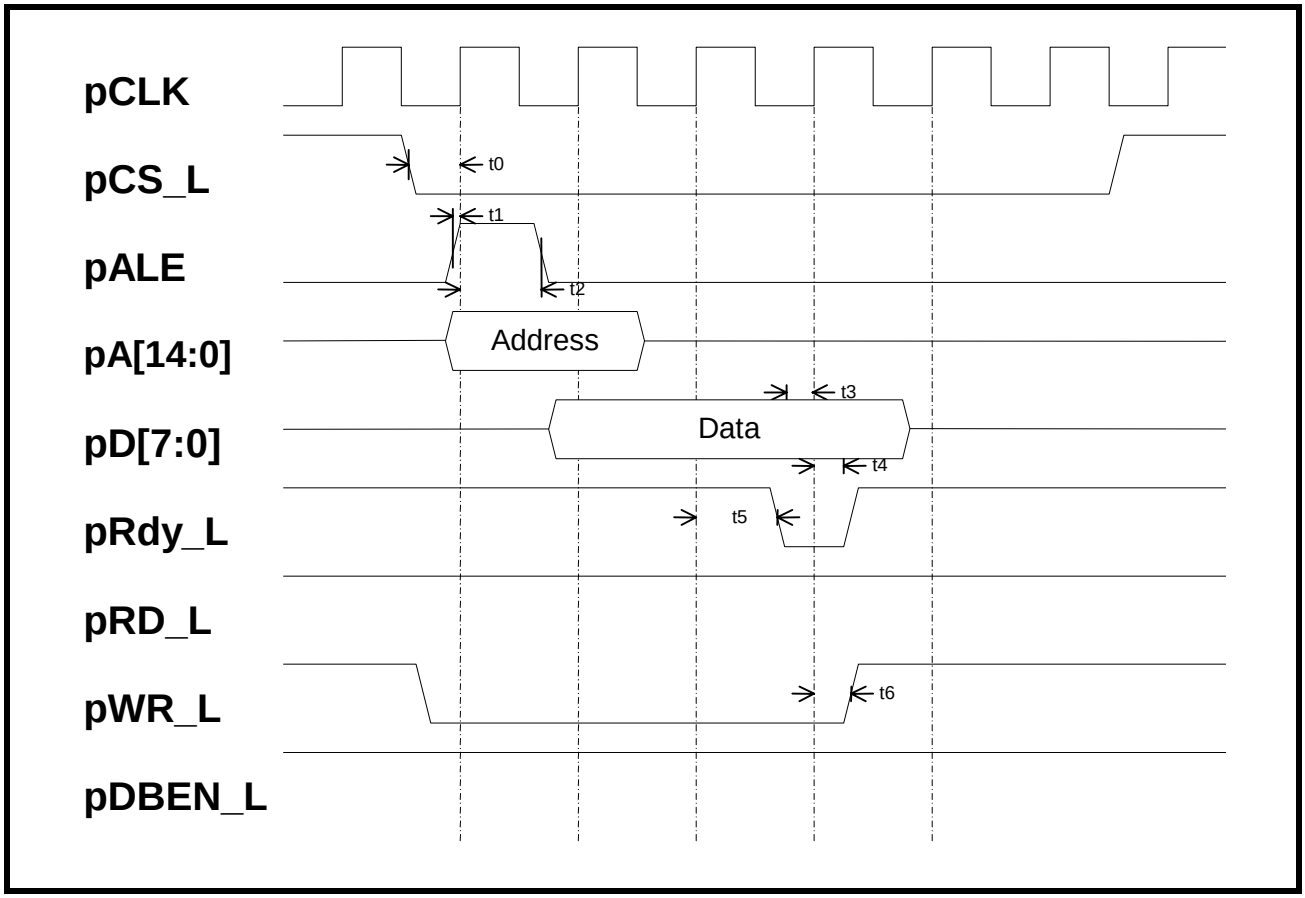
Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t0	pCS_L low to PCLK high	4	-	-
t1	pRW_L low to PCLK high	9	-	-
t2	Address setup time to PCLK high	4	-	-
t3	Address hold time from PCLK high	2	-	-
t4	Data setup time (WRITE cycle)	4	-	-
t5	Data hold time (WRITE cycle) from PCLK High	0	-	-
t6	pWE_L low to Clock high	4	-	-
t7	Clock high to pWE_L high from PCLK high	0	-	-
t8	Clock high to pRDY high	4.4	-	10.5
t9	Clock high to pRDY low	4.2	-	10.4
t10	Clock high to Data valid (READ cycle)	-	-	11

TABLE 10: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t11	Clock high to pOE_L low	11	-	-
t12	Clock high to pOE_L high	1.5	-	4.1

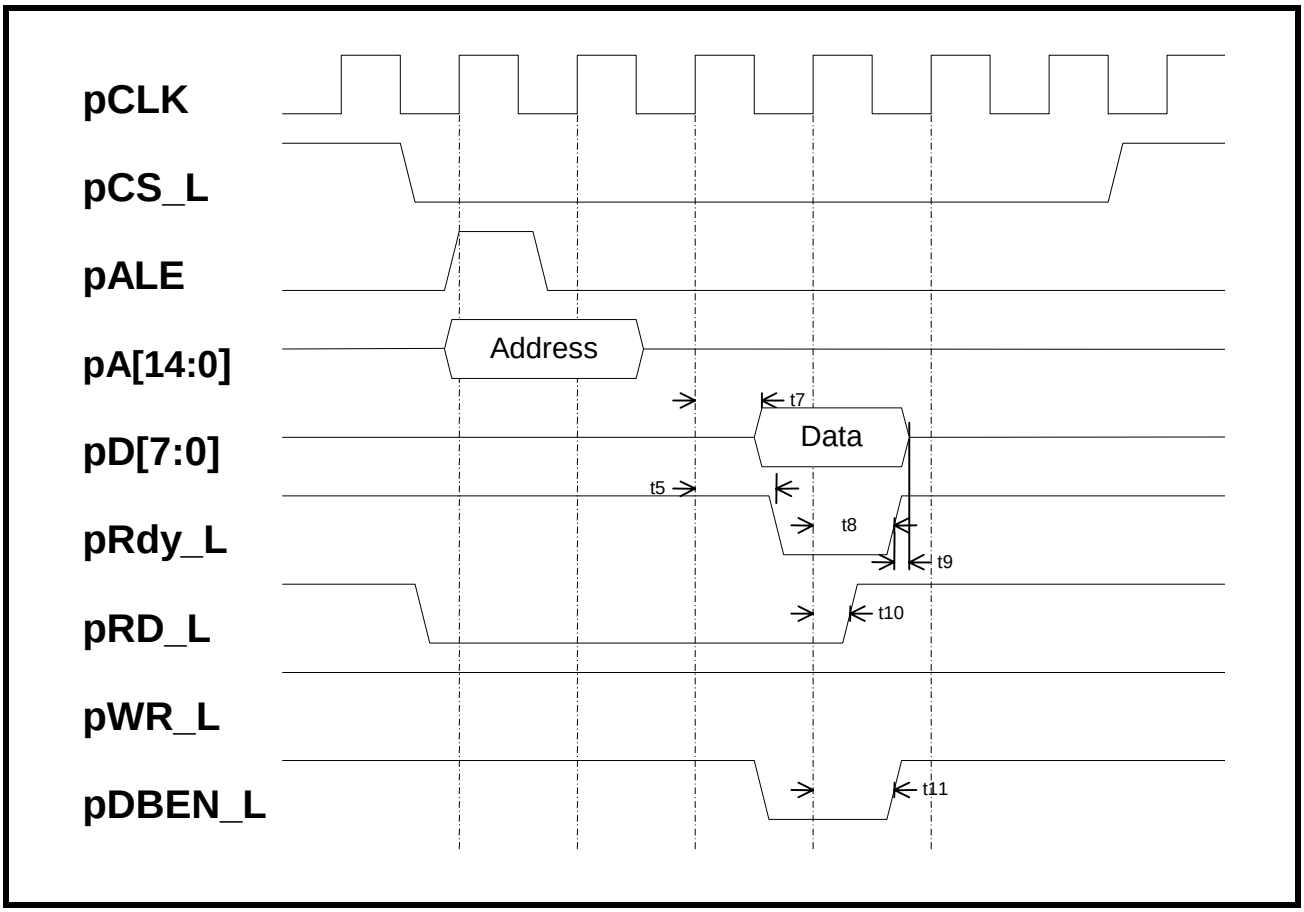
MICROPROCESSOR INTERFACE TIMING - IDT3051/52 MODE

FIGURE 12. SYNCHRONOUS MODE 4 - IDT 3051/52 INTERFACE TIMING (WRITE CYCLE)



NOTE: *The values for "t0" through "t11" can be found in* **Table 11**.

FIGURE 13. SYNCHRONOUS MODE 4 - IDT 3051/52 INTERFACE TIMING (READ CYCLE)



NOTE: The values for "t0" through "t11" can be found in **Table 11**.

TABLE 11: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t0	pCS_L low to Clock high	6	-	-
t1	pALE high to Clock high	1	-	-
t2	Clock high to pALE low	6	-	-
t3	Data setup time (WRITE cycle)	-	-	N/N
t4	Data hold time (WRITE cycle)	-	-	N/N
t5	Clock high to pRDY_L low	-	-	11
t6	Clock high to pWR_L high	6	-	-
t7	Clock high to Data valid (READ cycle)	-	-	N/N
t8	Clock high to pRDY_L high	-	-	11
t9	pRDY_L high to Data invalid	0	-	-

TABLE 11: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t10	Clock high to pRD_L high	11	-	-
t11	Clock high to pDBEN_L high	10	-	-

DS3/E3 LIU INTERFACE - LINE SIDE ELECTRICAL CHARACTERISTIC INFORMATION

E3 LINE SIDE PARAMETERS

The XRT79L71 line output at the Transmit Output complies with the pulse template requirements as specified in ITU-T G.703 for 34.368Mbps operation. The pulse mask as specified in ITU-T G.703 for 34.368Mbps is shown below in **Figure 14**.

FIGURE 14. PULSE MASK FOR E3 (34.368MBPS) INTERFACE AS PER ITU-T G.703

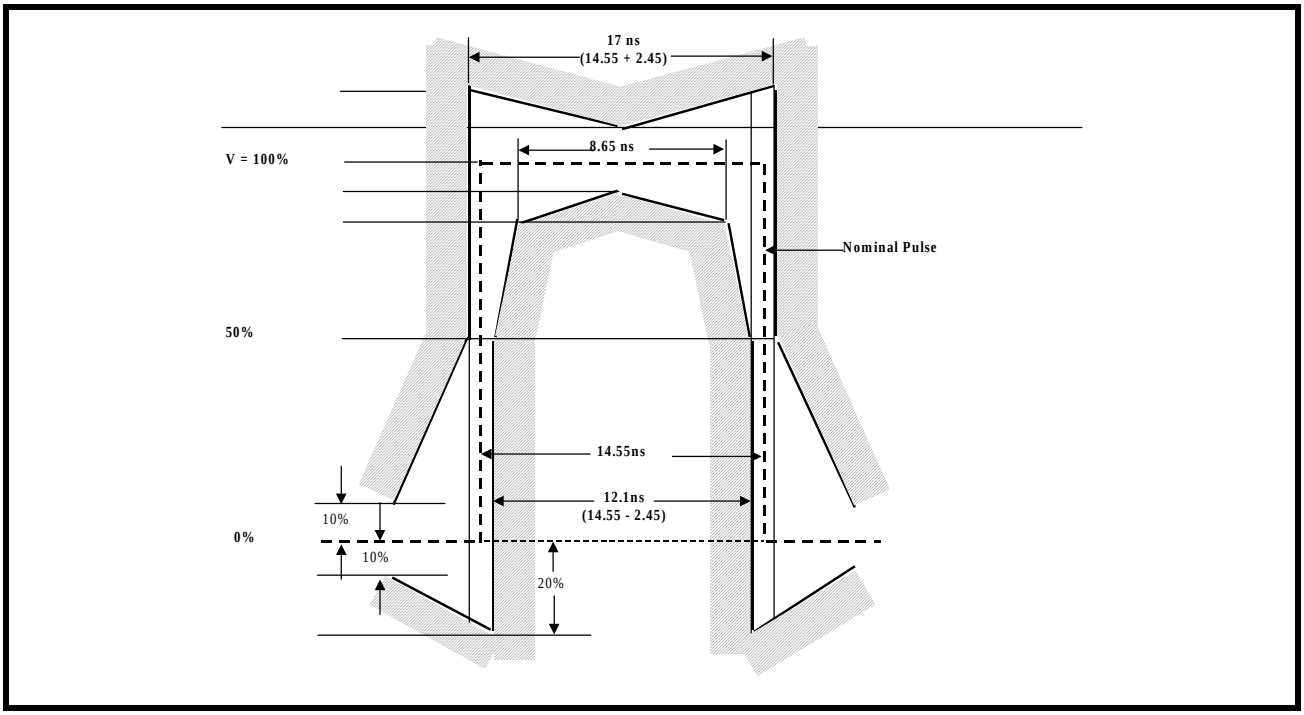


TABLE 12: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Transmit Intrinsic Jitter (without Jitter Attenuator in theTransmit path)		0.01	0.015	UI_{PP}

TABLE 12: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
Transmit Intrinsic Jitter (with Jitter Attenuator in the Transmit path)		0.02	0.03	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1200		feet
Interference Margin	-20	-14		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

DS3 LINE SIDE PARAMETERS

The XRT79L71 will output pulses that comply with the Isolated DSX-3 Pulse Template requirements per Bellcore GR-499-CORE. The pulse mask as specified in Bellcore GR-499-CORE is shown below in Figure 15. Additionally, the Equations that define both the "Upper" and "Lower" curves of the Pulse Template requirement is presented below in Table 13.

FIGURE 15. BELLCORE GR-499-CORE PULSE TEMPLATE REQUIREMENTS FOR DS3 APPLICATIONS

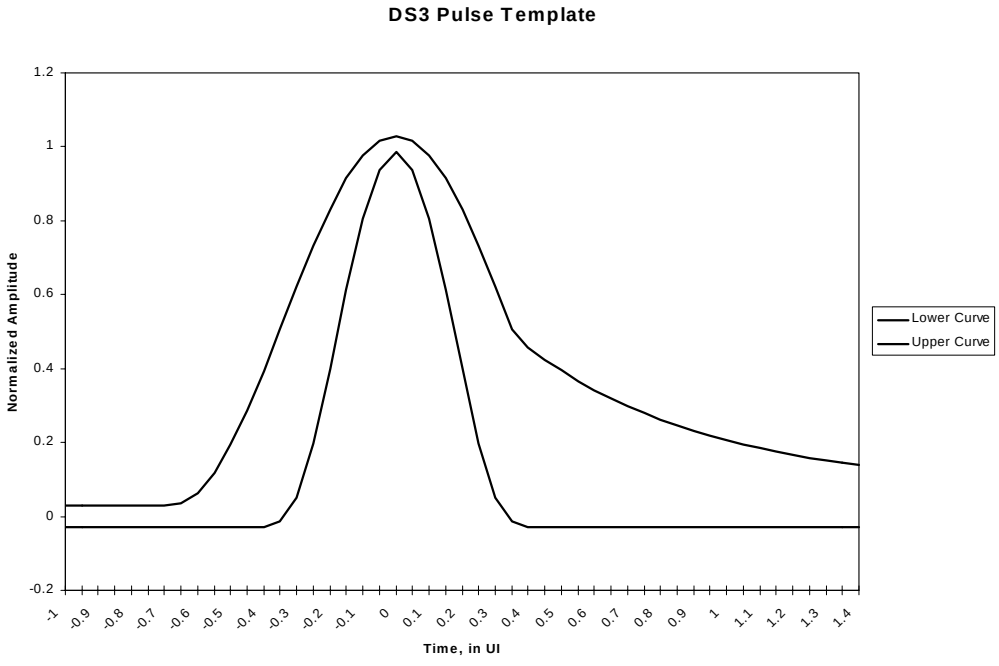


TABLE 13: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\left(\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\left(\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right)\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 14: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
Transmit Intrinsic Jitter (without Jitter Attenuator in Transmit path)		0.01	0.015	UI_{pp}
Transmit Intrinsic Jitter (withJitter Attenuator in Transmit path)		0.02	0.04	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

TRANSMIT UTOPIA INTERFACE

The purpose of the Transmit UTOPIA Interface block is to function as either a Standard UTOPIA Level 1, 2 or 3 Interface as it accepts ATM cell data from either an ATM Layer or ATM Adaptation Layer Processor, and routes this ATM cell data to the TxFIFO within the XRT79L71.

FIGURE 16. TIMING DIAGRAM FOR THE TRANSMIT UTOPIA INTERFACE BLOCK

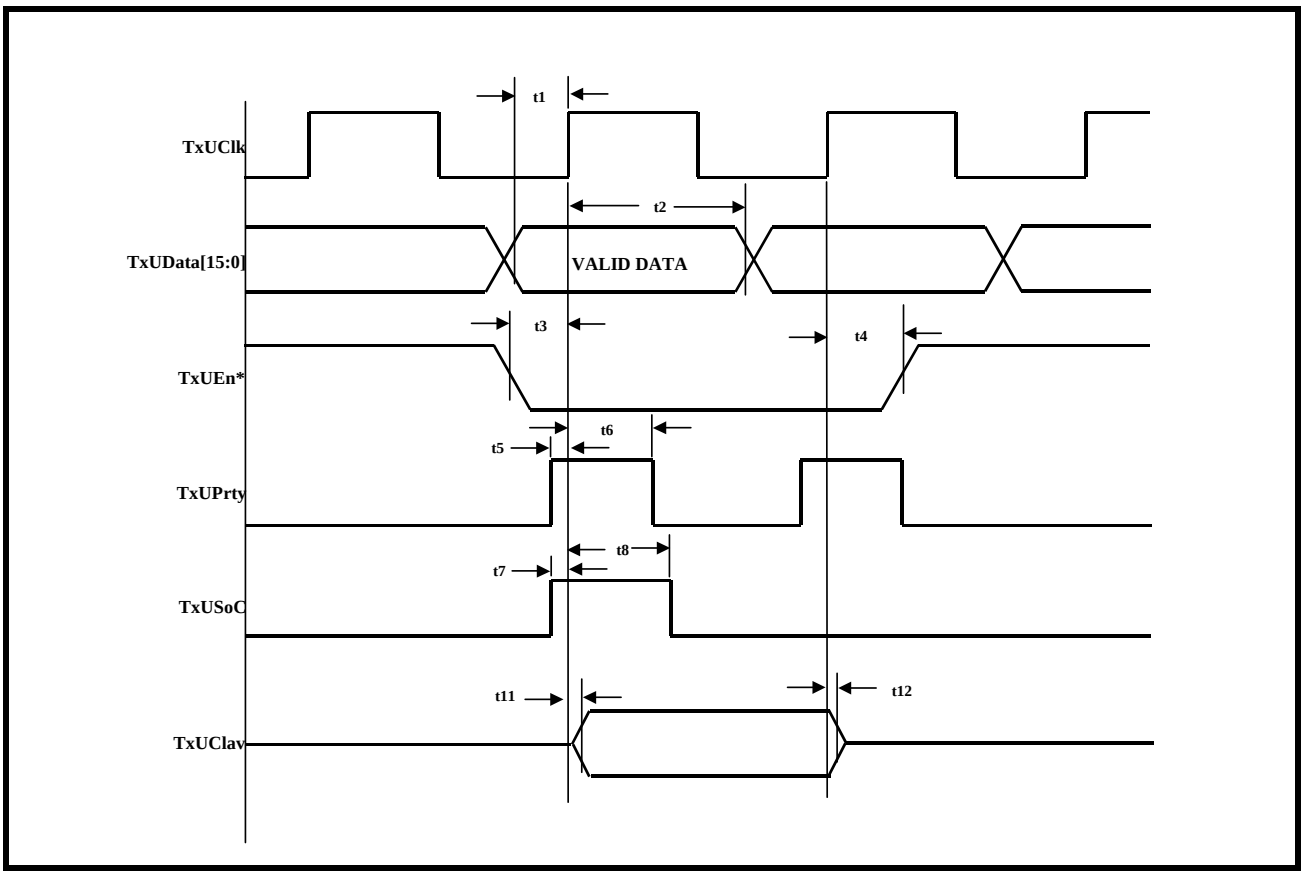


TABLE 15: TIMING INFORMATION FOR THE TRANSMIT UTOPIA INTERFACE BLOCK

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS
t1	TxUData[15:0] to rising edge of TxUClk Setup Time	4			ns
t2	TxUData[15:0] Hold Time from rising edge of TxUClk	1			ns
t3	TxUTOPIA Write Enable Setup Time to rising edge of TxUClk	4			ns
t4	TxUTOPIA Write Enable Hold Time from rising edge of TxUClk	1			ns
t5	TxUPrty Setup Time to rising edge of TxUClk	4			ns
t6	TxUPrty Hold Time from rising edge of TxUClk	1			ns
t7	TxUSoC Setup Time to rising edge of TxUClk	4			ns
t8	TxUSoC Hold Time from rising edge of TxUClk	1			ns
t9	TxUAddr[4:0] Setup Time to rising edge of TxUClk	4			ns
t10	TxUAddr[4:0] Hold Time from rising edge of TxUClk	1			ns

TABLE 15: TIMING INFORMATION FOR THE TRANSMIT UTOPIA INTERFACE BLOCK

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS
t11	TxUClav signal valid (not Hi-Z) from first TxUClk rising edge of valid and correct TxUAddr[4:0]	3.6		9.7	ns
t12	TxUClav signal Hi-Z from first TxUClk rising edge of different TxUAddr[4:0]	3.6		9.7	ns

TRANSMIT PAYLOAD DATA INPUT INTERFACE

TRANSMIT PAYLOAD DATA INPUT INTERFACE - TIMING REQUIREMENTS

TABLE 16: TIMING INFORMATION FO RTHE TRNASMIT PAYLOAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit Payload Data Input Interface - Loop-Timed/Serial Mode (See Figure 17)						
t_1	Payload data (TxSer) set-up time to rising edge of RxOutClk	12			ns	
t_2	Payload data (TxSer) hold time, from rising edge of RxOutClk	0			ns	
t_3	RxOutClk to TxFrame output delay			5	ns	
t_4	RxOutClk to TxOHInd output delay			6	ns	
Transmit Payload Data Input Interface - Local Timed/Serial Mode (See Figure 18)						
t_5	Payload data (TxSer) set-up time to rising edge of TxInClk	4			ns	
t_6	Payload data (TxSer) hold time, from rising edge of TxInClk	0			ns	
t_7	TxFrameRef set-up time to rising edge of TxInClk	2			ns	Framer IC is Frame Slave
t_8	TxFrameRef hold-time, from rising edge of TxInClk	0			ns	Frame IC is Frame Slave
t_9	TxInClk to TxOHInd output delay			15	ns	
t_{10}	TxInClk to TxFrame output delay			13	ns	
Transmit Payload Data Input Interface - Looped-Timed/Nibble Mode (See Figure 19)						
t_{11}	TxNib set-up time to third rising edge of RxOutClk	30			ns	
t_{12}	Payload Nibble hold time, from latching edge of RxOutClk	30			ns	
t_{13}	TxNibClk to TxNibFrame output delay			25 31	ns ns	DS3 Applications E3 Applications
t_{13A}	Max Delay of Rising Edge of TxNibClk to Data Valid on TxNib[3:0]			20 27	ns ns	DS3 Applications E3 Applications
Transmit Payload Data Input Interface - Local-Timed/Nibble Mode (See Figure 20						

TABLE 16: TIMING INFORMATION FO RTHE TRNASMIT PAYLOAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{14}	TxNib set-up time to third rising edge of TxInClk			20 27	ns ns	DS3 Applications E3 Applications
t_{15}	Payload Nibble hold time, from latching edge of TxInClk	0			ns	
t_{16}	TxFrameRef set-up time, to latching edge of TxInClk			20 27	ns ns	DS3 Applications E3 Applications Framer IC is Frame Slave
t_{17}	TxFrameRef hold time, from latching edge of TxNib-Clk	0			ns	Framer IC is Frame Slave
t_{18}	TxNibClk to TxNibFrame output delay time	20		25 31	ns ns	DS3 Applications E3 Applications

FIGURE 17. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L71 IS OPERATING IN BOTH THE DS3 AND LOOP-TIMING MODES

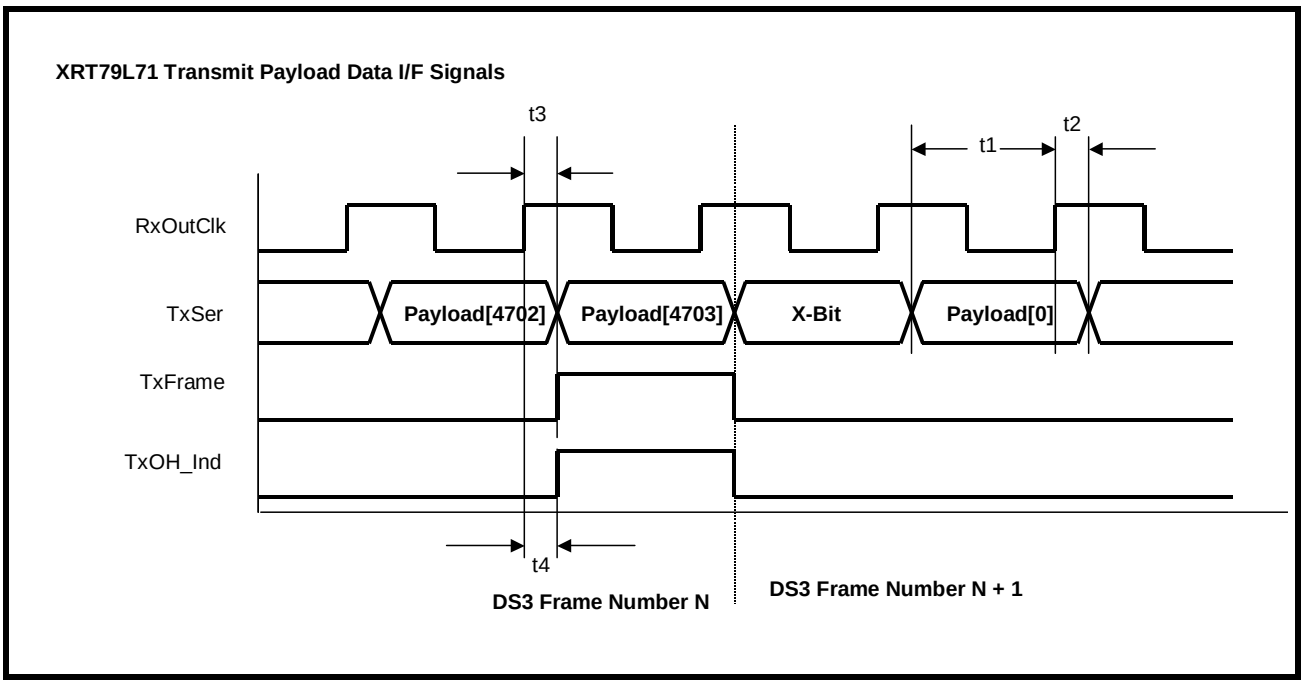


FIGURE 18. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L71 IS OPERATING IN BOTH THE DS3 AND LOCAL-TIMING MODES

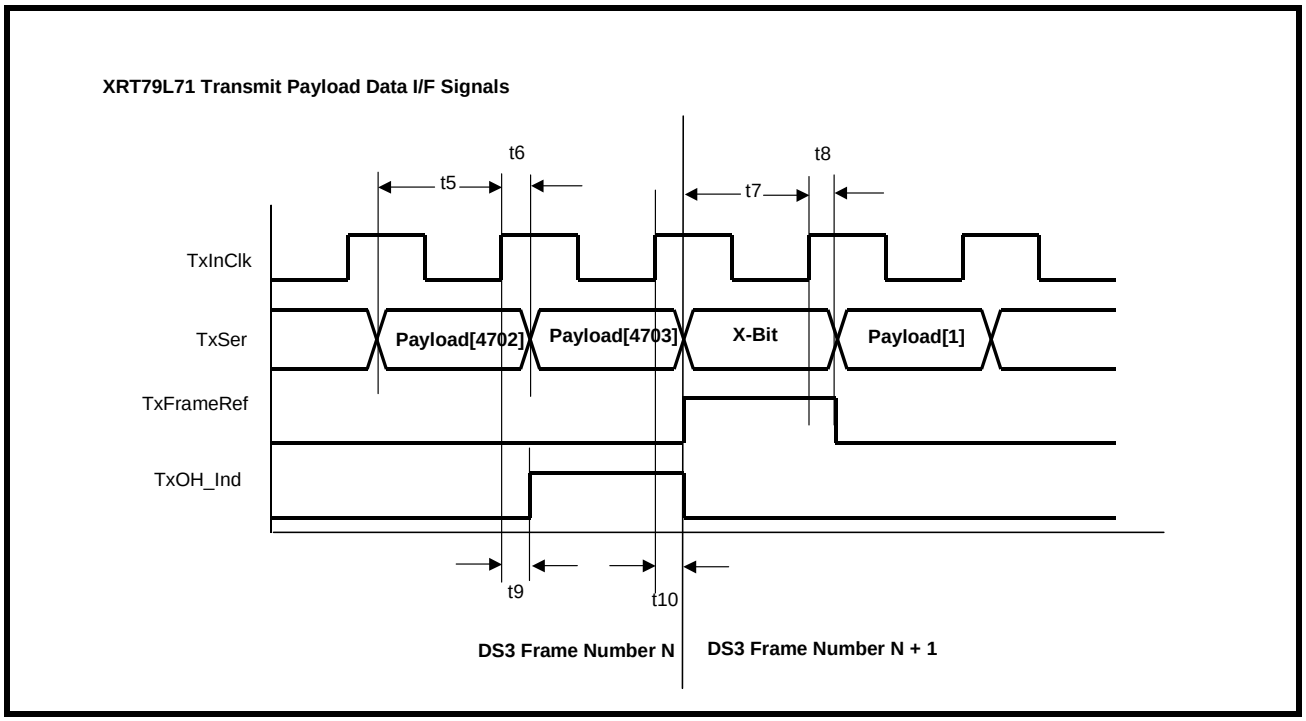


FIGURE 19. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L71 IS OPERATING IN BOTH THE DS3/NIBBLE-PARALLEL AND LOOP-TIMING MODES

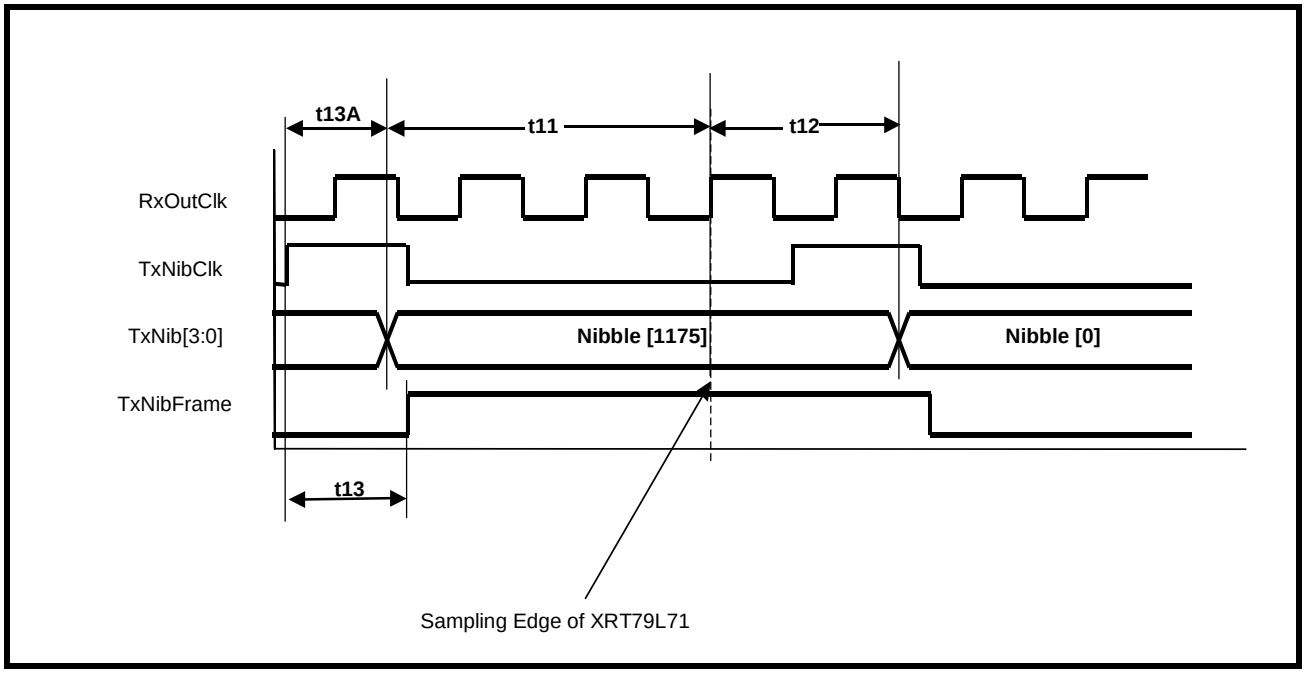
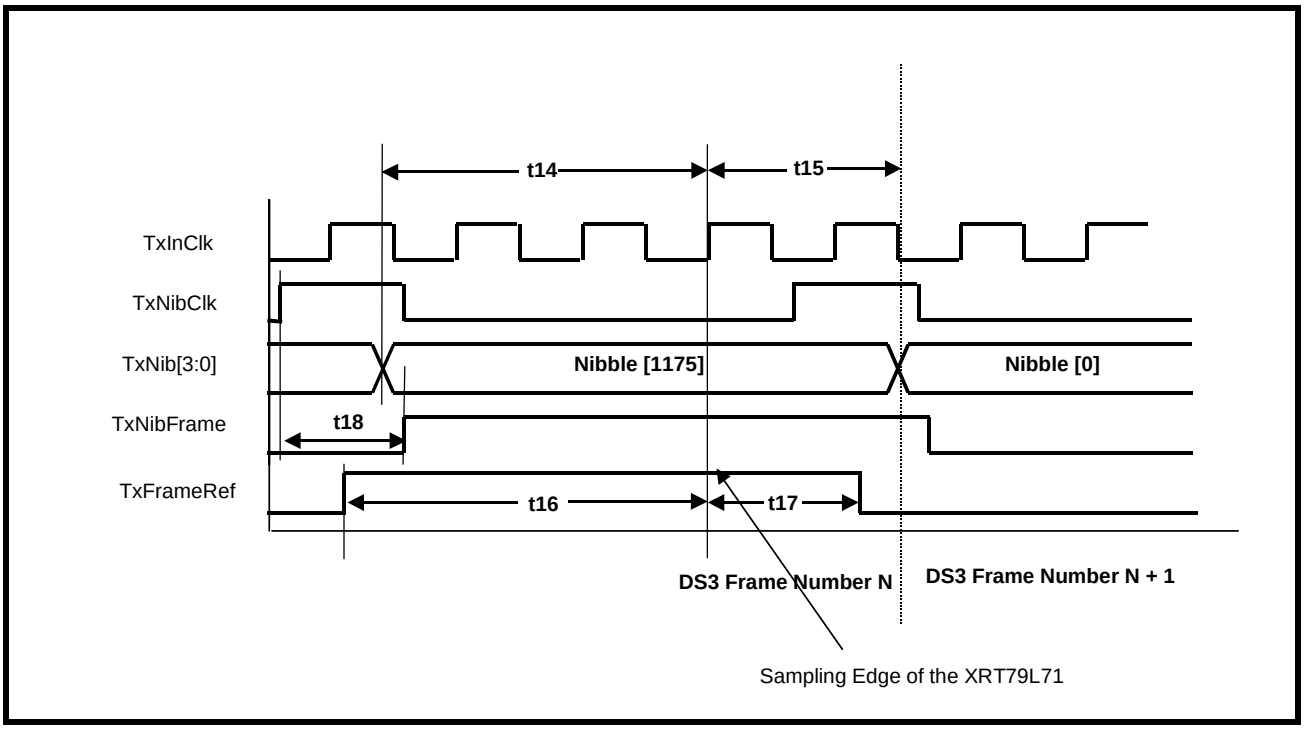


FIGURE 20. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L71 IS OPERATING IN BOTH THE DS3/NIBBLE-PARALLEL AND LOCAL-TIMING MODES



TRANSMIT OVERHEAD DATA INPUT INTERFACE

TRANSMIT OVERHEAD DATA INPUT INTERFACE - TIMING REQUIREMENTS

TABLE 17: TIMING INFORMATION FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
Transmit Overhead Input Interface Timing - Method 1 (Figure 21)						
t_{21}	TxOHClk to TxOHFrame output delay			111	ns	DS3 Applications
				0	ns	E3, ITU-T G.832 Applications
				0	ns	E3, ITU-T G.751 Applications
t_{22}	TxOHIns set-up time, to falling edge of TxOHClk	194			ns	DS3 Applications
		305			ns	E3, ITU-T G.832 Applications
		17			ns	E3, ITU-T G.751 Applications
t_{23}	TxOHIns hold time, from falling edge of TxOHClk	48			ns	DS3 Applications
		110			ns	E3, ITU-T G.832 Applications
		7			ns	E3, ITU-T G.751 Applications
t_{24}	TxOH data set-up time, to falling edge of TxOHClk	194			ns	DS3 Applications
		305			ns	E3, ITU-T G.832 Applications
		17			ns	E3, ITU-T G.751 Applications
t_{25}	TxOH data hold time, from falling edge of TxOHClk	48			ns	DS3 Applications
		110			ns	E3, ITU-T G.832 Applications
		7			ns	E3, ITU-T G.751 Applications
Transmit Overhead Data Input Interface - Method 2 (Figure 22)						

TABLE 17: TIMING INFORMATION FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{26}	TXOHIns to TxInClk (rising edge) set-up Time	254			ns	DS3 Applications
		72			ns	E3, ITU-T G.832 Applications
		15			ns	E3, ITU-T G.751 Applications
t_{27}	TxInClk clock (rising edge) to TxOHIns hold-time	0			ns	DS3 Applications
		0			ns	E3, ITU-T G.832 Applications
		0			ns	E3, ITU-T G.751 Applications
t_{28}	TXOH to TxInClk (rising edge) set-up Time	254			ns	DS3 Applications
		72			ns	E3, ITU-T G.832 Applications
		15			ns	E3, ITU-T G.751 Applications
t_{29}	TxInClk clock (rising edge) to TxOH hold-time	0			ns	DS3 Applications
		0			ns	E3, ITU-T G.832 Applications
		0			ns	E3, ITU-T G.751 Applications
t_{29A}	TxOHEnable to TxOHIns/TxOH Delay	1			ns	

FIGURE 21. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1 ACCESS)

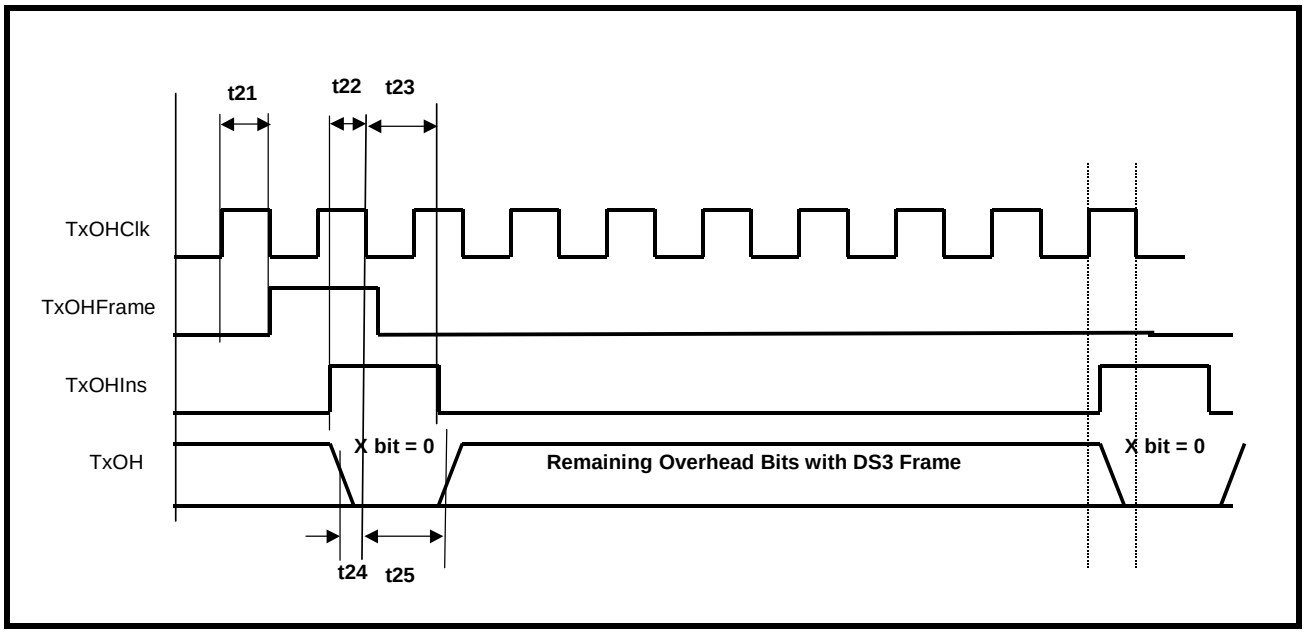
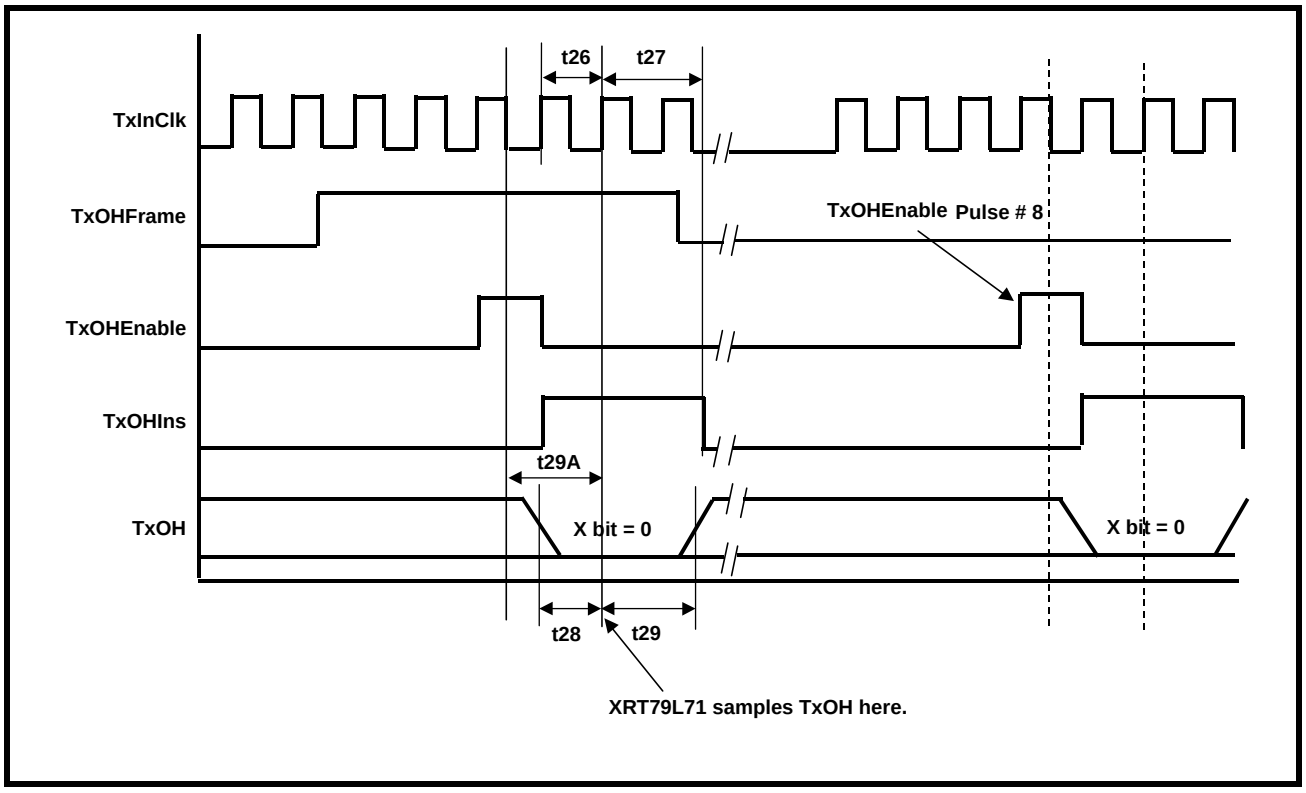


FIGURE 22. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2 ACCESS)



RECEIVE PAYLOAD DATA OUTPUT INTERFACE

RECEIVE PAYLOAD DATA OUTPUT INTERFACE - TIMING REQUIREMENTS

TABLE 18: TIMING INFORMATION FOR THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
Receive Payload Data Output Interface Timing - Serial Mode Operation (See Figure 23)						
t_{50}	Rising edge of RxClk to Payload Data (RxSer) output delay			13	ns	DS3 Applications
				16	ns	E3 Applications
t_{51}	Rising edge of RxClk to RxFrame output delay			13	ns	DS3 Applications
				16	ns	E3 Applications
t_{52}	Rising edge of RxClk to RxOHInd output delay.			13	ns	DS3 Applications
				16	ns	E3 Applications
Receive Payload Data Output Interface Timing - Nibble Mode Operation (see Figure 24)						
t_{53}	Falling edge of RxClk to rising edge of RxFrame output delay			2.1	ns	
t_{54}	Falling edge of RxClk to rising edge of RxNib[3:0] output delay			2	ns	

FIGURE 23. TIMING DIAGRAM FOR THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE (SERIAL MODE)

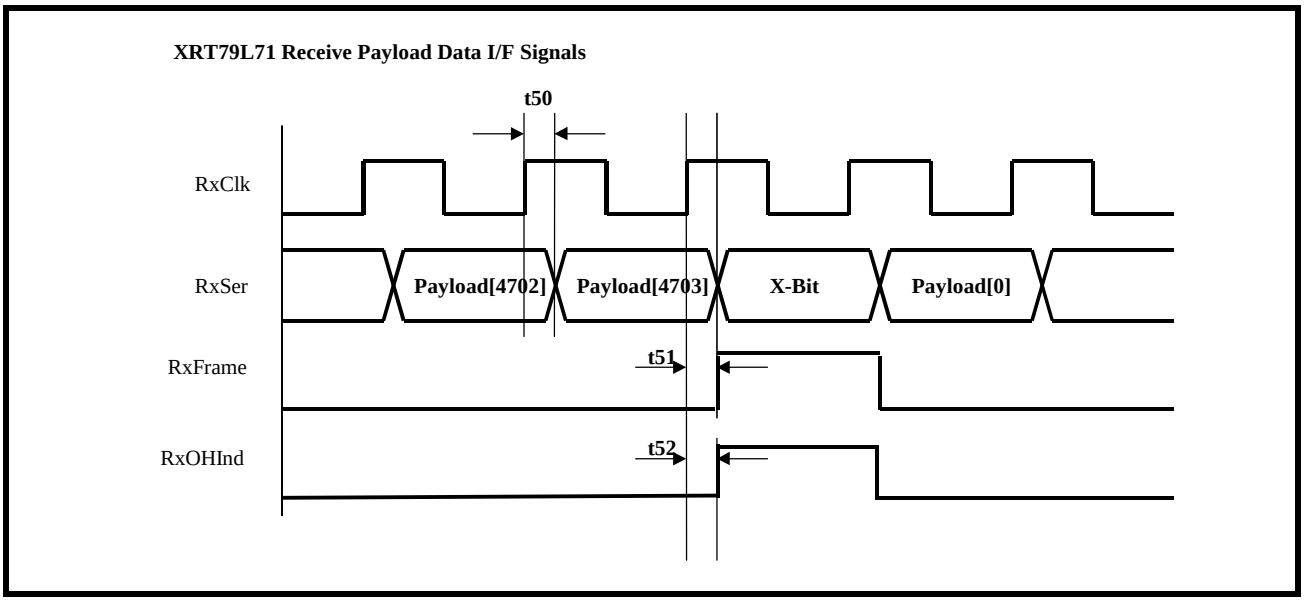
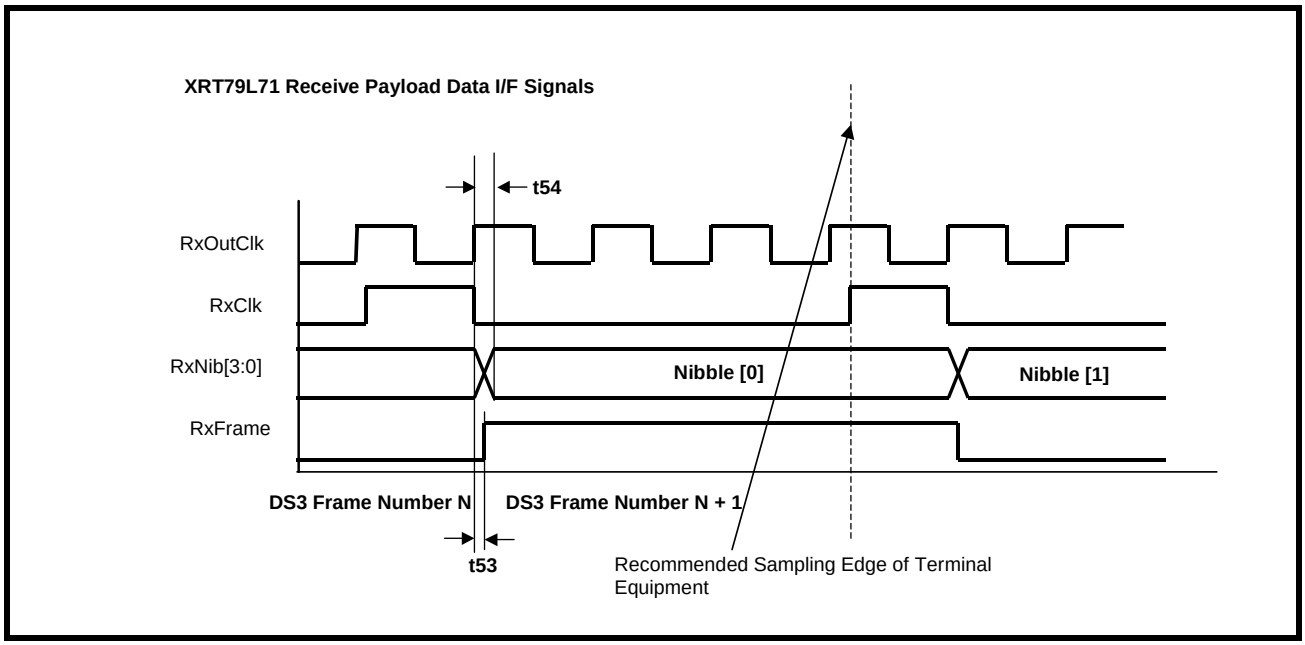


FIGURE 24. TIMING DIAGRAM FOR THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE (NIBBLE-PARALLEL MODE)



RECEIVE OVERHEAD DATA OUTPUT INTERFACE

RECEIVE OVERHEAD DATA OUTPUT INTERFACE - TIMING REQUIREMENTS

Table 13, Timing Information for the Receive Overhead Data Output Interface Block

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
Receive Overhead Data Output Interface Timing - Method 1 - Using RxOHClk (see Figure 21)						
t_{59A}	Falling edge of RxOHClk to RxOHFrame output	20		23	ns	DS3 Applications
		25		0	ns	E3 Applications
t_{59B}	Falling edge of RxOHClk to RxOH output delay	20		23	ns	DS3 Applications
		25		0	ns	E3 Applications
Receive Overhead Data Output Interface Timing - Method 2 - Using RxOHEnable (see Figure 22)						
t_{60}	Rising edge of RxOutClk to rising edge of RxOHEnable delay.	2		9.4	ns	
t_{60A}	Rising edge of RxOHFrame to rising edge of RxOHEnable delay			88	ns	DS3 Applications
				224	ns	E3, ITU-T G.832 Applications
				28	ns	E3, ITU-T G.751 Applications
t_{60B}	RxOH Data Valid to rising edge of RxOHEnable delay			88	ns	DS3 Applications
				85	ns	E3, ITU-T G.832 Applications
				28	ns	E3, ITU-T G.751 Applications

FIGURE 25. TIMING DIAGRAM FOR THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 1 - USING RXOHCLK)

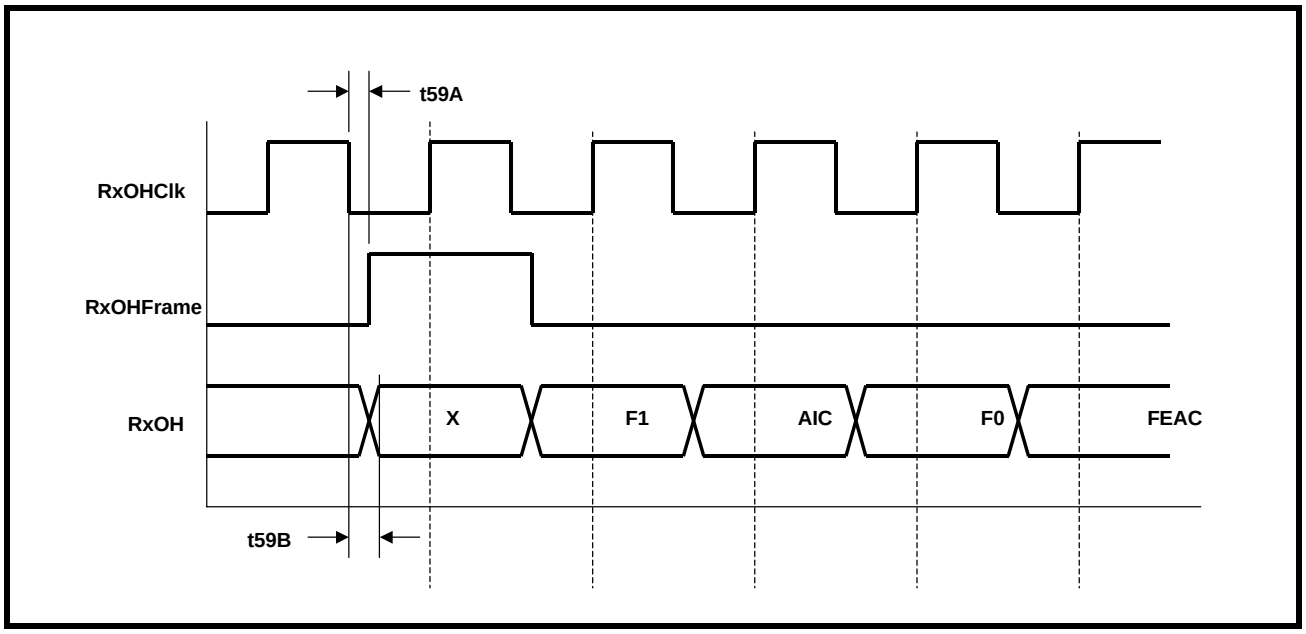
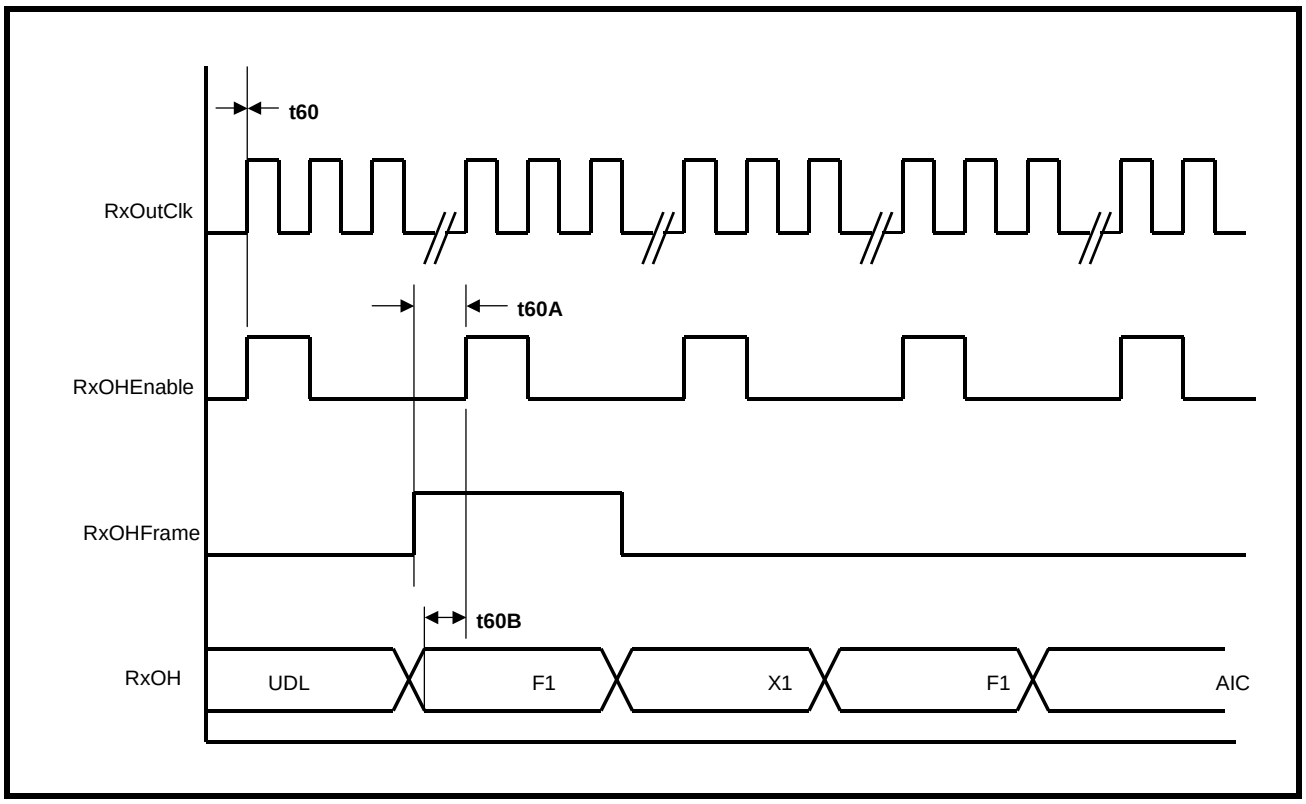


FIGURE 26. TIMING DIAGRAM FOR THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 2 - USING RXOHENABLE)



RECEIVE UTOPIA INTERFACE

RECEIVE UTOPIA INTERFACE

The purpose of the Receive UTOPIA Interface block is to function as either a Standard UTOPIA Level 1, 2 or 3 Interface as it outputs ATM cell data to either an ATM Layer or ATM Adaptation Layer Processor.

FIGURE 27. TIMING DIAGRAM FOR THE RECEIVE UTOPIA INTERFACE BLOCK

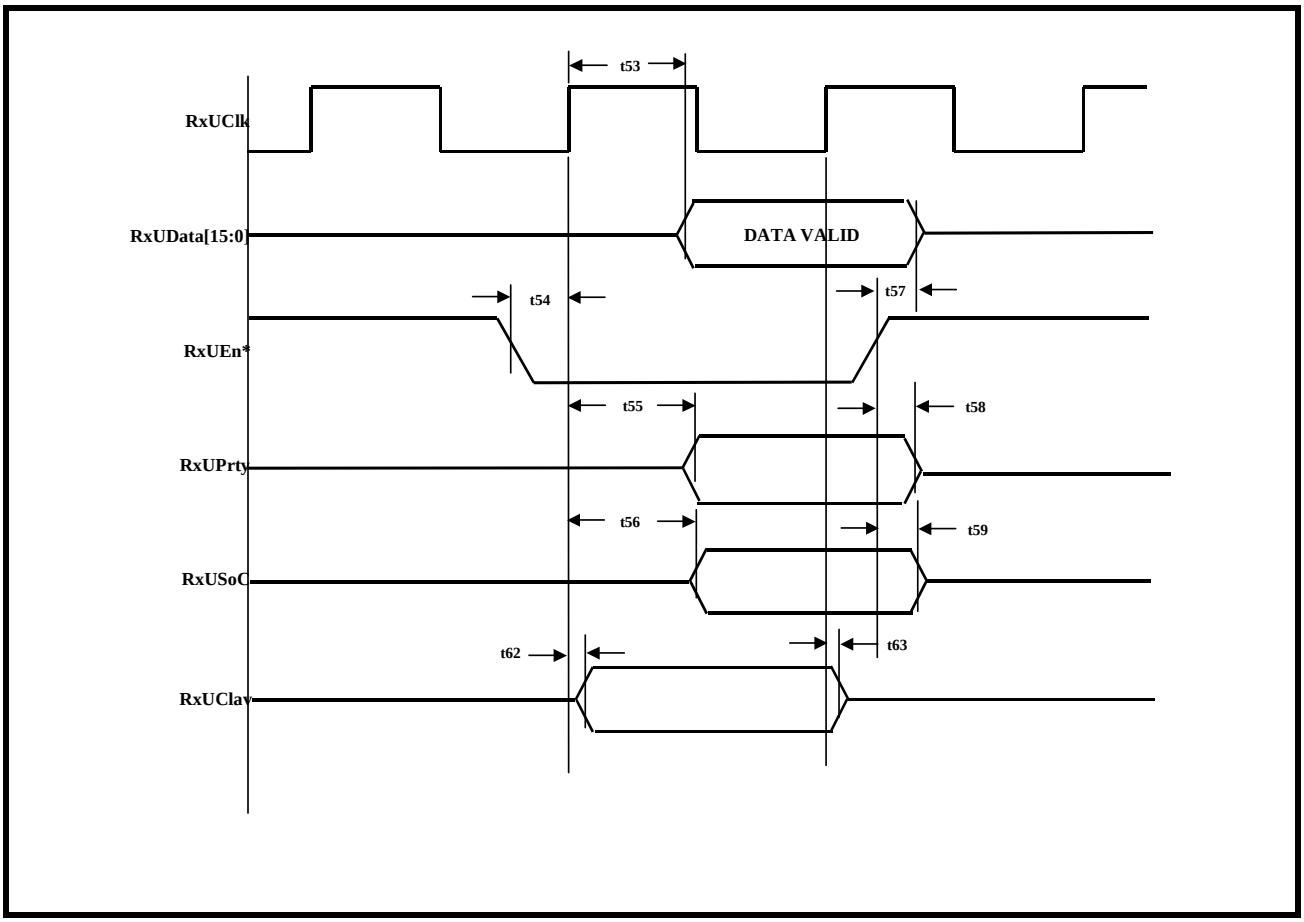


TABLE 19: TIMING INFORMATION FOR THE RECEIVE UTOPIA INTERFACE BLOCK

Symbol	PARAMETER	MIN.	TYP	MAX.	UNITS
Receive UTOPIA Interface Block (See Figure 22)					
t53	Delay time from rising edge of RxUClk to Data Valid at RxU-Data[15:0]	2.7		12	ns
t54	Rx UTOPIA Read Enable setup time to rising edge of RxUClk	4			ns
t55	Delay time from rising edge of RxUClk to valid RxUPrty bit	2.9		9.8	ns
t56	Delay time from rising edge of RxUClk to valid RxUSoC bit	3.5		9.7	ns
t57	Delay time from Read Enable false to Data Bus being tri-stated	1	11.5	16	ns
t58	Delay time from Read Enable false to RxUPrty bit being tri-stated	1	12	16	ns

TABLE 19: TIMING INFORMATION FOR THE RECEIVE UTOPIA INTERFACE BLOCK

Symbol	PARAMETER	MIN.	TYP	MAX.	UNITS
t59	Delay time from Read Enable false to RxUSoC bit being tri-stated	1	11.5	16	ns
t61	RxUAddr[4:0] Hold Time from rising edge of RxUClk	1			ns
t62	RxUClav signal valid (not Hi-Z) from first RxUClk rising edge of valid and correct RxUAddr[4:0]	2.5		8.6	ns
t63	RxUClav signal Hi-Z from first RxUClk rising edge of different RxUAddr[4:0].	2.5		8.6	ns
t58	Delay time from Read Enable false to RxUPrty bit being tri-stated	1	12	16	ns
t59	Delay time from Read Enable false to RxUSoC bit being tri-stated	1	11.5	16	ns
t60	RxUAddr[4:0] Setup Time to rising edge of RxUClk	4			ns
t61	RxUAddr[4:0] Hold Time from rising edge of RxUClk	1			ns
t62	RxUClav signal valid (not Hi-Z) from first RxUClk rising edge of valid and correct RxUAddr[4:0]	1	7.8	16	ns
t63	RxUClav signal Hi-Z from first RxUClk rising edge of different RxUAddr[4:0].	1	9.2	16	ns

12.0 ARCHITECTURAL/FUNCTIONAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - CLEAR CHANNEL FRAMER AND HIGH-SPEED HDLC CONTROLLER MODE APPLICATIONS (SEE 79L71-CC-ARC-DESC.PDF)

13.0 ARCHITECTURAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - ATM UNI APPLICATIONS (SEE 79L71-ATM-ARC-DESC.PDF)

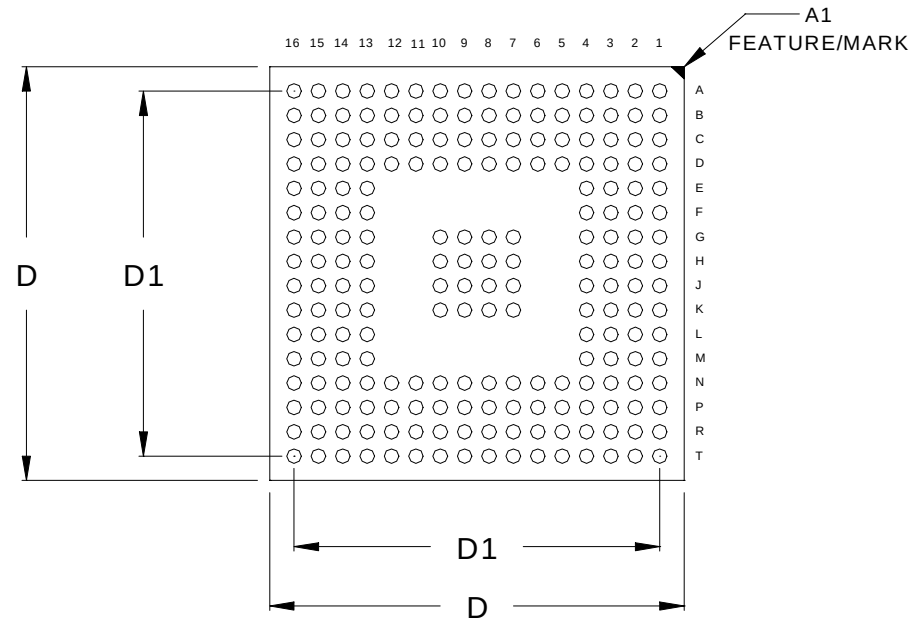
14.0 ARCHITECTURAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - POS-PHY/PPP APPLICATIONS (SEE 79L71-PPP-ARC-DESC.PDF)

ORDERING INFORMATION

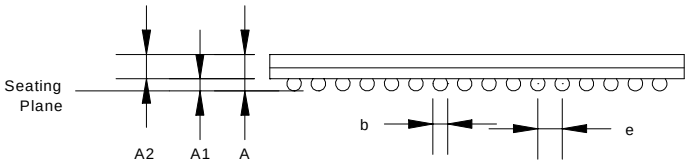
PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L71IB	17X17 mm 208 Ball Shrink Thin Ball Grid Array	-40^0C to $+85^0$C

PACKAGE DIMENSIONS

208 SHRINK THIN BALL GRID ARRAY (17.0 MM X 17.0 MM, STBGA)



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.047	0.067	1.20	1.70
A1	0.010	0.022	0.25	0.55
A2	0.031	0.043	0.80	1.10
D	0.661	0.677	16.80	17.20
D1	0.591 BSC		15.00 BSC	
b	0.018	0.022	0.45	0.55
e	0.0394 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	07/18/02	1st release of the XRT99L00 mkll.0 preliminary data sheet.
P1.0.1	02/12/03	Added package outline and pin-out diagram.
P1.0.2	05/03	Added Pin Descriptions
P1.0.3	06/03	Added Electrical Specifications and Register Information.
P1.0.4	07/03	Default Value added to Address Locations 104 and 105 in register map. Add pin TxSer (C9) to pin list. I/O Control Register (Direct Address = 0x1101, edit Bit 4 AMI/Zero Sup*.
P1.0.5	12/03	Created a Hardware Manual document.
P1.0.6	4/14	Changes and added additional description to pin list, CC, ATM, PPP and Register descriptions.
P1.0.7		
P1.0.8	10/30/05	Edit pin list.
1.0.0	06/07	Release to production and removed all TBD's.

NOTICE