AF8510C

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

■ Features

- Lower On-Resistance
- Simple Drive Requirement
- Fast Switching Performance
- Pb Free Plating Product

■ General Description

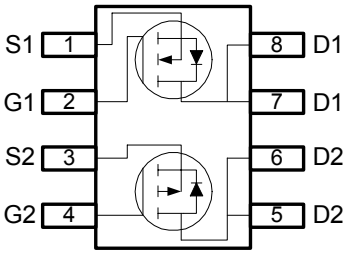
The advanced power MOSFET provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and costeffectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applicat ions such as DC/DC converters.

■ Product Summary

CH	BV_{DSS} (V)	$R_{DS(ON)}$ (mΩ)	I_D (A)
N	30	28	6.9
P	-30	55	-5.3

■ Pin Assignments

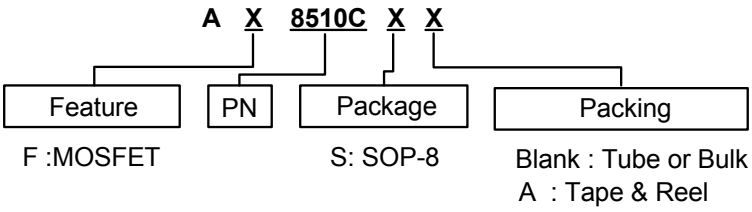


SO-8

■ Pin Descriptions

Pin Name	Description
S1	Source (NMOS)
G1	Gate (NMOS)
D1	Drain (NMOS)
S2	Source (PMOS)
G2	Gate (PMOS)
D2	Drain (PMOS)

■ Ordering information



■ Absolute Maximum Ratings

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage		30	-30	V
V_{GS}	Gate-Source Voltage		±20	±20	
I_D	Continuous Drain Current **(Note 1)**	T_A=25ºC	6.9	-5.3	V
		T_A=70ºC	5.5	-4.2	
I_{DM}	Pulsed Drain Current **(Note 2)**		30	-30	A
P_D	Total Power Dissipation	T_A=25ºC	2.0		W
	Linear Deratomg Factor		0.016		W/ ºC
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150		ºC

■ Thermal Data

Symbol	Parameter		Maximum	Units
Rthj-amb	Thermal Resistance Junction-ambient **(Note 1)**	Max.	62.5	ºC/W

■ N-CH Electrical Characteristics at T_J=25ºC unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
BV_{DSS} / T_J	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D=1mA	-	0.02	-	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance **(Note 3)**	V_{GS}=10V, I_D=5A	-	-	28	mΩ
		V_{GS}=4.5V, I_D=3A	-	-	40	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=5A	-	4.6	-	S
I_{DSS}	Drain-Source Leakage Current (T_J=25°C)	V_{DS}=30V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_J=70°C)	V_{DS}=24V, V_{GS}=0V	-	-	25	
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge **(Note 3)**	I_D=6.9A, V_{DS}=24V, V_{GS}=4.5V	-	10	16	nC
Q_{gs}	Gate-Source Charge		-	2	-	
Q_{gd}	Gate-Drain (“Miller”) Charge		-	6	-	
$t_{d(on)}$	Turn-On Delay Time **(Note 3)**	V_{DS}=15V, I_D=1A, R_G=3.3Ω, V_{GS}=10V R_D=15Ω	-	8	-	ns
t_r	Rise Time		-	7	-	
$t_{d(off)}$	Turn-Off Delay Time		-	20	-	
t_f	Fall-Time		-	6	-	
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1.0MHz	-	540	870	pF
C_{oss}	Output Capacitance		-	160	-	
C_{rss}	Reverse Transfer Capacitance		-	120	-	

■ Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward On Voltage **(Note 3)**	I_S=1.7A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=6.9A, V_{GS}=0V dI/dt=100A/μs	-	20	-	ns
Q_{rr}	Reverse Recovery Charge		-	11	-	nC

■ P-CH Electrical Characteristics at T_J=25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	-30	-	-	V
BV_{DSS} / T_J	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D=1mA	-	-0.023	-	V/°C
		V_{GS}=-10V, I_D=-5A	-	-	55	mΩ
		V_{GS}=-4.5V, I_D=-3A	-	-	90	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-5A	-	4.9	-	S
I_{DSS}	Drain-Source Leakage Current (T_J=25°C)	V_{DS}=-30V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (T_J=70°C)	V_{DS}=-24V, V_{GS}=0V	-	-	-25	
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge **(Note 3)**	I_D=-5.3A, V_{DS}=-24V, V_{GS}=-4.5V	-	9	15	nC
Q_{gs}	Gate-Source Charge		-	2	-	
Q_{gd}	Gate-Drain ("Miller") Charge		-	6	-	
$t_{d(on)}$	Turn-On Delay Time **(Note 3)**	V_{DS}=-15V, I_D=1A, R_G=3.3Ω, V_{GS}=-10V R_D=15Ω	-	10	-	ns
t_r	Rise Time		-	8	-	
$t_{d(off)}$	Turn-Off Delay Time		-	25	-	
t_f	Fall-Time		-	13	-	
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1.0MHz	-	580	930	pF
C_{oss}	Output Capacitance		-	180	-	
C_{rss}	Reverse Transfer Capacitance		-	120	-	

■ Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward On Voltage **(Note 3)**	I_S=1.7A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time)	I_S=-5.3A, V_{GS}=0V, dI/dt=100A/μs	-	21	-	ns
Q_{rr}	Reverse Recovery Charge		-	17	-	nC

Note 1: Surface mounted on 1 in^2 copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.
Note 2: Pulse width limited by Max. junction temperature.
Note 3: Pulse width ≤ 300us, duty cycle ≤ 2%.

■ Typical Performance Characteristics (N-Channel)

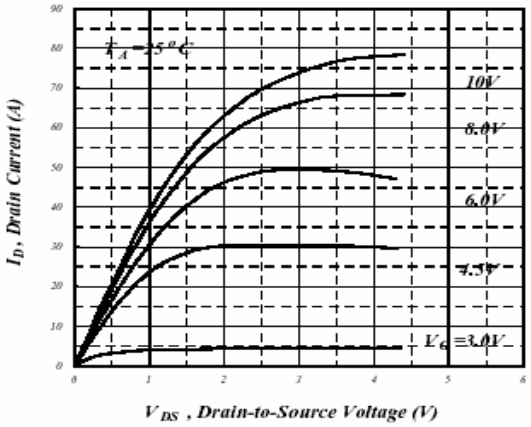


Fig 1. Typical Output Characteristics

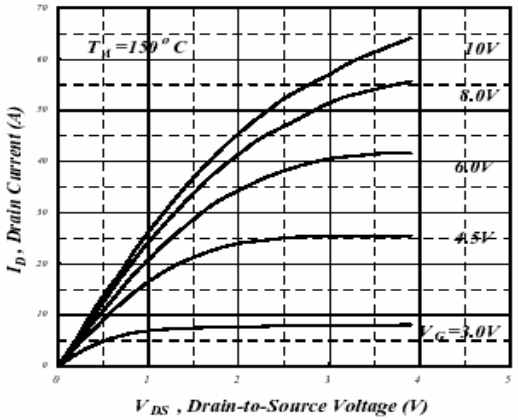


Fig 2. Typical Output Characteristics

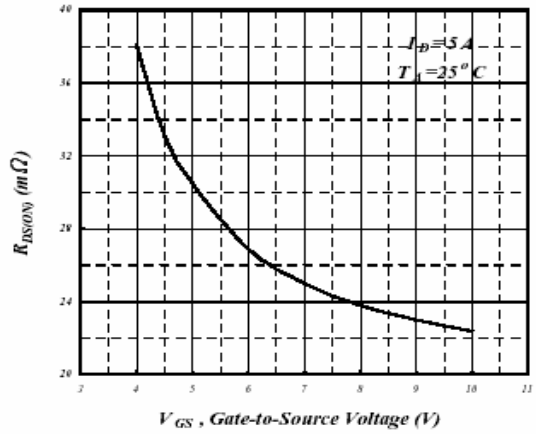


Fig 3. On-Resistance v.s. Gate Voltage

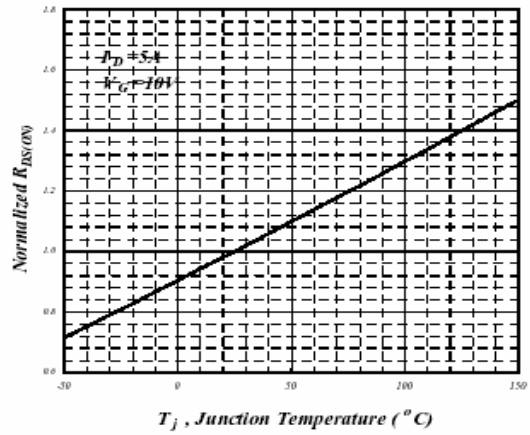


Fig 4. Normalized On-Resistance v.s. Junction Temperature

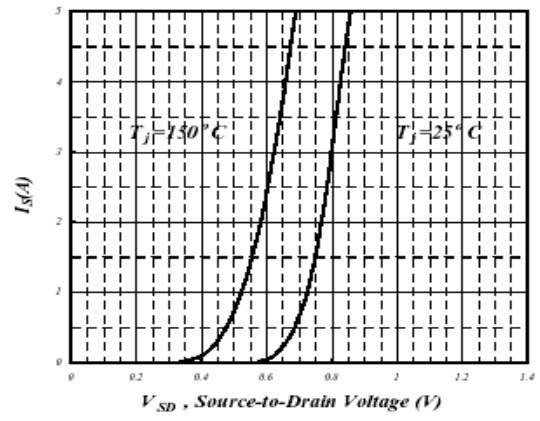


Fig 5. Forward Characteristic of Reverse Diode

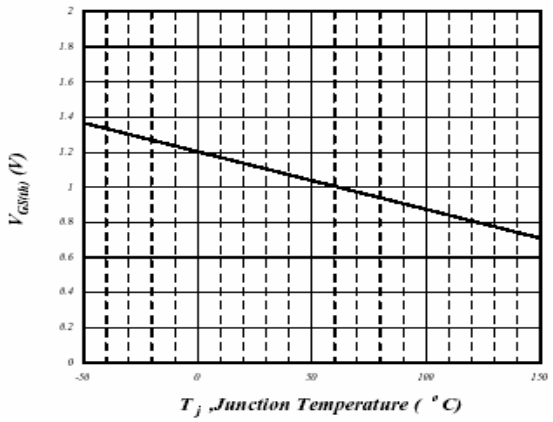


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

■ Typical Performance Characteristics (N-Channel) (Continued)

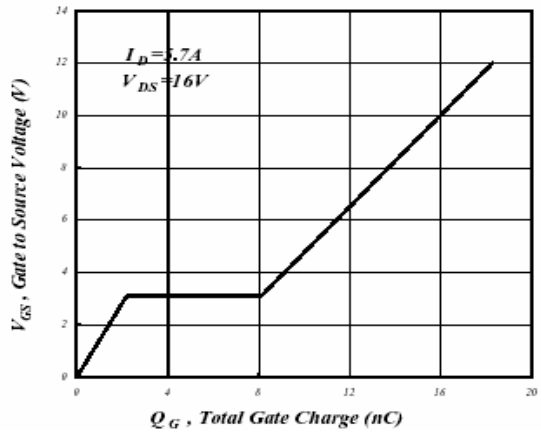


Fig 7. Gate Charge Characteristics

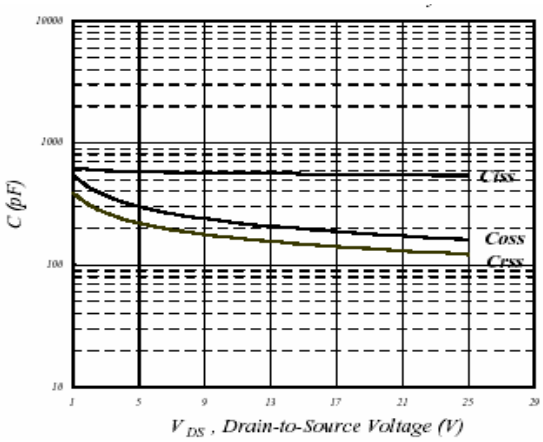


Fig 8. Typical Capacitance Characteristics

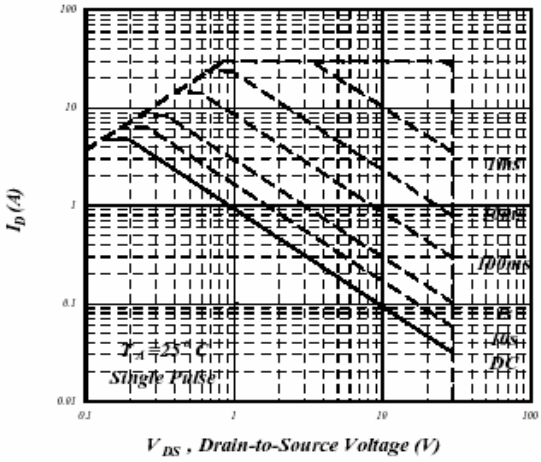


Fig 9. Maximum Safe Operation Area

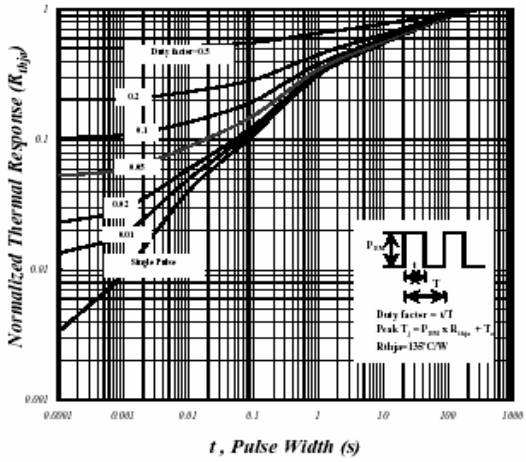


Fig 10. Effective Transient Thermal Impedance

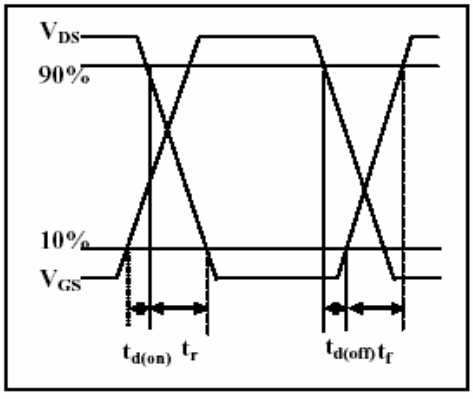


Fig 11. Switching Time Waveform

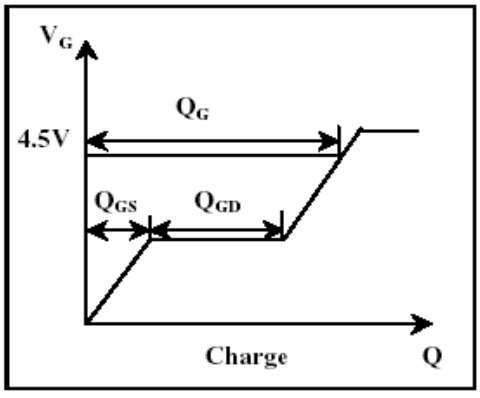


Fig 12. Gate Charge Waveform

■ Typical Performance Characteristics (P-Channel) (Continued)

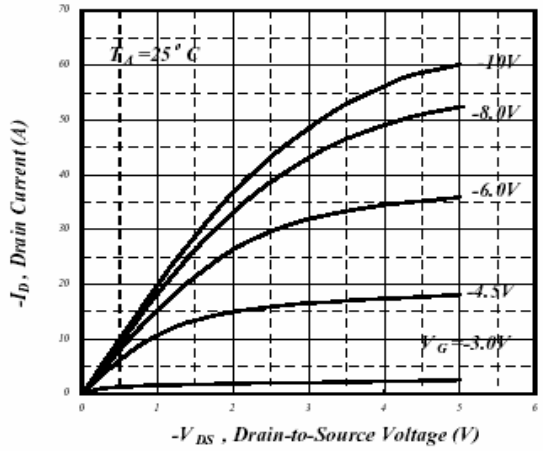


Fig 1. Typical Output Characteristics

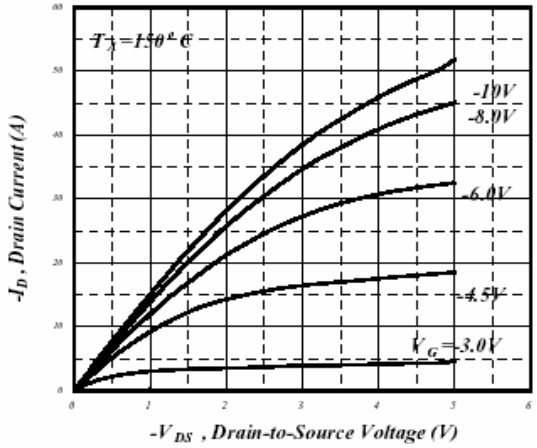


Fig 2. Typical Output Characteristics

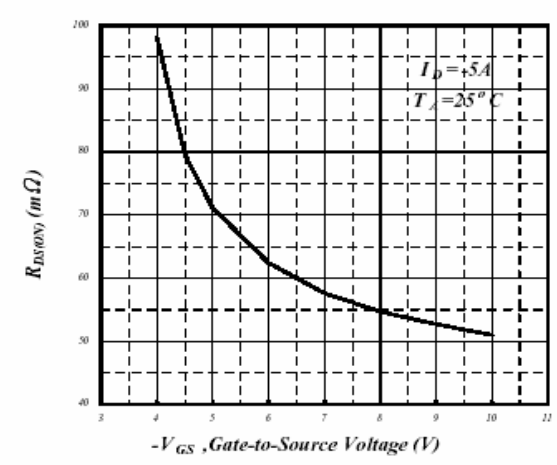


Fig 3. On-Resistance v.s. Gate Voltage

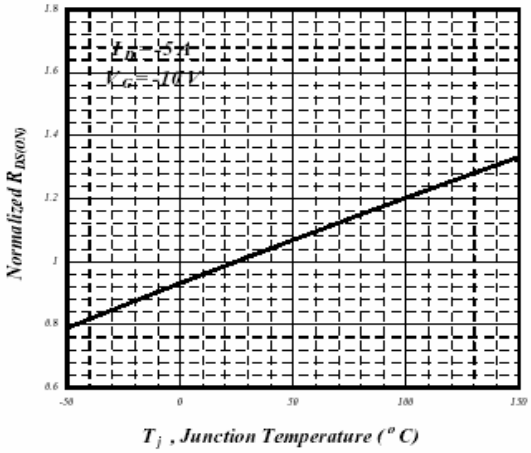


Fig 4. Normalized On-Resistance v.s. Junction Temperature

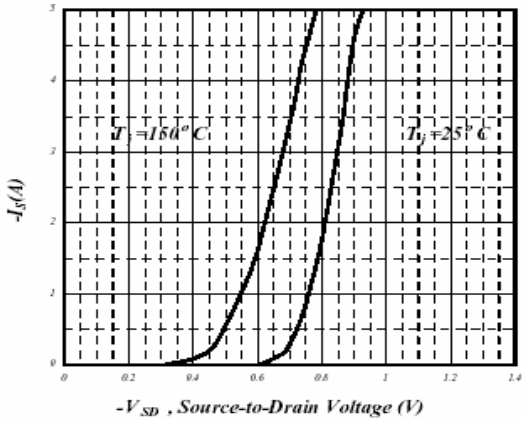


Fig 5. Forward Characteristic of Reverse Diode

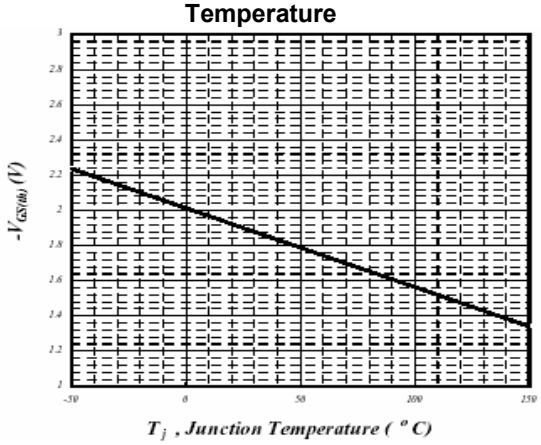


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

■ Typical Performance Characteristics (P-Channel) (Continued)

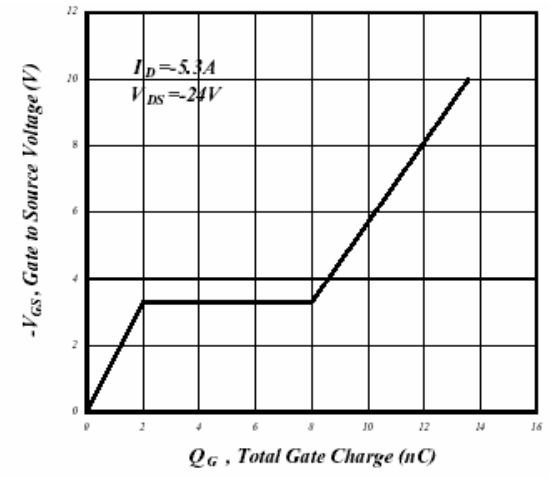


Fig 7. Gate Charge Characteristics

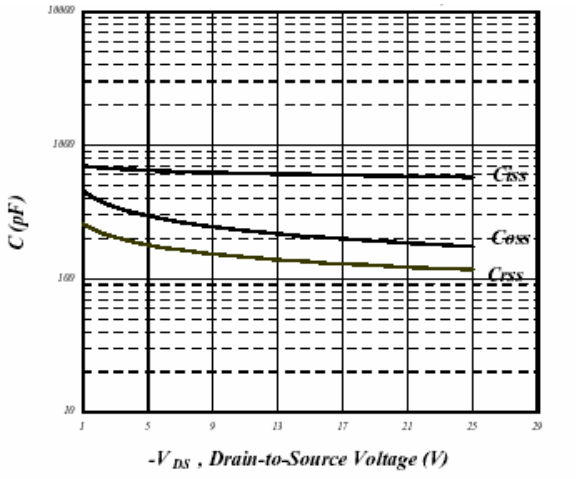


Fig 8. Typical Capacitance Characteristics

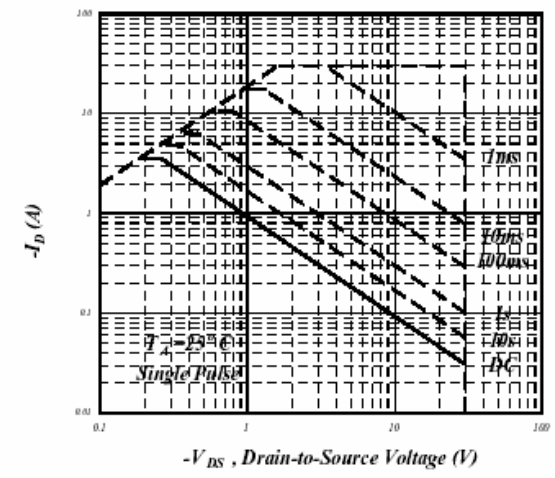


Fig 9. Maximum Safe Operation Area

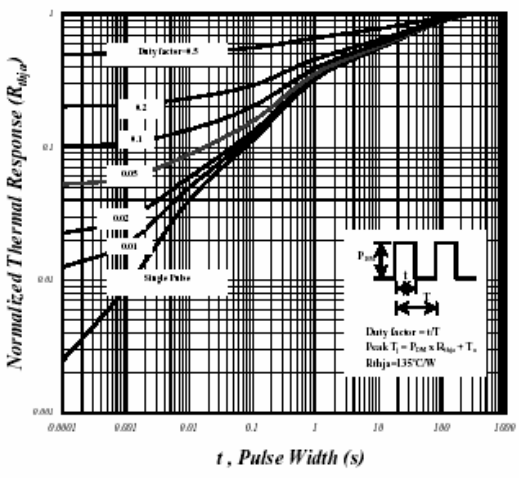


Fig 10. Effective Transient Thermal Impedance

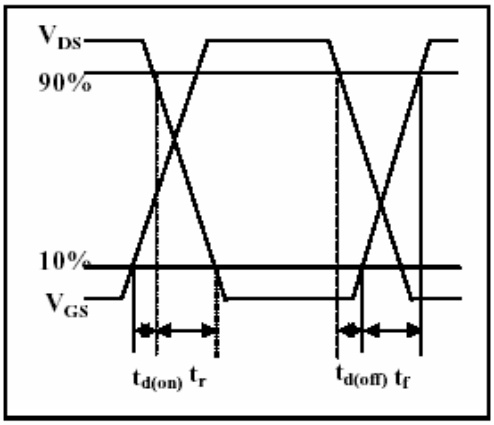


Fig 11. Switching Time Waveform

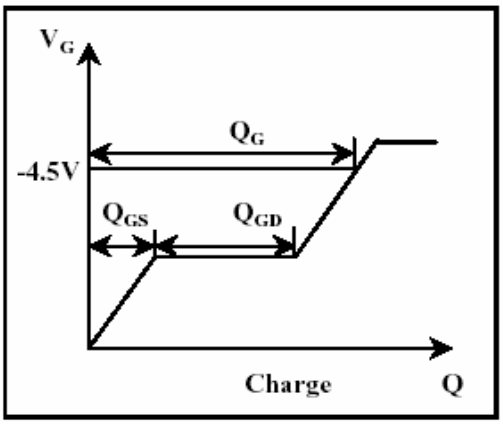
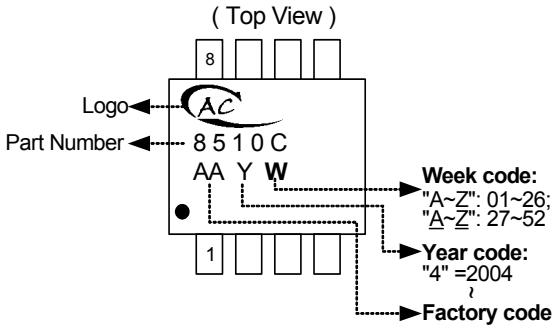


Fig 12. Gate Charge Waveform

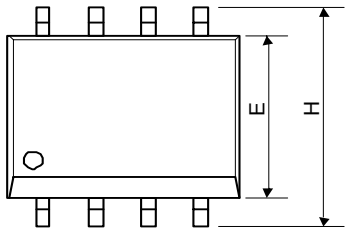
■ Marking Information

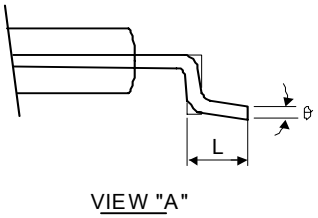
SO-8L

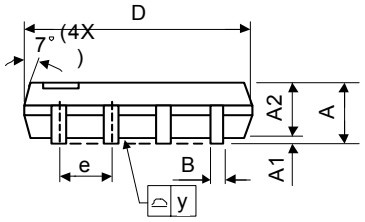


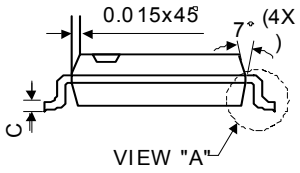
■ Package Information

Package Type: SO-8L









Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
	0^{O}	-	8^{O}	0^{O}	-	8^{O}