SGS-THOMSON MICROELECTRONICS

AN1013
APPLICATION NOTE

MONO CLASS_D AMPLIFIERS

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INTRODUCTION

The TDA7480/81/82 are single ended , split supply, class_D amplifiers. The output of the amplifier is a high frequency square wave (around 100Khz), rail to rail, with variable duty cycle.

The audio information is the average value of the output square wave.

To obtain the audio signal, the output must be low pass filtered.

The main issue of this amplifier is the very low dissipated power (the very high efficiency) compared to a normal class AB amplifier.

The preamplifier provides the voltage gain of the overall amplifier. The second stage is the power stage, with a gain 1.5, that is the high efficiency class_D amplifier.

The class_D amplifier stage is done with a multivibrator : with no signal it generates a 50% duty cycle square wave, with signal applied, it changes the duty cycle.

The switching frequency is set by the voltage on pin 9 (DIP20) or pin 6 (MW15).

The output power stage is done with N-ch DMOS power with the upper one supplied by a bootstrap capacitor (C11 in the application circuit).

1. CRITICAL COMPONENTS IN THE APPLICATION

A: Bypass high frequency filtering capacitor on supply

The most important filter capacitor is C5 (see application circuit) between pin 13/14 for MW15 package or pin 16/17 for DIP20 package.

The value of the parasitic inductance between this capacitance and the IC pins is related to the amplitude of the spikes on the power supply pins at every commutations of the output.

In fact, for any commutation, there is an abrupt variation of the current in the parasitic inductances Lpar in series to the supply. This abrupt variation increases as the output current increases and can be typically of some amperes on 10ns. With this slew rate of the current, also an inductance of about some the of nH (i.e. the lead inductance of the pin) generates voltage spikes of some volts.

Figure 1. Block Diagram

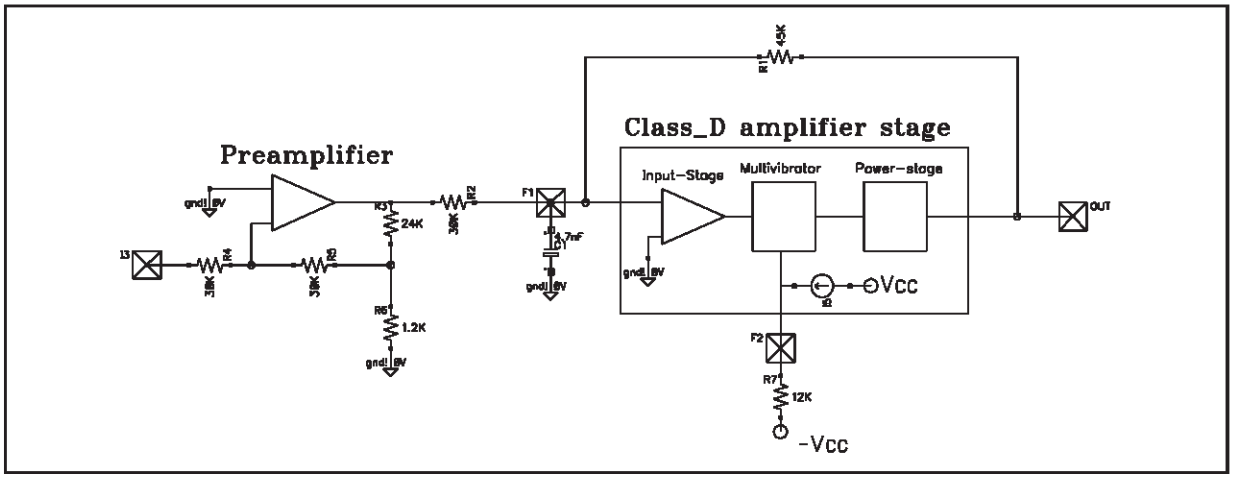
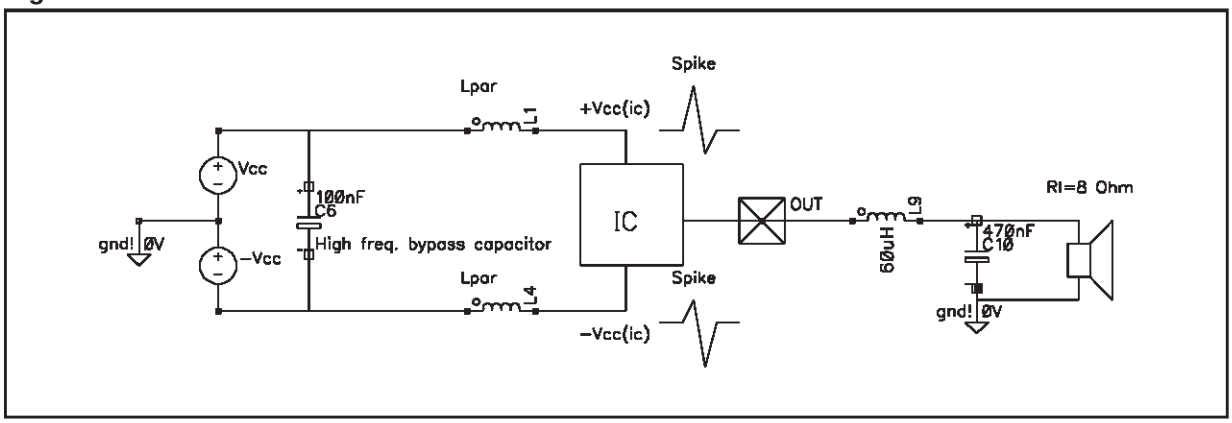


Figure 2



- The effects of these spikes are:
  Distortion / offset increase due to non linear coupling on internal elementary devices in signal circuit
- Overvoltage on the IC
- Strong noise on logic signal inside the chip, with the possibility of incertain logic levels dangerous for the IC.

To avoid this spikes generation it is mandatory to put the bypass capacitor at a distance much lower than 0.5cm from the IC pins. It is important, of course, the quality of the capacitor itself too.

- Other high frequency bypass capacitors that are important for the correct behaviour of the IC are the following:

C8 (MW15: pin6/8; DIP20: pin 9/1..3,18..20):

Again it is important the low inductance and the nearness to the IC pins.

The voltage on this pin sets the switching frequency of the IC.

The purpose of this capacitor is to filter the high frequency noise that can enter in the IC by pin 6 in MW15 or pin9 in DIP20. This high frequency noise can generate distortion/offset.

The maximum value of the capacitance that can be used, without switching frequency falls down for high frequency input signal (max 20Khz), can be calculated with this relation:

$$\frac{1}{2 \cdot \pi \cdot R4 \cdot C8} = 40KHz \qquad [1]$$

This means that C8 can be calculated as:

$$C8 = \frac{1}{2 \cdot \pi \cdot R4 \cdot 40KHz} \qquad [2]$$

For example if R4=12KΩ [switching frequency ~ 120Khz] --> C8(max) = 330pF

We suggest C8=280pF.

C4 (MW15:pin5; DIP20 pin 8):

This capacitor sets the bandwidth of the class-D amplifier [see section no.6].

It is important that the reference ground of this capacitor is as near as possible to the IC signal ground.

C3 (MW15 pin 9; DIP20 pin 11):

This capacitor filters the high frequency noise that can enter in the input and that can cause intermodulation aliasing noise at the output.

In fact no signal at frequency greater than half of the switching frequency can enter in the IC without generate aliasing noise

B: Electrolytic capacitors

The electrolytic capacitor (C7,C10 in application circuit) parameters to be considered are the following:

a. Value of the capacitance

b. Maximum operating voltage

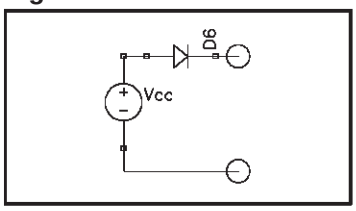
c. Series inductance/resistance at the switching frequency

c. The electrolytic capacitors supply the ripple current on the output inductance.This ripple is at switching frequency (around 100Khz). If the inductance/resistance, at the switching frequency, of the capacitor is high ,there is a strong modulation of the supply lines that can disturb every devices connected to the same supply lines.

a; b. The application of a Class_D amplifier single eneded ,split supply has the problem of modulation of the supply in low frequency operation or dc short circuit condition.

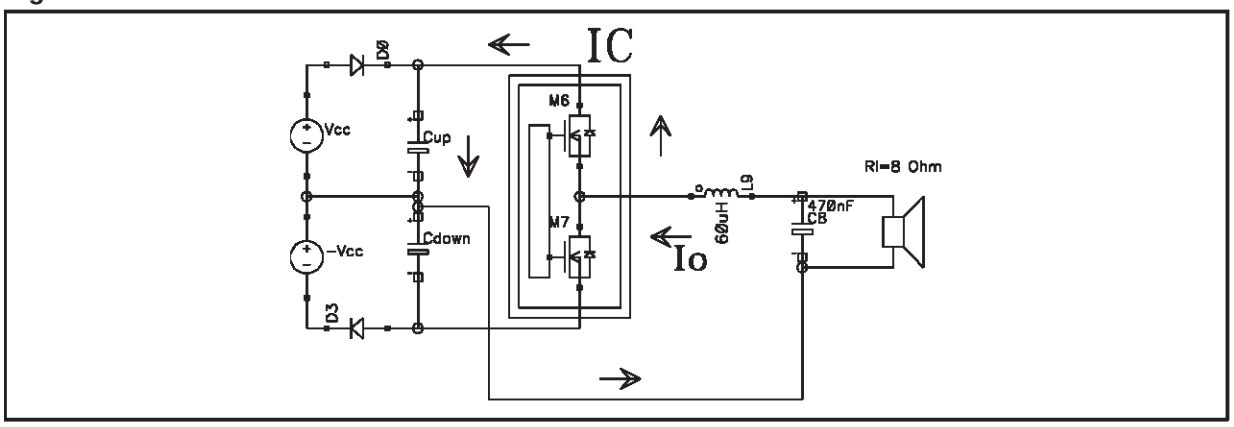
Normal power supply are able to deliver current but not to sink it.
We can figure it with an ideal supply with a diode in series (fig. 3).

Figure 3



The diode highlights the fact that the power supply cannot sink current.
The schematic of the IC in split supply is the following (fig. 4).

Figure 4



Let us suppose that the IC is sinking an average current Io from the load , as shown in the previous picture. The output duty cycle is shown in figure 5.

During the time T1 the current Io is freewheeling throught the capacitor Cup and this leads the +Vcc(IC) to increase. The freewheling current in Cup continues during all the negative sine cycle of the output. (the same problem is present in Cdown in positive sine cycle). If the signal frequency is high, the time duration of the freewheel current is small and so no deep modulation of the +Vcc(IC) is present, but in low frequency the effect occurs.
It is important to highlight that the total supply on the IC is increased by this freewheel effect. It is important, of course, to ensure that the total supply remains under the breakdown limit of the IC (60V).
The maximum supply voltage increase by freewheel is obtained when the output sine wave is around the half of the possible swing (peak to peak value =Vcc on the avaiable one of 2Vcc). In this condition a good approximation of the voltage increase can be calculated as

$$DV \approx \frac{V_{cc}}{R1} \cdot \frac{1}{16} \cdot \frac{1}{C} \cdot \frac{T_{sinewave}}{2} \qquad [3]$$

Figure 5.

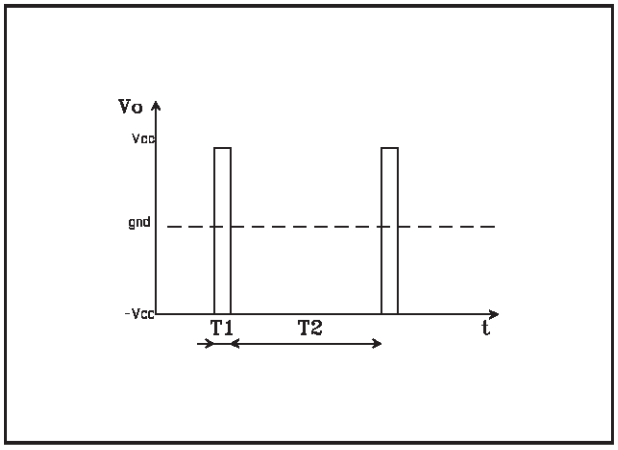
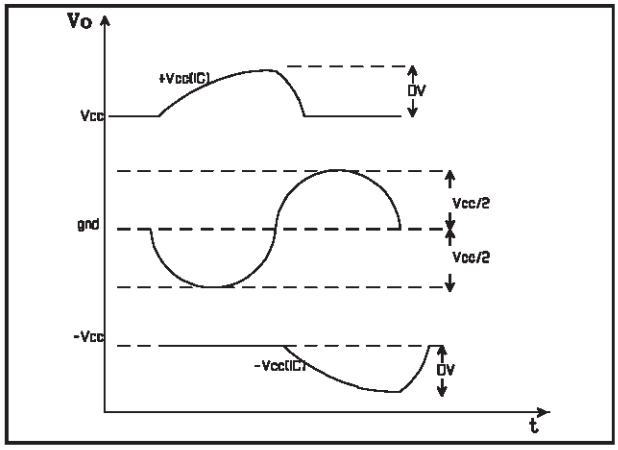


Figure 6.



For example: if signal frequency is 20hz, C = 2200µF, Rl = 8Ohm , Vcc = 20V (+-20V) from [3] the peak modulation of any supply is DV ~ 1.8V. (measured ~2V)

NOTE1 : From this formula it is clear that the IC is not able to deliver dc current without generating uncontrolled increase of the supply voltage (Tsinewave=infinite-->Dv=infinite).

This condition happens if the dc current on the load is bigger than the current sinked by the IC. For example a short circuit to gnd with the IC not supplied by any signal. In this case the offset of the IC on the short cicuit generates a dc current and so a supply voltage increase.
To avoid the sure breakdown of the IC there is an internal comparator that senses the total supply and put the IC in st-by if the total supply is over 55V (TYP)

This means that the electrolityc capacitor to be used must have the maximum operating voltage over the maximum of [55V - (Vcc)] and Vcc

To summarize the parameter of the electrolitic capacitors:

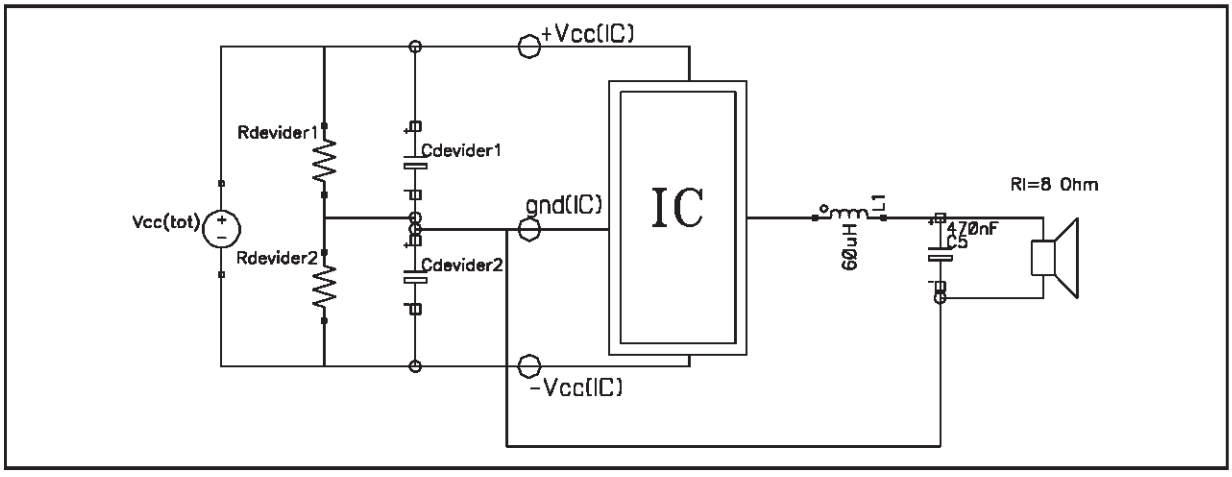
- Good ESR,ESL at switching frequency (around 100Khz)
- Value consistent with the formula [3]
- Maximum operating voltage of max[(55v-(Vcc); (Vcc)].

NOTE2 : Application in dummy split supply (fig. 7)

The circuit must be supplied with +Vcc, GND, -Vcc. The GND is half of the overall supply.

Using a single supply it is possible to obtain, by the use of a resistive/capacitive devider, the half Vcc to be used as GND. The schematic can be the following:

Figure 7



The advantage of this schematic is that it is no longer possible an increase of the overall supply (i.e. in low frequency operation or in short circuit condition) but only an unbalance between positive and negative supply (the middle of the devider is no more the half Vcc(tot))

Also in normal operation there can be an unbalance between supply.

DC operation

Due to output offset, there is a dc current that flows in the middle point of the divider GND

Iground = Output offset voltage/load resistance

So the offset of the GND respect to the half Vcc(tot) is: $DV = \frac{R_{divider}}{2} \cdot I_{ground}$

For example, with a 50mV offset, Rl = 8Ohm, Rdivider = 1KOhm the offset of GND respect to half Vcc is:

$$D = \frac{500 \cdot 50E - 3}{8} = 3.1V$$

It important to note that this GND offset increases as the load decreases (i.e. 4 Ohm)

Low Frequency operation

The impedance of GND is the following: $|Z| = \frac{1}{2} \cdot \frac{R_{divider}}{\sqrt{1 + (2 \cdot \pi \cdot f \cdot R_{divider} \cdot C_{divider})^2}}$

For example, with Rdevider = 1KOhm and Cdevider = 2200uF, the GND impedenceat 20 hz is around 1.8Ohm. Because the GND sinks all the current load, this means that ,with 8 Ohm load, on the GND at 20hz there is a modulation of about 1/4 of the output signal.

2. OUTPUT FILTER

To demodulate the pwm signal and obtain the audio signal, it is enought apply a low pass filter at the output of the amplifier. Of course this filter must not dissipate power. Typical solution is one or more LC cells in series.

For example, we can consider the case of one only cell at the output (fig 7)

The design of the LC filter must take into account the following parameters:

- Voltage ripple on the load
- Q factor of the LCR filter
- Inductance core : linearity and saturation
- Current ripple in the inductance

Voltage ripple and Q factor

The cut off frequncy of the LC filter is: $F_t = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$ [4]

For example, with the value suggested in the application circuit, L = 60uH, C = 470nF, the cut-off frequency is Ft = 30Khz.

After this frequency the slope of the Bode diagram is -40 dB/decade.

It is better to fix the cut-off frequency outside the audio bandwidth to avoid the peaking or overdamping of the LCR filter (the speakers impedance is not purely resistive) inside the audible frequency.

The maximum flat filter is load dependant.

To obtain it , it is important fill the following relation: $\frac{1}{2 \cdot \pi \cdot F_t \cdot R1 \cdot C} = \sqrt{2}$ [5]

From [5] it is clear that, fixing the cut-off frequency Ft, for a given load, there is just one value of capacitance C to be used to obtain the maximum flat filter. Then from the [4] we find L.

So, for any load impedance Rl, there is just one maximum flat filter for any cut-off frequency chosen. From [4] and [5] we can obtain the value of L and C as :

Figure 8

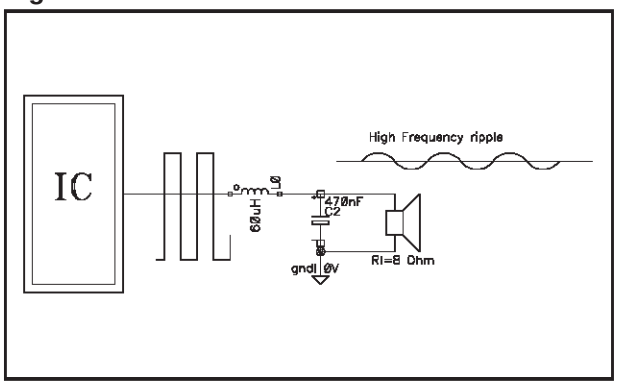
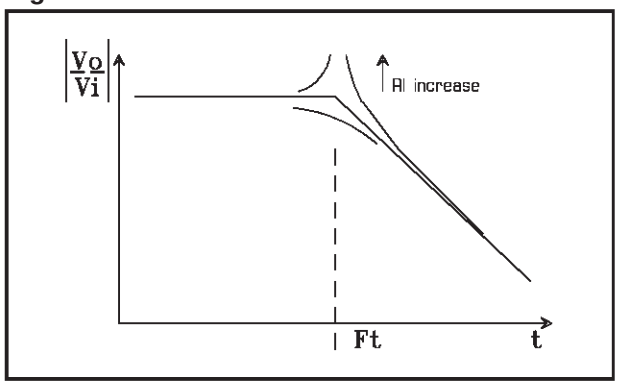


Figure 9



$$C = \frac{1}{2 \cdot \pi \cdot F_t \cdot R1 \cdot \sqrt{2}} \qquad [6] \qquad L = \frac{1}{4 \cdot \pi^2 \cdot F_t^2 \cdot C} \qquad [7]$$

For example, for Rl=8Ohm and Ft=30Khz, we can obtain, using the [6] [7] , the following values of L and C:

[6] --> C = 469nF; [7] --> L = 60µH

If the switching frequency is set at 120Khz the voltage ripple at the switching frequency on the 8 Ohm load, at ±20V, with L=60µH, C=470nF, is Vripple ~ 2V (the amplitude of the ripple is proportional to the Vcc). The ripple is not audible (~100Khz) and usually is not a problem. If it is, the solution is to add one or more LC filter cells at the output of the IC.

Inductance core

The core permeability has: hysteresis, not linearity, saturation. The hysteresis produces losses in the core. These losses affect the overall system efficiency but not, at first order, the dissipated power of the IC. A high losses core generally produces an increase of the bias current. The non linearity of the permeability with the increase of the magnetic field deteriorates the THD, usually the 3^ order harmonic, but not the sound quality because it is a low order harmonic.
Saturation of core can be dangerous because, for high current, it can transform the inductance in a short-circuit with all the risks related to this situation.

Current ripple

As first approssimation the peak value of the current in the inductance is (in no signal condition):

$$I_{ripple} = \frac{V_{CC}}{L} \cdot \frac{T}{2} \cdot \frac{1}{2} \qquad [8]$$

The decrease of the inductance value generates an increase of the ripple current in the inductance. For example with a switching frequency of 100Khz and +/-20V supply, the peak current ripple are the following:

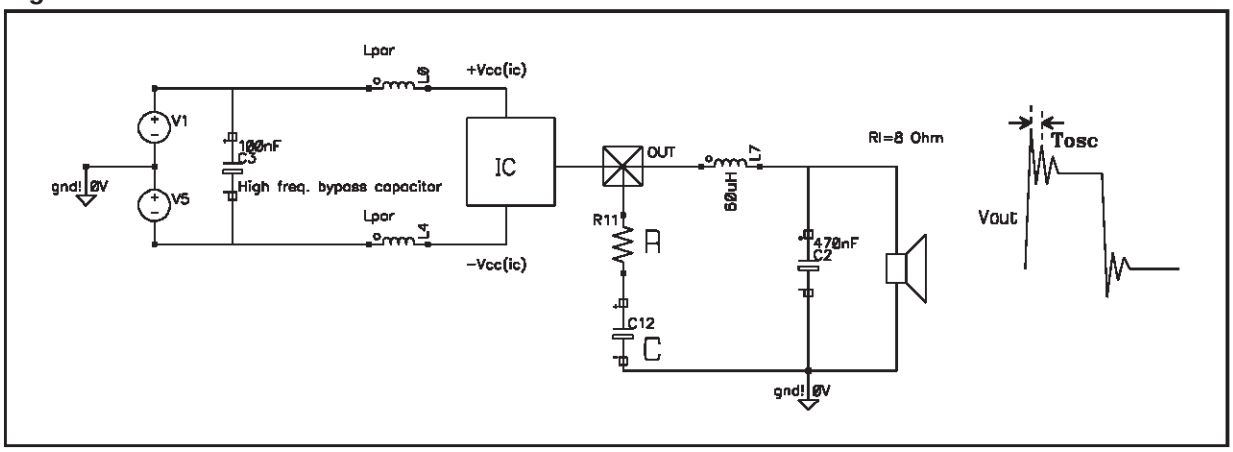
= 60µH; Iripple = 0.83A
= 30µH; Iripple = 1.66A

(i.e. L=60µH is the inductance of the maximum flat filter for 8Ω load with a cut off frequency of 30Khz (C=470nF); L=30µH is the inductance of max flat filter for 4Ω load with cut off frequency of 30Khz (C=940nF). It is important to note that the ripple current must stay under the threshold of the short circuit protection (see data-sheet). The increase of the inductance over the maximum flat filter value, generates an overdumped filter frequency responce (see fig. 8) and an anticipated dead zone step (see section 5)
.

3. SNUBBER

The snubber must be chosen to dump the overshoots produced at each commutation. To reach this goal, it is important that the snubber impedence seen by the circuit at frequency of the overshoot is resistive. The smaller is the resistance, the higher is the dumping produced by the snubber and so the smaller are the overshoots (but the losses on the snubber increases).

Figure 10



If Tosc is the period of the overshoot, the snubber must fit this relation (impedance at overshoot frequency: resistive):

$$\frac{1}{2 \cdot \pi \cdot R_{11} \cdot C_{12}} < \frac{1}{T_{osc}} \qquad [9]$$

The power dissipated by the resistance of the snubber, on average, can be approximated as:

$$P_{snub} = \frac{V_{CC}^{\ 2}}{R} \cdot \frac{DT}{T} \qquad [10]$$

where DT is the commutation time of the output.

For example, let us assume Vcc = 20V (+-20V),Tosc =300ns, R = 150Ω, Dt=50ns, T = 8.3µs (Freq. switching = 120Khz). In this case the capacitance to be used is (from [9]) C >318pF (i.e. in the application circuit: C = 560pF).

The power dissipated by the resistance of the snubber is (from [10]) Psnub ~ 16mW.
This is a very 'soft' snubber.

The strongest snubber that can be used to cut overshoot at frequency higher than about 2Mhz with 1/4W resistance , switching frequency 120 Khz and Vcc = 20V (+-20V), is:

R = 10Ω (1/4 W), C > 8nF (i.e. 12nF)

5. THD: SWITCHING FREQUENCY CHOICE

The THD of a class_D amplifier is due mainly to :

- Dead zone to avoid cross-conduction in the power stage
- Parasitic coupling of spikes in the signal circuit
- Non linearity of the modulation process
- Aliasing of the PWM spectrum inside the audio bandwidth
- The aliasing of the pwm spectrum inside the audio bandwidth is present for high frequency signal applied to the IC. For a switching frequency of 120 Khz no sensible aliasing was measured for input signal up to 20 Khz.

It seems enough to ensure good performance for audio signal. The eventual increase of the switching frequency improve this figure but worsens the efficiency and the dead zone distortion and makes the operation of the power stage more difficult.

We suggest a switching frequency between 110 -150 Khz.

The resistance R4 (pin 9 DIP20, pin 6MW15) set the switching frequency of the internal multivibrator. The relation is :

$$F_{sw} = \frac{Bf}{R4} \qquad (Bf = 1.4E9\ Hz\ Ohm) \qquad [11]$$

(i.e. : for R4 =12KΩ ---> Fswitching ~ 120Khz

- The non linearity of the modulation process is not a big problem . This generates low order harmonics easily lowered by the feedback.
- The parasitic coupling of the spikes is the most difficult problem to be solved.

At every commutation of the power stage it is produced high frequency noise on substrate and supply lines. This high frequency noise is almost made of a train of very sharp (nanosecons) spikes of some volts repeated at the switching frequency.

The spikes are coupled to the signal circuits via substrate and supply. Typically this coupling is not linear and the average result is an increase of offset and THD.

- The power stage must not cross-conduct. To avoid this there must be a dead time between the turn off and turn on of the power mosfet. This dead time generates a distortion with a harmonics distribution similar to the cross-over of a normal class AB amplifier.

The overall energy of this distortion can be roughly calculated , in open loop, as:

THD (dead zone, open loop) = Dead time*Fsw [12]

For example, with a dead zone of 60ns (the typical ICdead zone) and Fsw=120Khz, the dead zone THD, in open loop, is about 0.7%. This value is lowered by the loop.

Note that this THD increases as the switching frequency increases.

The harmonic distribution of this distortion is extended also to high order harmonics.
The typical shape of the THD vs Pout of a class-D amplifier is the following:
The Dead zone step of the THD vs Pout plot happens when the average output current Io is greater than the ripple current Iripple. From this point of wiew the ripple current has a role similar to the bias current in a class-AB amplifier: the higher is the ripple current (the bias current in AB stage) the lower is the dead zone distortion (the lower is the cross-over distortion).

6. FEEDBACK LOOP

A simple 1^ order loop is used to reduce the THD. To calculate the loop gain of the amplifier ,we can assume the Class_D amplifier like a normal operational amplifier if we consider the average of the pwm output instead of the instantaneus value.

The feedback network to be considered is the following (fig. 12)

Figure 11

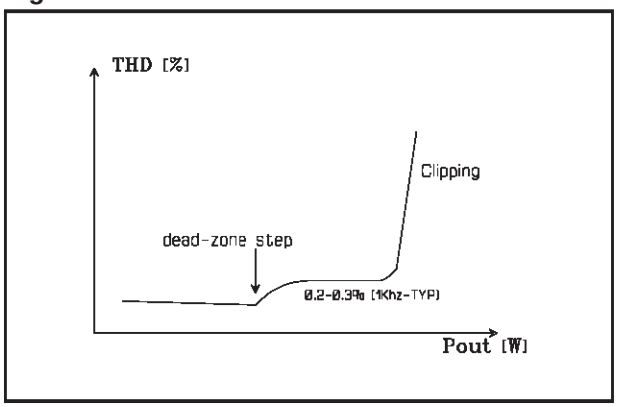


Figure 12

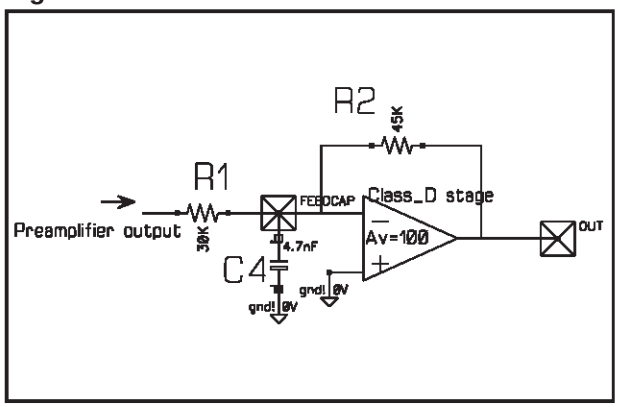
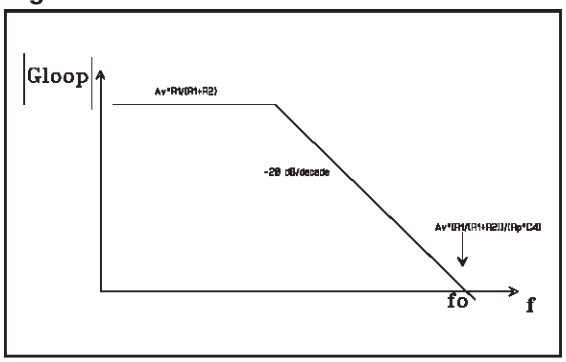


Figure 13



The loop gain of this configuration is the following (fig. 13)

The feedback works properly only if fo (unity-gain frequncy) is lower than the switching frequency fsw.

The optimum behaviour is obtained with fo ~ 0.7fsw. For example, with fsw =120Khz, the capacitance C4 (pin 8 DIP20, pin 5 MW15) is about 4.7nF.

If the switching frequency is changed, the C4 capacitance can be changed too to fit the following formula:

$$\frac{\frac{1}{2 \cdot \pi} \cdot A_V \cdot \frac{R1}{R1 + R2}}{R_p \cdot C4} = 0.7\ fsw \qquad [12]$$

From [12] it is possible to calculate the value of C4 vs switching frequency fsw:

$$C4 = \frac{\frac{1}{2 \cdot \pi} \cdot A_v \cdot \frac{R1}{R1 + R2}}{R_p \cdot 0.75 \cdot F_{sw}} \qquad [13]$$

where:

R1 = 30KΩ; R2 = 45KΩ;

$$R_p = \frac{R1 \cdot R2}{R1 + R2} = 18K\Omega$$

Av = 100;

fsw : switching frequency

With these values in [13], it is possible to obtain the final formula of C4 vs fsw to be used:

$$C4 = 5.05E{-}4\ \frac{F \cdot 141.414hz}{fsw} \qquad [14]$$

For example, with fsw =120Khz, with [14] C4 = 4.2nF.

A.1) Output LC filter dimensioning

The low pass filter placed after the switching stage is dimensioned to eliminate the high frequency PWM waves and to feed the Audio signal to the loudspeaker.

The TDA7480/81 operate at a switching frequency of 120Khz, the LC low pass filter suggested in the application circuit is a typical 2 pole Butterworth designed to have a cutoff frequency outside the Audio band (fc = 30KHz).

This filter topology was chosen because it offers the feature to be maximally flat in the passband.

The filter frequency response will be flat only if it is properly loaded on the specified

loudspeaker impedance for example 8 ohm (fig.14),

Figure 14

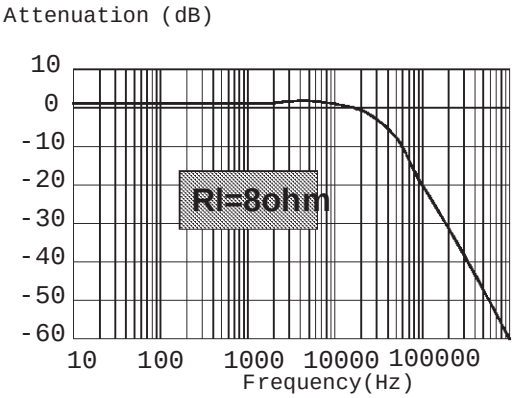
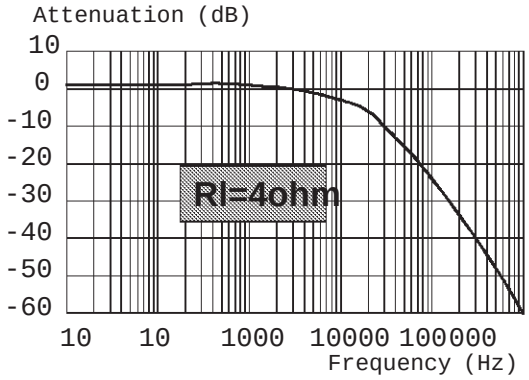


Figure 15



if a 4Ω loudspeaker was used without changing the filter components values, a high frequency loss would be caused (fig.15), otherwise if a 16Ω loudspeaker was used, an high frequency peaking would be caused (fig.16).

Figure 16

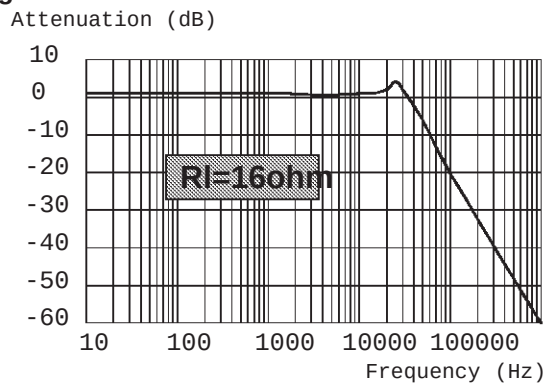
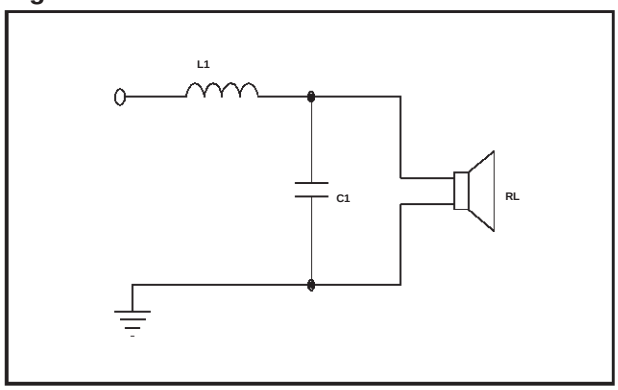


Figure 17



Class-D Amplifier TDA7480/81/82

Appendix to the Application Note

As explained, it is quite important to correctly dimension the filter components value to obtain the best performances from the application.
In the following section suggestions will be given for the right dimensioning. information

2 Pole Butterworth filter: (fig.17)

To avoid Underdamped or overdamped behaviour of the filter (fig.18) the amount of the ratio of inductance to capacitance Q (quality factor) Q= Rload $\sqrt{C/L}$ should be chosen between $0.6 \leq Q \leq 0.8$, in our application we used Q = 0.707 as god compromise that takes in account the impedance variation in real loudspeakers.

The equations to be used to calculate the filter components values are the following:

$$L = \frac{1.414 \cdot Rload}{2\pi \cdot F_c} \quad [1] \qquad C = \frac{0.707}{2\pi \cdot F_c \cdot Rload} \quad [2]$$

where: Fc=Cutofffrequency(30KHz;Rload=Loudspeakerimpedance)

Example: Fc = 30KHz, Rload = 8ohm

$$L = \frac{1.414 \cdot 8}{2\pi \cdot 30 \cdot 10^3} = 60\mu H \qquad C = \frac{0.707}{2\pi \cdot 30 \cdot 10^3 \cdot 8} = 0.47\mu F$$

Figure 18. Effect of inductance and Capacitance on Damping

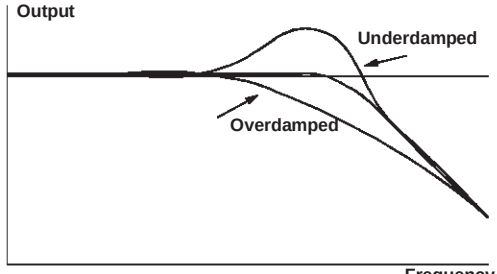


Fig.4
Effect of Inductance and Capacitance on Damping

If a sharper cutoff is preferred, to attenuate better the carrier frequency Butterworth filters of the 3rd or of the 4rth order could be used.

For example with a 3rd order filter (fig.19) the obtained frequency response is shown in fig.20.

The equations used to domension the passive components are the following:

$$L1 = \frac{0.5 \cdot Rload}{2\pi \cdot F_c} \qquad L2 = \frac{1.5 \cdot Rload}{2\pi \cdot F_c} \qquad C1 = \frac{1.33}{2\pi \cdot Rload \cdot F_c}$$

For Rload = 8ohm, Fc = 30Khz resulted L1 = 20µH, L2 = 63µH, C = 0.88µF

Figure 19

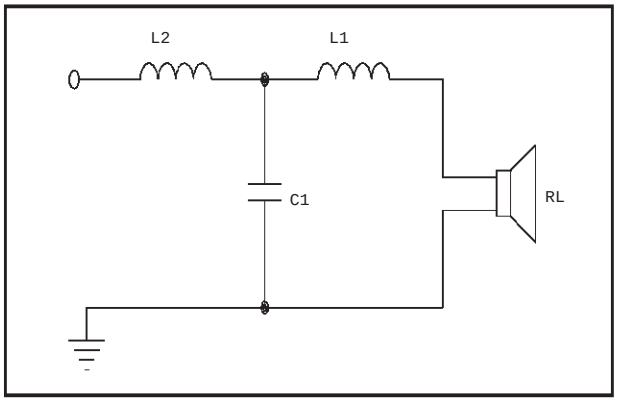
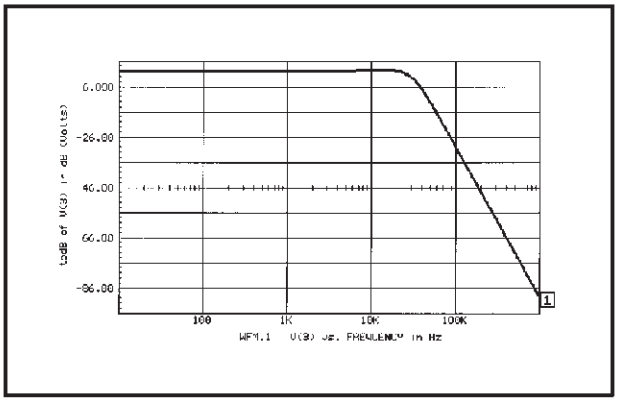


Figure 20. 3rd order Butterworth filter



Components choice:

Not only the right choice of the LC network values is important, but it is also the type of the passive components in the Class-D amplifier performances evenmore in terms of Losses and Harmonic distortion.

CAPACITOR: The losses in the filter capacitor due essentially to the ESR will be neglegible if Multilayer film capacitors are used. Multilayer Mylar, Polypropilen or Policarbonate film capacitors are the recomended choice, we advise to avoid using ceramic capacitors for such kind of application.

INDUCTOR: The losses in the inductor at low frequencies are mainly due to the coil winding series resistance. At higher frequencies, where the Skin Effect becomes of importance, a multiwire winding could be effective to obtain the maximum in terms of efficiency. However for most of the applications the use of a single wire winding with adequate cross section is enough.

The inductor used for the filter must sustain a DC current greater than the specified current limitation value (see the datasheet of the device of interest for the value to consider) without saturation and the coil material must show very low hysteresis losses.

To verify the linearity of the inductor, it's suggested to verify that the inductance change versus load current be less or equal than 10%.

Also the harmonic distortion is affected by the coil material.

The suggested coil materials are:

a) Ferrites: Gapped ferrites are suitable for this kind of application because they allow to counter frequency heating and distortion problems.

The shapes of the coil we suggest are E cores, RM and PM. The Ferrite material to use could be one of the following or others with similar characteristics (see the producers technical sheets for the details):

THOMSON - LCC	:	B50, B51
SIEMENS	:	T26, N27
PHILIPS	:	3C8
TDK	:	H7C1, H5B2, H7A

A cheap Ferrite solution consists of Radial Lead Inductors that are easy to find already wound (i.e TDK, Ferroxcube...). These inductors offer a good compromise in terms of features and cost but its important to verify the max. rated DC current they can sustain .

b) Molypermalloy (Magnetics): This is the coil we mount in our application board, due to the Toroidal shape that improves the RFI characteristics of the application.

This material, however, shows a little worse (though neglegible for this application) behaviour in terms of losses due to hysteresis, has the advantage of the distributed gaps that significantly lower the effective permeability and increases the energy storage capability reducing also the radiated magnetic field as a result of the elimination of the discontinuity associated with discrete air gap.

c) Ferrite powder cores: although also these material could be used for this kind of application it shows the worse behaviour in terms of heating and losses.

A.2) Selecting supply filter capacitors:

Referring to the application note section B results that the factors to take in account for the electrolytic filter capacitors selections concern:

- RMS ripple current rating
- Ripple voltage
- Voltage rating
- ESR

Considering these factors the electrolytic filter capacitors would show electrical characteristics as follows (for Vcc = +/-20V, Pout >20W):

- Rated voltage 50V
- Rated current > 1A
- Impedance at 20C/f = 100KHz < 100mΩ

A list of possible choices drawn from some of the major capacitors producers catalogs is the following:

ROEDERSTEIN:			
Type	**Capacitance (50V)(μF)**	**Impedance (Ω) 20C/100KHz**	**Rated Current (mA)**
EKC	1000	0.039	2150
EKE	1000 2200	0.060 0.037	1570 2270
SANYO:			
CG	1000 2200	0.072 0.045	1200 1400
MV-GX	1000 2200	0.046 0.029	1100 1900
NIPPON CHEMI-CON:			
SXE	1000 2200	0.049 0.034	1830 2460
LXF	1000 1500	0.030 0.024	1720 2070

Clearly this list must be taken only as example of the capacitors suitable for this kind of application,