

QuickChip Design Example 2 Low Power Silicon BJT LNA for 1.9GHz

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Abstract

A two-stage 1.9GHz monolithic low-noise amplifier (LNA) with a measured noise figure of 2.3dB and an associated gain of 15dB was fabricated in a standard silicon bipolar transistor array. It dissipates 5.2mW from a 3V supply including the bias circuitry. Input return loss and isolation are -9dB and -20dB, respectively.

I. Introduction

In portable communication equipment, such as cellular phones and digital cordless phones, manufacturers are trying to replace as many discrete devices as possible with high-density ICs to be competitive in size, weight, power dissipation, and price. In a number of recent papers low power LNAs for S-band have been described [1,2,3]. These LNAs were fabricated using some sophisticated GaAs full-custom processes. Since the high frequency performance of state-of-the-art silicon bipolar processes are continuously improving lowcost semi-custom arrays with a limited choice of components provide a reasonable solution for RF applications.

In order to demonstrate such a solution, we present in this letter a very low-power monolithic 1.9GHz silicon LNA which draws a total current of 1.75mA including bias circuit.

II. Circuit Design

A schematic of the two-stage LNA is shown in **Fig. 1**. The circuit employs a high-gain common-emitter stage (Q1-RL) and a emitter-follower output stage (Q2-Q3). This approach eliminates the need for coupling capacitors. The current of the first stage is set by a resistive parallel feedback (R3 and R4), which is connected to the external matching inductor (L1) such that no noise degradation occurs. Thus, only a single supply voltage is required. This feedback also improves both the bias and RF stability of the amplifier.

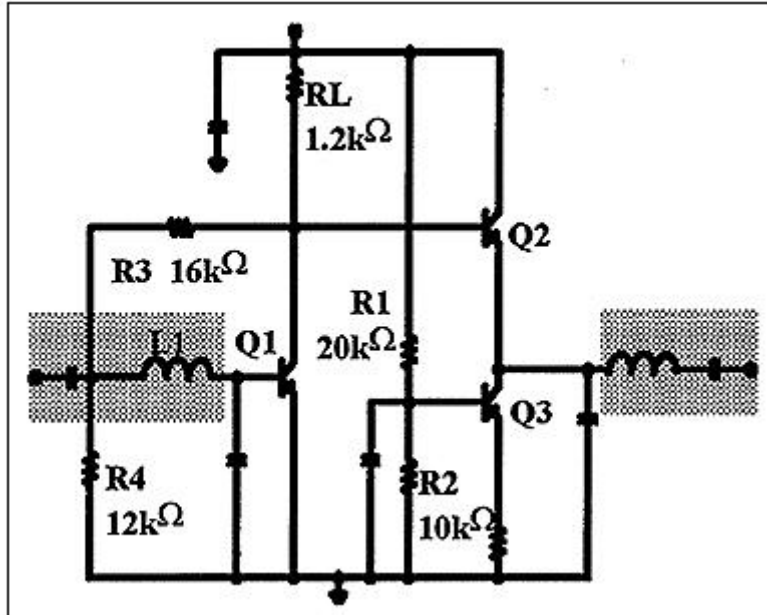


Figure 1. Simplified schematic of the LNA (gray area: off-chip matching)

The circuit was simulated with Spice and with a linear simulator based on measured S- and noise parameter data of the active device. Good agreement between simulated and measured performance is found as shown in Fig. 2.

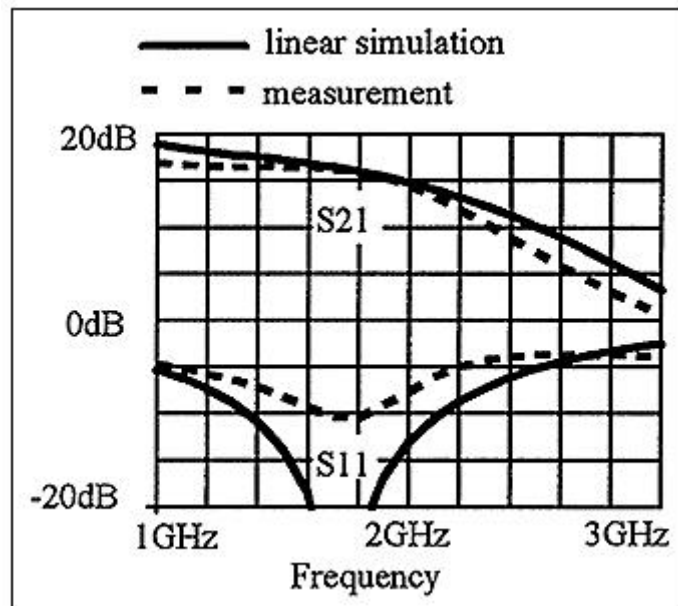


Figure 2. Simulated vs. measured gain and input return loss

III. Measurements

The circuit was fabricated on a "Quickchip" transistor array with the Maxim GST-2 foundry process. **Fig. 3** shows the gain and noise figure of the circuit measured with the HP8970B/HP8971C noise figure meter. The amplifier shows a rather flat frequency response of the noise figure from 700MHz up to 2GHz. The best 50W noise figure of 2.3dB is achieved between 1.7 and 2.3 GHz. Note that the active device has a minimum noise figure of 1.5dB at 1.9GHz.

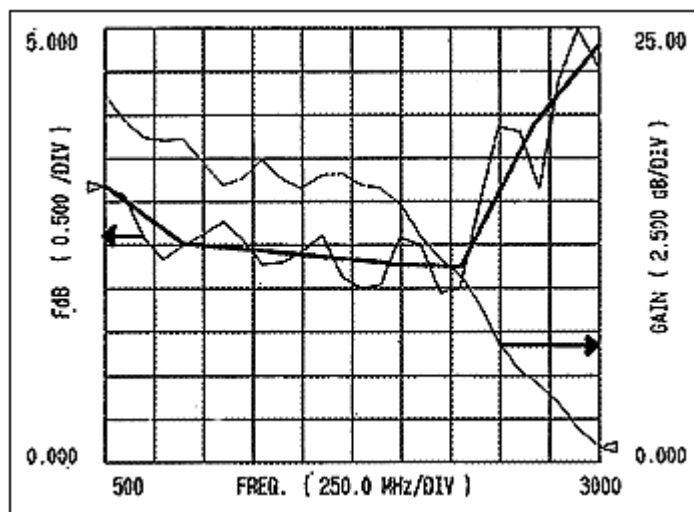


Figure 3. Measured gain and noise figure ($V_{CC} = 3V$, $I_{CC} = 1.75mA$ (bold line: average noise figure))

The small signal gain is larger than 15dB up to 2GHz at the nominal bias of 3V. The corresponding gain/DC-power figure of merit is 2.9dB/mW. Compared to other L-band LNAs, this design shows low power consumption and a competitive noise figure as seen from **Fig. 4**.

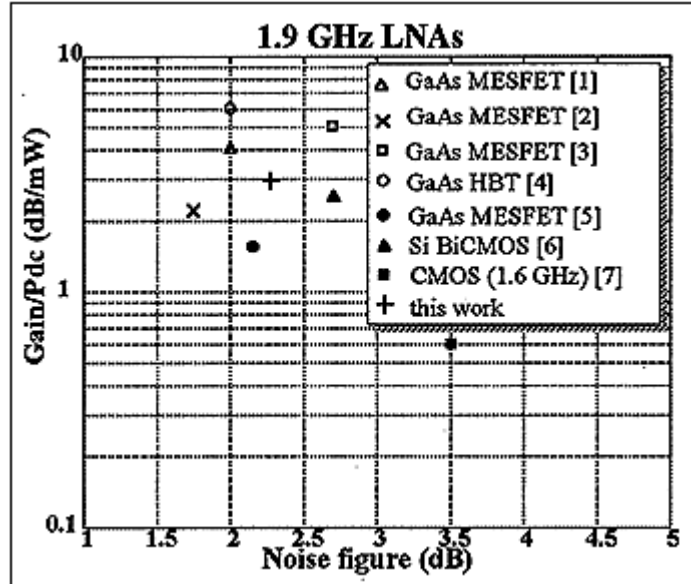


Figure 4. Gain to DC power ratio plotted versus noise figure for several state-of-the-art L- and S-band LNAs

The noise figure is also quite insensitive to bias voltage variations. Varying the supply voltage from 2.7 to 5V the noise figure remains between 2.2 and 2.5dB.

The designed amplifier has a measured -1dB input compression point of -24dBm, which equals an output compression point of -9dBm. The third order intermodulation intercept point is measured at -21dBm input power. This is adequate for DECT handheld terminal.

Fig. 5 shows a photograph of the lower right part of the 1.9 x 1.8mm² large chip containing the LNA. In Fig. 6 the chip can be seen as mounted on the substrate and bonded to the printed input and output matching inductors.

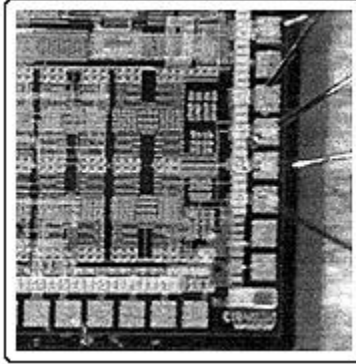


Figure 5. shows a photograph of the lower right part of the $1.9 \times 1.8 \text{ mm}^2$ large chip containing the LNA. In Fig. 6 the chip can be seen as mounted on the substrate and bonded to the printed input and output matching inductors.

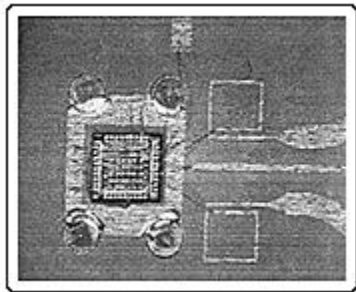


Figure 6. Photograph of the Quickchip mounted on the test substrate. On the right are the printed inductors for input and output matching.

IV Conclusions

A silicon bipolar low power LNA for 1.9GHz has been designed and tested. It shows a noise figure of 2.3dB along with a 15dB gain. The power consumption is only 5.2mW resulting in a high gain/DC-power figure of merit of 2.9dB/mW. The design was done on a transistor array showing almost no performance degradation relative to full custom design.

V Acknowledgement

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References

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