32-bit Secure Microcontrollers

AT91SC 192192CT-USB Summary

Features

General

- Based on the ARM® SC100™ SecureCore™ 32-bit RISC Processor
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb® High-code-density 16-bit Instruction Set
- Von Neumann Load/Store Architecture
  - Single 32-bit Data Bus for Instructions and Data
- 3-stage Pipeline Architecture
  - Fetch, Decode, and Execute Stages
- 8-bit, 16-bit, and 32-bit Data Types
- On-chip Programmable System Clock up to 50MHz
- Very Low Power Consumption
  - Industry Leader in MIPS/Watt
  - Low power Idle and Power down Modes
- Bond Pad Locations Confirming to ISO7816-2
- ESD Protection to ±6000V
- Operating ranges: 1.62V to 5.5V, PC Industry Compatible, GSM/3G Compliant, EMV

Memory

- 192K Bytes of Flash Program Memory and 192K Bytes of Eeprom
  - Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
- EEPROM Erase Only Mode
- Write EEPROM With or Without Autoerase
- 24K Bytes of RAM (2K Bytes shared with AdvX ™ crypto processor)
- 32K Bytes of ROM dedicated to Atmel's crypto Library

Peripherals

- USB Interface (5 Endpoints)
  - USB V2.0 Full-speed (12Mbps), Suspend/Resume Modes Supported
  - 4 Configurable Endpoints in Addition to Endpoint EP0
  - Dynamic Pull-up Attachment
- USB_IC (Inter Chip) 0.8e Interface
- Serial Peripheral Interface (SPI) Controller (up to 20MHz)
- One ISO 7816 Controller
  - Up to 625kbps at 5 MHz
- Interface for External NAND Flash Memory
- Single Wire Interface (Digital Interface to RF front end chip)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 15-vector Interrupt Controller
- Hardware DES and Triple DES (DPA Resistant)
- Checksum Accelerator
- CRC 16/32 Engine
- 32-bit Cryptographic Accelerator for Public Key Operations
  - RSA, DSA, ECC, Diffie-Hellman
- High performance Hardware Java Card Accelerator

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Protection Against Physical Attack
- Environmental Protection Systems
- Voltage, Frequency, Light, and Temperature Protection Systems
- Secure Memory Management/ Access Protection/ MPU

Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Development Tools and Software

- **Hardware Development Support on the ATV4-91SC Voyager Emulation Platform**
- **Software Libraries and Bootloader in ATMEL's ROM (Crypto Library and Generic drivers)**
- **Application Notes**

Description

The AT91SC192192CT-USB is a low power, high performance, 32-bit RISC microcontroller with Flash/Eeprom program and data memories and cryptographic accelerator, based on the ARM SC100 advanced secure processor. This general purpose 32-bit processor offers high performance, very low power consumption, and additional features to help combat fraud.

The AT91SC192192CT-USB features 192K bytes of high performance Flash (fast erase/write time, high endurance).

The AT91SC192192CT-USB features 192K bytes of high performance Eeprom (fast erase/write time, high endurance).

The AT91SC192192CT-USB also features a USB full speed 2.0 port to allow very high speed transactions with a USB host terminal. USB interface requires the addition of an external 48MHz resonator.

The AT91SC192192CT-USB features a SPI (Serial Peripheral Interface) port to provide either high speed interface with external terminal or to connect external NOR Flash memory. It also features an interface for NAND Flash memory.

On top of the SC100s MPU, a real hardware firewall can be used to increase the overall security level of the application without intense software development.

The cryptographic accelerator featured in the AT91SC series is the AdvX™, an N-bit multiplier-accumulator dedicated to performing fast encryption and authentication functions. AdvX is based on a custom 32-bit co-processor, thus enabling fast computation and low power operation. The AdvX in conjuction with controlling firmware running within the SC100 core, supports standard finite arithmetic functions (including RSA, DSA, DH and ECC) and GF(2N).

Unique hardware features significantly accelerate the execution of Java Card Byte Code by removing the common software bottlenecks encountered during the implementation of a Java Virtual Machine.

Additional security features include power and frequency protection logic, logical scrambling on program data and addresses, power analysis countermeasures, and memory access controlled by a supervisor mode.

Pin Configuration

The AT91SC192192CT-USB pinout configuration confirms to the ISO7816-2 interface.

Note: By convention, the $\overline{\text{RST}}$ pin corresponds to the RST signal of the ISO7816-3 Protocol, both are active low.)

GND	Ground (reference voltage)	**$\overline{\text{WE}}$**	Flash Interface (Write Enable)
Vcc	Power Supply Input	**ALE**	Flash Interface (Address Latch Enable)
ISO I/O0	Input or Output for serial data (ISO7816	**CLE**	Flash Interface (Command Latch Enable)
ISO CLK	Clock signal input to external clock operating circuit	**$\overline{\text{CE}}$**	Flash Interface (Chip Enable)
ISO $\overline{\text{RST}}$	Reset signal input, a low state stops the ARM core	**$\overline{\text{RE}}$**	Flash Interface (Read Enable)
C6	SWP dedicated pin	**IO0**	Flash Interface IO0
USB D+	USB D+	**IO1**	Flash Interface IO1
USB D-	USB D-	**IO2**	Flash Interface IO2

USB XIN	USB XIN
USB XOUT	USB XOUT
$\overline{\text{WP}}$	Flash Interface (Write Protect)
IO3	Flash Interface IO3
$\overline{\text{SS}}$/IO4	SPI Slave Select/Flash Interface IO4
SCK/IO5	SPI Clock/Flash Interface IO5
MOSI/IO6	SPI Master Output-Slave Input/Flash Interface IO6
MISO/IO7	SPI Master Output-Slave Input/Flash Interface IO7

Architectural Overview

The SC100 is a 3 stage pipeline, 32-bit RISC processor. It uses a Von Neumann Load/store architecture, this architecture is characterized by a single data and address bus for instruction data. The SC100 processor employs a unique architectural strategy known as Thumb®, a super reduced instruction set that is ideally suited for high volume applications with memory restrictions, and applications where code density is an important factor. Essentially, the SC100 processor has two instruction sets:

- The standard ARM instruction set using 32-bit instructions and offering maximum performance
- The Thumb instruction set using 16-bit instructions and offering maximum code density

Both instruction sets operate on 8-bit, 16-bit and 32-bit data types.

The Thumb's 16-bit instruction length allows it to achieve almost twice the density of standard ARM code, whilst retaining most of the ARM performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because the 16-bit Thumb instructions operate on the same 32-bit register set as the 32-bit ARM instruction set. Thumb code can be up to 35% smaller than the equivalent ARM code, whilst providing 160% of the performance of an equivalent ARM processor connected to a 16-bit memory system.

Figure 1 shows the block diagram of the AT91SC192192CT-USB device.

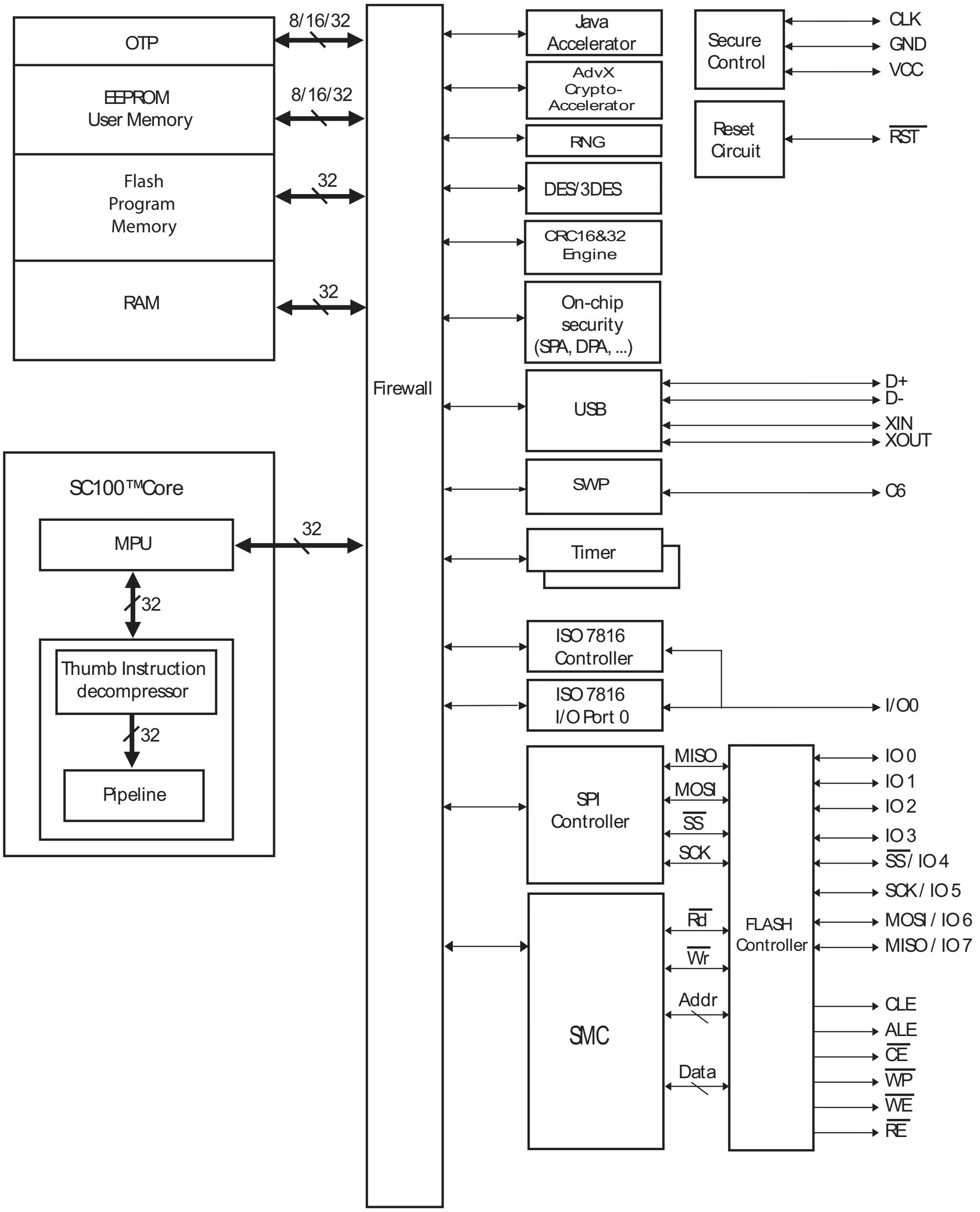


Figure 1. AT91SC192192CT-USB Block Diagram

Figure 2. AT91SC192192CT-USB Pinout (LQFP64)

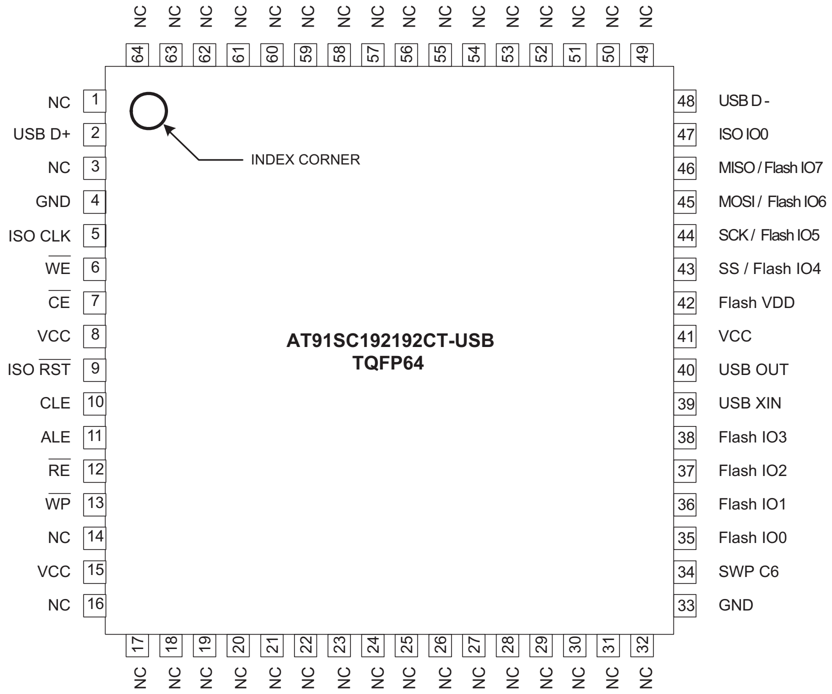
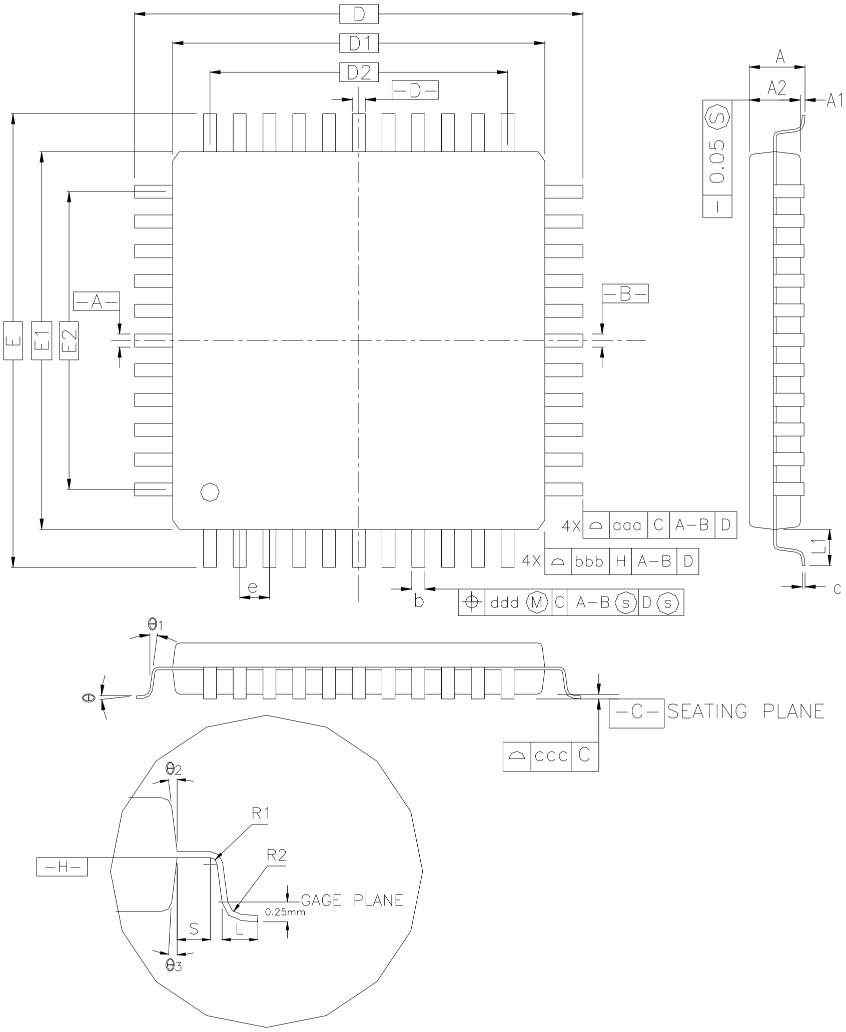


Figure 3. R-LQFP064 Package



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC.			0.472 BSC.		
D_1	10.00 BSC.			0.393 BSC.		
E	12.00 BSC.			0.472 BSC.		
E_1	10.00 BSC.			0.393 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.295		
E2	7.50			0.295		
	TOLERANCES OF FORM AND POSITION					
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

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