Structure Silicon monolithic Integrated circuit
Product Clock Generator

Type **BU2396KN**

Feature To generate clocks for digital still camera system
Connecting a crystal oscillator generates multiple clock signals with a built-in PLL.

○Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5 ～ 7.0	V
Input Voltage	VIN	-0.5 ～ VDD+0.5	V
Storage Temperature range	Tstg	-30 ～ 125	℃
Power dissipation	PD	530 ※1	mW

※1 A measure value at mounting on 50×50×1.6mm glass epoxy substrate.
In the case of exceeding Ta=25℃, 5.3mW should be reduced per 1℃.
※ The radiation-resistance design is not carried out.
※ Operation is not guaranteed.

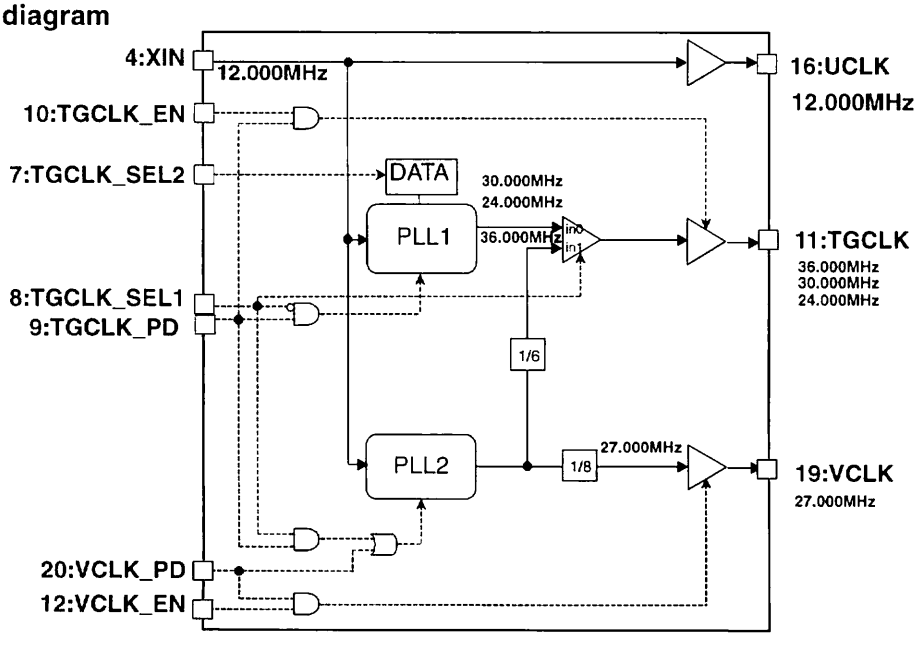
○Operating Conditions (Ta=-5℃~+70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	3.0	3.3	3.6	V
Input "H" Voltage	VIH	0.8VDD	-	VDD	V
Input "L" Voltage	VIL	0.0	-	0.2VDD	V
Output load	CL	0	-	15	pF

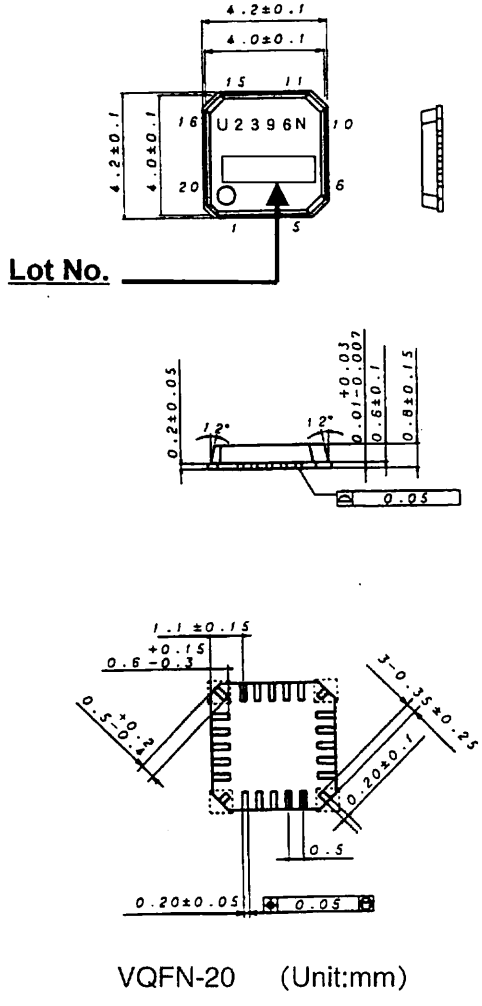
○Electrical Characteristics (VDD=3.3V, Ta=25℃, Crystal =12.000000MHz, unless otherwise specified.)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Action circuit current	IDD	—	23	35	mA	
Output H voltage TGCLK	VOH1	VDD-0.5	–	–	V	When current load =-–5.0mA
VCLK	VOH2	VDD-0.5	–	–	V	When current load =–5.0mA
UCLK	VOHR	VDD-0.5	–	–	V	When current load =–5.0mA
Output L voltage TGCLK	VOL1	–	–	0.5	V	When current load =5.0mA
VCLK	VOL2	–	–	0.5	V	When current load =5.0mA
UCLK	VOLR	–	–	0.5	V	When current load =5.0mA
Pull-Up resistance value TGCLK_SEL1 TGCLK_SEL2	Pullup-R	125	250	375	KΩ	Specified by a current value running when a voltage of 0V is applied to a measuring pin. (R=VDD／I)
Pull-Down resistance value TGCLK_EN、TGCLK_PD VCLK_EN、VCLK_PD	Pulldown-R	25	50	75	KΩ	Specified by a current value running when a VDD is applied to a measuring pin. (R=VDD／I)
Output frequency						
TGCLK SEL1:L SEL2:L	TGCLK_1		24.000000		MHz	XIN＊ (48/4) /6
SEL1:L SEL2:H	TGCLK_2		30.000000		MHz	XIN＊ (60/4) /6
SEL1:H	TGCLK_3		36.000000		MHz	XIN＊ (54/3) /6
VCLK	VCLK		27.000000		MHz	XIN＊ (54/3) /8
UCLK	UCLK		12.000000		MHz	XIN
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Rise-Time	tr		2.0		nsec	Period of transition time required for the output to reach 80% from 20% of VDD.
Fall-Time	tf		2.0		nsec	Period of transition time required for the output to reach 20% from 80% of VDD.
Period-Jitter 1 σ	P-J1 σ		50		psec	
Period-Jiiter MIN-MAX	P-J MIN-MAX		300		psec	
Output Lock-Time	Tlock			1	msec	

○ Block diagram



○Package outline, Appearance of Marker ○Pin function



VQFN-20 (Unit:mm)

Pin No.	PIN NAME	機 能
1	AVDD	Analog power source
2	AVDD	Analog power source
3	AVSS	Analog GND
4	XIN	Crystal IN
5	XOUT	Crystal OUT
6	TEST1	TEST pin, normally open, equipped with pull-down
7	TGCLK_SEL2	TGCLK frequency selection equipped with pull-up
8	TGCLK_SEL1	TGCLK frequency selection equipped with pull-up
9	TGCLK_PD	TGCLK Power-Down control H:enable, L:Power-Down equipped with pull-down
10	TGCLK_EN	TGCLK output control, H: Enable, L: Output fixed to L equipped with pull-down
11	TGCLK	36M、30M、24M output
12	VCLK_EN	VCLK output control H:enable, L: Output fixed to L equipped with pull-down
13	VSS1	TGCLK,UCLK & Internal digital GND
14	VDD1	TGCLK,UCLK & Internal digital power supply
15	VDD1	TGCLK,UCLK & Internal digital power supply
16	UCLK	12M output
17	VSS2	VCLK GND
18	VDD2	VCLK power source
19	VCLK	27M output
20	VCLK_PD	VCLK Power-Down control H:enable, L:Power-Down equipped with pull-down

●Cautions on use (BU2396KN)

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)
Mount 0.1μFs as bypass capacitors in the vicinity of the IC pins between 1&2 PIN and 3PIN, 13PIN and 14&15PIN, and 17PIN and 18PIN, respectively.

* Even though we believe that the example of the application circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.
* As to the jitters, the TYP values vary with the substrate, power supply, output loads, noises, and others. Besides, for the use, the operating margin should be thoroughly checked.

●Cautions on use(common)

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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As of 18th. April 2005