STS-12/STM-4 DS3/E3/STS-1E SONET/SDH Mapper

Part Number S1204CBI21, Revision 1.5, Dec. 2002

Features

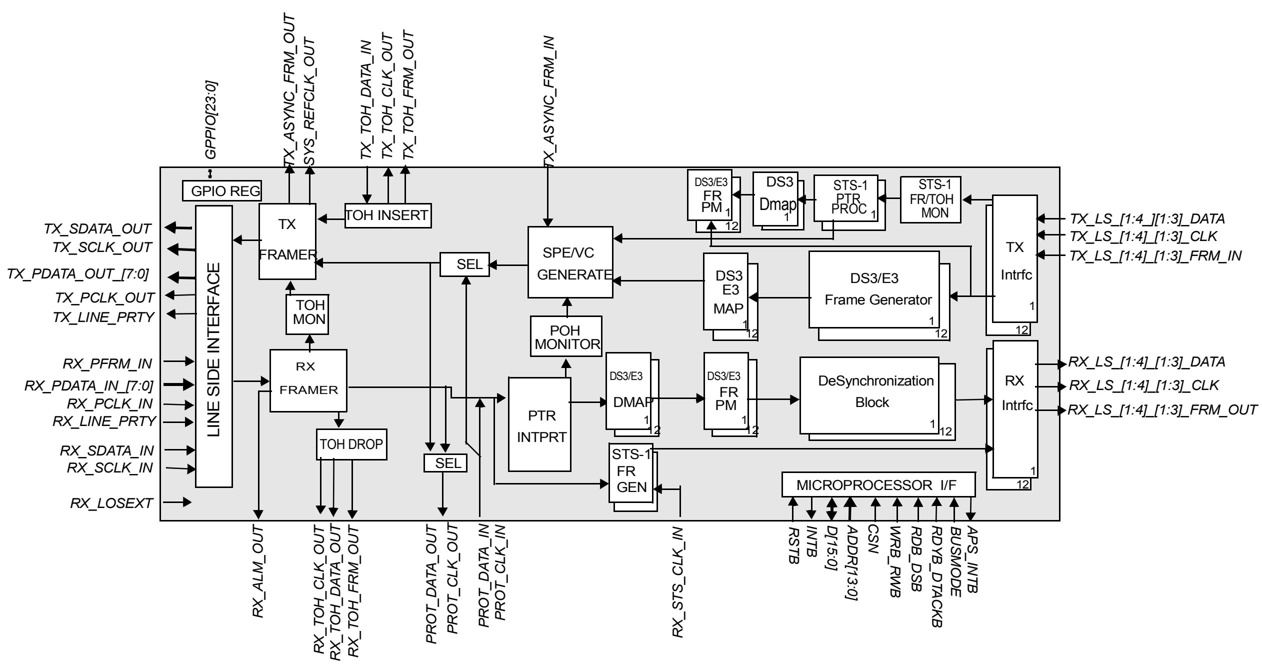
- Processes any valid combination of SONET/SDH STS-1/AU-3 or TUG-3/AU-4 tributaries in STS-12/STM-4 or STS-3/STM-1.
- Terminates/generates SONET/SDH section, line, and path OH
- Provides on the SONET/SDH side a serial 622 MHz or a 77.76 MHz 8-bit interface for STS-12/STM-4 applications; or a serial 155.52 MHz interface for STS-3/STM-1 applications.
- Supports flexible assignment of STS-1E and DS3 or STS-1E and E3 mappings on a per tributary basis.
- Provides STS-1E mapping/demapping for up to 12 STS-1s.
- Provides DS3 or E3 mapping/demapping for up to 12 tributaries, through SONET STS1, SDH AU-3, and/or TUG-3/AU-4 containers.
- Supports mixed M23 and C-bit parity DS3 frame formats on a per-tributary basis.
- Supports mixed G.751 and G.832 E3 frame formats on a per-tributary basis.
- Supports full-featured DS3/E3/STS-1E performance monitoring in both transmit and receive directions.
- 12 serial clock/data ports are provided on the system side for DS3/E3/STS-1E interfaces.
- Integrates DS3/E3 desynchronizer circuitry necessary to provide DS3/E3 clear channel outputs that meet Bellcore, ANSI and ITU jitter requirements.
- 622/155 MHz APS interface for redundancy applications.
- Loopback capability for SONET/SDH and DS3/E3/STS-1Es data streams.

The ORINOCO is a highly integrated chip that implements SONET/SDH processing and DS3/E3/STS-1E mapping functions for an STS-12/STM-4 or STS-3/STM-1 data stream. The ORINOCO is compliant with the following standards: Bellcore GR-253, GR-499 and GR-820; ANSI T1.105 and T1.107; and ITU G.751-2; G.775, G.783, G.804, G.823-5, and G.832.

The ORINOCO supports full-duplex processing of SONET/SDH data streams with section, line, & path overhead processing. The device supports framing, scrambling/descrambling, alarm signal insertion/detection, and bit interleaved parity (B1/B2/B3) processing. Serial interfaces for E1, E2, F1 and Line and Section DCC are also provided.

A general purpose microprocessor interface is provided for device initialization, control, and monitoring. This interface can operate either as an 8-bit asynchronous interface, or a 16-bit synchronous interface. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configuration.

Figure 1: Block Diagram



Final/Production Release Information - The information contained in this document is about a product in its fully tested and characterized phase.All features described herein are supported. Contact AMCC for updates to this document and the latest product status

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Overview

SONET/SDH Processing

The ORINOCO implements SONET/SDH processing for STS-12/STM-4 or STS-3/STM-1 data streams. It can support STS-1 signals within an STS-12 or STS-3, or any combination of TUG-3/AU-4 or AU-3 signals within an STM-1 or STM-4. The ORINOCO supports the mapping of DS3, E3 or STS-1 tributaries into SONET or SDH. For DS3/E3/STS-1E tributaries, the ORINOCO provides full framing and performance monitoring.

In the SONET/SDH receive direction, the ORINOCO performs framing, descrambling, and TOH monitoring, including B1/B2 performance monitoring, serial channel access to the DCC, User Channel and Orderwire bytes, and monitoring of the J0, K1K2 (APS, AIS-L and RDI-L detection), S1 and M1 bytes. While processing the received pointers, the ORINOCO locates the start of the embedded SPEs and provides monitoring capabilities for the POH and pointer bytes.

In the SONET/SDH transmit direction, the ORINOCO generates the appropriate SPE/VCs containing the input DS3/E3/STS-1E signals, including generation of path overhead (with generation of AIS-P and RDI-P). A SONET/SDH STS-12/STM-4 or STS-3/STM-1 frame is then created, with its corresponding TOH. The user has the ability to control the contents of all defined TOH bytes, including register map control of the K1K2, J0, M1 and S1 bytes, as well as serial channel access to the DCC, User Channel and Orderwire bytes. The B1 and B2 bytes are automatically generated, as well as AIS-L and RDI-L indications.

The ORINOCO is SONET and SDH standards compliant with Bellcore GR-253 and GR-499 and ITU G.707 and G.783.

DS3/E3 Processing

The ORINOCO provides DS3/E3 mapper and de-mapper functions. The DS3/E3 mapper accepts data from an external DS3/E3 input, looped-back DS3/E3 tributaries, or internal DS3/E3 frame generators. The ORINOCO provides full DS3/E3 framing and performance monitoring in both transmit and receive directions.

The ORINOCO supports both M23 and C-bit parity DS3 frame formats. It provides the following DS3 mapping options: DS3/STS-1, DS3/AU-3 and DS3/TUG-3/AU-4.

The ORINOCO supports both the G.751 and G.832 E3 frame formats. It provides the following E3 mapping options: E3/AU-3 and E3/TUG-3/AU-4.

DS3 monitoring functionality includes support for AIS, idle, RAI, AIC, FEAC, path parity, FEBE detection/insertion, detection of DS3 frame errors (OOF and SEF), and DS3 performance monitoring per ANSI T1.231.

E3 monitoring functionality includes detection of REI, RDI, LOF, AIS, and BIP-4/BIP-8 parity errors, as well as errored block and errored second indications.

STS-1 Processing

The ORINOCO provides STS-1 mapper and de-mapper functions. The STS-1 mapper accepts data from external STS-1E inputs and/or from looped-back STS-1 tributaries. The ORINOCO provides full STS-1 framing, descrambling, performance monitoring and pointer processing in the transmit direction. In the receive direction, the ORINOCO provides full STS-1 frame generation and scrambling.

Line Interface

On the line side, the ORINOCO supports an 8-bit parallel interface which operates at 77.76 MHz for STS-12/STM-4 applications. In this mode, the device is connected to the S3037 parallel-to-serial converter (see application figure below). Optionally, the ORINOCO supports a serial line interface which operates at 622.08 MHz for STS-12/STM-4 applications, or at 155.52 MHz or STS-3/STM-1. In these applications, the device is connected to the S3024 clock recovery device.

APS Interface

The ORINOCO provides APS input and output interfaces to convey signals between two S1204 devices configured for APS operation. This configuration supports both 1+1 and 1:1 configurations. The APS interface consists of serial clock and data, operating a 622 MHz for STS-12/STM-4 operation, or 155 MHz for STS-3/STM-1 operation.

System Interface

The ORINOCO supports up to 12 DS3/E3/STS1 tributaries. In the SONET/SDH Receive direction, the ORINOCO generates a serial (NRZ) data signal, accompanied by a smoothed DS3/E3 clock and a start of frame indication for each DS3/E3 tributary. For STS-1E tributaries, the ORINOCO provides RX serial (NRZ) data and clock and frame start signals at 51.84 MHz.

In the SONET/SDH Transmit direction, the ORINOCO provides two modes of operation. In clear-channel mode, the ORINOCO accepts a full DS3/E3 signal, payload and overhead bits, and performs framing on the incoming signal. The frame start inputs are ignored in this mode of operation. In DS3 payload only mode, the ORINOCO accepts the DS3 payload only on the data inputs. The frame start signal indicates the start of the payload (the first data bit following the X1 overhead bit). The ORINOCO maps the DS3 payload data into a full DS3 frame, prior to mapping into a SONET/SDH SPE.

DS3/E3 Desynchronizer

The ORINOCO provides for dense DS3/E3 integration by performing all functions related to DS3/E3 desynchronization. The clock smoother consists of a single, off-chip clock reference together with 12 independent on-chip digitally controlled modulators, digital filters and frequency detectors. This desynchronizer circuitry provides jitter and wander compliance to the ANSI T1-105.03-1994 and ANSI T1-105.03b-1997 specifications.

Packaging and Power

The ORINOCO is packaged in a ceramic ball grid array totaling 474 pins (CBGA474). Two power sources, +3.3V and +2.5V, supplies the I/O and core voltages respectively.

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Applications

- Edge and MultiService Switches
- Optical Transport Systems
- WAN Aggregation Terminals
- SONET/SDH Multiplexers and Digital Cross Connects

Figure 2: Applications

APPLICATION: *- Universal DS3 Line Card for Multi-Service Applications*
- High Density ATM over DS3 Termination
- High Density DS3 Aggregation for Synchronous X-Connects

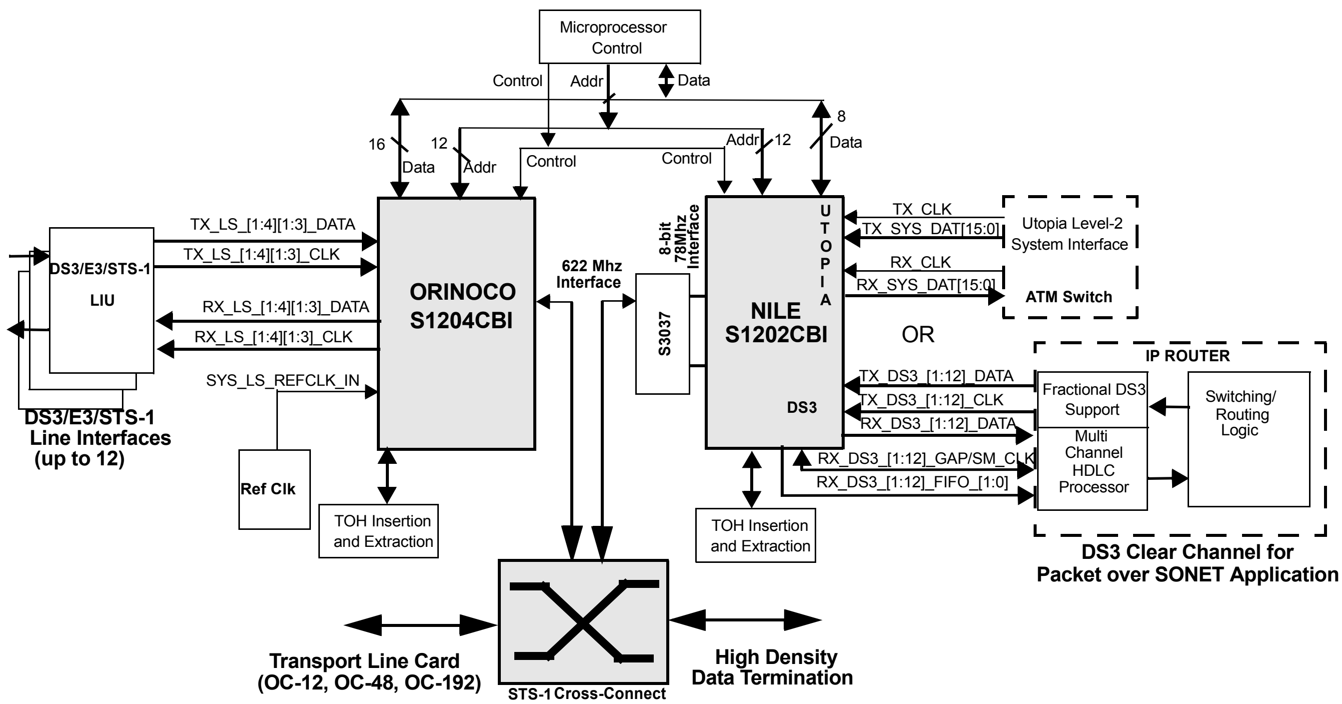

Figure 3: Application OC-12

APPLICATION: *OC-12 Aggregation using the Serial 622 Mbit/s Interface*

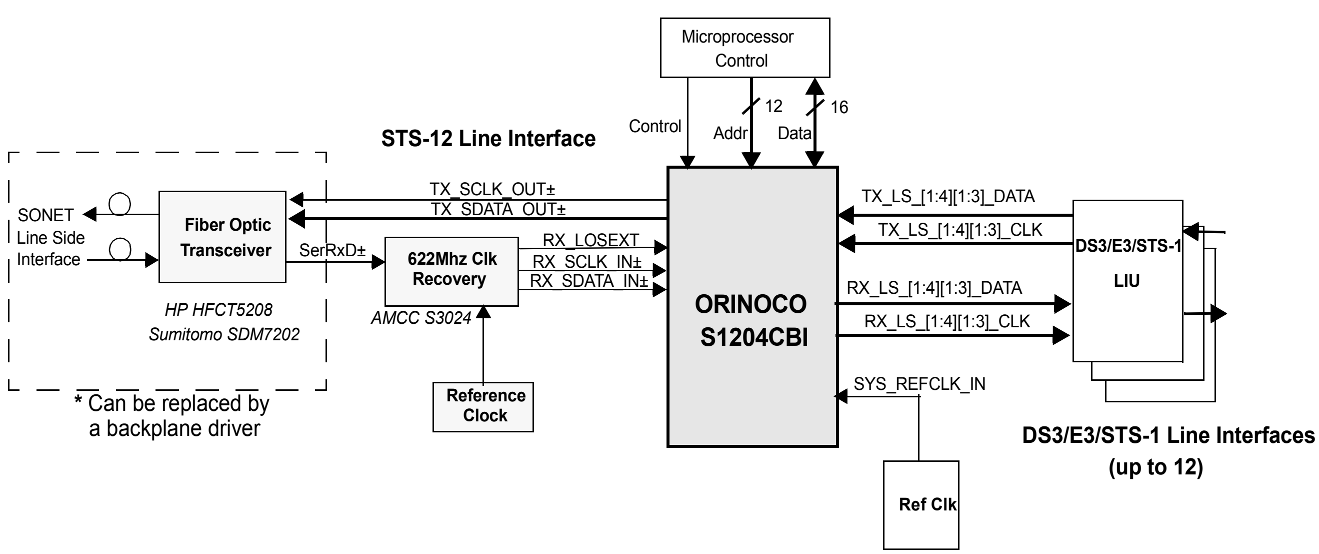

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Figure 4: Application OC-12

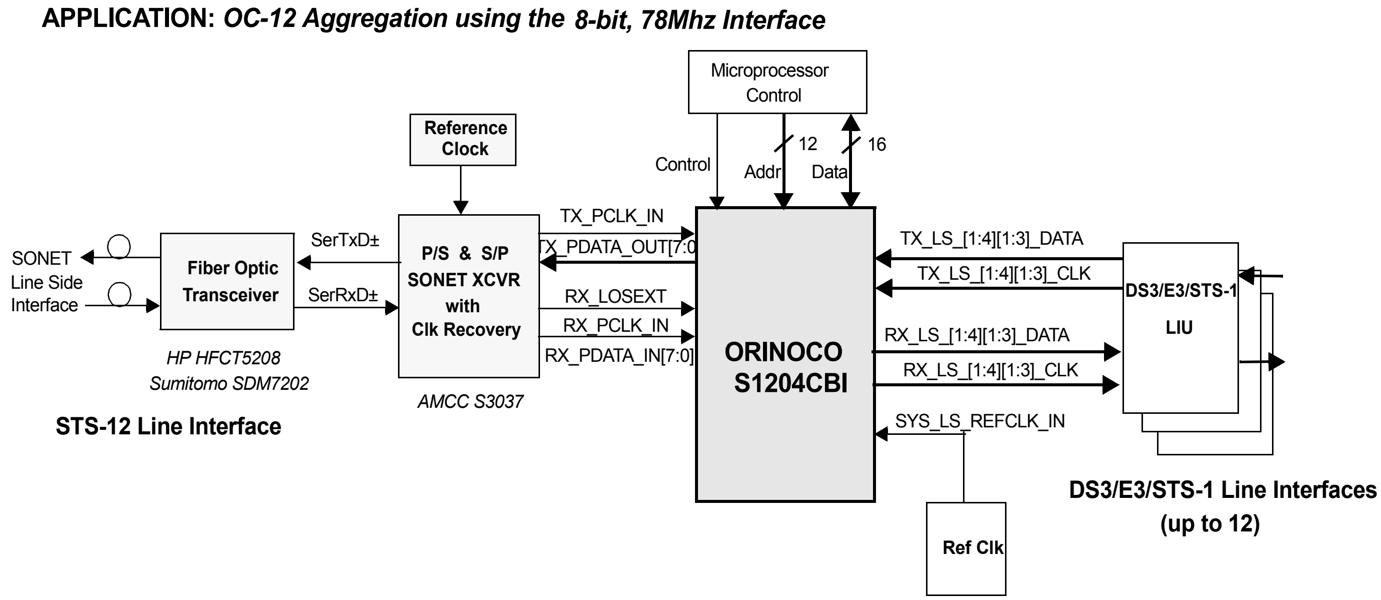
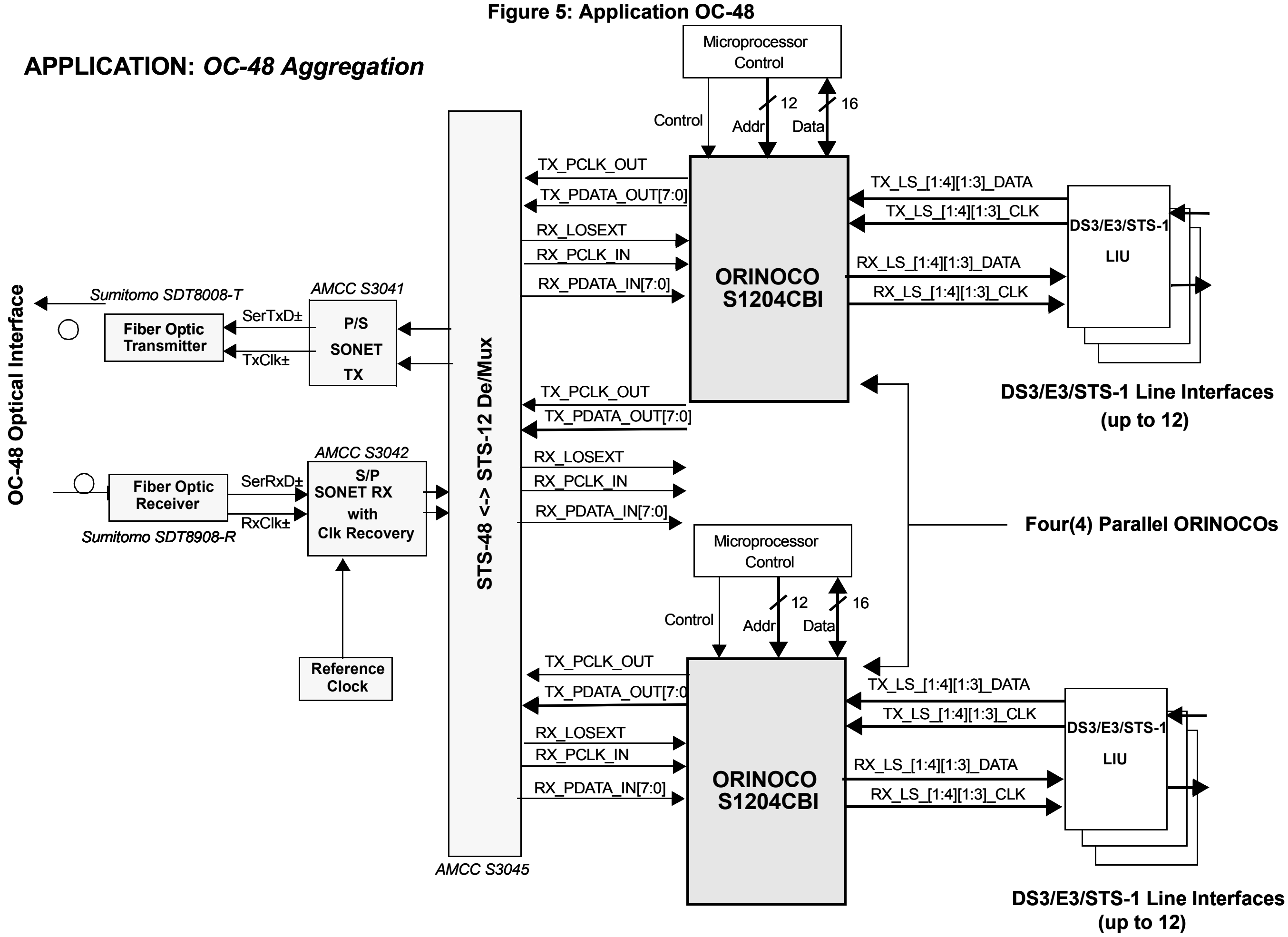


Figure 5: Application OC-48



200 Minuteman Road • Andover, MA 01810 • Tel: 978-247-8000 • Fax: 978-623-0024 • http://

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