



# ESDALC6V1P6

## QUAD LOW CAPACITANCE TRANSIL™ ARRAY FOR ESD PROTECTION

ASD

### MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals.

### FEATURES

- 4 Unidirectional Transil™ functions
- Breakdown voltage  $V_{BR} = 6.1 \text{ V min.}$
- Low diode capacitance (12pF @ 0V)
- Low leakage current < 500 nA
- Very small PCB area < 2.6 mm<sup>2</sup>
- Lead-free package

### DESCRIPTION

The ESDALC6V1P6 is a monolithic array designed to protect up to 4 lines against ESD transients.

The device is ideal for situations where board space saving is required.

### BENEFITS

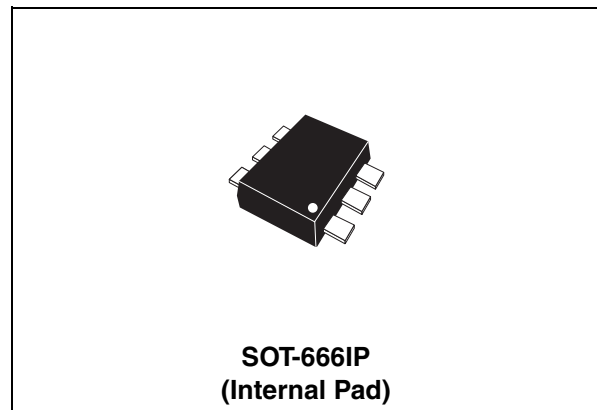
- High ESD protection level
- High integration
- Suitable for high density boards

### COMPLIES WITH THE FOLLOWING STANDARDS:

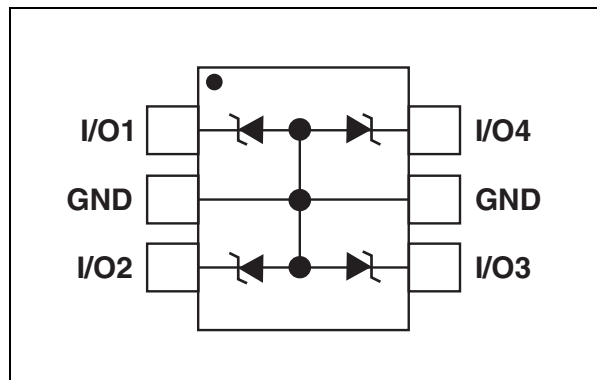
- IEC61000-4-2 level 4:
  - 15kV (air discharge)
  - 8kV (contact discharge)
- MIL STD 883E-Method 3015-7: class3

### Order Codes

Part Number	Marking
ESDALC6V1P6	D



### FUNCTIONAL DIAGRAM



## ESDALC6V1P6

### ABSOLUTE RATING ( $T_{amb} = 25^{\circ}\text{C}$ )

Symbol	Parameter		Value	Unit
$V_{PP}$	ESD discharge	IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	$\pm 15$ $\pm 8$	kV
$P_{PP}$	Peak pulse power (8/20 $\mu\text{s}$ ) (see note 1) $T_j$ initial = $T_{amb}$		30	W
$T_j$	Junction temperature		125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		-55 to +150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s at 5mm for case		260	$^{\circ}\text{C}$
$T_{op}$	Operating temperature range		-40 to +125	$^{\circ}\text{C}$

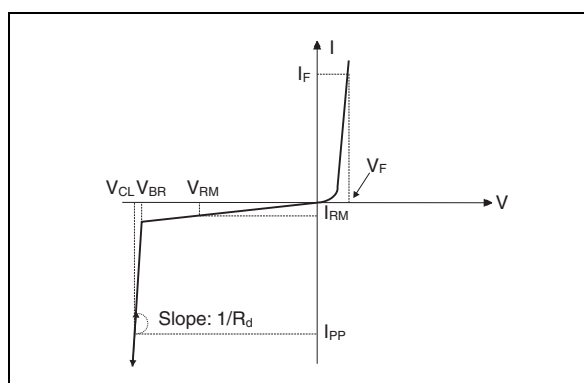
**Note 1:** for a surge greater than the maximum values, the diode will fail in short-circuit.

### THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient on printed circuit on recommended pad layout	220	$^{\circ}\text{C/W}$

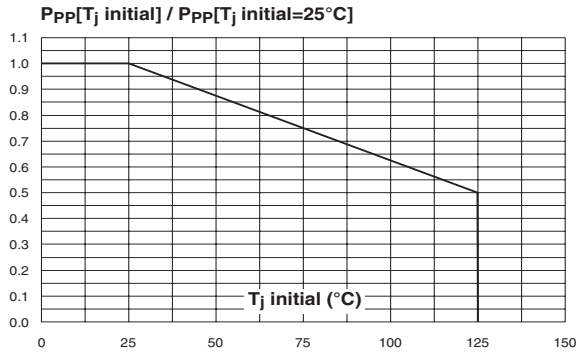
### ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ )

Symbol	Parameter
$V_{RM}$	Stand-off voltage
$V_{BR}$	Breakdown voltage
$V_{CL}$	Clamping voltage
$I_{RM}$	Leakage current
$I_{PP}$	Peak pulse current
$\alpha T$	Voltage temperature coefficient
$V_F$	Forward voltage drop
C	Capacitance
$R_d$	Dynamic resistance

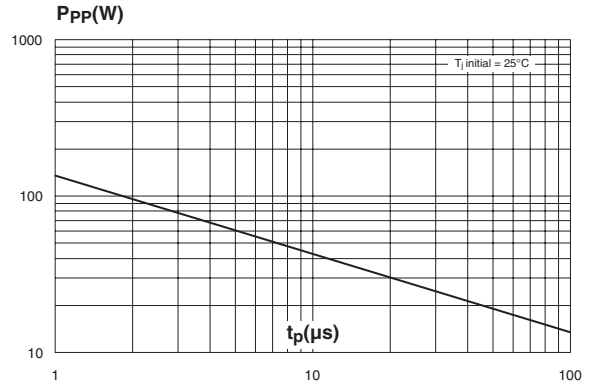


Part Number	$V_{BR}$		@ $I_R$	$I_{RM}$ max.	@ $V_{RM}$	$R_d$ typ.	$\alpha T$ max.	C typ. @ 0V
	min.	max.						
	V	V	mA	$\mu\text{A}$	V	$\Omega$	$10^{-4}/^{\circ}\text{C}$	pF
ESDALC6V1P6	6.1	7.2	1	0.5	3	1.5	4.5	12

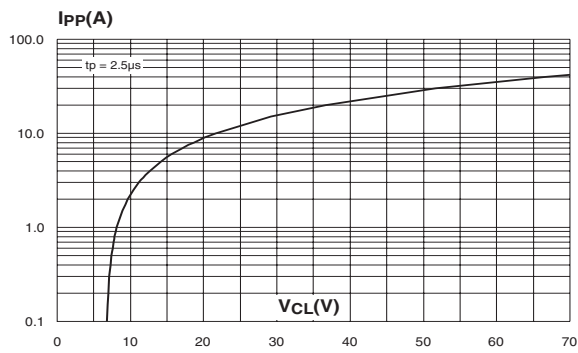
**Fig. 1:** Peak power dissipation versus initial junction temperature.



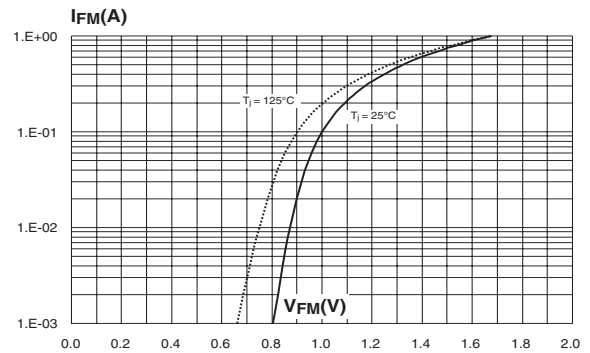
**Fig. 2:** Peak pulse power versus exponential pulse duration ( $T_j$  initial = 25°C).



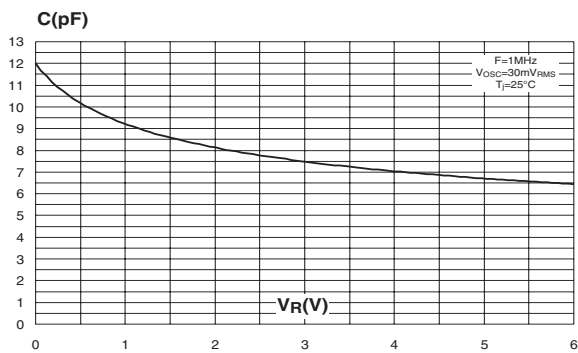
**Fig. 3:** Clamping voltage versus peak pulse current ( $T_j$  initial = 25°C). Rectangular waveform  $t_p = 2.5\mu\text{s}$ .



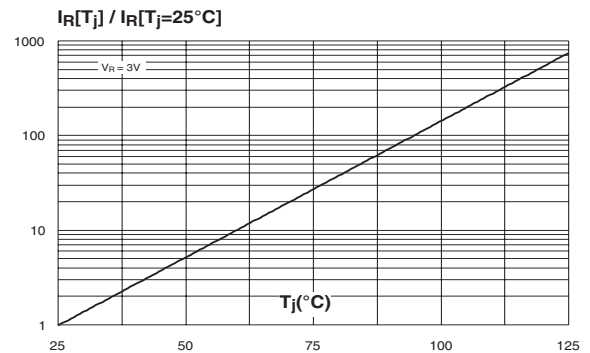
**Fig. 4:** Peak forward voltage drop versus peak forward current (typical values).



**Fig. 5:** Capacitance versus reverse applied voltage (typical values).



**Fig. 6:** Relative variation of leakage current versus junction temperature (typical values).



**TECHNICAL INFORMATION**

**1. ESD protection by ESDALC6V1P6**

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

As a transient voltage suppressor, ESDALC6V1P6 is an ideal choice for ESD protection by suppressing ESD events. It is capable of clamping the incoming transient to a low enough level such that any damage is prevented on the device protected by ESDALC6V1P6.

ESDALC6V1P6 serves as a parallel protection elements, connected between the signal line and ground. As the transient rises above the operating voltage of the device, the ESDALC6V1P6 becomes a low impedance path diverting the transient current to ground.

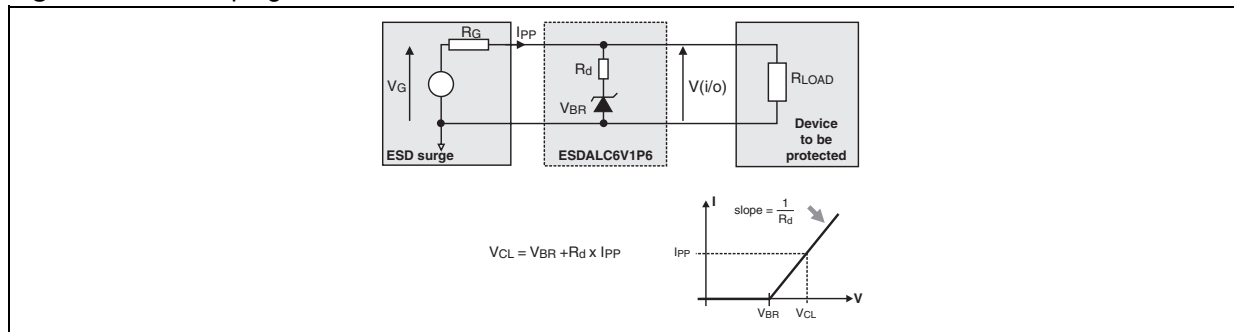
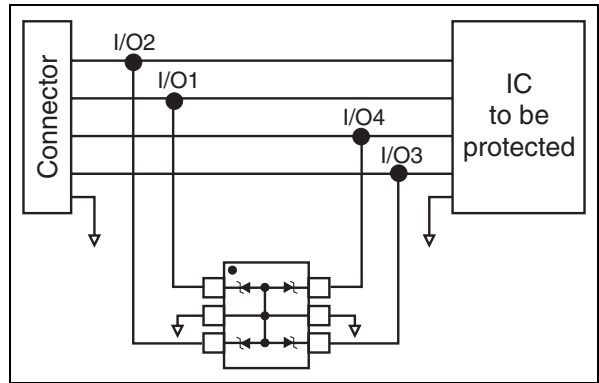
The clamping voltage is given by the following formula:

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

As shown in *figure A2*, the ESD strikes are clamped by the transient voltage suppressor.

**Fig. A2:** ESD clamping behavior.

**Fig. A:** Application example.



To have a good approximation of the remaining voltages at both  $V_{i/o}$  side, we provide the typical dynamical resistance value  $R_d$ . By taking into account the following hypothesis:

$$R_G > R_d \text{ and } R_{load} > R_d$$

we have:

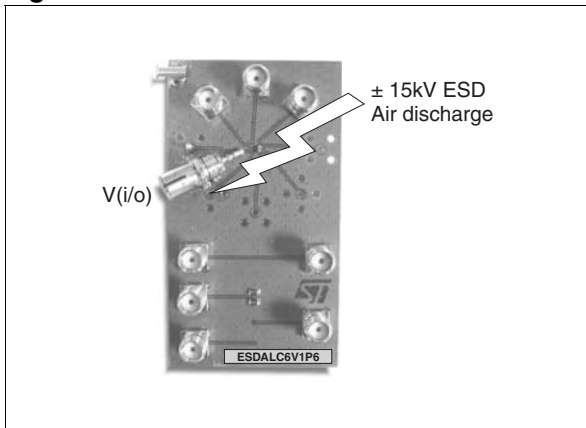
$$V(i/o) = V_{BR} + R_d \times \frac{V_G}{R_G}$$

The results of the calculation done  $V_G = 8kV$ ,  $R_G = 330\Omega$  (IEC61000-4-2 standard),  $V_{BR} = 6.4V$  (typ.) and  $R_d = 1.5\Omega$  (typ.) give:

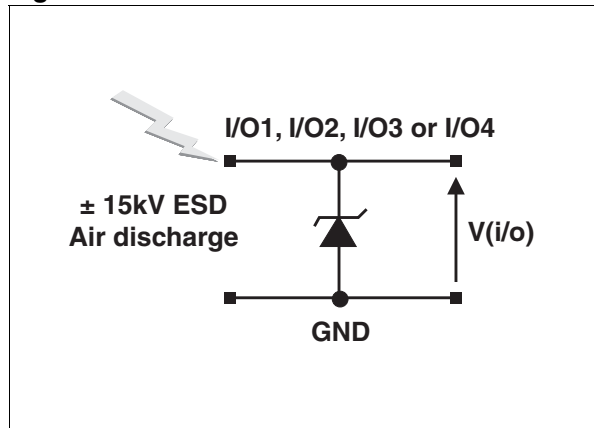
$$V(i/o) = 42.8 \text{ Volts}$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the  $V_{i/o}$  side.

**Fig. A3:** ESD test board.

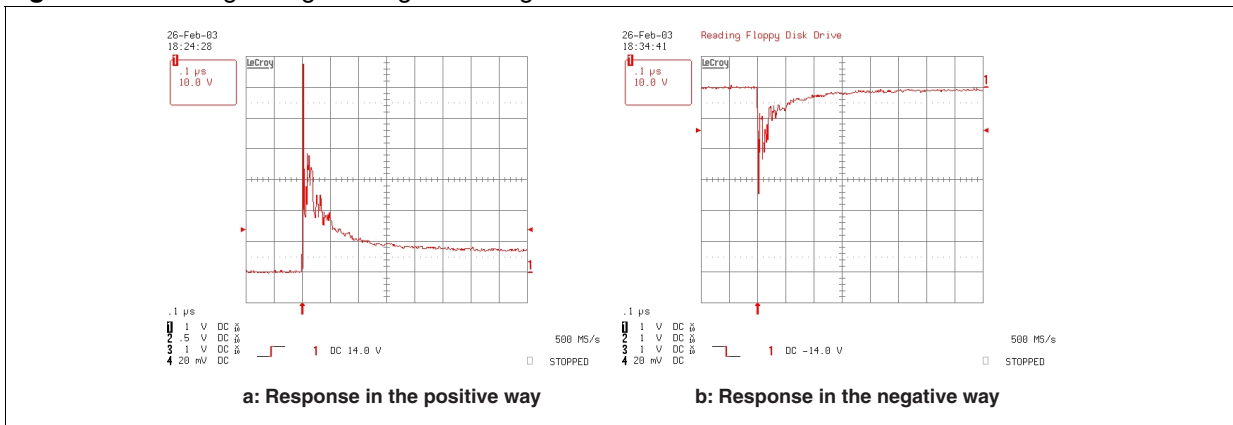


**Fig. A4:** ESD test condition.



The measurements done here after show very clearly (*figure A5*) the high efficiency of the ESD protection: the clamping voltage  $V(i/o)$  becomes very close to  $V_{BR}$  (positive way, *figure A5a*) and  $-V_F$  (negative way, *figure A5b*).

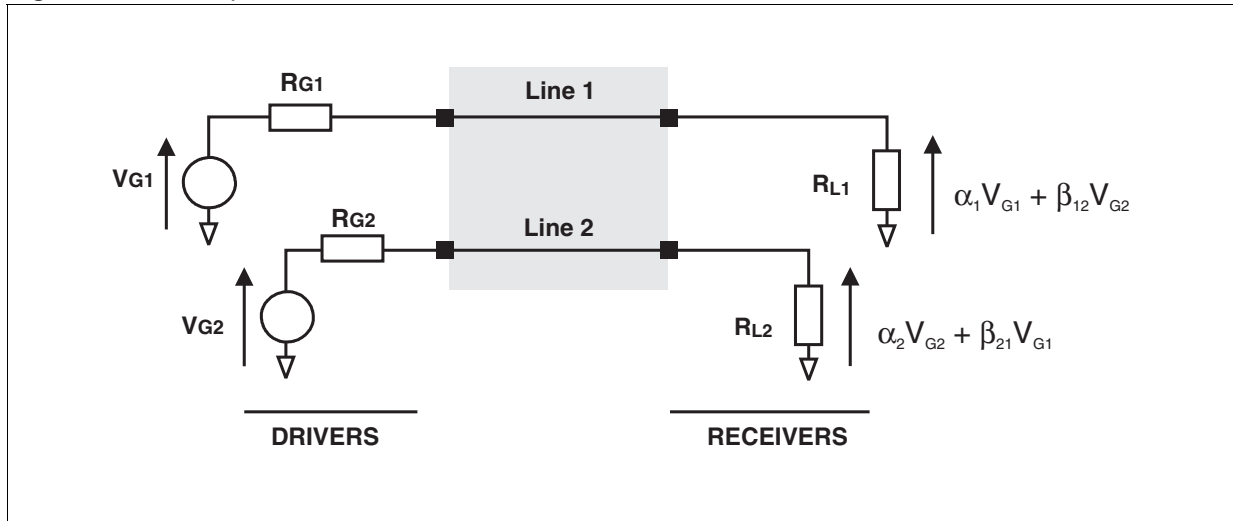
**Fig. A5:** Remaining voltage during ESD surge.



One can note that the ESDALC6V1P6 is not only acting for positive ESD surges but, also, for negative ones. For this kind of disturbances, it clamps close to ground voltage as shown in *figure A5b*.

2. Crosstalk behavior

Fig. A6: Crosstalk phenomenon.



The crosstalk phenomena are due to the coupling between 2 lines. Coupling factors ( $\beta_{12}$  or  $\beta_{21}$ ) increase when the gap across lines decreases, particularly in silicon dice. In the example above, the expected signal on load  $R_{L2}$  is  $\alpha_2 V_{G2}$ , in fact the real voltage at this point has got an extra value  $\beta_{21} V_{G1}$ . This part of the  $V_{G1}$  signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few k $\Omega$ ).

Fig. A7: Analog crosstalk test configuration.

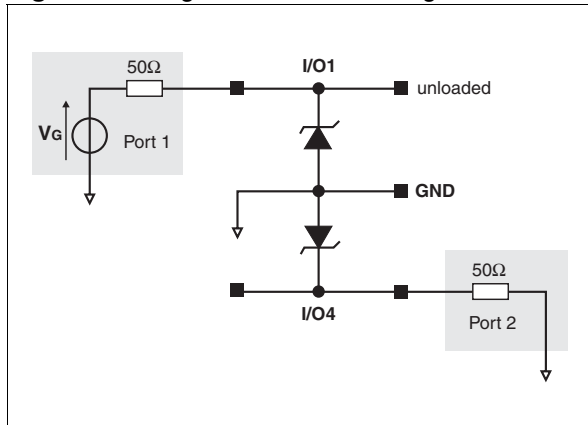


Fig. A8: Typical analog crosstalk response.

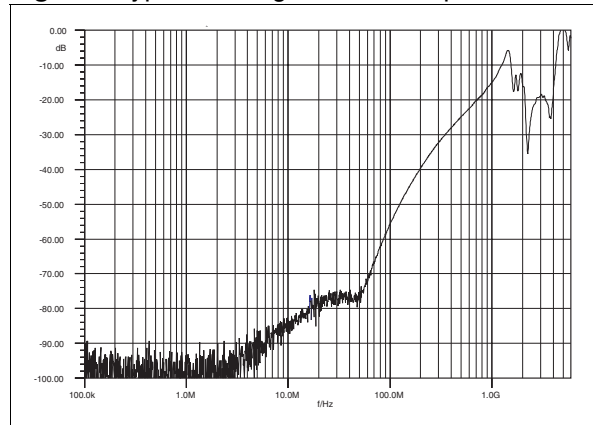
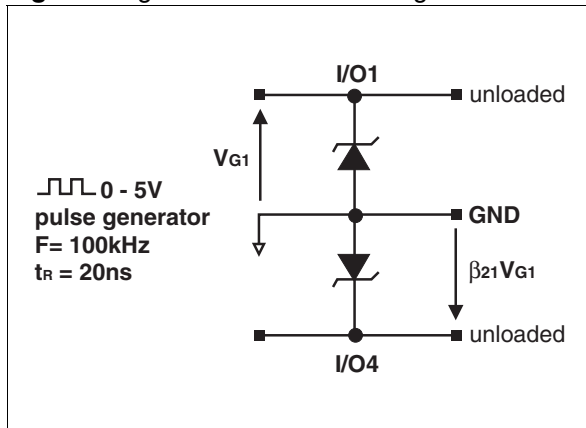


Figure A7 gives the measurement circuit for the analog crosstalk application. In figure 8, the curve shows the effect of the cell I/O1 on the cell I/O4. In usual frequency range of analog signals (up to 100 MHz) the effect on disturbed line is less than -55dB.

**Fig. A9:** Digital crosstalk test configuration.



**Fig. A10:** Typical digital crosstalk response.

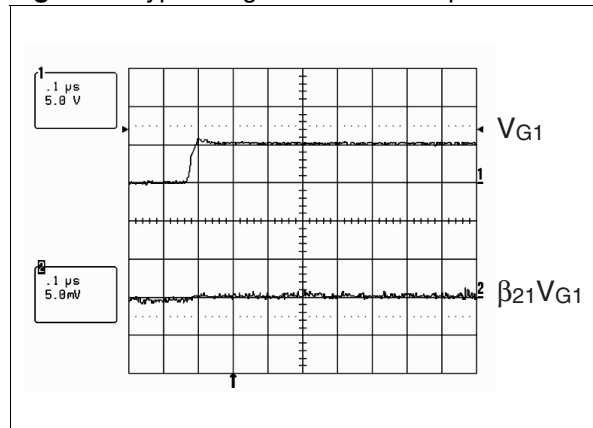


Figure A9 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A10 shows that in such a condition, ie signal from 0 to 5V and rise time of a few ns, the impact on the disturbed line is less than 5 mV peak to peak. No data disturbance was noted on the concerned line. The measurements performed with falling edges give an impact within the same range.

### 3. PCB layout recommendations

As ESD is a fast event, the  $dI/dt$  caused by this surge is about 30A/ns (risetime=1ns,  $I_{\text{peak}}=30\text{A}$ ), that means each nH causes an overvoltage of 30V.

Thus, the circuit board layout is a critical design step in the suppression of ESD induced transients by reducing parasitic inductances. To ensure that, the following guidelines are recommended :

- The ESDALC6V1P6 should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.
- All conductive loops, including power and ground loops should be minimized.
- The ESD transient return path to ground should be kept as short as possible.
- The connections from the ground pins to the ground plane should be the shortest possible.

### 4. Comparison with varistors

	Varistors	TRANSIL™
Leakage current	--	+++
Protection efficiency	--	++
Ageing	--	++

#### Low leakage current for Transil™ device

- Improve the autonomy of portable equipments as mobile

#### Better efficiency in terms of ESD protection by using Transil™ device

- Varistors are bidirectional devices and so are not suitable to protect sensitive ICs, because they will be submitted to high voltages in the negative way.
- Ratio  $V_{CL}/V_{BR}$  lower for Transil™ device
- Less dispersion in terms of  $V_{BR}$

#### No ageing phenomena regarding ESD events with Transil™ device

- Higher efficiency in terms of ESD protection

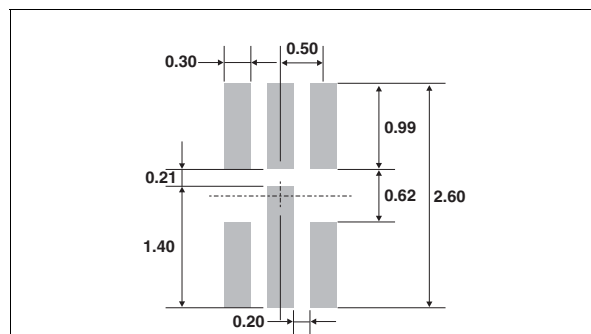
## ESDALC6V1P6

### PACKAGE MECHANICAL DATA

SOT-666IP (internal Pad)

REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.53	0.60	0.021	0.024
A3	0.13	0.18	0.005	0.007
D	1.50	1.70	0.059	0.067
D2	1.05	1.25	0.041	0.049
E	1.50	1.70	0.059	0.067
E1	1.10	1.30	0.043	0.051
E2	0.23	0.43	0.009	0.017
L1	0.11	0.26	0.004	0.010
L2	0.10	0.30	0.004	0.012
L3	0.05	-	0.002	-
L4	0.83 Ref		0.032	
b	0.14	0.25	0.006	0.010
b1	-	0.34		0.013
e	0.50 Bsc		0.020	
e1	0.20		-	0.008
Θ	8°	12°	8°	12°

### FOOT PRINT DIMENSIONS (in millimeters)

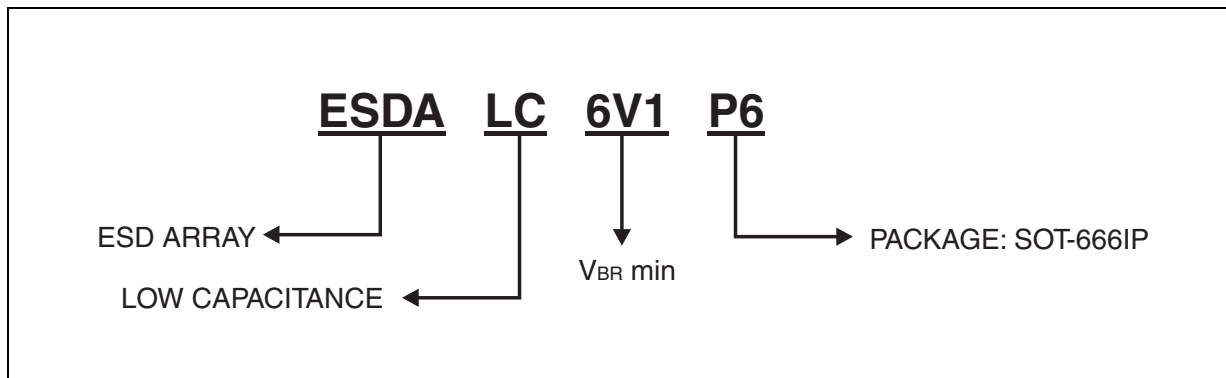


In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).



## ESDALC6V1P6

### ORDER CODE



### ORDERING INFORMATION

Part Number	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1P6	D	SOT-666IP	2.9 mg	3000	Tape & reel

### REVISION HISTORY

Table 1: Revision history

Date	Revision	Description of Changes
January-2004	1	First issue
25-May-2004	2	SOT-666 Internal Pad version package change
05-Jul-2004	3	Stylesheet update. No content change.
02-Nov-2005	4	Lead-free statement added. Footprint diagram modified. Ordering information and revision history moved to end of datasheet.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.  
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

**STMicroelectronics GROUP OF COMPANIES**

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -  
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States

[www.st.com](http://www.st.com)