

SOJ, TSOP
Commercial Temp
Industrial Temp

256K x 8

2Mb Asynchronous SRAM

8, 10, 12, 15 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

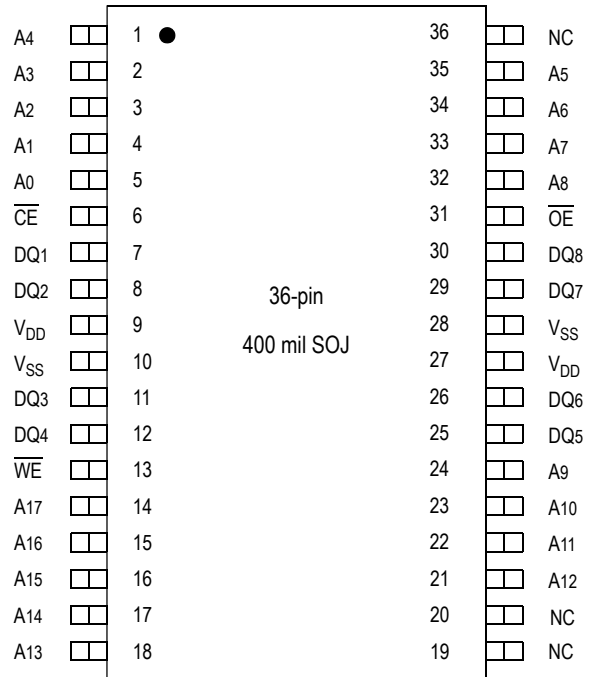
Features

- Fast access time: 8, 10, 12, 15 ns
- CMOS low power operation: 150/125/110/90 mA at minimum cycle time.
- Single 3.3 V \pm 0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: -40° to 85° C
- Package line up
 - J: 400 mil, 36-pin SOJ package
 - TP: 400 mil, 44-pin TSOP Type II package

Description

The GS72108 is a high speed CMOS Static RAM organized as 262,144 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS72108 is available in 400 mil SOJ and 400 mil TSOP Type-II packages.

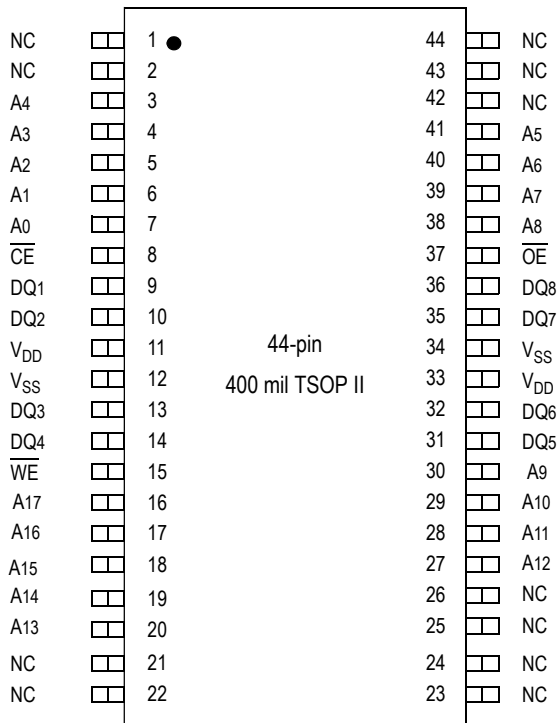
SOJ 256K x 8-Pin Configuration



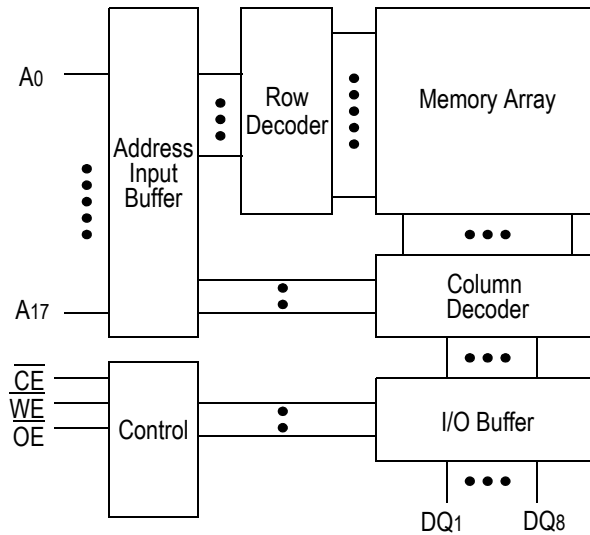
Pin Descriptions

| Symbol | Description |
|----------------------------------|---------------------|
| A ₀ –A ₁₇ | Address input |
| DQ ₁ –DQ ₈ | Data input/output |
| \overline{CE} | Chip enable input |
| \overline{WE} | Write enable input |
| \overline{OE} | Output enable input |
| V_{DD} | +3.3 V power supply |
| V_{SS} | Ground |
| NC | No connect |

TSOP-II 256K x 8-Pin Configuration



Block Diagram



Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | DQ1 to DQ8 | V _{DD} Current |
|------------------------|------------------------|------------------------|--------------|-------------------------|
| H | X | X | Not Selected | ISB1, ISB2 |
| L | L | H | Read | I _{DD} |
| L | X | L | Write | |
| L | H | H | High Z | |

Note: X: "H" or "L"

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|-----------------------------|------------------|--|------|
| Supply Voltage | V _{DD} | -0.5 to +4.6 | V |
| Input Voltage | V _{IN} | -0.5 to V _{DD} +0.5 (≤ 4.6 V max.) | V |
| Output Voltage | V _{OUT} | -0.5 to V _{DD} +0.5 (≤ 4.6 V max.) | V |
| Allowable power dissipation | PD | 0.7 | W |
| Storage temperature | T _{STG} | -55 to 150 | °C |

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|----------|-------|-----|----------------|------|
| Supply Voltage for -10/12/15 | V_{DD} | 3.0 | 3.3 | 3.6 | V |
| Supply Voltage for -8 | V_{DD} | 3.135 | 3.3 | 3.6 | V |
| Input High Voltage | V_{IH} | 2.0 | — | $V_{DD} + 0.3$ | V |
| Input Low Voltage | V_{IL} | -0.3 | — | 0.8 | V |
| Ambient Temperature, Commercial Range | T_{Ac} | 0 | — | 70 | °C |
| Ambient Temperature, Industrial Range | T_{AI} | -40 | — | 85 | °C |

Note:

1. Input overshoot voltage should be less than $V_{DD} + 2$ V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

Capacitance

| Parameter | Symbol | Test Condition | Max | Unit |
|--------------------|-----------|-----------------|-----|------|
| Input Capacitance | C_{IN} | $V_{IN} = 0$ V | 5 | pF |
| Output Capacitance | C_{OUT} | $V_{OUT} = 0$ V | 7 | pF |

Notes:

1. Tested at $T_A = 25^\circ\text{C}$, $f = 1$ MHz
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|------------------------|----------|--|------------------|-----------------|
| Input Leakage Current | I_{IL} | $V_{IN} = 0$ to V_{DD} | -1 μA | 1 μA |
| Output Leakage Current | I_{LO} | Output High Z $V_{OUT} = 0$ to V_{DD} | -1 μA | 1 μA |
| Output High Voltage | V_{OH} | $I_{OH} = -4\text{mA}$ | 2.4 | — |
| Output Low Voltage | V_{OL} | $I_{LO} = +4\text{mA}$ | — | 0.4 V |

Power Supply Currents

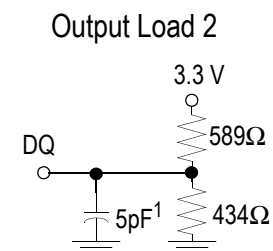
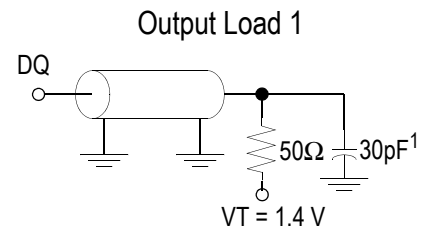
| Parameter | Symbol | Test Conditions | 0 to 70°C | | | | -40 to 85°C | | |
|--------------------------|-----------------|---|-----------|--------|--------|-------|-------------|--------|--------|
| | | | 8 ns | 10 ns | 12 ns | 15 ns | 10 ns | 12 ns | 15 ns |
| Operating Supply Current | $I_{DD}(\max)$ | $\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0 \text{ mA}$ | 150 mA | 125 mA | 110 mA | 90 mA | 135 mA | 120 mA | 100 mA |
| Standby Current | $I_{SB1}(\max)$ | $\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time | 55 mA | 50 mA | 45 mA | 40 mA | 60 mA | 55 mA | 50 mA |
| Standby Current | $I_{SB2}(\max)$ | $\overline{CE} \geq V_{DD} - 0.2 \text{ V}$ All other inputs $\geq V_{DD} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$ | 15 mA | | | | 25 mA | | |

AC Test Conditions

| Parameter | Conditions |
|------------------------|--------------------------|
| Input high level | $V_{IH} = 2.4 \text{ V}$ |
| Input low level | $V_{IL} = 0.4 \text{ V}$ |
| Input rise time | $t_r = 1 \text{ V/ns}$ |
| Input fall time | $t_f = 1 \text{ V/ns}$ |
| Input reference level | 1.4 V |
| Output reference level | 1.4 V |
| Output load | Fig. 1 & 2 |

Note:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ}



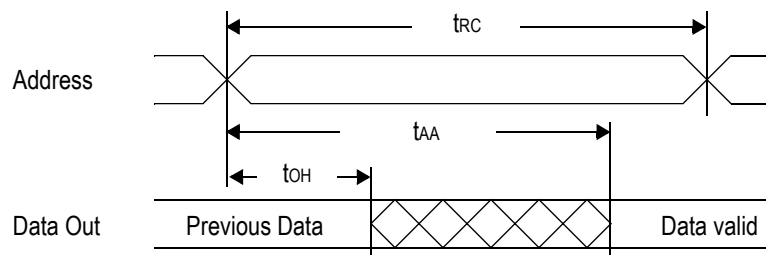
AC Characteristics

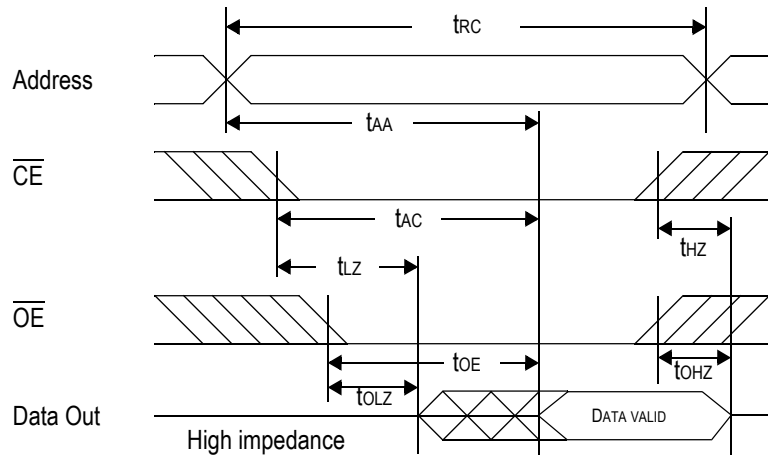
Read Cycle

| Parameter | Symbol | -8 | | -10 | | -12 | | -15 | | Unit |
|--|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read cycle time | t_{RC} | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| Address access time | t_{AA} | — | 8 | — | 10 | — | 12 | — | 15 | ns |
| Chip enable access time (\overline{CE}) | t_{AC} | — | 8 | — | 10 | — | 12 | — | 15 | ns |
| Output enable to output valid (\overline{OE}) | t_{OE} | — | 3.5 | — | 4 | — | 5 | — | 6 | ns |
| Output hold from address change | t_{OH} | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| Chip enable to output in low Z (\overline{CE}) | t_{LZ}^* | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| Output enable to output in low Z (\overline{OE}) | t_{OLZ}^* | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Chip disable to output in High Z (\overline{CE}) | t_{HZ}^* | — | 4 | — | 5 | — | 6 | — | 7 | ns |
| Output disable to output in High Z (\overline{OE}) | t_{OHZ}^* | — | 3.5 | — | 4 | — | 5 | — | 6 | ns |

* These parameters are sampled and are not 100% tested.

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

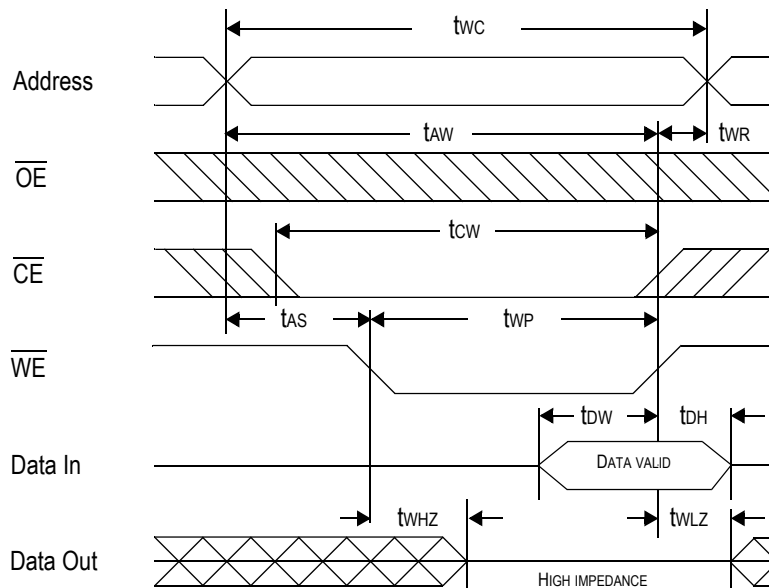


Read Cycle 2: $\overline{WE} = V_{IH}$

Write Cycle

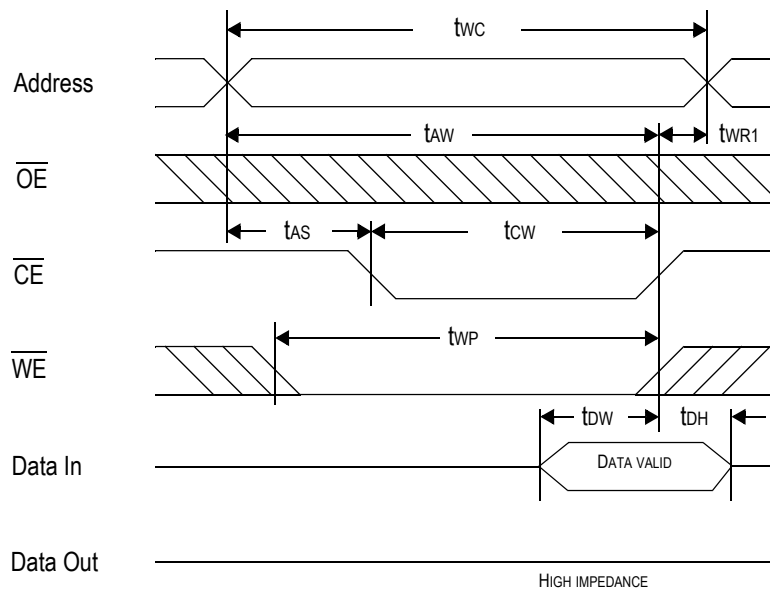
| Parameter | Symbol | -8 | | -10 | | -12 | | -15 | | Unit |
|---|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write cycle time | t_{WC} | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| Address valid to end of write | t_{AW} | 5.5 | — | 7 | — | 8 | — | 10 | — | ns |
| Chip enable to end of write | t_{CW} | 5.5 | — | 7 | — | 8 | — | 10 | — | ns |
| Data set up time | t_{DW} | 4 | — | 5 | — | 6 | — | 7 | — | ns |
| Data hold time | t_{DH} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Write pulse width | t_{WP} | 5.5 | — | 7 | — | 8 | — | 10 | — | ns |
| Address set up time | t_{AS} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time (\overline{WE}) | t_{WR} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Write recovery time (\overline{CE}) | t_{WR1} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Output Low Z from end of write | t_{WLZ}^* | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| Write to output in High Z | t_{WHZ}^* | — | 3.5 | — | 4 | — | 5 | — | 6 | ns |

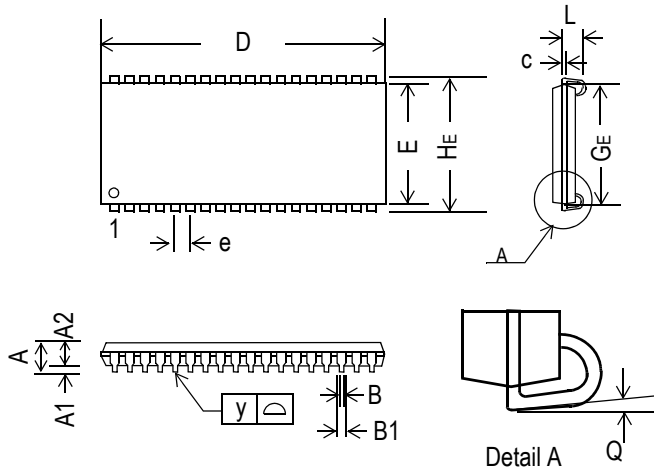
* These parameters are sampled and are not 100% tested.

Write Cycle 1: \overline{WE} control



Write Cycle 2: \overline{CE} control

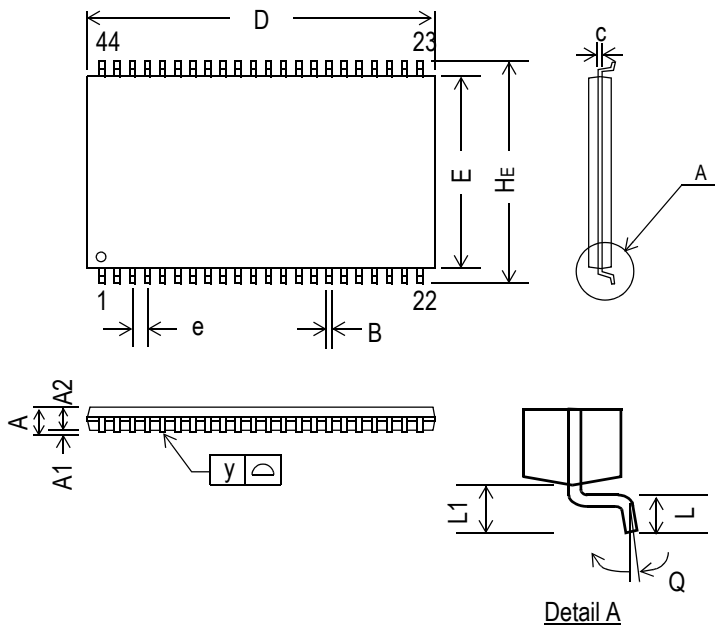


36-Pin SOJ, 400 mil


| Symbol | Dimension in inch | | | Dimension in mm | | |
|--------|-------------------|-------|-------|-----------------|-------|-------|
| | min | nom | max | min | nom | max |
| A | — | — | 0.146 | — | — | 3.70 |
| A1 | 0.026 | — | — | 0.66 | — | — |
| A2 | 0.105 | 0.110 | 0.115 | 2.67 | 2.80 | 2.92 |
| B | 0.013 | 0.017 | 0.021 | 0.33 | 0.43 | 0.53 |
| B1 | 0.024 | 0.028 | 0.032 | 0.61 | 0.71 | 0.81 |
| c | 0.006 | 0.008 | 0.012 | 0.15 | 0.20 | 0.30 |
| D | 0.920 | 0.924 | 0.929 | 23.37 | 23.47 | 23.60 |
| E | 0.395 | 0.400 | 0.405 | 10.04 | 10.16 | 10.28 |
| e | — | 0.05 | — | — | 1.27 | — |
| HE | 0.430 | 0.435 | 0.440 | 10.93 | 11.05 | 11.17 |
| GE | 0.354 | 0.366 | 0.378 | 9.00 | 9.30 | 9.60 |
| L | 0.082 | — | — | 2.08 | — | — |
| y | — | — | 0.004 | — | — | 0.10 |
| Q | 0° | — | 10° | 0° | — | 10° |

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: inches

44-Pin, 400 mil TSOP-II


| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------------|-------------------|-------|-------|-----------------|-------|-------|
| | min | nom | max | min | nom | max |
| A | — | — | 0.047 | — | — | 1.20 |
| A1 | 0.002 | — | — | 0.05 | — | — |
| A2 | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| B | 0.01 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| c | — | 0.006 | — | — | 0.15 | — |
| D | 0.721 | 0.725 | 0.729 | 18.31 | 18.41 | 18.51 |
| E | 0.396 | 0.400 | 0.404 | 10.06 | 10.16 | 10.26 |
| e | — | 0.031 | — | — | 0.80 | — |
| H _E | 0.455 | 0.463 | 0.471 | 11.56 | 11.76 | 11.96 |
| L | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 | 0.60 |
| L1 | — | 0.031 | — | — | 0.80 | — |
| y | — | — | 0.004 | — | — | 0.10 |
| Q | 0° | — | 5° | 0° | — | 5° |

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

Ordering Information

| Part Number * | Package | Access Time | Temp. Range | Status |
|----------------------|-----------------|--------------------|--------------------|---------------|
| GS72108TP-8 | 400 mil TSOP-II | 8 ns | Commercial | |
| GS72108TP-10 | 400 mil TSOP-II | 10 ns | Commercial | |
| GS72108TP-12 | 400 mil TSOP-II | 12 ns | Commercial | |
| GS72108TP-15 | 400 mil TSOP-II | 15 ns | Commercial | |
| GS72108TP-8I | 400 mil TSOP-II | 8 ns | Industrial | |
| GS72108TP-10I | 400 mil TSOP-II | 10 ns | Industrial | |
| GS72108TP-12I | 400 mil TSOP-II | 12 ns | Industrial | |
| GS72108TP-15I | 400 mil TSOP-II | 15 ns | Industrial | |
| GS72108J-8 | 400 mil SOJ | 8 ns | Commercial | |
| GS72108J-10 | 400 mil SOJ | 10 ns | Commercial | |
| GS72108J-12 | 400 mil SOJ | 12 ns | Commercial | |
| GS72108J-15 | 400 mil SOJ | 15 ns | Commercial | |
| GS72108J-8I | 400 mil SOJ | 8 ns | Industrial | |
| GS72108J-10I | 400 mil SOJ | 10 ns | Industrial | |
| GS72108J-12I | 400 mil SOJ | 12 ns | Industrial | |
| GS72108J-15I | 400 mil SOJ | 15 ns | Industrial | |

* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example:
GS72108TP-8T

Revision History

| Rev. Code: Old; New | Types of Changes Format or Content | Page #/Revisions/Reason |
|---|---------------------------------------|--|
| 72108 1.04d 5/1999/721081.05 1/ 2000 | Content | • Page 2/Pins 16–20 and 26–30 on 44-pin TSOP II Pin Configuration/ Correction |
| GS72108Rev1.05 10/19991/ 2000K;Rev 5 2/2000L | Format/Content | • GSI Logo |
| 721081.05 1/2000 | Content | • Corrected TSOP-II pin configuration diagram (A17–A13 in lower left quadrant; A9–A12, A18 in lower right quadrant) |
| | Format | • Updated format to comply with Technical Publications standard • Specifically noted that numbers in Power Supply Currents table are worst case scenario |
| 72108_r1_07; 72108_r1_08 | Content | • Removed all references to “U” package |