

# HD49801FB Preliminary

## Digital Signal Processing IC for CCD Cameras

### Description

The HD49801FB is an IC that integrates all the functions required for CCD camera signal processing (except the CDS and AGC blocks) in a single chip.

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### Features

- Allows microprocessor control (over a serial interface) of all image quality controls.
  - Handles all formats; NTSC, PAL, SECAM (however, does not include a SECAM encoder).
  - Handles 510H/760H CCD image sensors.
- Generates high quality chroma and luminance signals using three-line matrix processing supported by a built-in line memory (1H × 2).

## Pin Functions

Pin No.	Pin Name	Signal	I/O	Function Description
1	PLLPO	PLL posi out	O	In PAL/SECAM modes, the fsc and $f_H$ gen lock phase detection output
2	PLLNO	PLL nega out	O	
3	VRI	Vertical reset in	I	External reset input for the vertical synchronization signal; high = reset
4	CBLKO	Composite blanking out	O	Composite horizontal and vertical blanking signal
5	CSYNCO	Composite SYNC out	O	Composite horizontal and vertical synchronization and blanking signal
6	VDO	Vertical driving out	O	Vertical synchronization signal
7	FVO	Field vertical out	O	Field vertical synchronization signal
8	BFO	Burst flag out	O	Burst flag output
9	IDO	Line ID out	O	Line ID PAL: High = (R-Y) +, low = (R-Y) - SECAM: High = B-Y, low = R-Y
10	SSG $V_{SS}$	$V_{SS}$ for SSG	$V_{SS}$	SSG (SYNC signal generator) ground
11	FF SCO	4fsc out	O	4fsc output
12	PAD $V_{SS}$	$V_{SS}$ for PAD	$V_{SS}$	PAD $V_{SS}$
13	X4FSCI	4fsc osc in	osc	4fsc oscillator circuit input (NTSC: 4fsc = 14.31818 MHz)
14	X4FSCO	4fsc osc out	osc	4fsc oscillator circuit output (PAL/SECAM: 4fsc = 17.734475 MHz)
15	SCO	Sub carrier out	O	fsc output
16	CCK	C clock for DAC	O	Clock output for chroma signal (C) D/A converter; frequency = 4fsc
17	CO (8)	Chroma out (8): MSB	O	Chroma signal (C) output (Data format: offset binary)
18	CO (7)	Chroma out (7)	O	
19	CO (6)	Chroma out (6)	O	
20	CO (5)	Chroma out (5)	O	
21	CO (4)	Chroma out (4)	O	
22	CO (3)	Chroma out (3)	O	
23	CO (2)	Chroma out (2)	O	
24	CO (1)	Chroma out (1): LSB	O	
25	TEST1	Test 1	I	Test pin: Fix at the low level
26	YCK	Y clock for DAC	O	Clock output for luminance signal (Y) D/A converter; frequency = 4fsc
27	YO (8)	Y out (8): MSB	O	Luminance signal (Y) output
28	YO (7)	Y out (7)	O	
29	YO (6)	Y out (6)	O	
30	YO (5)	Y out (5)	O	
31	YO (4)	Y out (4)	O	
32	YO (3)	Y out (3)	O	
33	YO (2)	Y out (2)	O	
34	YO (1)	Y out (1): LSB	O	

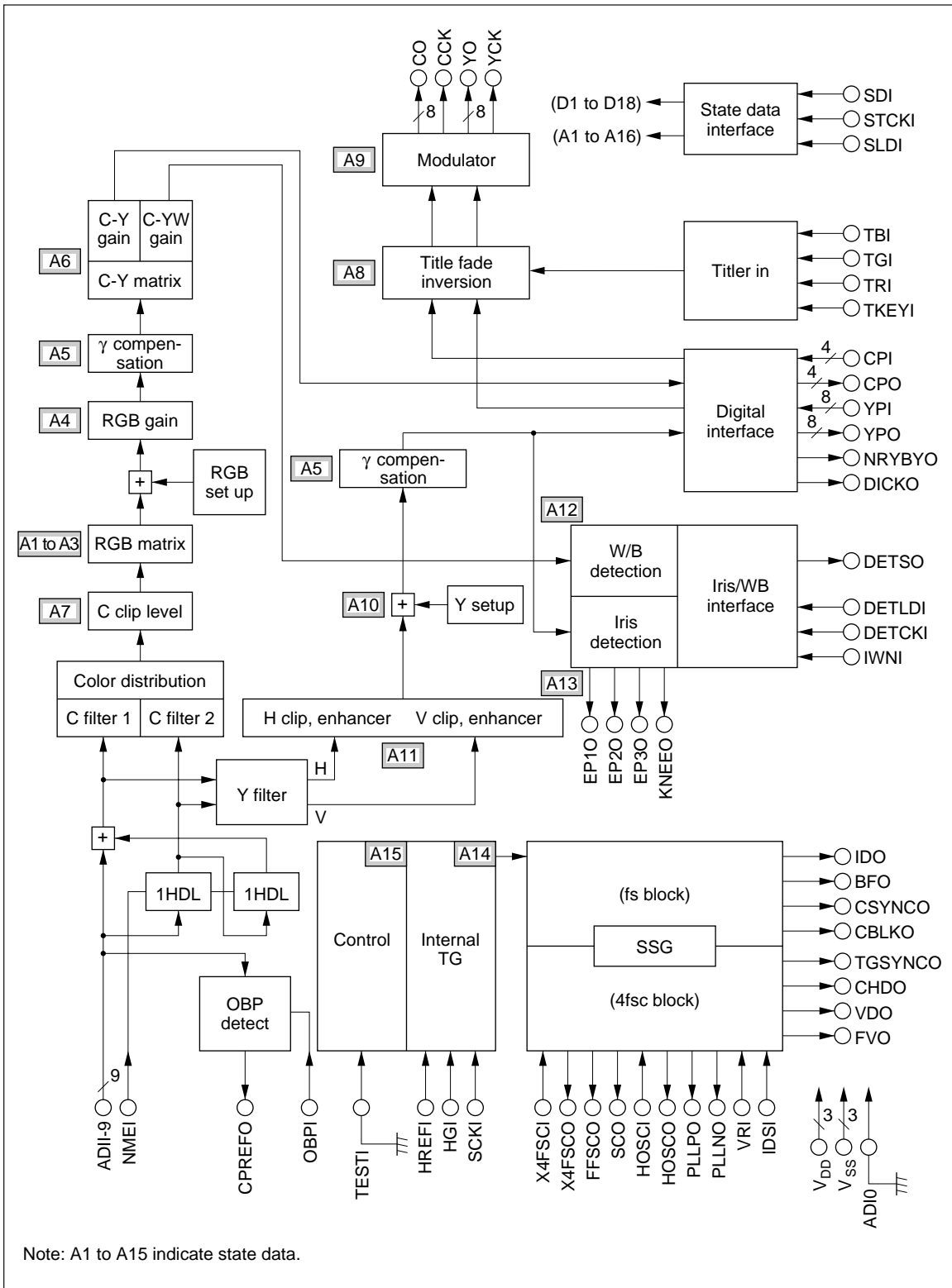
## Pin Functions (cont)

Pin No.	Pin Name	Signal	I/O	Function Description
35	YPO (8)	Y pararell out (8): MSB	O	Y digital interface output
36	YPO (7)	Y pararell out (7)	O	Outputs the post-gamma compensation Y signal
37	YPO (6)	Y pararell out (6)	O	
38	CORE V <sub>DD</sub>	V <sub>DD</sub> for core	V <sub>DD</sub>	V <sub>DD</sub> for core, V <sub>DD</sub> = 5 V <sup>+0.25 V</sup> <sub>-0.50 V</sub>
39	YPO (5)	Y pararell out (5)	O	Y digital interface output
40	YPO (4)	Y pararell out (4)	O	
41	YPO (3)	Y pararell out (3)	O	
42	YPO (2)	Y pararell out (2)	O	
43	YPO (1)	Y pararell out (1): LSB	O	
44	YPI (8)	Y pararell in (8): MSB	I	Y digital interface input
45	YPI (7)	Y pararell in (7)	I	
46	YPI (6)	Y pararell in (6)	I	
47	YPI (5)	Y pararell in (5)	I	
48	YPI (4)	Y pararell in (4)	I	
49	YPI (3)	Y pararell in (3)	I	
50	YPI (2)	Y pararell in (2)	I	
51	YPI (1)	Y pararell in (1): LSB	I	
52	CPO (4)	C pararell out (4): MSB	O	C digital interface output (data format: two's complement) Color difference signals R-Y and B-Y Upper to lower order
53	CPO (3)	C pararell out (3)	O	
54	CPO (2)	C pararell out (2)	O	
55	CPO (1)	C pararell out (1): LSB	O	
56	CPI (4)	C pararell in (4): MSB	I	C digital interface input (data format: two's complement)
57	CPI (3)	C pararell in (3)	I	
58	CPI (2)	C pararell in (2)	I	
59	CPI (1)	C pararell in (1): LSB	I	
60	NRYBYO	R-Y, B-Y phase out	O	C digital interface phase output; high = (B-Y) phase, low = (R-Y) phase
61	DICKO	Digital interface clock out	O	Digital interface clock output, frequency = fs
62	CORE V <sub>SS</sub>	V <sub>SS</sub> for core	V <sub>SS</sub>	V <sub>SS</sub> for core
63	HREFI	Horizontal reference in	I	Horizontal scan reference signal Reference for memory start/stop, BF, CBLK, and CSYNC
64	HGI	Horizontal gate in	I	Line signals (two types) determination input; high = a, b; low = c, d (state data A7)
65	SCKI	Sensor clock in	I	Sensor clock (system clock) fs input
66	ADI (9)	AD in (9): MSB	I	A/D input
67	ADI (8)	AD in (8)	I	
68	ADI (7)	AD in (7)	I	

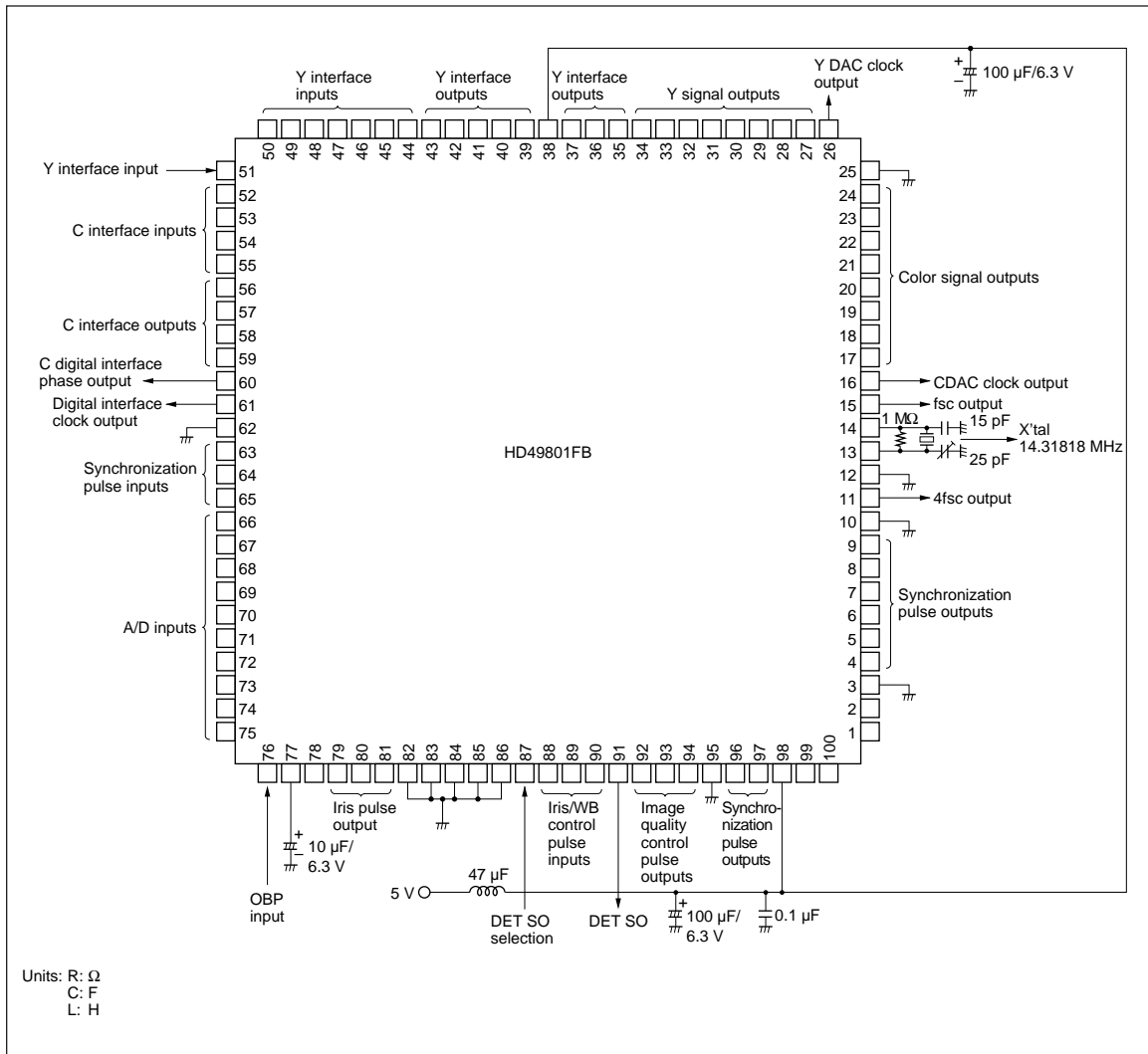
## Pin Functions (cont)

Pin No.	Pin Name	Signal	I/O	Function Description	
69	ADI (6)	AD in (6)	I	A/D input	
70	ADI (5)	AD in (5)	I		
71	ADI (4)	AD in (4)	I		
72	ADI (3)	AD in (3)	I		
73	ADI (2)	AD in (2)	I		
74	ADI (1)	AD in (1): LSB	I		
75	ADI (0)	AD in (0)	I	Fix at the low level	
76	OBPI	Optical black pulse in	I	Sensor optical black period input; high during the OB period	
77	CPREFO	Clamp reference out	O	Feedback clamp OBP detection output (0 V to 5 V)	
78	KNEEO	Knee point out	O	Knee point setting output; high = iris region 6	
79	EP3O	Iris V edge pulse 3 out	O	Iris V-window pulse 3 V direction iris setting region output	
80	EP2O	Iris V edge pulse 2 out	O		Iris V-window pulse 2
81	EP1O	Iris V edge pulse 1 out	O		Iris V-window pulse 1
82	TBI	Titler B in	I	Title color setting signal	
83	TGI	Titler G in	I		
84	TRI	Titler R in	I		
85	TKEYI	Titler key in	I	Title on/off signal; high = on, low = off	
86	NMEI	Memory enable bar in	I	Line memory R/W enable signal; high = disable, low = enable	
87	IWNI	Iris/white balance in	I	DETSO function selection (iris/WB) input; high = iris, low = WB	
88	PAD V <sub>DD</sub>	V <sub>DD</sub> for PAD	V <sub>DD</sub>	V <sub>DD</sub> for pad, V <sub>DD</sub> = 5 V <sup>+0.25 V</sup> <sub>-0.50 V</sub>	
89	DETLDI	DET load in	I	Iris/WB load pulse	
90	DETCKI	DET clock in	I	Iris/WB clock pulse	
91	DETSO	DET serial out	O	Iris: Average value (22b)/peak value (11b) WB: Mg-G (11b), R-B (11b)	
92	SLDI	State load in	I	Image quality control data (state data) load pulse	
93	STCKI	State clock in	I	Image quality control data (state data) clock pulse	
94	SDI	State data in	I	Image quality control data (state data) input	
95	IDSI	Line ID reset in	I	In PAL/SECAM mode, line ID reset input; high = reset	
96	TGSYNCO	TG sync out	O	TG CSYNC output	
97	CHDO	Camera HD out	O	Camera horizontal synchronization output	
98	SSG V <sub>DD</sub>	V <sub>DD</sub> for SSG	V <sub>DD</sub>	V <sub>DD</sub> for SSG, V <sub>DD</sub> = 5 V <sup>+0.25 V</sup> <sub>-0.50 V</sub>	
99	XHCKI	H osc in	osc	H oscillator input (NTSC: 260 f <sub>H</sub> = 4.090908 MHz)	
100	XHCKO	H osc out	osc	H oscillator output (PAL/SECAM: 282 f <sub>H</sub> = 4.40625 MHz)	

Block Diagram



Standard External Circuits



NTSC Standard External Circuits



**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

Item		Symbol	Rated Value	Unit
Power supply voltage		$V_{CC}$	-0.3 to +6.7	V
Pin voltage		$V_{ti}$	-0.3 to $V_{CC} + 0.3$	V
Pin voltage		$V_{to}$	-0.3 to $V_{CC} + 0.3$	V
Output voltages	Corresponding to one output	$I_o$	-16 to +16	mA
	Corresponding to one GND to $V_{CC}$	$I_{ot}$	-70 to +70	mA
Operating temperature		$T_{opr}$	-10 to +75	$^\circ\text{C}$
Storage temperature		$T_{stg}$	-55 to +125	$^\circ\text{C}$

- Notes: 1. This IC can be permanently damaged by operating at values in excess of its absolute maximum ratings. Furthermore, it is desirable to operate this IC within the conditions for the electrical characteristics specifications during normal operation. Exceeding those conditions can result in incorrect operation and a reduction in reliability.
2. All voltages are specified with GND = 0 V as the reference.
3. This IC is for use in consumer products. It should not be used in industrial products, or in products that will be used outdoors for extended periods.

**Electrical Characteristics** ( $V_{CC} = 5\text{ V}$ ,  $V_{IHC} = +0.25\text{ V}$ ,  $V_{ILC} = -0.50\text{ V}$ ,  $T_a = -10^\circ\text{C}$  to  $+75^\circ\text{C}$ )

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltages*	$V_{IHC}$	$V_{CC} \times 0.7$	—	—	V	CMOS levels
	$V_{ILC}$	—	—	$V_{CC} \times 0.3$	V	CMOS levels
Output voltages*	$V_{OH}$	2.4	—	—	V	$I_{OH} = 2/4\text{ mA}$
	$V_{OL}$	—	—	0.4	V	$I_{OL} = -2/-4\text{ mA}$
Input leakage current	$I_{LI}$	-1.0	—	1.0	$\mu\text{A}$	$V_{IN} = 0$ to $V_{CC}$
Output leakage current	$I_{LO}$	-1.0	—	1.0	$\mu\text{A}$	Output high impedance state
Current dissipation	$I_{CC}$	—	—	110	mA	With $V_{CC} = 5\text{ V}$ , and no load, $T_a = 25^\circ\text{C}$ , $f_{CLK} = 14.3\text{ MHz}$

Note: \* I/O voltage levels are measured in steady state.



**Crystal Oscillator Circuit**

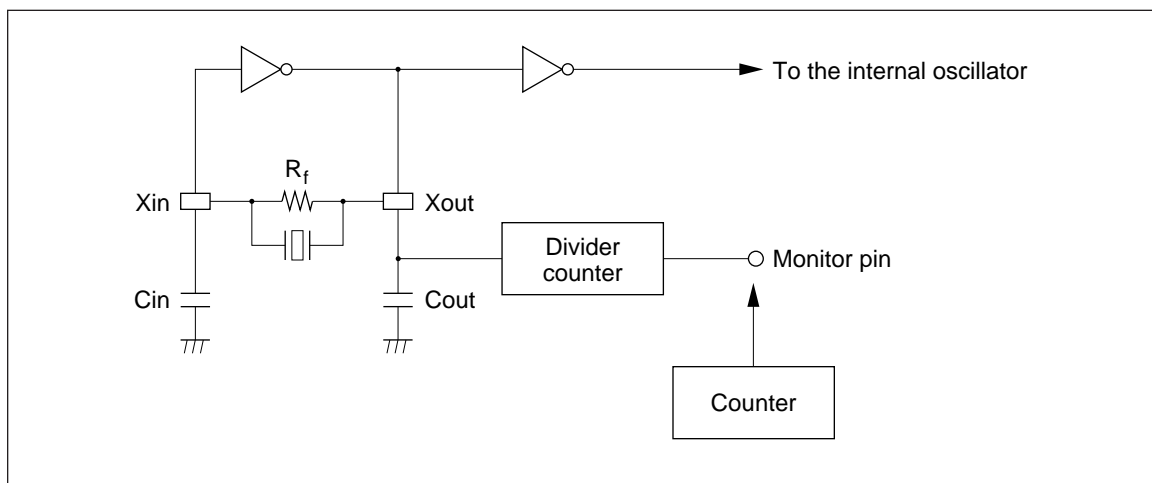
- Test conditions

$V_{CC} = 5\text{ V} \pm 5\%$   
 $C_{in}, C_{out} = 22\text{ pF}$   
 $R_f = 10\text{ M}\Omega$

- Test method

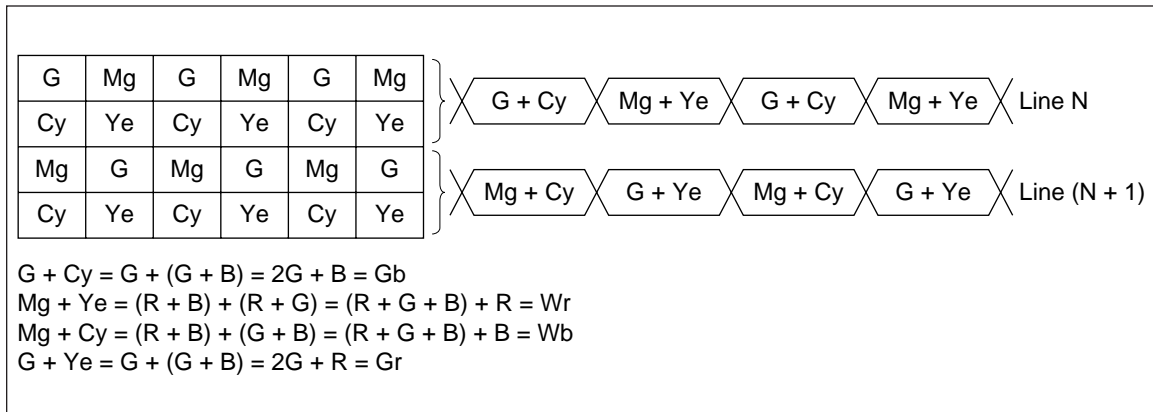
Test at  $f_{min} = 8\text{ MHz}$  and  $f_{max} = 20\text{ MHz}$  under the above conditions.

Note that the oscillator start time ( $t_{osc\ max}$ ) is 250 ms.



**Test Circuit**

**Overview of Pixel Mixing CCD-RGB Simultaneous Processing**



**Pixel Mixing CCD Mode Figure**

RGB matrix

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} K_{Gb,r} & K_{Wr,r} & K_{Wb,r} & K_{Gr,r} \\ K_{Gb,g} & K_{Wr,g} & K_{Wb,g} & K_{Gr,g} \\ K_{Gb,b} & K_{Wr,b} & K_{Wb,b} & K_{Gr,b} \end{bmatrix} \begin{bmatrix} Gb \\ Wr \\ Wb \\ Gr \end{bmatrix}$$

Y matrix

- Line N  
 $Y = Gb + Wr = (2G + B) + (2R + G + B) = 2R + 3G + 2B$
- Line (N + 1)  
 $Y = Wb + Gr = (R + G + 2B) + (2G + R) = 2R + 3G + 2B$

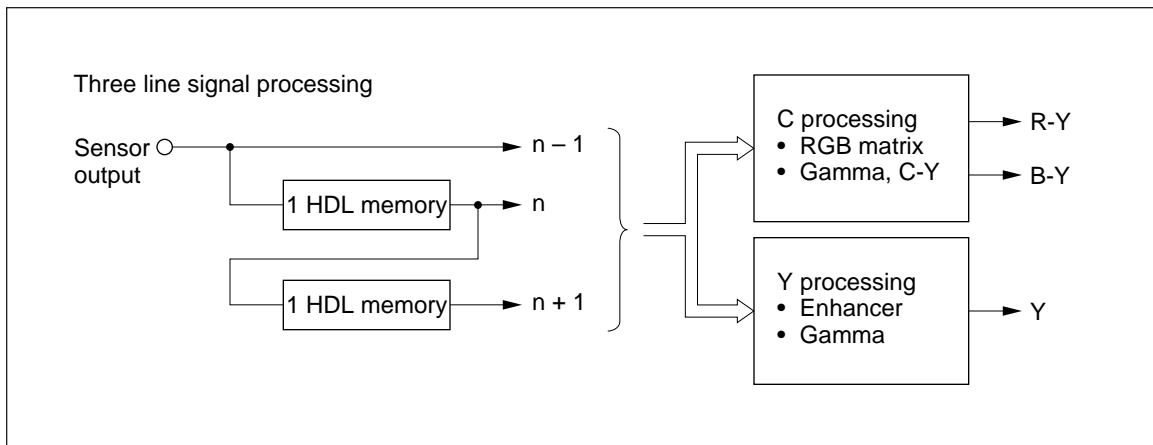
**Line Signal Processing**

RGB matrix

$$\begin{bmatrix} R_{n+1} \\ G_{n+1} \\ B_{n+1} \end{bmatrix} = A \begin{bmatrix} G_{bn} \\ W_{rn} \\ (W_{bn-1} + W_{bn+1})/2 \\ (G_{rn-1} + G_{rn+1})/2 \end{bmatrix}$$

C-Y matrix

$$\begin{bmatrix} (R-Y)_{n+1} \\ (B-Y)_{n+1} \end{bmatrix} = C \begin{bmatrix} R_{n+1} \\ G_{n+1} \\ B_{n+1} \end{bmatrix} = CA \begin{bmatrix} G_{bn} \\ W_{rn} \\ (W_{bn-1} + W_{bn+1})/2 \\ (G_{rn-1} + G_{rn+1})/2 \end{bmatrix}$$



**CCD Camera RGB Simultaneous Processing**



**State Data Details**

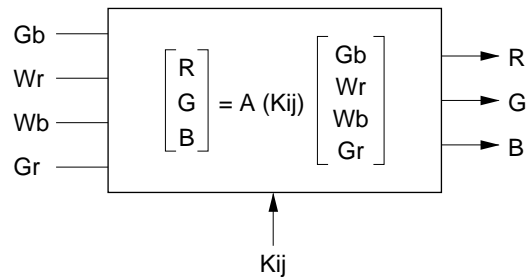
The following items describe the state data (A1 to A16) in detail.

**State Data A1 to A3: RGB matrix**

This data specifies color reproducibility and moire pattern suppression.

Coefficient $K_{Gb, j}$								Coefficient $K_{Wr, j}$								Coefficient $K_{Wb, j}$								Coefficient $K_{Gr, j}$								Address															
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	0	D	D				
11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	0	0	D	D
Mantissa								Exponent																		(j = RGB)																					

Address	Matrix
0 0 0 0	R
0 0 0 1	G
0 0 1 0	B



$$K_{ij} = (-1)^{D_{11}} \cdot 2^{-(D_{10} \times 2^1 + D_9 \times 2^0)} \cdot (D_8 \times 2^{-1} + D_7 \times 2^{-2} + D_6 \times 2^{-3} + D_5 \times 2^{-4} + D_4 \times 2^{-5} + D_3 \times 2^{-6} + D_2 \times 2^{-7} + D_1 \times 2^{-8})$$

Where: i = Gb, Wr, Wb, Gr  
j = R, G, B

Determine the size of the coefficients so that  $\text{MAX}(K_{Gb,j}, K_{Wr,j}, K_{Wb,j}, K_{Gr,j}) = 255/256(000111111111)$ .

**State Data A4: W/B RGB gain**

This data adjusts the amplitude of the color signal and determines the color reproducibility. It also adjusts the white balance for images of white objects.

R gain: $G_R$								G gain: $G_G$								B gain: $G_B$								Address												
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	0	1	1	
11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	0	0	1	1
Mantissa								Exponent																												

$$G_i = 2 (D_{11} \times 2^2 + D_{10} \times 2^1 + D_9 \times 2^0 + 1) \cdot (D_8 \times 2^{-1} + D_7 \times 2^{-2} + D_6 \times 2^{-3} + D_5 \times 2^{-4} + D_4 \times 2^{-5} + D_3 \times 2^{-6} + D_2 \times 2^{-7} + D_1 \times 2^{-8})$$

**HD49801FB****HD49801FB**

	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	Gi
Max	1	0	1	1	1	1	1	1	1	1	1	$2^6 \times 255/256$
				⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
				1	0	0	0	0	0	0	0	$2^6 \times 128/256$
	1	0	0	1	1	1	1	1	1	1	1	$2^5 \times 255/256$
			⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
			1	0	0	0	0	0	0	0	0	$2^5 \times 128/256$
	0	0	1	1	1	1	1	1	1	1	1	$2^2 \times 255/256$
			⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
			1	0	0	0	0	0	0	0	0	$2^2 \times 128/256$
	0	0	0	1	1	1	1	1	1	1	1	$255/256$
			⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Min				0	0	0	0	0	0	0	0	0

- Setting the gains

- Set up the RGB matrix.

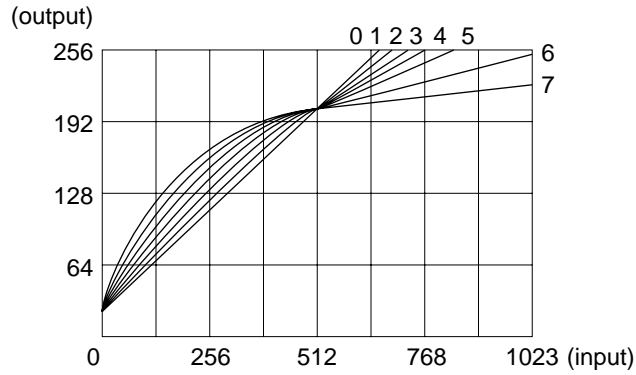
- Adjust the black level for the above matrix.

- Hold  $G_R$  and  $G_B$  at 0, and increase  $G_G$ . Determine the gain at which the output signal is saturated, and take half of that gain to be the rated gain.

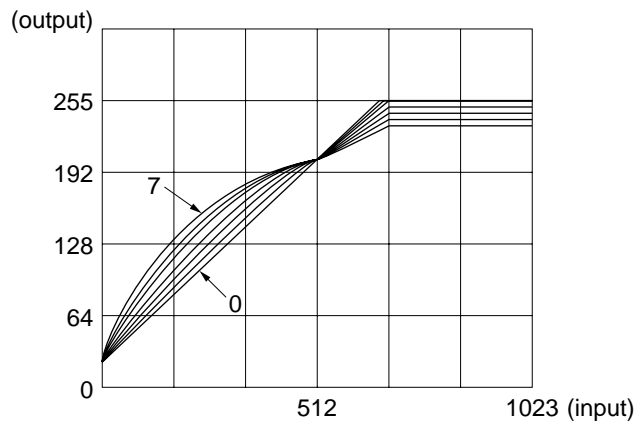
- Determine  $G_R$  and  $G_B$  for the gain  $G_G$  determined above.

**State Data A5:  $\gamma$  characteristics**

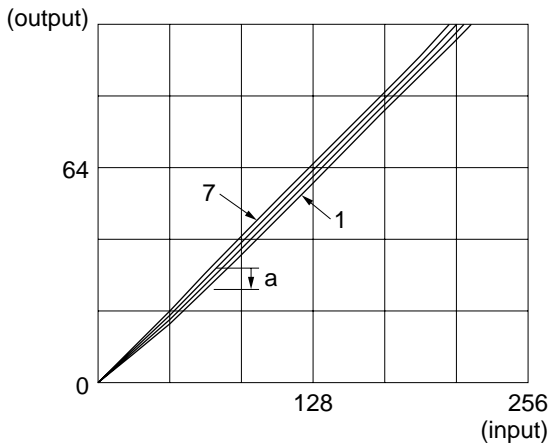
One of eight different curves can be selected for the  $\gamma$  characteristics by specifying the value (0 to 7) of this state data item.



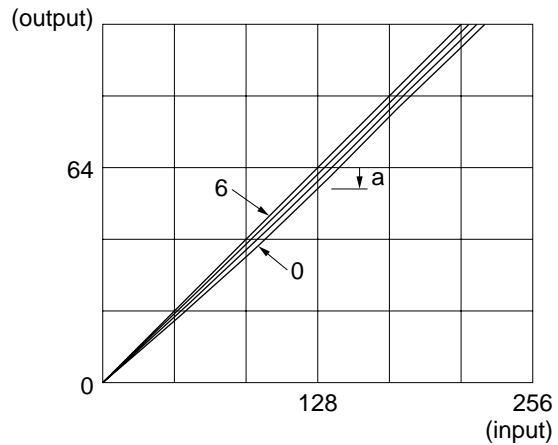
(1) Y- $\gamma$  I/O characteristics (state data values 0 to 7)



(2) C- $\gamma$  I/O characteristics (state data values 0 to 7)



(3) CL- $\gamma$  I/O characteristics  
(state data values 0, 2, 4, and 6)  
C- $\gamma$  state data value 0  
(shifted by only the amount  $a$   
from the output level of (2))



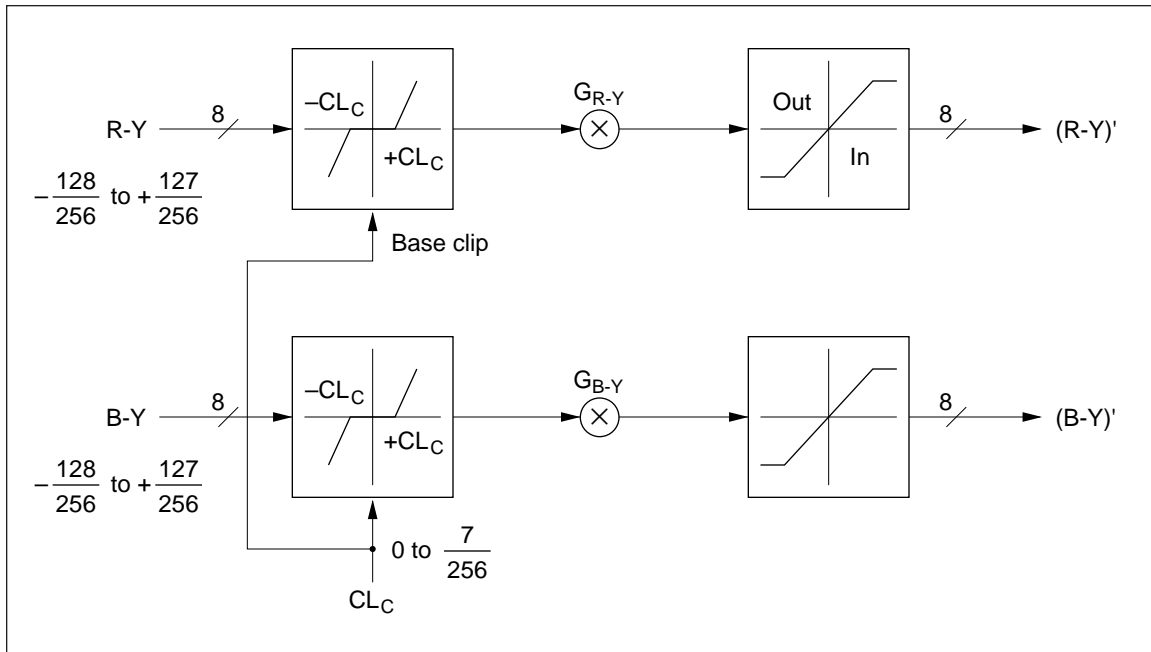
(4) CL- $\gamma$  I/O characteristics  
(state data values 1, 3, 5, and 7)  
C- $\gamma$  state data value 0  
(shifted by only the amount  $a$   
from the output level of (2))

**State Data A6:** Color difference gain, base clip

This data determines the signal levels of the color difference signals.

C clip $CL_C$			R-Y gain $G_{R-Y}$							R-Y gain $G_{R-Y}$							Address			
D3	D2	D1	D7	D6	D5	D4	D3	D2	D1	D7	D6	D5	D4	D3	D2	D1	0	1	0	1

- Color difference gain control characteristics



$$G_{R-Y}, G_{B-Y} = D7 \times 2^0 + D6 \times 2^{-1} + D5 \times 2^{-2} + D4 \times 2^{-3} + D3 \times 2^{-4} + D2 \times 2^{-5} + D1 \times 2^{-6} \quad (0 \text{ to } 2)$$

- Base clip level control characteristics

$$C_{LC} \text{ max} = 7/256 = 0.0273437$$

$$C_{LC} = D3 \times 2^{-6} + D2 \times 2^{-7} + D1 \times 2^{-8}$$

- Setting the gains

- The ratio of the gains R-Y and B-Y is determined by the color reproduction.
- Increase the color difference gain from the gain ratio from item (a) above.
- Set the gain to have a 10% to 20% margin from the gain at the point the output signal clips in item (b) above.  
I.e., (set gain) = (clipping gain)  $\times$  0.8 to 0.9





**State Data A8 (1 to 3): Encoder (FADE)**

This data determines the fade level for the luminance and chroma signals.

	Address H				Address			Data							
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
1								Y fade							
	1	1	1	0	0	0	0	D1	D2	D3	D4	D5	D6	D7	D8
2								C fade							
	1	1	1	0	1	0	0	D1	D2	D3	D4	D5	D6	D7	D8
3					Y inversion →			← C inversion							
	1	1	1	0	0	1	0	D1	D2						

1: Y fade

D8 = 1: Through

When D8 = 0, the following weighting formula is used.

$$D7 \times 2^{-1} + D6 \times 2^{-2} + D5 \times 2^{-3} + D4 \times 2^{-4} + D3 \times 2^{-5} + D2 \times 2^{-6}$$

D1 is fixed at 0.

Note: However, since the encoder fade precision is inadequate, improved fading characteristics can be obtained by using the iris function for Y fading.

2: C fade

$$D8 \times 2^0 + D7 \times 2^{-1} + D6 \times 2^{-2} + D5 \times 2^{-3} + D4 \times 2^{-4} + D3 \times 2^{-5} + D2 \times 2^{-6} + D1 \times 2^{-7}$$

Range: 1 to 255/128

3: Y and C inversion

D1 = 0; D2 = 0: Normal

D1 = 1; D2 = 1: Inversion

**State Data A9: 1 to 4 (MOD)**

Determines the luminance signal black level and the chroma signal burst level. These four data items determine the (R-Y) burst level for PAL format TV signals.

	Address H				Address		Data							
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
1							BLK level							
	0	0	0	1	0	0	D1	D2	D3	D4	D5	D6	D7	D8
2							Pedestal*							
	0	0	0	1	1	0	D1	D2	D3	D4	D5	D6	D7	D1
3							Burst level (B-Y)							
	0	0	0	1	0	1	D1	D2	D3	D4	D5	D6	D7	
4							Burst level (R-Y)							
	0	0	0	1	1	1	D1	D2	D3	D4	D5	D6	D7	

Note: Set D1 according to the delay sensor clock as follows.  
 14.3 MHz: D1 = 1  
 9.5 MHz: D1 = 0

- State data A9 (1 to 4): Encoder (MOD) control characteristics

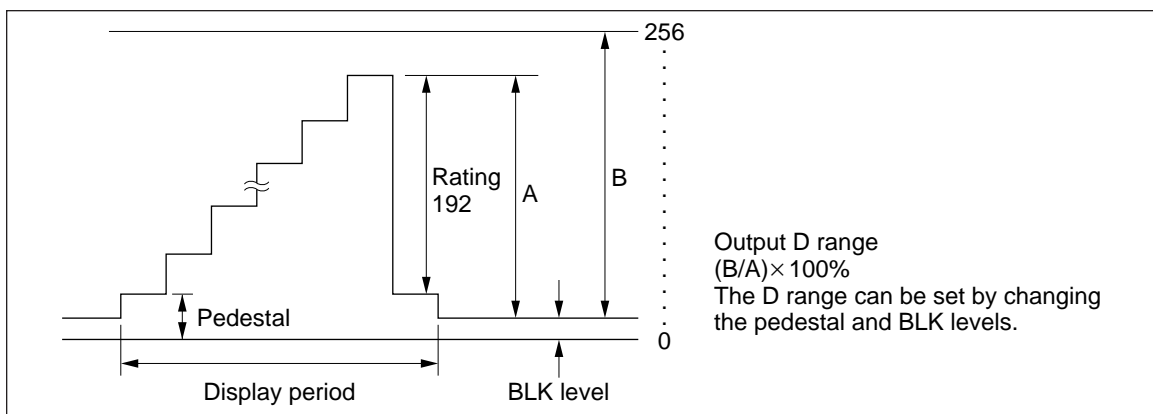
1: Setup  
 $(D7 \times 2^6 + D6 \times 2^5 + D5 \times 2^4 + D4 \times 2^3 + D3 \times 2^2 + D2 \times 2^1 + D1) \times 2/256$

2: Pedestal  
 $D7 \times 2^6 + D6 \times 2^5 + D5 \times 2^4 + D4 \times 2^3 + D3 \times 2^2 + D2 \times 2^1 + D1/256$

Note: However, when the A9 to A2 D8 bit (delay) is set to 1, the Y data is delayed by one fs clock cycle.

3: Burst level (B-Y)  
 $D7 \times 2^6 + D6 \times 2^5 + D5 \times 2^4 + D4 \times 2^3 + D3 \times 2^2 + D2 \times 2^1 + D1/256$

- 4: Burst level (R-Y)
- Used in PAL mode
  - In NTSC mode, used for phase adjustment

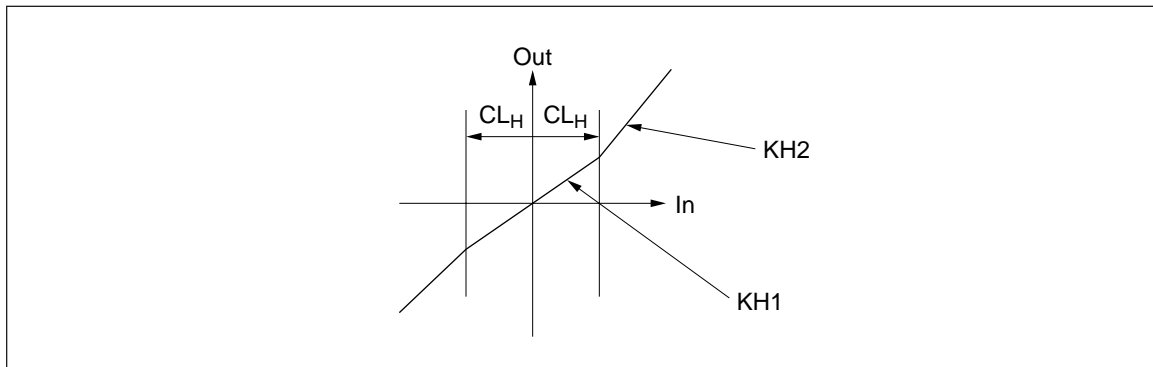




**State Data A11: H and V enhancer**

This data specifies boundary compensation on video signals.

H enhancer frequency characteristics		H enhancer noise coefficient: KH1					V base clip CL <sub>V</sub>				V enhancer noise coefficient: K <sub>V</sub>					H base clip CL <sub>H</sub>				H enhancer coefficient: KH2					Address			
D2	D1	D5	D4	D3	D2	D1	D4	D3	D2	D1	D5	D4	D3	D2	D1	D4	D3	D2	D1	D5	D4	D3	D2	D1	1	0	1	0



$KH1, KH2, K_V = D5 \times 2^{-1} + D4 \times 2^{-2} + D3 \times 2^{-3} + D2 \times 2^{-4} + D1 \times 2^{-5}$  (0 to 1)  
 $CL_V, CL_H = D4 \times 2^3 + D3 \times 2^2 + D2 \times 2^1 + D1 \times 2^0 / 1024$

**H Enhancer: Frequency characteristics**

D2	D1	Peak Frequency
0	0	0.25 fs
0	1	0.25 fs
1	0	0.275 fs
1	1	0.3 fs

**State Data A12 (1 to 5):** White balance detection

This data determines the white balance detection region, sets the dead band, and determines the control range.

	Address H				Address			Data														
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	
1								R-Y gain				B-Y gain										
	1	1	0	1	0	0	0	D1	D2	D3	D4	D1	D2	D3	D4							
2								Y level 1				Y level 2										
	1	1	0	1	1	0	0	D1	D2	D3	D4	D1	D2	D3	D4							
3								Offset ⊕						Offset ⊖								
	1	1	0	1	0	1	0	D1	D2	D3	D4	D5	D6	D1	D2	D3	D4	D5	D6			
4								C level 1 ⊕							C level 1 ⊖							
	1	1	0	1	1	1	0	D1	D2	D3	D4	D5	D6	D7	D1	D2	D3	D4	D5	D6	D7	
5								C level 2 ⊕							C level 2 ⊖							
	1	1	0	1	0	0	1	D1	D2	D3	D4	D5	D6	D7	D1	D2	D3	D4	D5	D6	D7	

- 1: R-Y gain, B-Y gain  
 These adjust the R-B/Mg-g detection axis.  
 $Gain = D4 \times 2^{-1} + D3 \times 2^{-2} + D2 \times 2^{-3} + D1 \times 2^{-4}$
- 2: Y level 1, Y level 2  
 When the Y signal is used as the white detection area data, the Y signal detection range is set by Y level 1 (lower bits) and Y level 2 (upper bits).  
 The data consists of 8 bits, and the upper 4 bits (D1 to D4) can be changed.
- 3: Offset  
 The control center can be shifted by setting the offset.  
 Of the 8 bits of this data, the data that can be changed consists of 6 bits ( $64/256 = 1/4$ ), and the offset level can be changed over up to 1/4 of the full data range.

4, 5: C levels

This data specifies the white detection region.

Of all 8 bits of this data, the data that can be changed consists of 7 bits ( $128/256 = 1/2$ ), and the white detection region can be changed over up to 1/2 of the full data range.

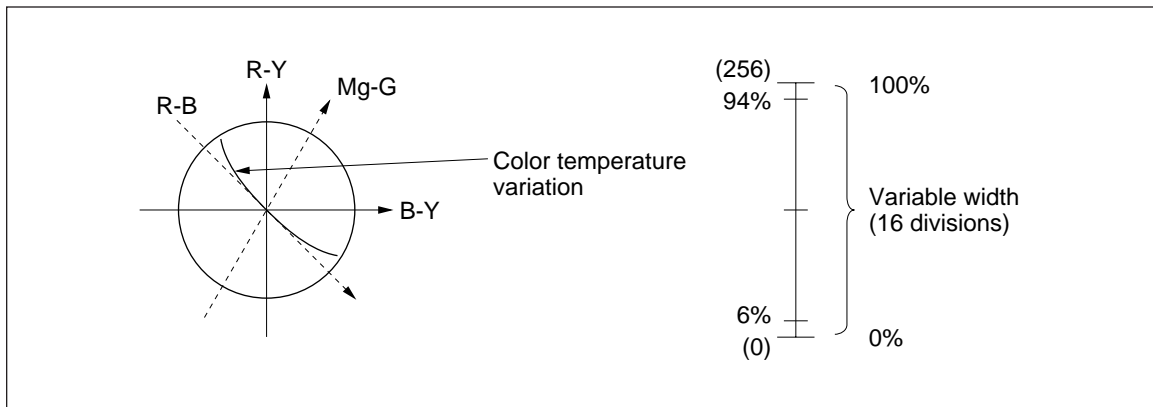
The C level data correspondences are as follows:

C level 1(+) → The down direction of the (Mg-G) signal.

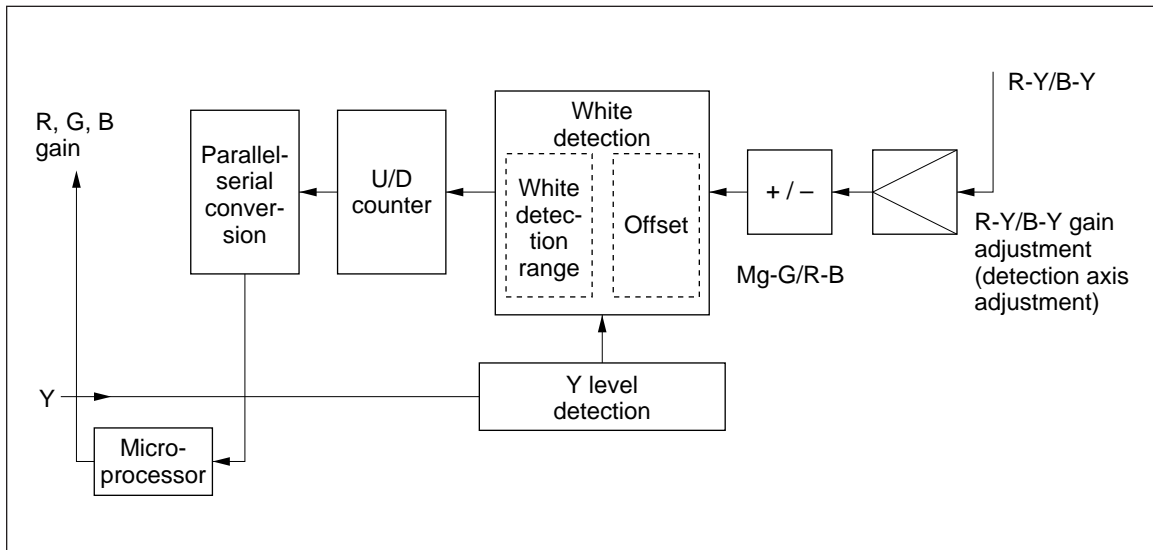
C level 1(-) → The down direction of the (R-B) signal.

C level 2(+) → The up direction of the (Mg-G) signal.

C level 2(-) → The up direction of the (R-B) signal.



Y Detection Variable Width



White Balance Detection Block Diagram

State Data A13 (1 to 16): Iris

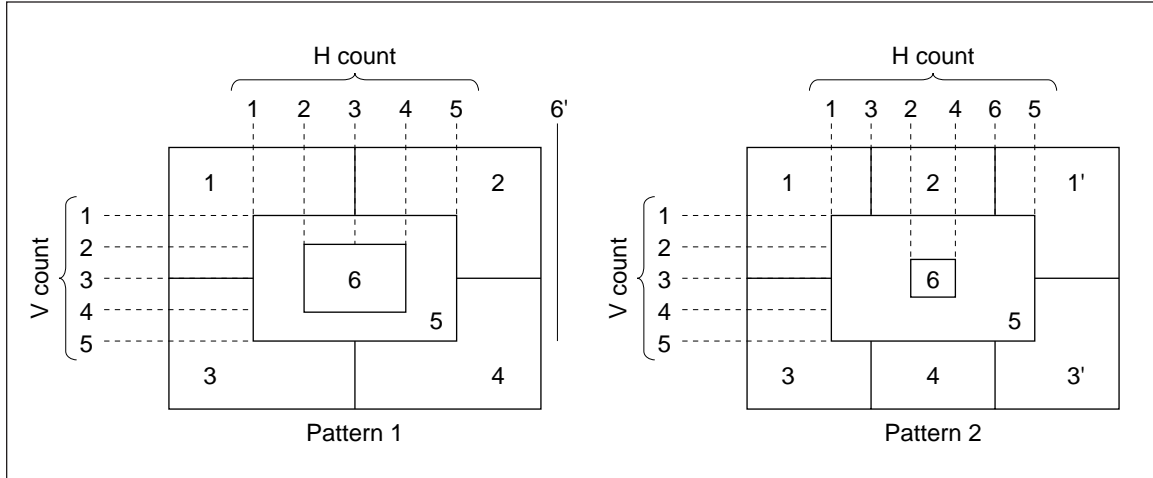
This data determines the regions required for iris control, and selects the type of iris data to be extracted.

	Address H				Address				Data									
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18
1									H count 1									
	0	0	1	1	0	0	0	0	D1	D2	D3	D4	D5					
2									H count 2									
	0	0	1	1	1	0	0	0	D1	D2	D3	D4	D5					
3									H count 3									
	0	0	1	1	0	1	0	0	D1	D2	D3	D4	D5					
4									H count 4									
	0	0	1	1	1	1	0	0	D1	D2	D3	D4	D5					
5									H count 5									
	0	0	1	1	0	0	1	0	D1	D2	D3	D4	D5					
6									H count 6									
	0	0	1	1	1	0	1	0	D1	D2	D3	D4	D5					
7																		
	0	0	1	1	0	1	1	0										
8																		
	0	0	1	1	1	1	1	0										
9									V count 1									
	0	0	1	1	0	0	0	1	D1	D2	D3	D4	D5					
10									V count 2									
	0	0	1	1	1	0	0	1	D1	D2	D3	D4	D5					
11									V count 3									
	0	0	1	1	0	1	0	1	D1	D2	D3	D4	D5					
12									V count 4									
	0	0	1	1	1	1	0	1	D1	D2	D3	D4	D5					
13									V count 5									
	0	0	1	1	0	0	1	1	D1	D2	D3	D4	D5					
14									Peak detection region									
	0	0	1	1	1	0	1	1	D1	D2	D3							
15									Knee									
	0	0	1	1	0	1	1	1	D1	D2								
16									Iris region									
	0	0	1	1	1	1	1	1	D1	D2	D3							



- Iris

Pattern 1 is selected if the H count 6 is in the blanking period, and pattern 2 is selected otherwise.



The screen is divided into 6 regions

- The full integrated value (the average value of Y following  $\gamma$  processing) for each region is calculated for each field.
- Also, once for each field, the peak value for region 1 is detected.
- However, the detection region can be set to an arbitrary region (regions 1 to 6).

Each region can be changed in units of 32 fs<sup>-1</sup> horizontally, and 16 lines vertically.

State Data	D3	D2	D1	Region
	0	0	0	1
	0	0	1	2
	0	1	0	3
	0	1	1	4
	1	0	0	5
	1	0	1	6
	1	1	0	Peak data

Note: For the peak data, the region is specified by the A13 to A14 peak detection region.

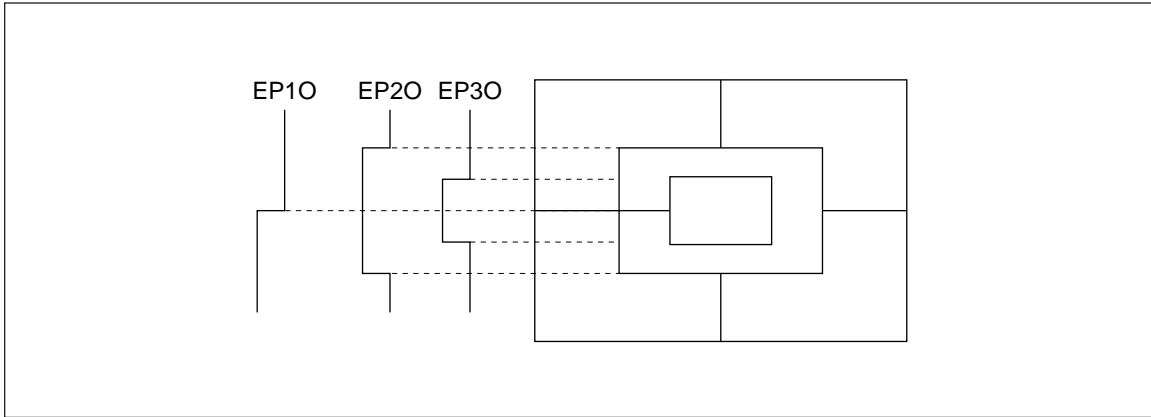
Iris control is performed with the average value acquired by adding the weighted average values for each region.

$$Y = \frac{\sum_{i=1}^6 Y_i \cdot k_i}{\sum_{i=1}^6 k_i}$$

Where: Y: The average value for a single field.  
 Y<sub>i</sub>: The average value for each region.  
 k<sub>i</sub>: The weighting for each region.

- The meaning and use of EP1O, EP2O, and EP3O

These operate as the iris V window pulses, and output V direction edge pulses for the iris detection region.



**State Data A14 (1 to 16): H synchronization pulse timing**

This data specifies both the data acquisition timing conforming to that required by the CCD sensor as well as the horizontal synchronization pulse generation.

	Address H				Address				Data									
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18
1									Memory R/W start									
	1	0	1	1	0	0	0	0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
2									Memory R/W stop									
	1	0	1	1	1	0	0	0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
3									H synchronization pulse 1									
	1	0	1	1	0	1	0	0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
4									H synchronization pulse 2									
	1	0	1	1	1	1	0	0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
5																		
	1	0	1	1	0	0	1	0										
6																		
	1	0	1	1	1	0	1	0										
7																		
	1	0	1	1	0	1	1	0										
8																		
	1	0	1	1	1	1	1	0										
9									H synchronization pulse 3									
	1	0	1	1	0	0	0	1	D1	D2	D3	D4	D5	D6	D7	D8		
10									H synchronization pulse 4									
	1	0	1	1	1	0	0	1	D1	D2	D3	D4	D5	D6	D7	D8		
11									H synchronization pulse 5									
	1	0	1	1	0	1	0	1	D1	D2	D3	D4	D5	D6	D7	D8		
12									H synchronization pulse 6									
	1	0	1	1	1	1	0	1	D1	D2	D3	D4	D5	D6	D7	D8		
13									H synchronization pulse 7									
	1	0	1	1	0	0	1	1	D1	D2	D3	D4	D5	D6	D7	D8		
14									H synchronization pulse 8									
	0	0	1	1	1	0	1	1	D1	D2	D3	D4	D5	D6	D7	D8		
15									H synchronization pulse 9									
	1	0	1	1	0	1	1	1	D1	D2	D3	D4	D5	D6	D7	D8		
16																		
	1	0	1	1	1	1	1	1										

**State Data A16 (1 to 2):** Mode setting

This data determines the handling of the TV format, whether the digital interface is used, and the data input format.

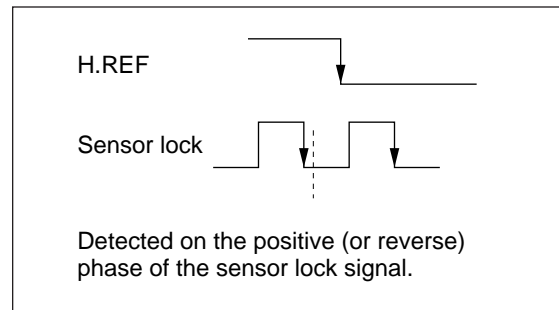
	Address H				L																							
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28
1					0	SECAM	PAL	HCKC	DCKC	NE	PLLON	DCE	GE	Test mode														
2	1	1	1	1	1	All 0																						

- TV format

SECAM	PAL	
0	0	NTSC
0	1	PAL
1	0	SECAM

- HCKC: REF and OBP latch phase

1: Positive phase (rising edge)  
0: Reverse phase (falling edge)



- DCKC: AD1 to AD9 latch phase

1: Positive phase (rising edge)  
0: Reverse phase (falling edge)

- NE

1: Does not encode  
0: Does encode

Note: When NE is set to 1, no encoding is performed, and the color difference signal is output from the CO pin without modulation.  
The HD49801FB should normally be used with NE = 0.

- DCE: Digital interface control

1: On  
0: Off

- PLLON

Set to 1 when locking externally in NTSC mode.

- GE: Grey code enable

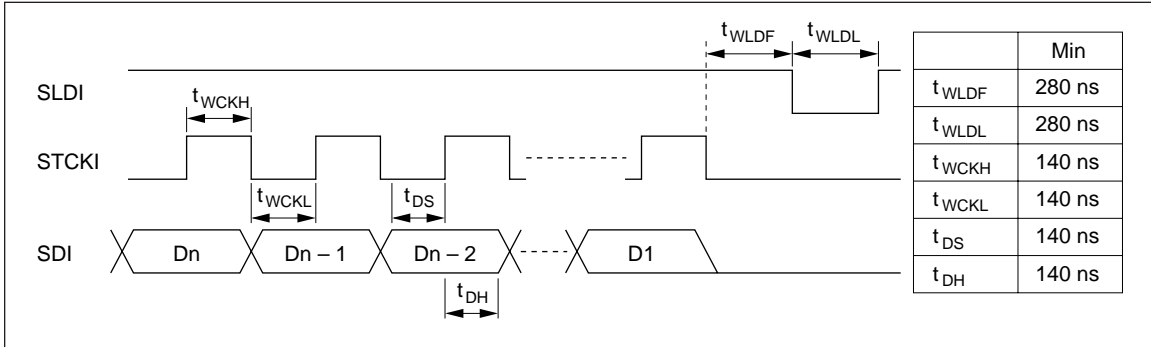
1: Grey code  
0: Binary code

- A2 to A16 are for use in test mode, and D6 to D28 should be set to all zeros in advance.

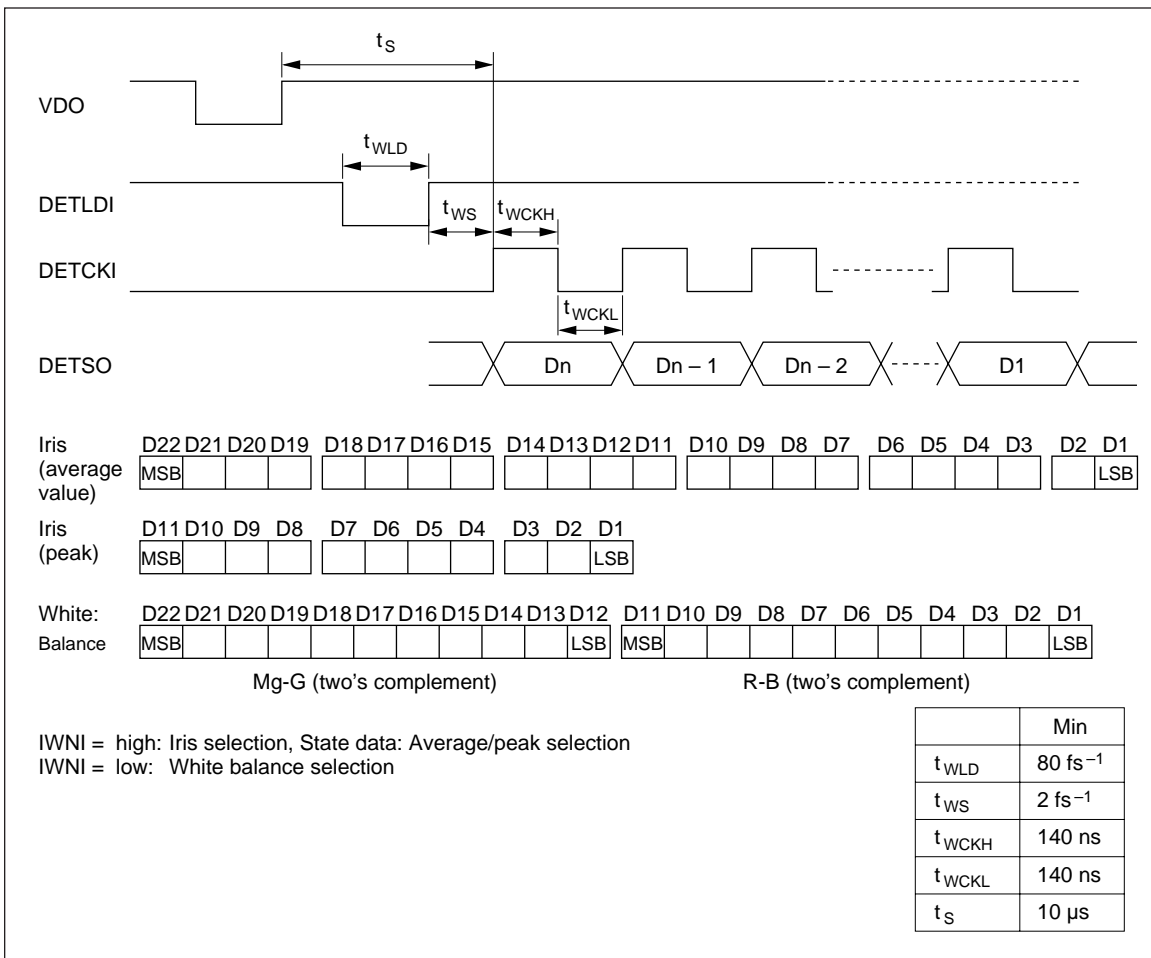
State Data Transfer Timing Specifications

Image Quality Control Protocol Timing

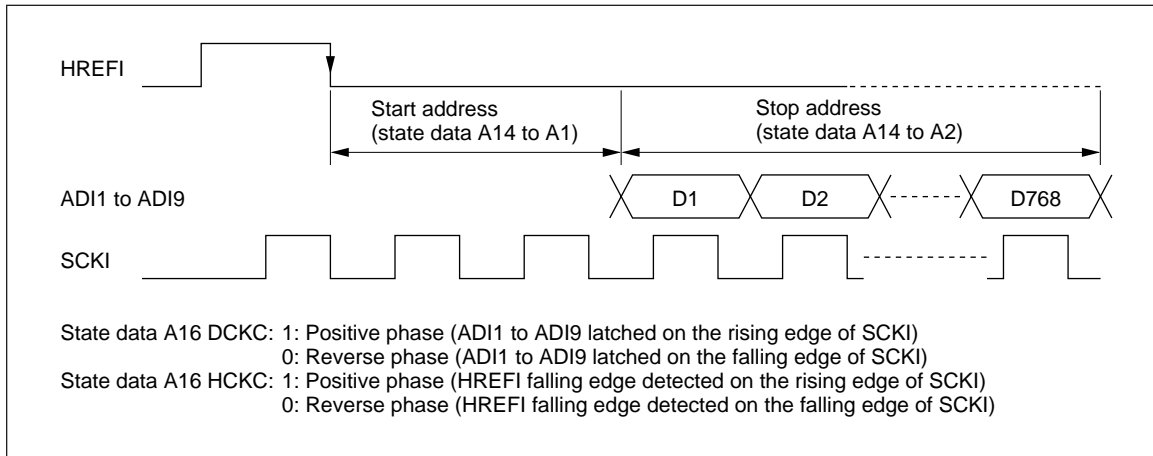
- Image quality control data (state data) transfer protocol



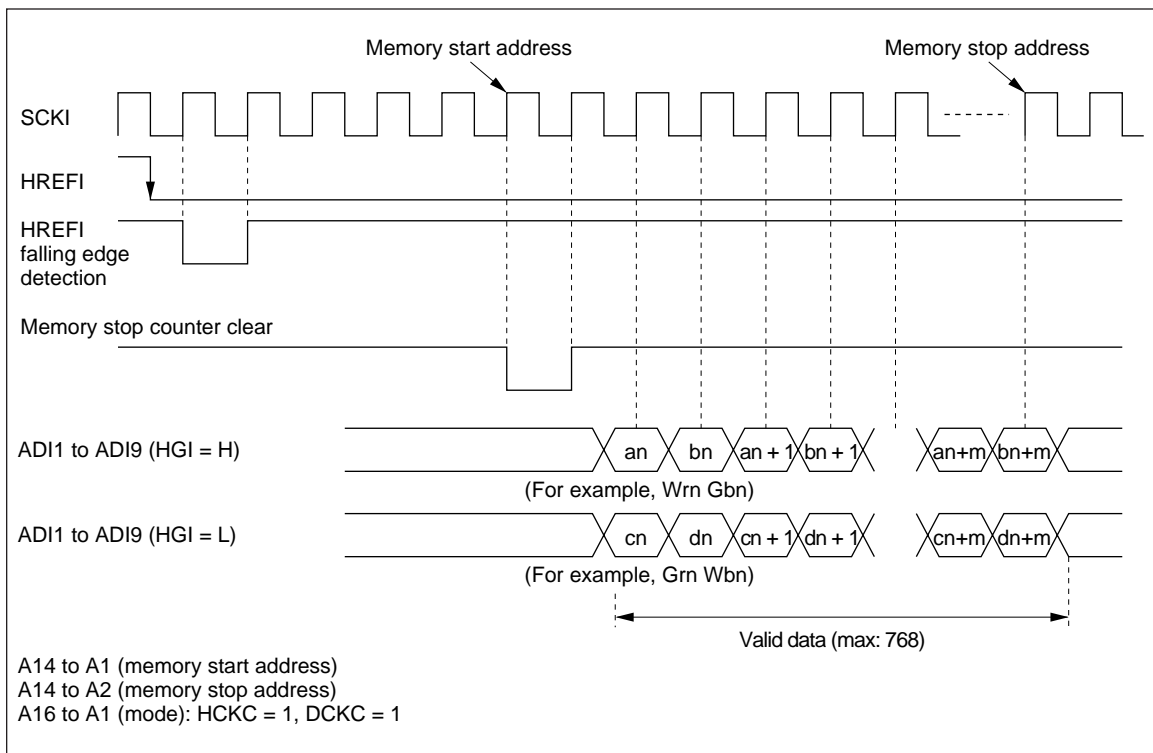
- Iris, W/B data transfer protocol



- A/D input data (line delay memory R/W) transfer protocol



- Line delay memory R/W setting example



The relationship between the CCD sensor complementary color signals (Wrn, Gbn, Grn, and Wbn) and state data A7 (a, b, c, d) is determined by the relationship between the HGI input and the start address.

HGI is a line determination input, and when high, the two complementary color signals correspond to (a, b), and when low, they correspond to (c, d).

- Definition of H.REF
  - H.REF is the standard for determining:
    - Memory R/W start/stop timing
    - BF, CBLK, CSYNC pulse timing
- Conditions required of H.REF
  - H.REF is a pulse generated from the sensor clock (fs), and must be phase stable with respect to fs.
  - It must be a continuous pulse with no missing pulse periods during the BLK or other period.
  - Synchronization is horizontal scan synchronization.
  - $t_{WH} = \text{Min } 2 \text{ fs}^{-1}$
  - Timing corresponding to the effective pixel region for the falling edge of HREFI.

	<b>Min</b>
$t_F$	30 fs <sup>-1</sup>
$t_B$	0

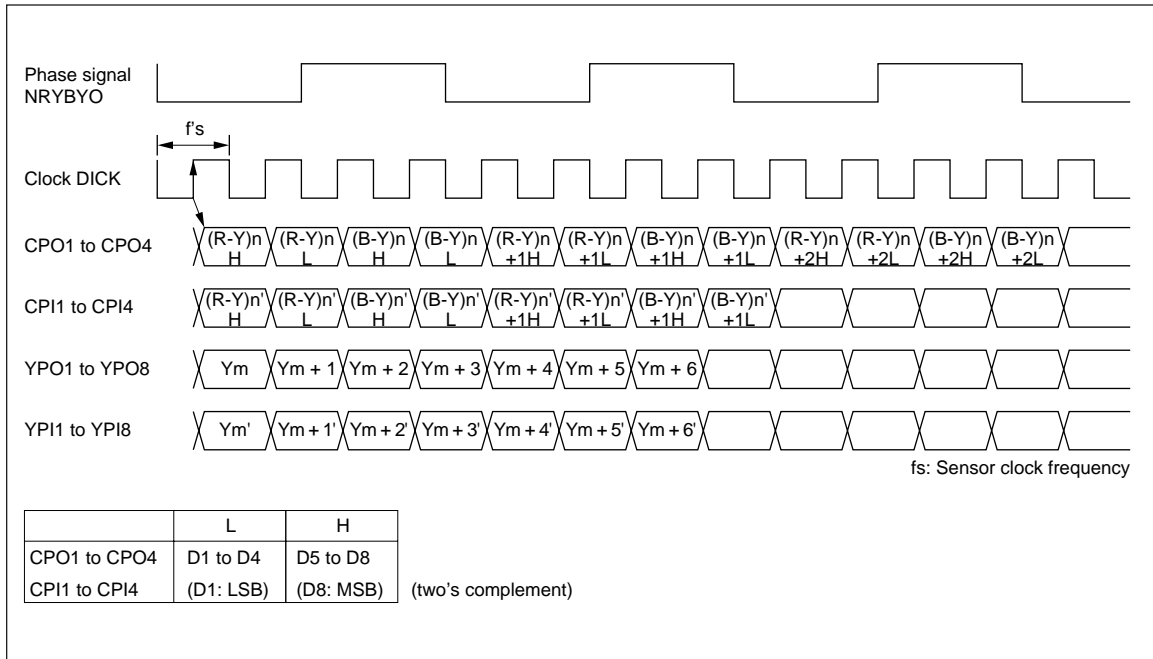
However, there are no special requirements when the following relationship is met:  $f_s = 4n \cdot f_H$  (where n is an integer).

- Setting example for H synchronization pulses (for an NTSC 270,000 pixel CCD)

<b>Name</b>	<b>Symbol</b>	<b>D10</b>	<b>D1</b>	<b>Notes</b>	
H synchronization pulse 1	H1	10 0001	1011	539	Values with respect to the falling edge of HREFI.
H synchronization pulse 2	H2	00 1110	1100	236	
H synchronization pulse 3	H3	0001	0110	22	Values with respect to H synchronization pulses 1 and 2.
H synchronization pulse 4	H4	0010	1110	46	
H synchronization pulse 5	H5	0100	0011	67	
H synchronization pulse 6	H6	0101	1010	90	
H synchronization pulse 7	H7	0101	1111	95	
H synchronization pulse 8	H8	0111	1000	120	
H synchronization pulse 9	H9	1000	1011	138	

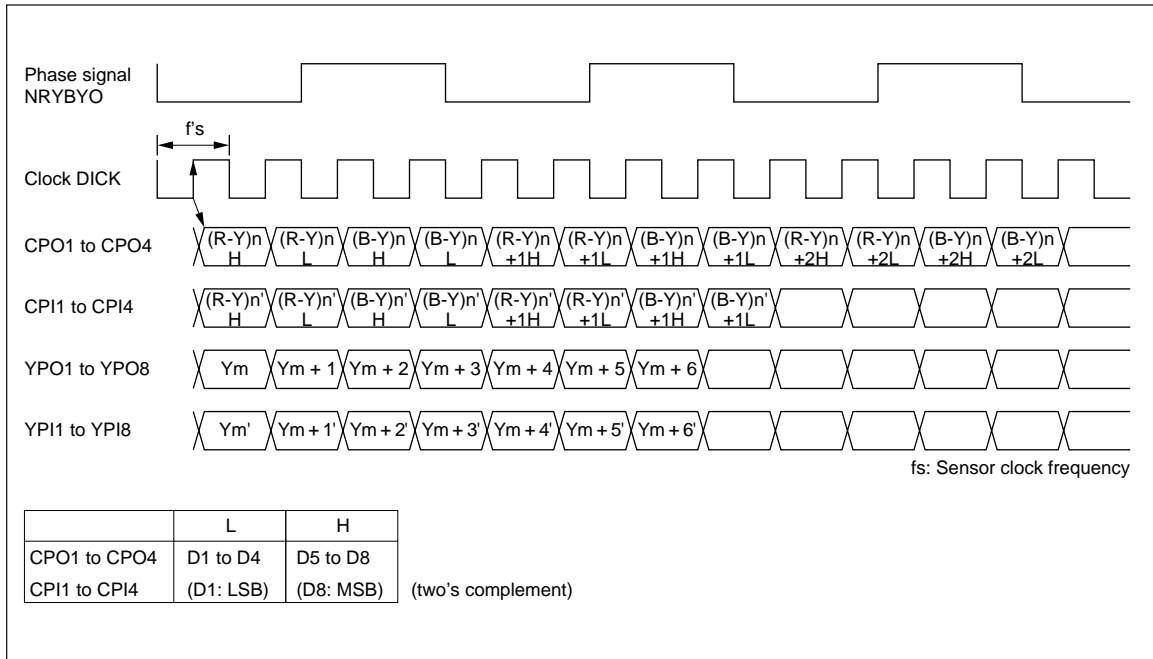
- When a 410,000 pixel CCD is used, the following timings, which are related to the sensor clock and the sensor specifications, change.
  - Memory R/W start/stop addresses
  - BF, CBLK, CSYNC pulse timings
  - Iris state data A13, H count 1 to 6

- Notes on the Y/C digital interface
  - Y is the post-gamma compensation output, and the color signal is the color difference signal output.
  - The digital interface clock is proportional to the sensor clock frequency.
  - It can handle 270,000 or 410,000 pixel sensors, and either the NTSC or PAL format.
  - The upper 4 bits are added to the lower 4 bits, which are delayed by 1 clock cycle, and output.





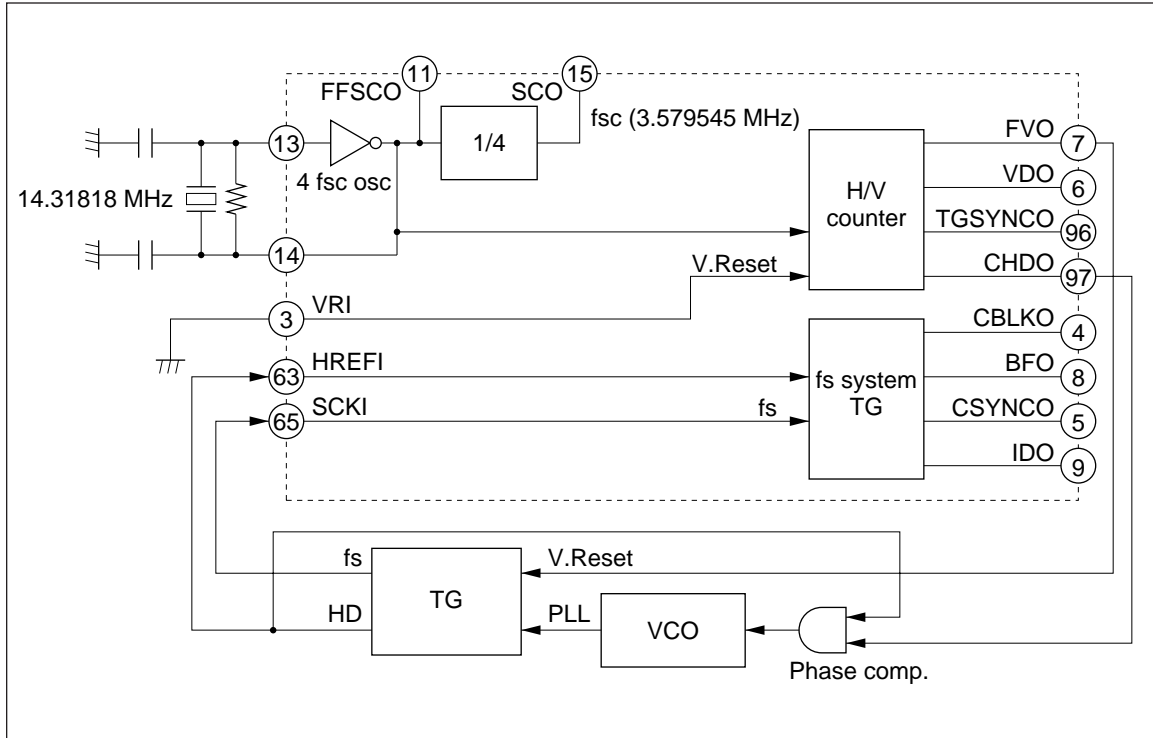
- Notes on the Y/C digital interface
  - Y is the post-gamma compensation output, and the color signal is the color difference signal output.
  - The digital interface clock is proportional to the sensor clock frequency.
  - It can handle 270,000 or 410,000 pixel sensors, and either the NTSC or PAL format.
  - The upper 4 bits are added to the lower 4 bits, which are delayed by 1 clock cycle, and output.



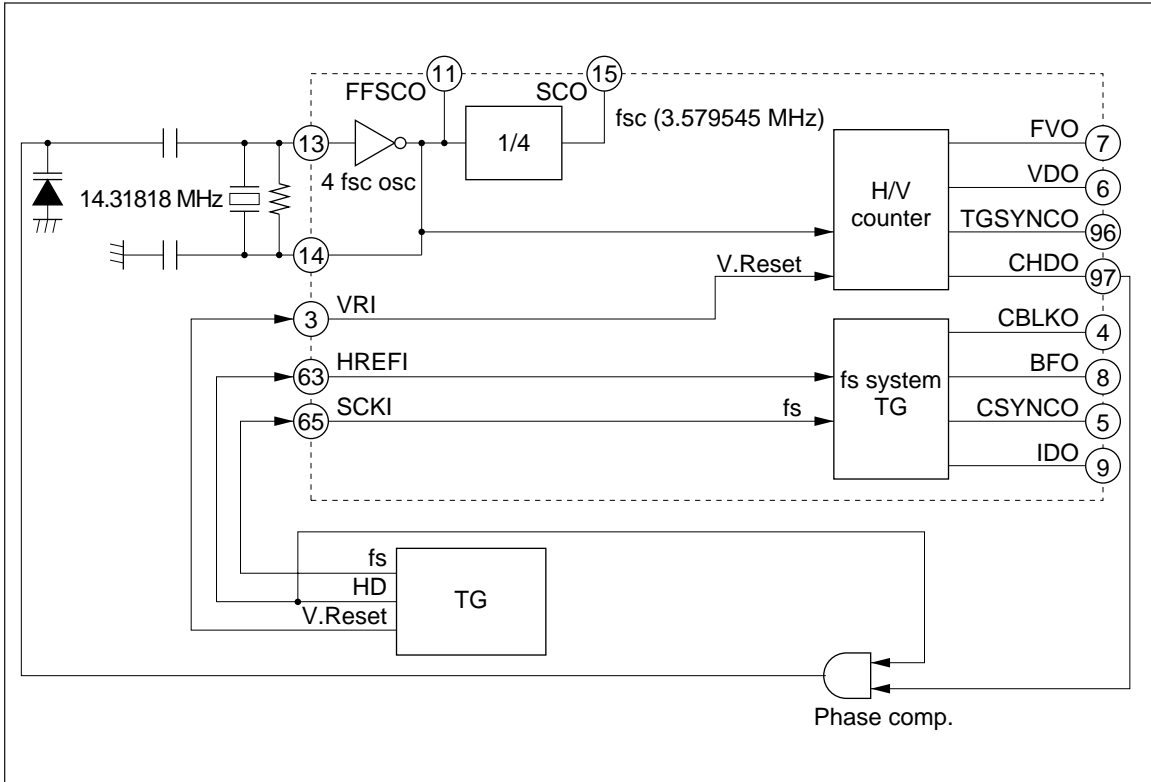
SSG Internal Block Diagram

The PLL format corresponding to the TG or TV formats used can be selected in the HD49801FB.

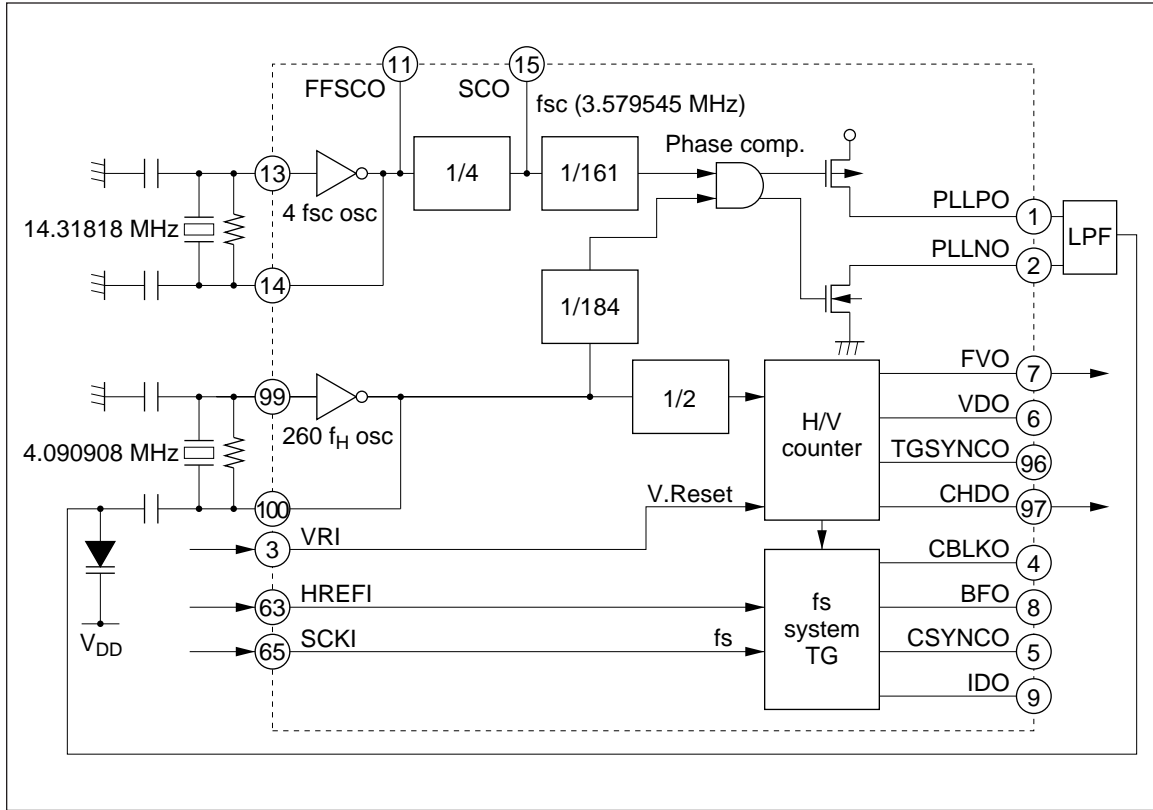
- NTSC
  - The H oscillator is unused (state data A16 PLLON = 0)
  - When the PLL is applied to the sensor side TG:



- NTSC
  - The H oscillator is unused (state data A16 PLLON = 0)
  - When the PLL is applied to the DSP side 4 fsc.



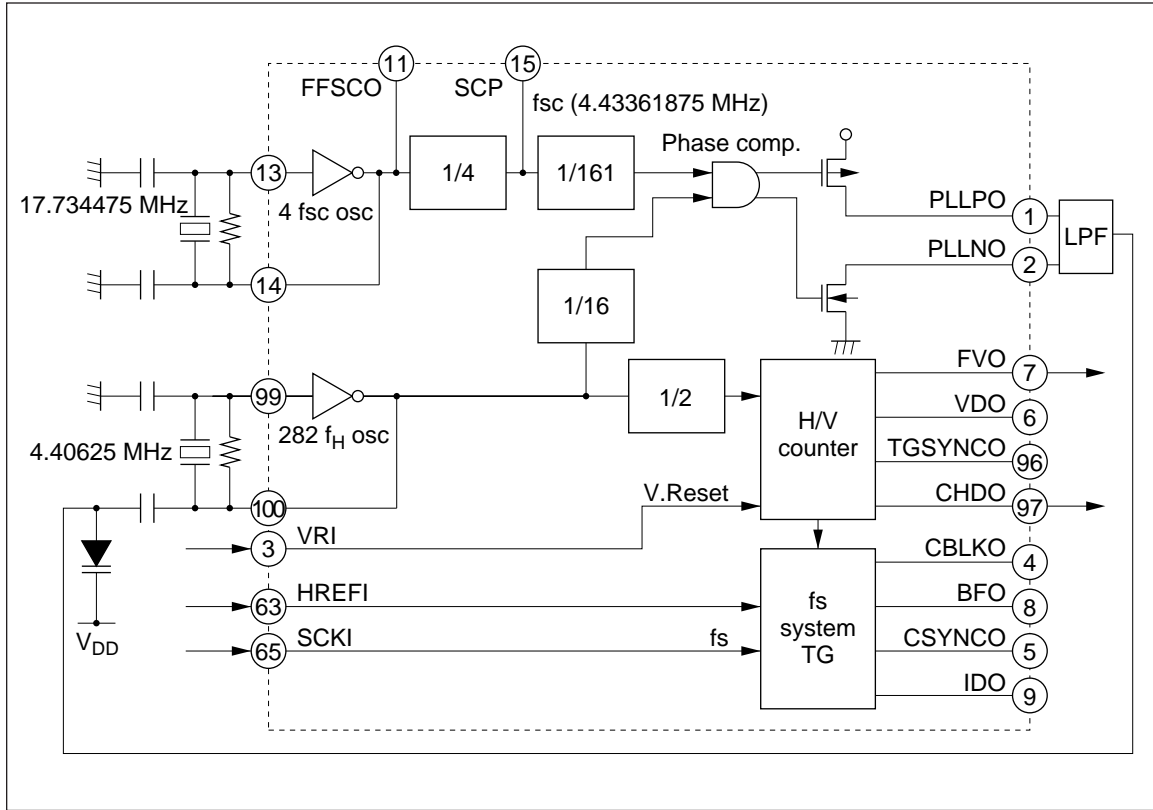
- NTSC
  - The H oscillator is used (state data A16 PLLON = 1)
  - See the description of NTSC on pages 34 and 35 for sensor side TG.



- PAL/SECAM

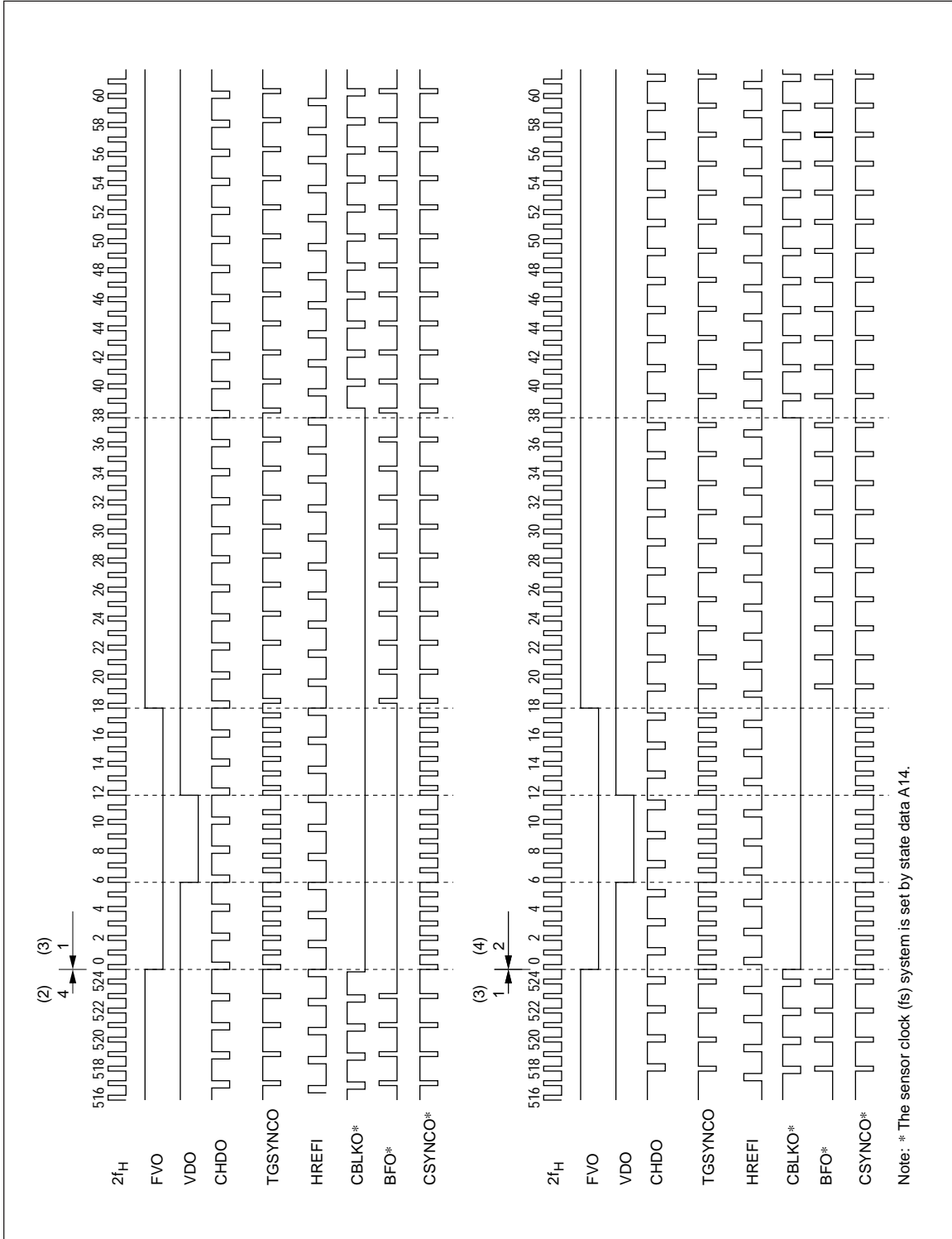
- The H oscillator is used (state data A16 PLLON = 1)

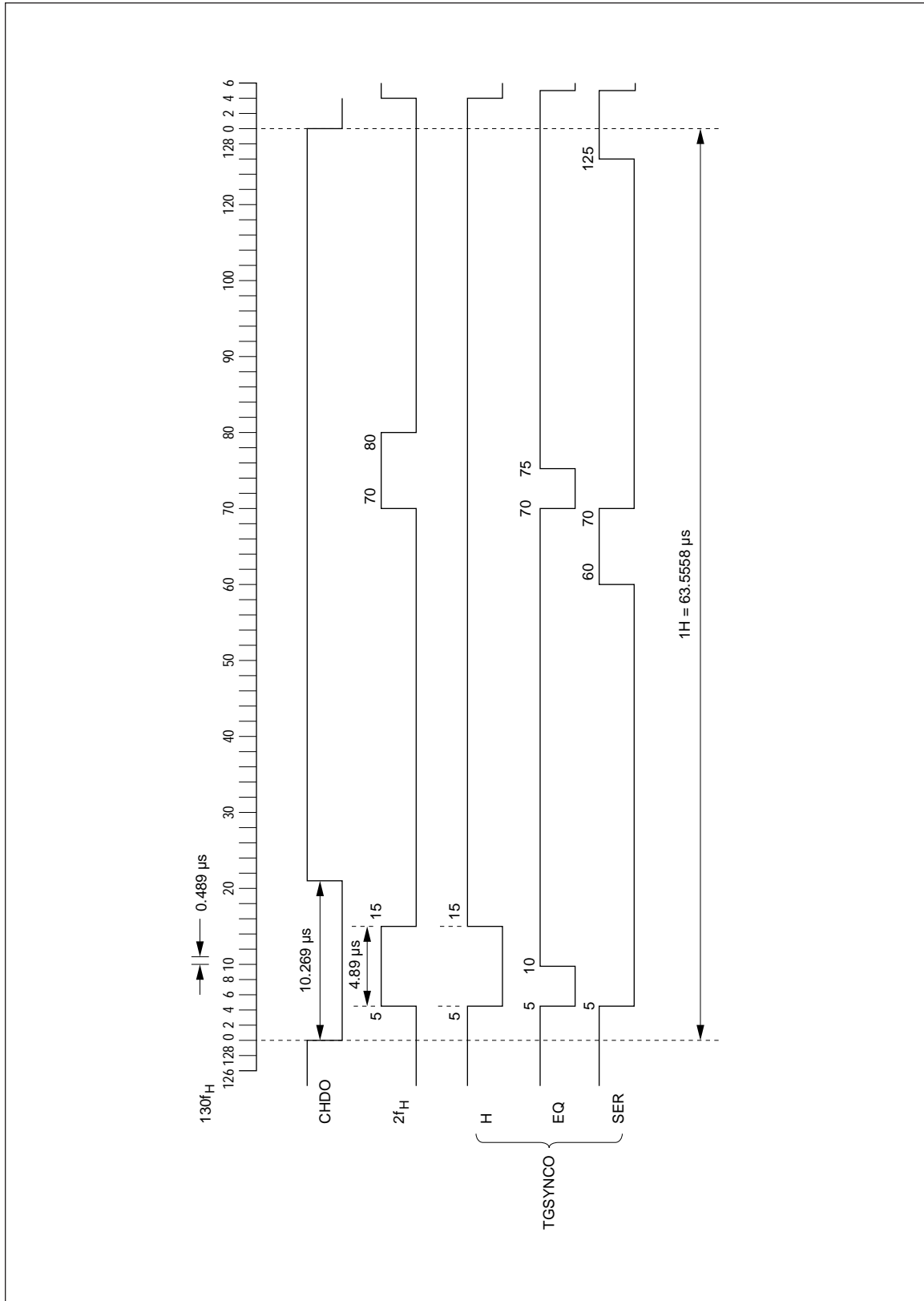
- See the description of NTSC on pages 34 and 35 for sensor side TG.



NTSC Timing Chart

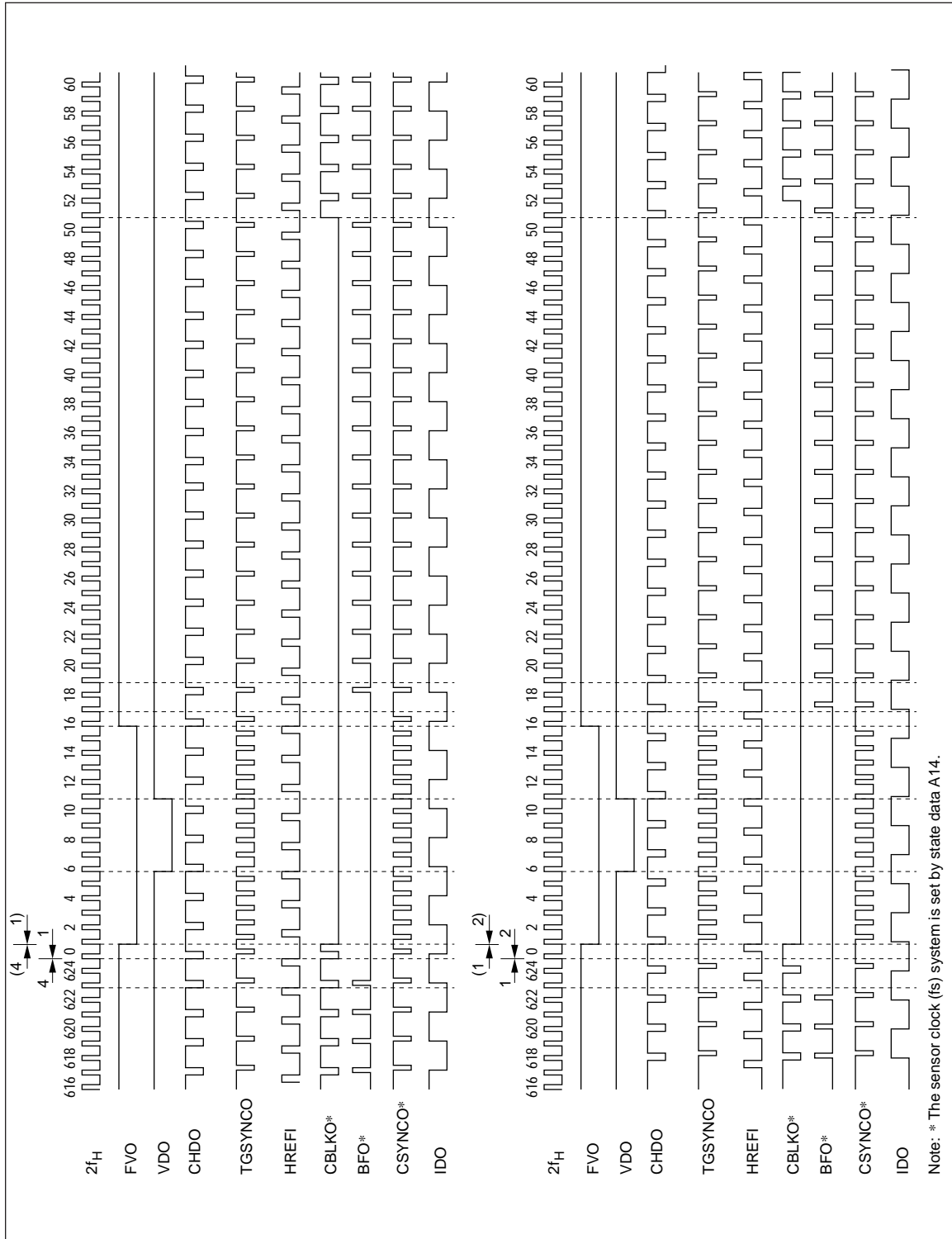
This figure shows the timing chart conforming to the NTSC TV format.



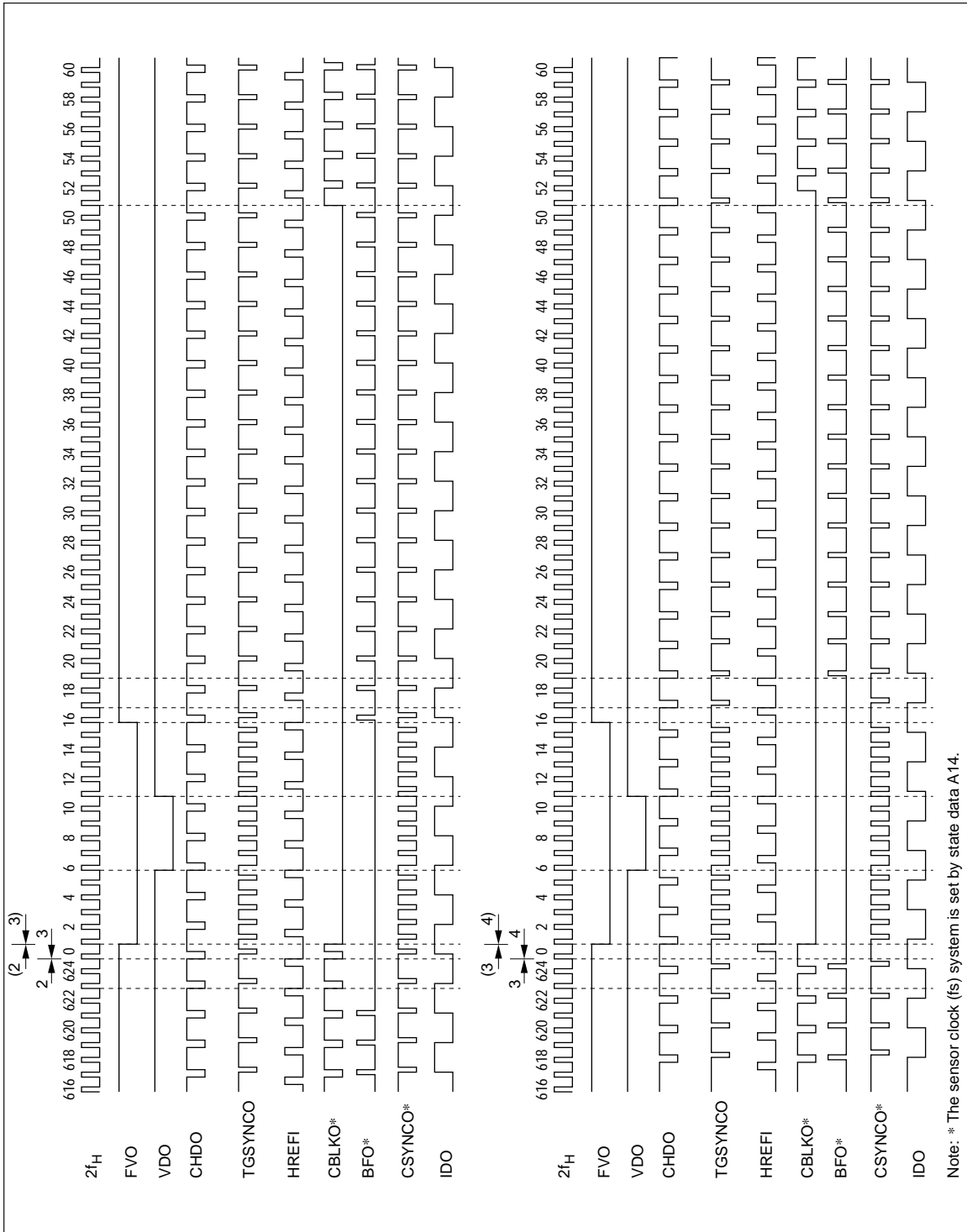


PAL/SECAM Timing Chart

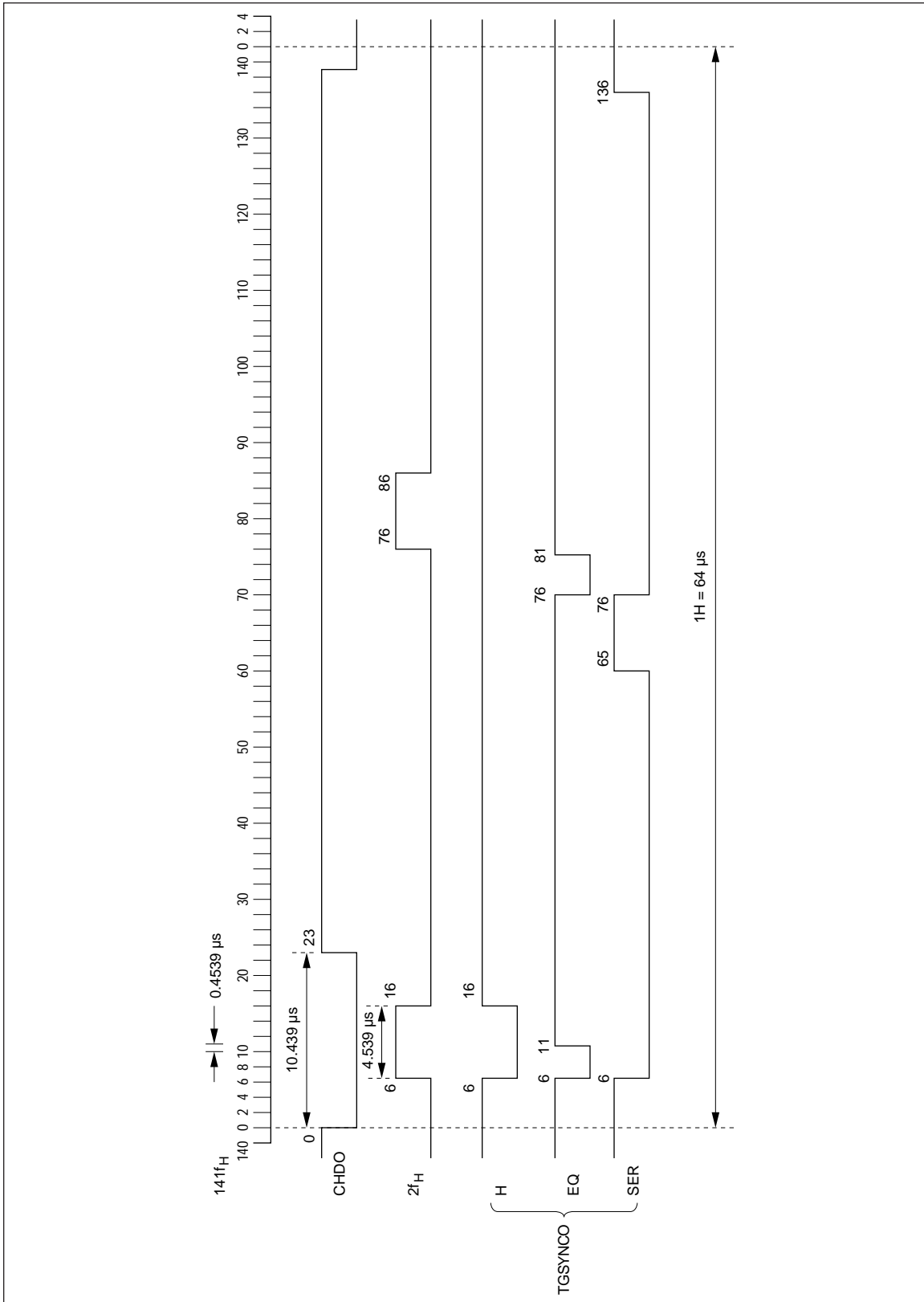
This figure shows the timing chart conforming to the PAL TV format.





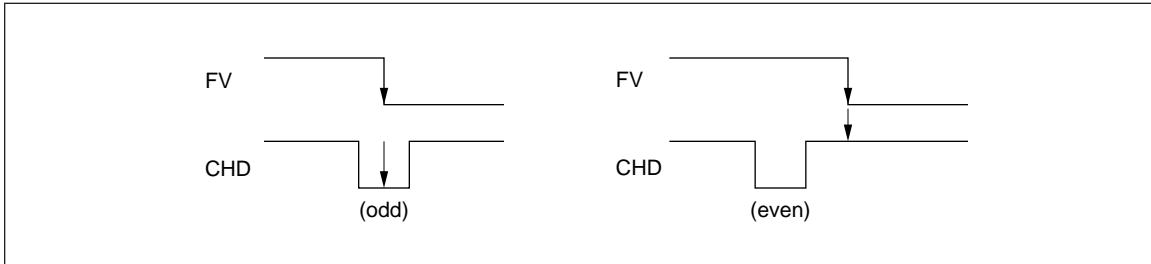


Note: \* The sensor clock (fs) system is set by state data A14.



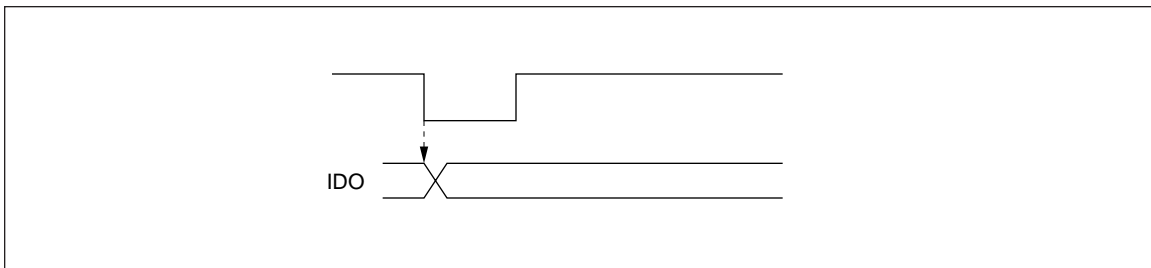
- Odd/even determination signal

This is determined by latching CHD on the falling edge of FV.



- IDO for PAL/SECAM

The change point agrees with the falling edge of C.SYNC.



In PAL mode:

ID = high: Modulates at R-Y  $\oplus$  polarity

ID = low: Modulates at R-Y  $\ominus$  polarity

In SECAM mode:

ID = high: B-Y output

ID = low: R-Y output

The (R-Y) polarity inversion in PAL mode is performed in the encoder that follows the digital interface.