Initial Release

HV461FG Ring Generator Controller IC

Features

- 3.3V operation, logic inputs 3.3V & 5V compatible
- Digital control of ring frequency, amplitude, and offset
- Control via 8-bit bus or via individual inputs
- 8 built-in ring frequencies: $16^{2}/_{3}$, 20, 25, $33^{1}/_{3}$, 40, 50, 60Hz
- External ring frequency input
- Low distortion sine wave synthesizer
- AC-only, AC+DC, or DC-only ringer output
- Adjustable over-current protection
- Internal precision voltage references
- Power-on reset and undervoltage lockout for hotswap capability
- Sync output with adjustable lead time for synchronizing ringing relays
- Fault output for problem detection
- Open or closed loop operation
- Efficient 4-quadrant operation
- Zero-cross turn-on with zero-cross turn-off option

Applications

- PBX
- DLC
- Key Systems
- Remote Terminal
- Wireless Loop Systems

Description

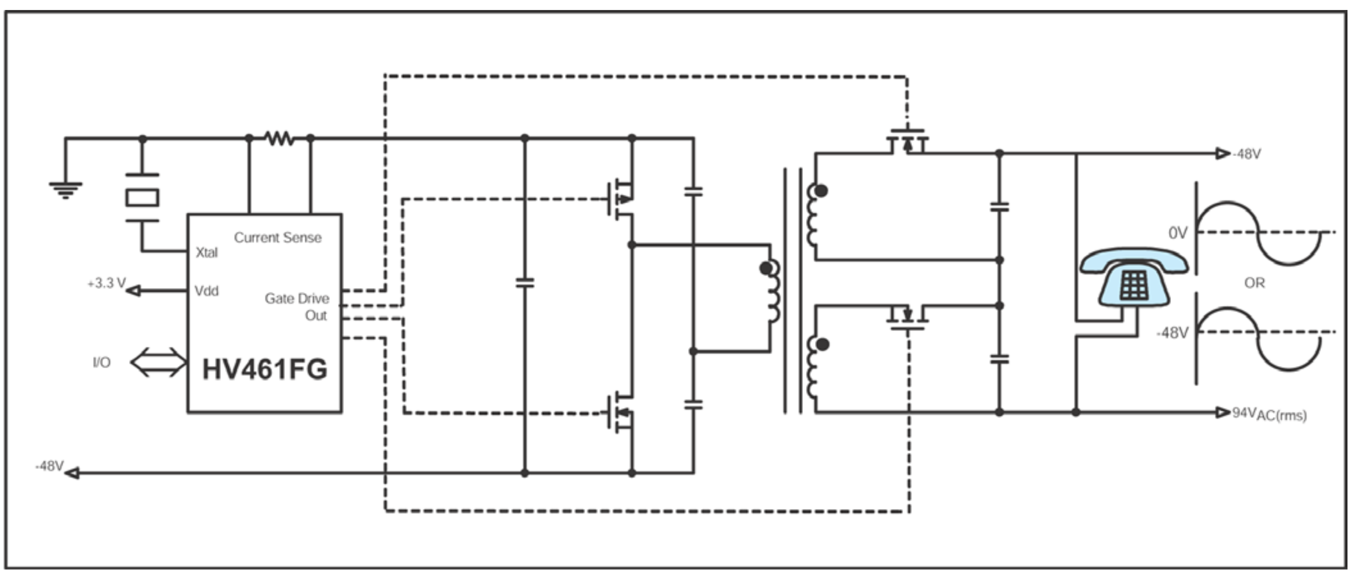
The HV461FG is a highly integrated Ring Generator controller IC designed to work with a patented four-quadrant inverter topology, with Synchronous Rectifiers on the secondary side to achieve higher efficiencies. The inverter delivers the desired ring voltage from a standard -48V Telecom power supply.

HV461 consists of a sine wave synthesizer that can provide eight different ring frequencies for universal applications. Any other frequency in the 12 to 63 Hz range can be obtained by applying an external logic signal to the IC. A transparent latch permits control of the ringer output through the 8-bit bus or individually. The output amplitude and DC offset can be digitally controlled providing high flexibility to the designers. The patented inverter topology using the HV461 controller IC is capable of achieving higher efficiencies, typically over 80%, and drive up to a 40 REN load.

The controller allows ring generators to provide a floating 94VAC (rms) waveform that can be referenced to either the –48V or any other offset level by using the programmable offset pins of the IC. Output offset may be achieved by directly generating the offset within the power stage, or by floating the output stage on a DC source, or both.

HV461 also has an internal Boost Converter that can be used to provide the gate drive voltages for the two MOSFETS on the primary side and the two secondary rectifiers on the secondary side.

Typical Application



Absolute Maximum Ratings

V_{DD}	+4.0V
Digital Inputs	-0.5V to +7.0V
Analog Inputs	-0.5V to +7.0V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

Ordering Information

Package Option	Order Number
48 lead TQFP	HV461FG

Specifications *(unless otherwise specified: V_{DD} = +3.3V, T_A = -40ºC to +85ºC)*

External Supply

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	
I_{DD}	Supply Current (AVDD + DVDD)		7	30	mA	f_{PWM}=100kHz f_{osc}=19.6608MHz SW outputs NC Open loop config External V_{GD}

Gate Drive Supply

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{GD}	Boost circuit voltage	9.0	9.6	10.2	V	
I_{GD}	Gate drive supply current			5 10	mA mA	V_{DD}=2.97-3.63V, SW outputs unloaded V_{DD}=2.50-2.93V, SW outputs unloaded
$V_{DR(lo)}$	Drive voltage, low			0.2	V	I_{OUT}=-10µA
$V_{DR(hi)}$	Drive voltage, hi	V_{DD}-0.4			V	I_{OUT}=10µA
t_{RISE}	Rise time			100	ns	C_L=200pF
t_{FALL}	Fall time			100	ns	C_L=200pF
f_{GD}	Converter frequency	same as PWM				
D_{GD}	Duty cycle	45	50	55	%	

Voltage Reference

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{REF1}	Reference voltage 1	1.237	1.250	1.263	V	T_a=25ºC
TC_{REF1}	Temperature coefficient		200		µV/ºC	
ΔV_{ref1}	Output regulation	-6.25		+6.25	mV	I_{out}=±100µA
V_{REF2}	Reference voltage 2	2.475	2.500	2.525	V	T_a=25ºC
TC_{REF2}	Temperature coefficient		500		µV/ºC	
ΔV_{ref2}	Output regulation	-12.5		0	mV	I_{out}=0–100µA source

Logic Inputs

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{IN(lo)}$	Input voltage low			$0.3 \cdot V_{DD}$	V	
$V_{IN(hi)}$	Input voltage high	$0.7 \cdot V_{DD}$			V	
$I_{IN(lo)}$	Input current low			-1	µA	V_{IN}=0V
$I_{IN(hi)}$	Input current high			1	µA	V_{IN}=5.0V
C_{IN}	Input capacitance			10	pF	
t_S	Set-up time			100	ns	
t_H	Hold time			100	ns	

RESET

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{RESET(ON)}$	RESET on voltage	1.200	1.325	1.450	V	
$V_{RESET(OFF)}$	RESET off voltage	1.000	1.125	1.250	V	
$V_{RESET\ (HYS)}$	RESET hysteresis	0.150	0.200	0.250	V	
I_{P-UP}	RESET pull-up current	7.0	10.0	13.0	µA	

Undervoltage Lockout

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{DD(ON)}$	V_{DD} on voltage	2.75	2.85	2.95	V	
$V_{DD(OFF)}$	V_{DD} off voltage	2.60			V	
$V_{DD(HYS)}$	V_{DD} hysteresis		0.10		V	
$V_{GD(ON)}$	V_{GD} on voltage	same as V_{GD} regulation point			V	
$V_{GD(OFF)}$	V_{GD} off voltage	7.0			V	
$V_{GD(HYS)}$	V_{GD} hysteresis	0.20			V	

Fault Output

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{OUT(lo)}$	Output voltage low			0.2	V	I_{OUT}=1mA
$K_{FAULT(on)}$	FAULT on threshold	6	8	10	%*	C_{FAULT}=10µF
$K_{FAULT(off)}$	FAULT off threshold	1	2	3	%*	C_{FAULT}=10µF
$t_{FAULT(hold)}$	FAULT hold time	50			mS	C_{FAULT}=10µF

* *Percent of time PWM overrange or overcurrent is active.*

Amplifiers

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IN}	Input Range	0.25		2.50	V	
I_{IN}	Input Bias Current	-500		500	nA	V_{IN}=0.5V to V_{DD}-0.5
V_{OFFSET}	Input Offset Voltage	-5		5	mV	
$V_{OUT(min)}$	Min output		0.1	0.2	V	I_{OUT}=±100uA
$V_{OUT(max)}$	Max output	V_{DD} -0.2	V_{DD} -0.1			I_{OUT}=±100uA
A_{VOL}	Open Loop Gain	60	80		dB	
CMRR	Common mode rejection ratio	-40	-60		dB	

GBW	Gain-Bandwidth Product	1			MHz	
SL	Slew Rate	0.1			V/μs	
PSRR	Power supply rejection ratio	-30			dB	f<10kHz

Sinewave Synthesizer

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DC}	DC level	1.237	1.250	1.263	V	
A	Amplitude	1.940	2.000	2.060 0	V_{P-P} V_{P-P}	AMP≠00 AMP=00
f_0	Frequency		16 $^2/_3$		Hz	FREQ=000, f_{OSC}=19.6608MHz
f_1	Frequency		20		Hz	FREQ=001, f_{OSC}=19.6608MHz
f_2	Frequency		25		Hz	FREQ=010, f_{OSC}=19.6608MHz
f_3	Frequency		30		Hz	FREQ=011, f_{OSC}=19.6608MHz
f_4	Frequency		33 $^1/_3$		Hz	FREQ=100, f_{OSC}=19.6608MHz
f_5	Frequency		40		Hz	FREQ=101, f_{OSC}=19.6608MHz
f_6	Frequency		50		Hz	FREQ=110, f_{OSC}=19.6608MHz
f_7	Frequency		60		Hz	FREQ=111, f_{OSC}=19.6608MHz
Δf	Frequency accuracy			0.1	%	f_{osc}=19.6608MHz
THD	Harmonic distortion			3	%	C_{SINE}=33nF f_{ring}=16 2/3 to 60Hz
R_{OUT}	Output resistance	14.4 72.0	16.0 80.0	17.6 88.0	kΩ kΩ	AMP≠00 AMP=00

External Ring Frequency

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$f_{CAP(lo)}$	Capture frequency low*		12		Hz	loop filter=(33μF+10kΩ)||4.7μF
$f_{CAP(hi)}$	Capture frequency high*		63		Hz	loop filter=(33μF+10kΩ)||4.7μF
$V_{IN(lo)}$	Input low			$0.3 \cdot V_{DD}$	V	
$V_{IN(hi)}$	Input high	$0.7 \cdot V_{DD}$			V	
$\Delta\theta_{RING}$	Phase jitter, sine ref out	-5		+5	deg	loop filter=(33μF+10kΩ)||4.7μF

** Lock range is the same as capture range*

Sine Reference Attenuator

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DC}	DC level	1.237	1.250	1.263	V	$V_{IN(DC)}$=1.250V
A_{OFF}	Attenuation			0.010	V/V	AMP=00
A_{LO}	Attenuation	0.495	0.500	0.505	V/V	AMP=01
A_{MED}	Attenuation	0.742	0.750	0.758	V/V	AMP=10
A_{HI}	Attenuation	0.990	1.000	1.010	V/V	AMP=11
V_{IN}	Input range	0.2		V_{DD}-0.2V	V	

DC REF Multiplexer

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IN}	Input range	0.0		V_{DD}	V	
I_{IN}	Input bias current	-500		+500	nA	
I_{OFF}	Off leakage current			1.0	μA	V_{IN} = 0.5 to V_{DD}-0.5V

ENABLE and SYNC

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{OUT(lo)}$	SYNC output voltage low			0.2	V	I_{OUT} = 1mA sink
$V_{OUT(hi)}$	SYNC output voltage high	V_{DD} - 0.2			V	I_{OUT} = 1mA source
t_{ON}	ENABLE delay, on			5	µs	
t_{OFF}	ENABLE delay, off	 0		60 1	µs ring cycle	SYNCMODE=0 SYNCMODE=1
$\tau_{SYNC(ON)}$	SYNC on lead time	4.5	5	5.5	ms	C_{SINE}=0 R_{SYNC}=154kΩ C_{SYNC}=47nF
$\tau_{SYNC(OFF)}$	SYNC off delay	-250	0	+250	µs	C_{SINE}=10nF
$t_{SYNC(rise)}$	SYNC rise time			300	ns	C_L=50pF
$t_{SYNC(fall)}$	SYNC fall time			300	ns	C_L=50pF

PWM Controller

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
PWM Frequency						
f_{PWM}	PWM frequency	21.25 127.5	25.00 150.0	28.75 172.5	kHz kHz	R_{PWM}=500kΩ R_{PWM}=83kΩ
$t_{PWMSYNC(OUT)}$	PWM sync output pulse width	30	50	70	ns	
$t_{PWMSYNC(IN)}$	PWM sync input pulse width	25			ns	
$f_{PWMSYNC(IN)}$	PWM sync input frequency range	25		150	kHz	
$V_{PWMSYNC(lo)}$	PWM sync output low voltage			0.2	V	I_{OUT}=1mA sink
$I_{PWMSYNC}$	PWM sync pull-up current		100		µA	
Switch Driver Outputs						
$V_{OUT(lo)}$	Output voltage, low			0.2	V	I_{OUT}=20mA sink
$V_{OUT(hi)}$	Output voltage, high	V_{GD}-0.2			V	I_{OUT}=20mA source
t_{RISE}	Rise time			50	ns	C_L=4nF
t_{FALL}	Fall time			50	ns	C_L=4nF
Timing						
D	Duty cycle	23 48 73	25 50 75	27 52 77	% % %	PWMin=0.625V PWMin=1.250V PWMin=1.875V V_{DCL}=0V
D_{limit}	Duty cycle limit	12 72 22 62	20 80 30 70	28 88 38 78	% % % %	V_{DCL} = 0.50V, PWM_{IN}=0V V_{DCL} = 0.50V, PWM_{IN}=2.5V V_{DCL} = 0.75V, PWM_{IN}=0V V_{DCL} = 0.75V, PWM_{IN}=2.5V
I_{DCL}	V_{DCL} input current			1	µA	V_{DCL}=0-1V
t_{DB}	Primary switch deadband	0 0.95	100 1.00	150 1.05	ns µs	C_{DB}=0pF R_{DB}=14kΩ, C_{DB}=100pF
t_{DLY}	Secondary switch delay	0 0.95	100 1.00	150 1.05	ns µs	C_{DLY}=0pF R_{DLY}=14kΩ, C_{DLY}=100pF

Switch Outputs

ENABLE	AMP	OFF	SW1	SW2	SW3	SW4
0	00	XX	Off	Off	Off	Off
0	≠00	XX	Off	Off	Switching	Switching
1	XX	XX	Switching	Switching	Switching	Switching

X = don't care, ≠00 = 01,10, or 11

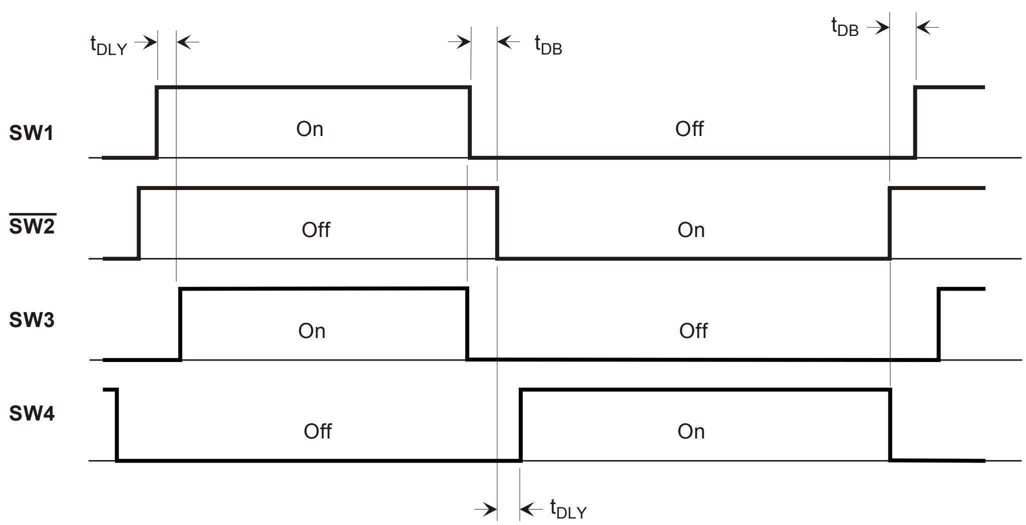


Figure 1: Switch Timing Diagram

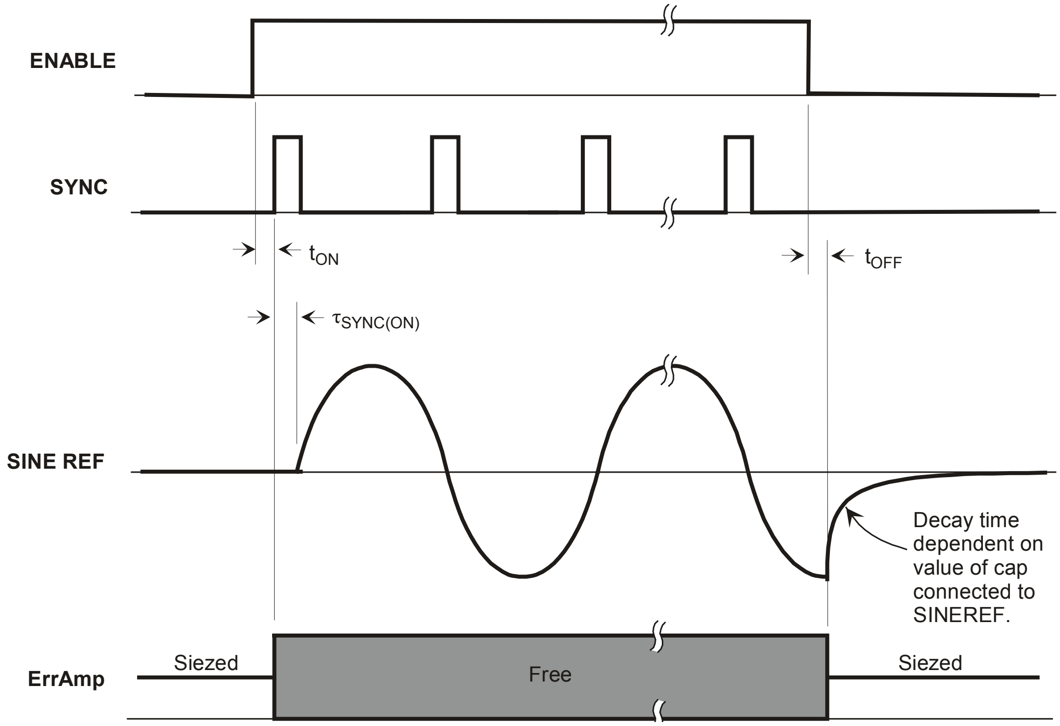


Figure 2: ENABLE and SYNC Timing – SYNCMODE=0

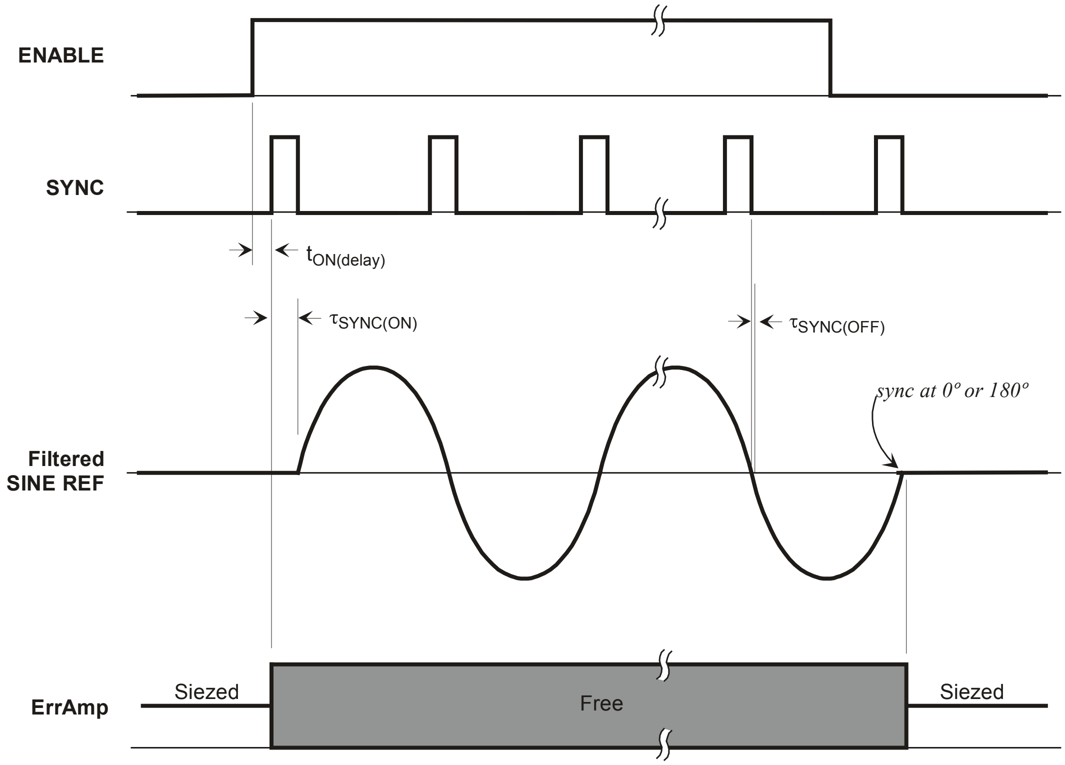


Figure 3: ENABLE and SYNC Timing – SYNCMODE=1

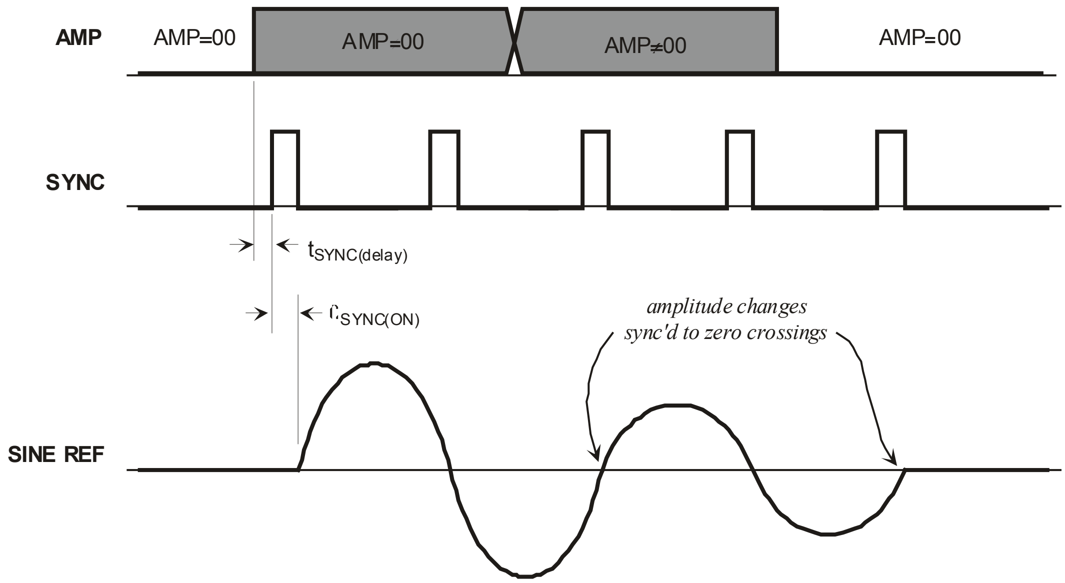


Figure 4: AMP Timing

Typical Application

Figures 5 and 6 on pages 9 and 10 show the schematic of a typical 15 REN ring generator application. The basic design equations for elements connected to different pins are given in the Pin Descriptions Table beginning on page 11.

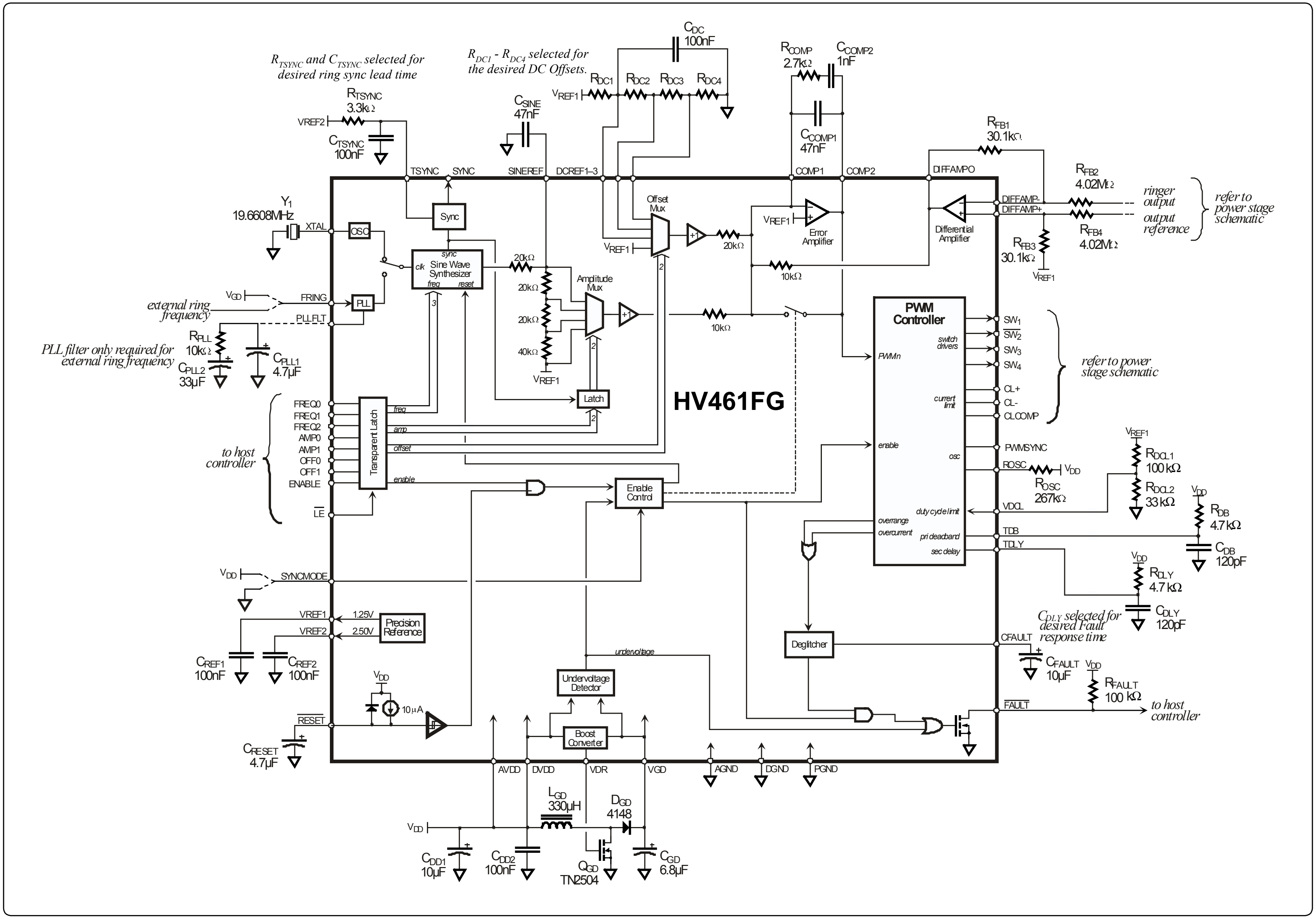


Figure 5: Block Diagram and Typical Application

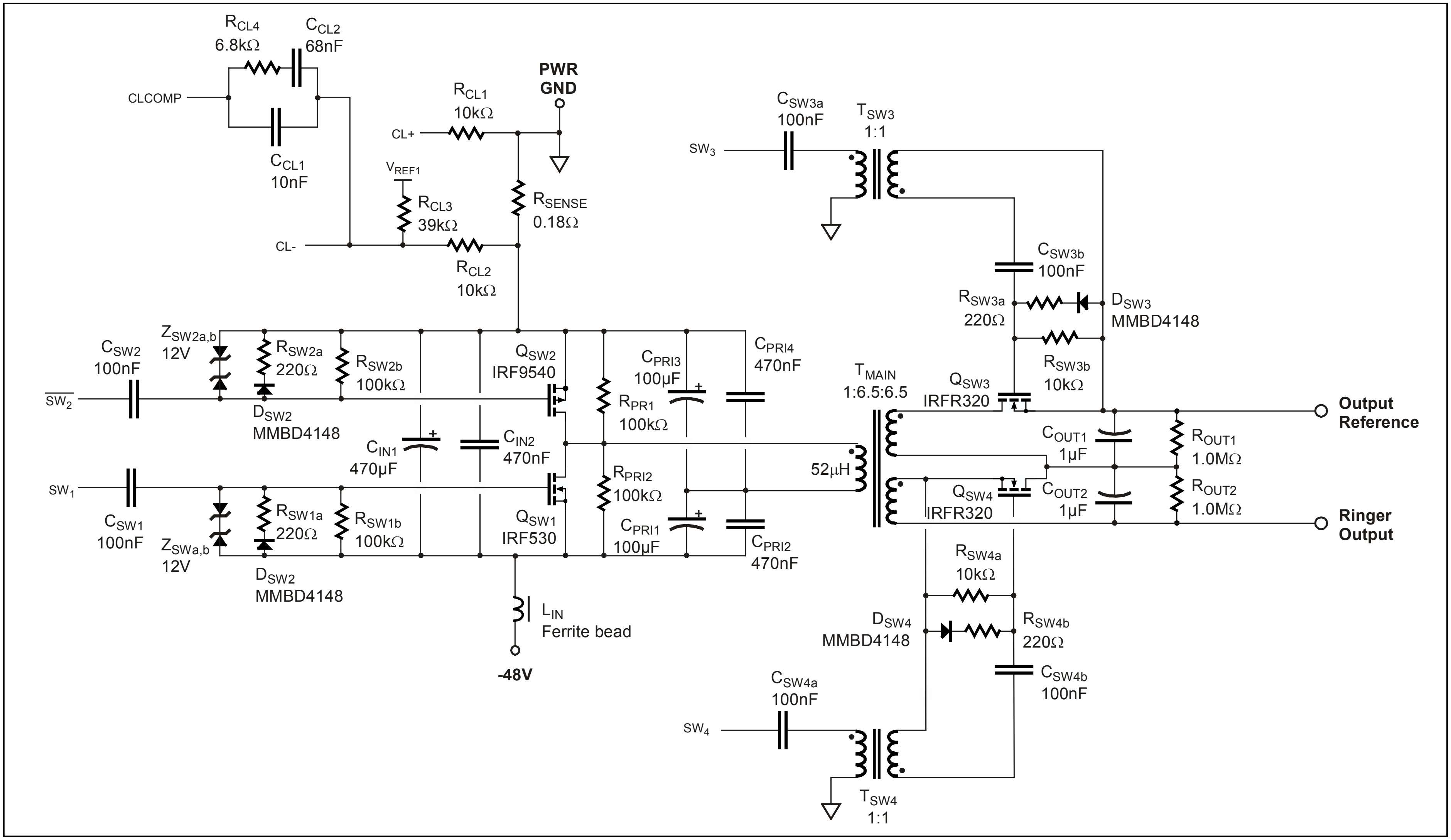
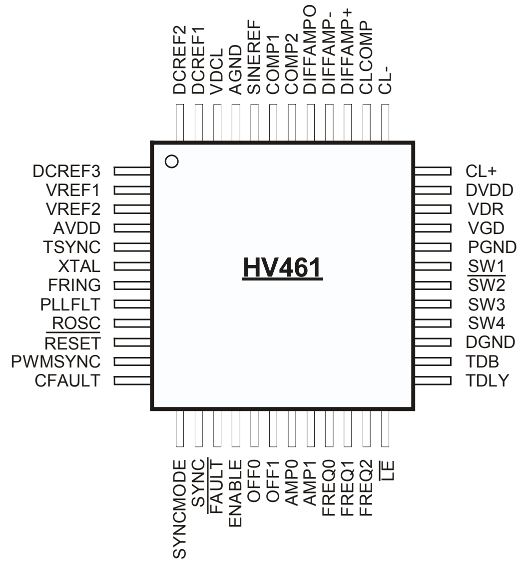


Figure 6: Typical Power Stage for 15 REN Ring Generator

Pin Descriptions



Pin	Name	Description
1	DCREF3	See DCREF1 and DCREF2 (pins 47 & 48).
2	VREF1	Outputs a 1.25V nominal reference voltage. Bypass with a 100nF capacitor to ground.
3	VREF2	Outputs a 2.50V nominal reference voltage. Bypass with a 100nF capacitor to ground.
4	AVDD	Supply for the analog section. 3.0 to 3.6V Must be from the same source as DVDD. Bypass with a 100nF capacitor to ground as close as possible to the IC.
5	TSYNC	An RC network connected to this pin determines the SYNC pulse lead time (see SYNC pin 14). t_{LEAD} = 0.48RC If unused, this pin should be left unconnected.
6	XTAL	A crystal from this pin to ground provides the frequency reference for the internal sine wave synthesizer. A 19.6608MHz baud rate crystal provides the 8 most common ring frequencies. The crystal is operated in the series mode. A loading capacitor is not necessary. See also FREQ0–2 (pins 21–23) and FRING (pin 7).
7	FRING	Ring frequency is normally selected from the 8 built-in frequencies using control inputs FREQ0–2. Other arbitrary frequencies in the range of 12 to 70Hz may be obtained by applying an external signal to FRING. This external signal sets the ring frequency at a 1:1 ratio. The ring signal remains a sine wave, with amplitude and offset still controlled via AMPx and OFFx. The ring signal, while frequency locked to the FRING signal, is not phase–synchronized to it. This allows the ring signal to immediately start at 0º when enabled via ENABLE or AMP≠00. When unused, this input must be connected to V_{GD}.
8	PLLFLT	Phase locked loop filter. An RC network connected to this pin stabilizes the PLL that locks on to the optional external ring frequency signal. (See FRING, pin 7) The RC network determines the lock time of the PLL. Due to the low frequencies involved, it may take a couple seconds to lock to the external signal. See the typical application schematic for typical values. When unused, this pin should be left unconnected.
9	ROSC	A resistor from this pin to V_{DD} sets the PWM frequency. $f_{PWM} \approx 12.5\text{GHz}\Omega / R_{OSC}$ (valid for 20-150kHz)
10	$\overline{\text{RESET}}$	A capacitor from this pin to ground provides a power–on reset interval. It has an internal 10µA pull–up to charge the external reset capacitor. Alternatively, an external logic–level or open–drain signal may be applied to implement the reset function. During the reset interval when V_{RESET}<1.325V, the ringer output is disabled regardless of the state of the ENABLE input, allowing time for the host controller to assume control. Use a low leakage tantalum or ceramic capacitor. $t_{RESET} = 1.325\text{V} \cdot C_{RESET} / 10\mu\text{A}$
11	PWMSYNC	This pin functions as both an input and an output. It is open–drain with an internal 100µA pull–up. As an output, it provides a short, low–going pulse at the internal PWM frequency. As an input, it synchronizes internal PWM frequency to the externally applied signal, provided the external signal is at a higher frequency. The low-going applied sync pulse should be between 25ns and less than the PWM period in duration. The external source should be open drain. If the PWMSYNC pins of multiple HV461s are tied together, their PWM frequencies will be phase–locked to the HV461 with the highest free-running frequency. A maximum of 10 HV461s may be tied together. If unused, this pin should be left unconnected.

12	CFAULT	A capacitor from this pin to ground sets the integration time of the FAULT detection circuitry. A larger capacitor provides less suseptability to transient problems, while a smaller capacitor provides quicker response. Values in the range of 1µF to 100µF are appropriate. If the FAULT output is not used, this pin should be grounded. See also FAULT (pin 15).
13	SYNCMODE	With SYNCMODE low, ringer output ceases the instant ENABLE goes low. When high, ringer output ceases at the next ring signal phase crossing (0º/180º) after ENABLE goes low.
14	SYNC	Outputs a pulse indicating sine reference 0º and 180º phase crossing (not to be confused with zero–voltage crossing). The rising edge precedes phase crossing by a user–adjustable time period (see TSYNC pin 44). Falling edge coincides with sine reference phase crossing. SYNC is digitally derived, therefore phase shifts caused by the external filter capacitor at SINEREF will not be reflected at the SYNC output.
15	$\overline{FAULT}$	Indicates abnormal operating conditions of output overcurrent, supply undervoltage (V_{DD} & V_{GD}), or PWM overrange (duty cycle limit – see VDCL, pin 3). Together, these 3 conditions catch most any problem. When an overcurrent or overrange condition exists for more than 8% of the time, this output becomes active. It is cleared when the problem occurs less than 2% of the time. Undervoltage conditions immediately activate the FAULT output. It is active low and open drain to allow wire-ORing. See CFAULT (pin 15) for additional information.
16	ENABLE	Ringer output enable. Active high. When enabled, the ring signal always starts immediately at 0 degrees. If AMP≠00, SW1 and SW2 are held off when ENABLE=0 but SW3 and SW4 continue switching. If AMP=00, SW3 and SW4 are held off as well. When disabled, the error amplifier is set at unity gain to prevent saturation, reducing turn-on glitches when re-enabled. See SYNCMODE (pin 13) for additional information.
17	OFF0	Sets ring DC offset. Offset changes are effected at the next phase crossing (0º/180º) of the ring signal. Except for 00, offsets are set by the voltages at DCREF1–3. (OFF0 is LSB) Offset = ½ x Gain x (V_{DCREFx} - V_{REF1})
18	OFF1	00 = 0V 01 = DCREF1 10 = DCREF2 11 = DCREF3
19	AMP0	Sets ring amplitude. Amplitude changes are effected at the next phase crossing (0º/180º) of the ring signal. Amplitudes, as a percentage of full scale, are: (AMP0 is LSB) Full scale amplitude = $0.707V_{RMS}$ x Gain
20	AMP1	00 = 0% 01 = 50% 10 = 75% 11 = 100%
21	FREQ0	Sets ring frequency. Frequency changes are effected at the next phase crossing (0º/180º) of the ring signal. Frequencies when using a 19.6608MHz crystal are: (FREQ0 is LSB)
22	FREQ1	000 = 16.7Hz 001 = 20Hz 010 = 25Hz 011 = 30Hz
23	FREQ2	100 = 33.3Hz 101 = 40Hz 110 = 50Hz 111 = 60Hz
24	$\overline{LE}$	Latch enable. The latch gates control inputs FREQ0–2, AMP0–1, OFF0–1, and ENABLE. When LE is high, latch outputs follow inputs. On a low–going transition, outputs are latched.
25	TDLY	An RC network on this pin sets the primary to secondary switch delay. This prevents the secondary–side switches (SW3&4) from turning on prematurely. t_{DLY}=0.48RC
26	TDB	An RC network on this pin sets the deadband (break–before–make time) on the primary–side switches (SW1&2). Deadband prevents both switches from conducting simultaneously. t_{DB}=0.48RC
27	DGND	Digital ground. Connect to AGND and PGND close to the IC.
28	SW4	Secondary–side switch driver output.
29	SW3	Secondary–side switch driver output.
30	$\overline{SW2}$	Primary–side N-channel switch driver output.
31	SW1	Primary–side P-channel switch driver output.
32	PGND	Power ground. Connect to AGND and DGND close to the IC.
33	VGD	Supply for the SW1–4 drivers. An external boost converter controlled by VDR provides 9.6V for driving the power stage MOSFETs. An undervoltage condition on this supply pin disables ringer output and activates the FAULT output.
34	VDR	Gate drive for the external boost converter circuit. Outputs a fixed 50% duty cycle at the ringer PWM frequency (see ROSC, pin 9). Output voltage regulation is via burp-mode operation. This output is boostrapped to VGD, thus during startup VDR amplitude is VDD and after startup is VGD. (See VGD, pin 33)
35	DVDD	Supply for the digital section. 3.0V to 3.6V input. Undervoltage disables ringer output. Must be from the same source as AVDD. Bypass with a 100nF capacitor to ground as close as possible to the IC. An undervoltage condition on this supply pin disables ringer output and activates the FAULT output.
36	CL+	Current limit amplifier non-inverting input.

<table>
<tr><td>37</td><td>CL-</td><td colspan="2">Current limit amplifier inverting input.</td></tr>
<tr><td>38</td><td>CLCOMP</td><td colspan="2">Current limit compensation. An RC network connected between this pin and CL- establishes current limit reaction time and stability.</td></tr>
<tr><td>39</td><td>DIFFAMP+</td><td>Differential amplifier non-inverting input.</td><td rowspan="3">The differential amplifier sets gain, establishing output amplitude and DC offset in conjunction with AMPx and OFFx. Gain = R_{FB2}/R_{FB1} ($R_{FB3}=R_{FB1}$ and $R_{FB4}=R_{FB2}$, see schematic)</td></tr>
<tr><td>40</td><td>DIFFAMP-</td><td>Differential amplifier inverting input.</td></tr>
<tr><td>41</td><td>DIFFAMPO</td><td>Differential amplifier output.</td></tr>
<tr><td>42</td><td>COMP2</td><td colspan="2" rowspan="2">Error amplifier compensation. An RC network connected between these pins establishes loop stability. COMP1 is the error amp inverting input. COMP2 is the error amp output.</td></tr>
<tr><td>43</td><td>COMP1</td></tr>
<tr><td>44</td><td>SINEREF</td><td colspan="2">Sine wave reference. Amplitude is $2V_{P-P}$ nominal. Output impedance is approximately 16kΩ. An external 33nF capacitor from this pin to ground should be employed to remove high frequency synthesizer ripple. Synthesizer ripple is at a frequency of $2^{15} \cdot f_{RING}$</td></tr>
<tr><td>45</td><td>AGND</td><td colspan="2">Analog ground. Connect to AGND and DGND close to the IC.</td></tr>
<tr><td>46</td><td>VDCL</td><td colspan="2">Voltage applied to this pin sets the min/max duty cycle limits. If the PWM controller hits these limits, clipping of the ringer output will occur and the FAULT output will be activated. $D_{MIN}=0.4V_{DCL}$ $D_{MAX}=1–0.4V_{DCL}$</td></tr>
<tr><td>47</td><td>DCREF1</td><td colspan="2" rowspan="2">In conjunction with the OFFx control inputs, voltages applied to these inputs set the output DC offset. Output offset is the selected DCREFx voltage multiplied by gain. See also OFF0 & OFF1 (pins 17 & 18)</td></tr>
<tr><td>48</td><td>DCREF2</td></tr>
</table>

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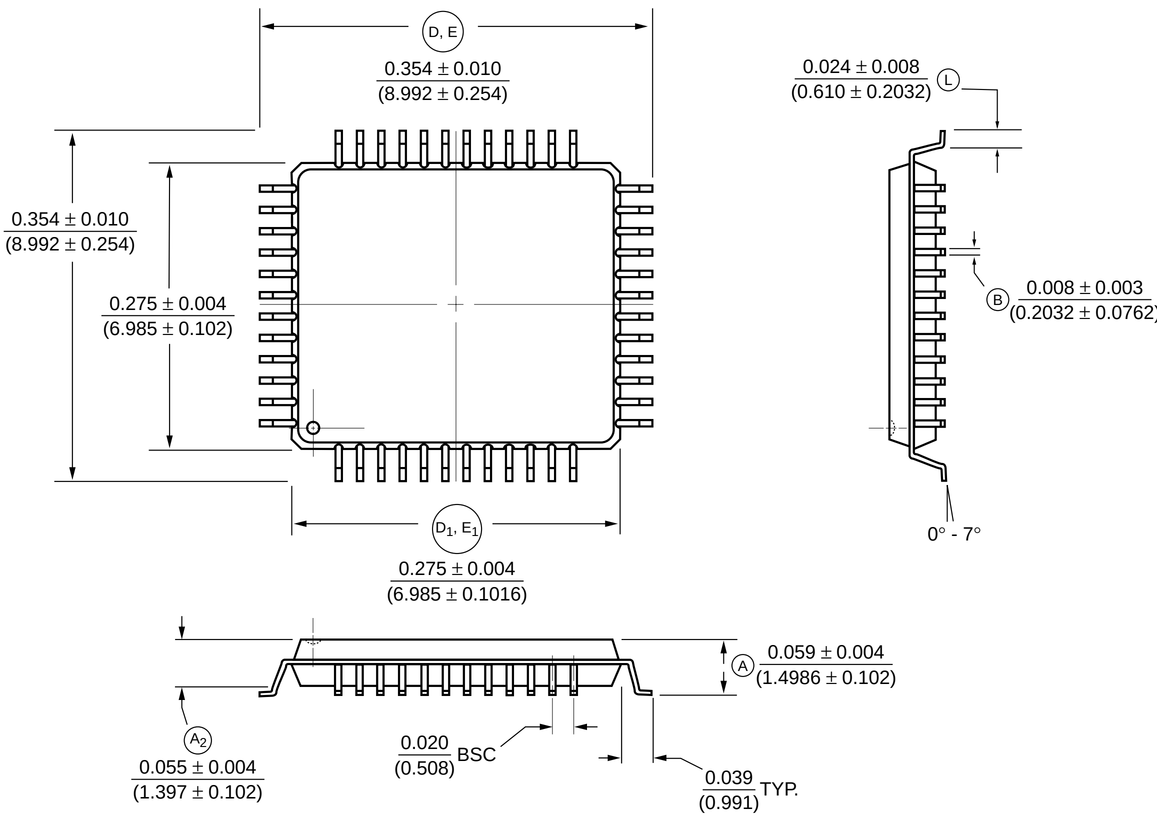
48-LEAD TQFP PACKAGE (FG)



Note: Circle (e.g. (B)) indicates JEDEC Reference.

Measurement Legend = Dimensions in Inches / (Dimensions in Millimeters)

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