	No.3127	C MOS LSI
		LC5805
SINGLE-CHIP 4-BIT MICROCOMPUTER WITH LCD DRIVER		

The LC5805 is a C-MOS 4-bit microcomputer that operates on low voltage, very low current and contains LCD drivers. It contains a 4-bit parallel processing ALU, many LCD segment outputs, many I/O ports, a 32.768kHz crystal oscillator, and a divider. It is ideally suited for use in desk-top calculator, camera, speech synthesis LSI controller, equipment controller applications as well as high-grade game watch/clock applications.

(1) Hardware features

- Supply voltage: 1.5V or 3.0V (typ.) (mask option)
- Very low current dissipation:
 - 3.0 μ A type. (1.5V supply voltage, at watch/clock operating mode)
 - 1.5 μ A type. (3.0V supply voltage, at watch/clock operating mode)
- Built-in crystal oscillator for watch/clock (32.768kHz crystal connected externally)
- Many output pins for LCD panel drive (42 pins)

Drivable LCD panel	Number of drivable LCD segments
1/3 bias 1/3 duty	126 segments
1/2 bias 1/3 duty	126 segments
1/2 bias 1/2 duty	84 segments
Static	42 segments
- Many input/output pins
 - Ports for input only: 2 ports/8 pins
 - Input/output common ports: 2 ports/8 pins
 - Control output pins: 4 pins
- Possible to use LCD panel drive output pins as ports for output only (mask option)
Note: For the Ag version (1.5V), the segment output pins cannot be used as ports for output only.
- With initial reset pin
- ROM: 1024 x 16 bits
- RAM: 128 x 4 bits
- Cycle time: 244 μ s . (or 122 μ s ./mask option)
- Built-in step-up circuit, step-down circuit
- Shipping style: Chip (or QIP80)

(2) Software features

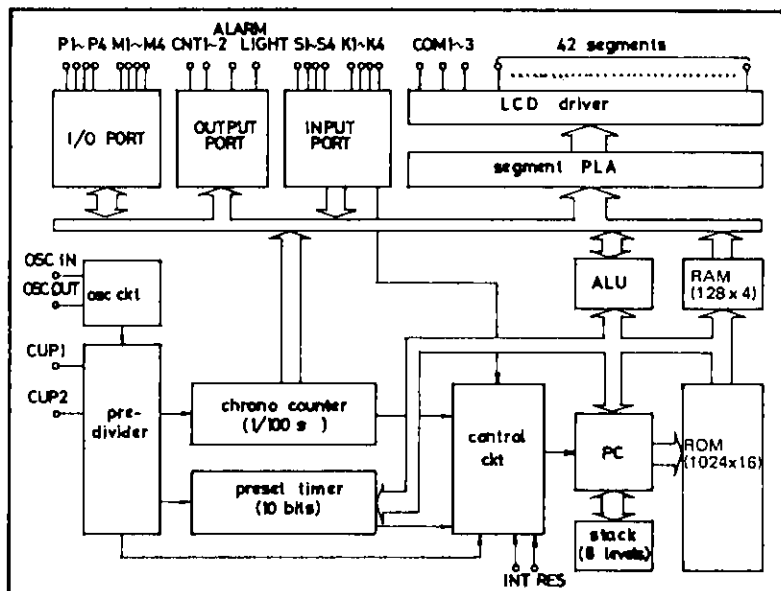
- Powerful instruction set: 119 instructions
- 8-level subroutine nesting (common with interrupt)
- External interrupt function
- 15-bit divider for watch/clock
- Built-in counter for 1/100-second chronograph
- Built-in 10-bit programmable timer
- HALT function
- Automatic select of all addresses (direct addressing type)
- Single stepping of all instructions
- Built-in data pointer

(3) Application development tools

For performing application development, the evaluation chip (LC5899) and the dedicated application development tools are prepared.

- SDS410 system
Application development program of microcomputer can be made in assembly language (edit, assemble).
- EVA510 + TB51 + display board + LC5899
By connecting to the SDS410, application development program can be corrected and debugged. The EVE510 is a control ROM-replaced version of the EVA410.
- TB51 + display board + LC5899
By using the EPROM (2732) with application development program data written in, mounting evaluation can be performed.

Equivalent Circuit Block Diagram

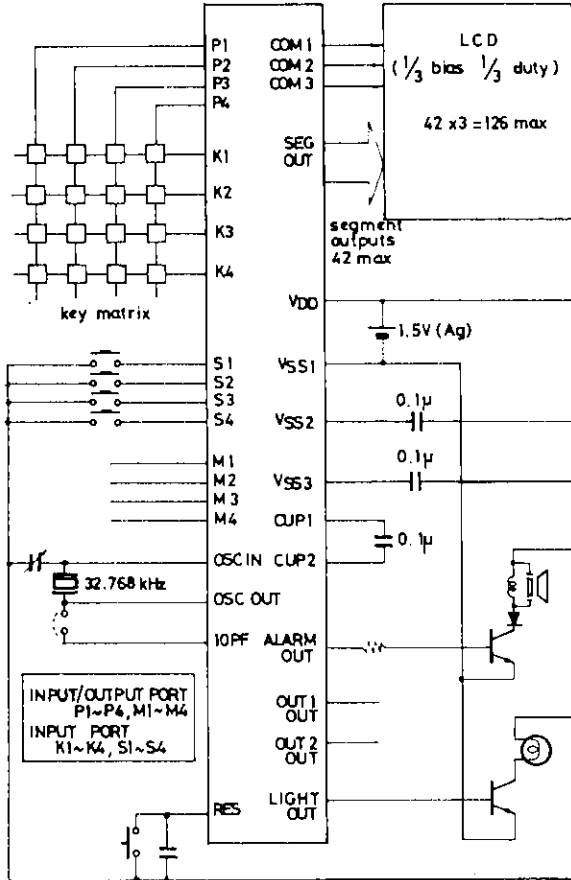


Application Areas

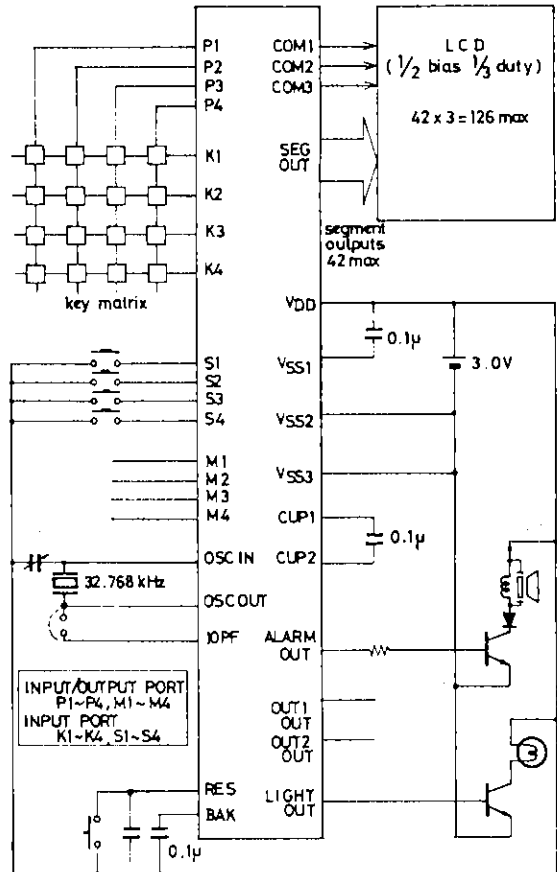
- 1) Multifunction watch/clock with calculator
- 2) Controller of speech synthesis LSI
- 3) Watch/clock with memory (external memory)
- 4) Controller of camera
- 5) Mechanical controller of VTR, radio-cassette recorder, tape deck, etc.
- 6) Controller of telephone dialer, etc.

Sample Application Circuits

(1) Typical application circuit using Ag battery (1/3 bias 1/3 duty)

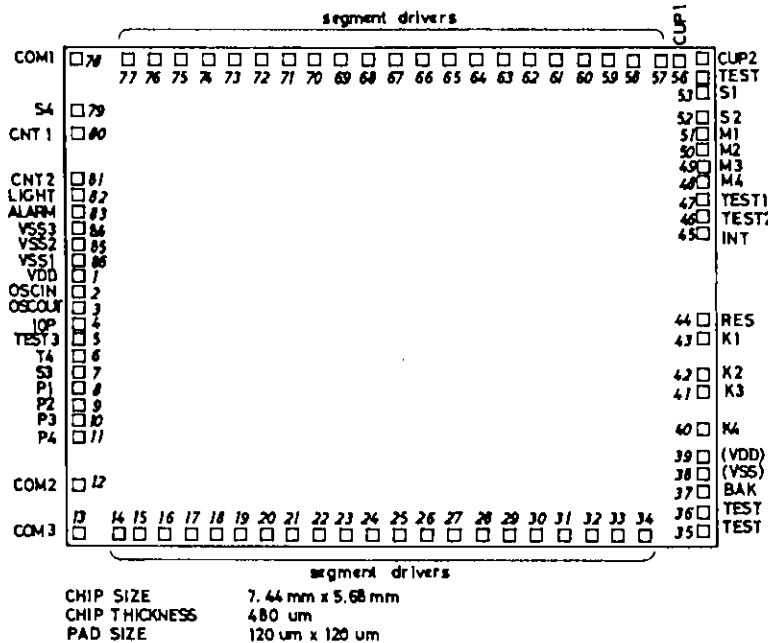


(2) Typical application circuit using Li battery (1/2 bias 1/3 duty)



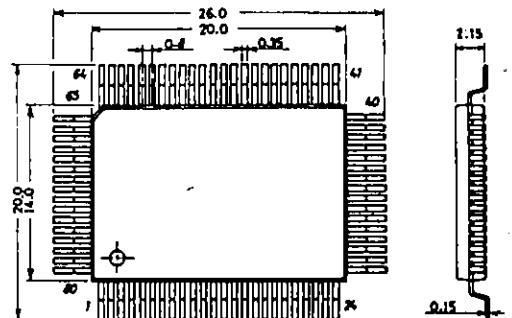
Unit (capacitance: F)

Pad Assignment of LSI Chip



Package Dimensions

(unit: mm) 3044B-Q80A1C



SANYO: QIP80A

Pad Name and Coordinates

Pin assignment of QIP80					Pin assignment of QIP80				
	Pad No.	Pin name	X (μm)	Y (μm)		Pad No.	Pin name	X (μm)	Y (μm)
73	1	VDD	-3560	+ 193	30	44	RES	+3560	- 314
74	2	OSCIN	"	+ 12	32	45	INT	"	+ 676
75	3	OSCOU	"	- 168	33	46	TEST2	"	+ 856
-	4	10P	"	- 348	34	47	TEST1	"	+1083
76	5	TEST3	"	- 527	35	48	M4	"	+1264
77	6	T4	"	- 708	36	49	M3	"	+1444
78	7	S3	"	- 888	37	50	M2	"	+1623
-	8	P1	"	-1068	38	51	M1	"	+1804
-	9	P2	"	-1247	39	52	S2	"	+1983
79	10	P3	"	-1428	40	53	S1	"	+2294
80	11	P4	"	-1608	-	54	TEST	"	+2475
1	12	COM2	"	-2146	41	55	CUP2	"	+2684
2	13	COM3	"	-2684	42	56	CUP1	+3256	"
3	14	Seg	-3042	"	43	57	Seg	+3065	"
4	15	↑	-2810	"	44	58	↑	+2770	"
5	16		-2516	"	45	59		+2475	"
6	17		-2221	"	46	60		+2179	"
7	18		-1925	"	47	61		+1884	"
8	19		-1630	"	48	62		+1588	"
9	20		-1334	"	49	63		+1294	"
10	21		-1040	"	50	64		+ 998	"
11	22		- 744	"	51	65		+ 693	"
12	23		- 438	"	52	66		+ 386	"
13	24		- 133	"	53	67		+ 81	"
14	25		+ 174	"	54	68		- 226	"
15	26		+ 480	"	55	69		- 532	"
16	27		+ 786	"	56	70		- 837	"
17	28		+1093	"	57	71		-1143	"
18	29		+1398	"	58	72		-1450	"
19	30		+1703	"	59	73		-1756	"
20	31		+2010	"	60	74		-2061	"
21	32		+2315	"	61	75		-2367	"
22	33		+2621	"	62	76		-2674	"
23	34	Seg	+2928	"	63	77	Seg	-2980	"
-	35	TEST	+3560	"	64	78	COM1	-3560	"
-	36	TEST	"	-2473	65	79	S4	"	+2079
25	37	BAK	"	-2253	66	80	CNT1	"	+1832
-	38	(VSS)	"	-2031	67	81	CNT2	"	+1272
-	39	(VDD)	"	-1851	68	82	LIGHT	"	+1092
26	40	K4	"	-1545	69	83	ALARM	"	+ 913
27	41	K3	"	-1110	70	84	VSS3	"	+ 733
28	42	K2	"	- 928	71	85	VSS2	"	+ 552
29	43	K1	"	- 494	72	86	VSS1	"	+ 372

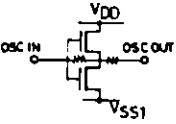
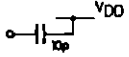
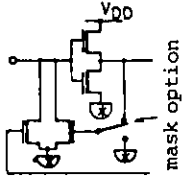
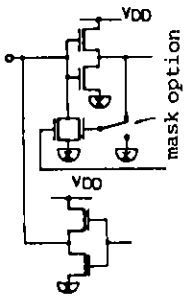
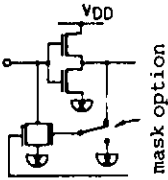
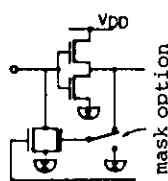
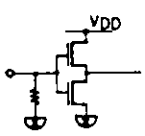
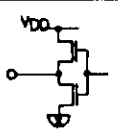
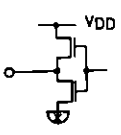
The above pad coordinates are such that the chip center is taken as the origin and the values of (X, Y) represent the coordinates of the center of each pad.

Pin 24 of QIP80: NC

Pin 31 of QIP80: SUB

(NC, SUB: Open)

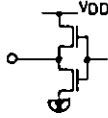
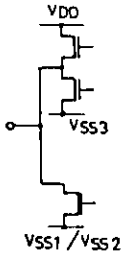
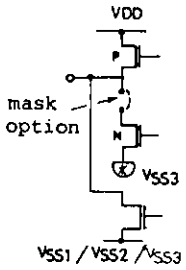
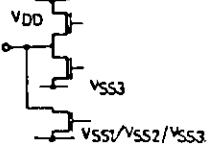
Pin Description

Pad No.	Pin Name	Input/Output	Circuit Configuration	Function
2	OSCIN	Input		32.768kHz crystal is connected across OSCIN and OSCOUT for oscillation. Used as reference clock for watch/clock and system clock. 20pF capacitor is connected across OSCOUT and VDD.
3	OSCOUT	Output		
4	10P	—		Connected to OSCOUT and used as oscillation phase compensation capacitor.
53 52 7 79	S1 S2 S3 S4	Input		Port for input only. With 7ms or 32ms chattering eliminator. By applying VDD to S1 to S4 simultaneously, LSI inside is reset. (mask option)
8 9 10 11 51 50 49 48	P1 P2 P3 P4 M1 M2 M3 M4	Input/Output		Input/output pins for selecting between the following 2 operations with instruction. (1) Input pin for fetching data into RAM. (2) Output pin for outputting data from RAM.
43 42 41 40	K1 K2 K3 K4	Input		(1) Input pin for fetching data into RAM through 7ms or 32ms chattering eliminator. (2) K4 signal is used to operate decimal counter (for 1/100-second count) inside LSI with instruction.
45	INT	Input		External interrupt request control input pin.
44	RES	Input		Input pin for resetting LSI inside.
37	BAK			(-) power supply pin for logic unit inside LSI. When using 3.0V supply, a capacitor must be connected across BAK and VDD to prevent logic unit from malfunctioning.
80 81	CNT1 CNT2	Output		Pins for output only.
82	LIGHT	Output		Pin for output only. Suited for outputting signal to drive transistor for light.

Continued on next page.

LC5805

Continued from preceding page.

Pad No.	Pin Name	Input/Output	Circuit Configuration	Function																																									
83	ALARM	Output		Pin for output only. Used to output 4kHz, 2kHz, 1kHz modulation signal with instruction. Also used to output non-modulation signal.																																									
1	VDD			(+) Power supply pin.																																									
84 85 86	VSS3 VSS2 VSS1			(-) Power supply pin. • 1.5V/3.0V selectable with mask option. For 1.5V use, apply (-) side to VSS1. For 3.0V use, apply (-) side to VSS2. • Also used as power supply for LCD drive.																																									
<table border="1" data-bbox="874 667 1423 878"> <thead> <tr> <th rowspan="2"></th> <th colspan="3">1.5V USE</th> <th colspan="3">3.0V USE</th> </tr> <tr> <th>static</th> <th>1/2bias</th> <th>1/3bias</th> <th>static</th> <th>1/2bias</th> <th>1/3bias</th> </tr> </thead> <tbody> <tr> <td>VDD</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>VSS1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>VSS2</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>VSS3</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>The above Table shows how to connect external parts in each case.</p>						1.5V USE			3.0V USE			static	1/2bias	1/3bias	static	1/2bias	1/3bias	VDD							VSS1							VSS2							VSS3						
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VDD																																													
VSS1																																													
VSS2																																													
VSS3																																													
55 56	CUP1 CUP2			Pins for connecting voltage step-up (step-down) capacitor.																																									
78 12 13	COM1 COM2 COM3	Output		Output pins for LCD panel common electrode. The following pin is used in each case.																																									
<table border="1" data-bbox="896 1108 1407 1303"> <thead> <tr> <th></th> <th>Static</th> <th>1/2 duty</th> <th>1/3 duty</th> </tr> </thead> <tbody> <tr> <td>COM1</td> <td>○</td> <td>○</td> <td>○</td> </tr> <tr> <td>COM2</td> <td>—</td> <td>○</td> <td>○</td> </tr> <tr> <td>COM3</td> <td>—</td> <td>—</td> <td>○</td> </tr> <tr> <td>Alternating frequency</td> <td>32Hz</td> <td>32Hz</td> <td>43Hz</td> </tr> </tbody> </table>						Static	1/2 duty	1/3 duty	COM1	○	○	○	COM2	—	○	○	COM3	—	—	○	Alternating frequency	32Hz	32Hz	43Hz																					
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Alternating frequency	32Hz	32Hz	43Hz																																										
14 to 22 57 to 64	Segment driver	Output		Output pins for LCD panel segments. • Also used as output ports with mask option. • When LSI inside is in reset mode, 32Hz, 64Hz or 128Hz static light-up signal is outputted at COM1 to COM3 and each LCD segment output and all LCD panel segments light up. • Segment PLA system is adopted to support any type of LCD layout.																																									
23 to 34 65 to 77	Segment driver	Output		Output pins for LCD panel segments. • Also used as output ports with mask option.																																									
5 6 35 36 46 47 54	TEST3 T4 TEST TEST TEST2 TEST1 TEST			Test pins (not used by user).																																									
38 39	(VSS) (VDD)			Backup power supply pin. Normally, not used.																																									

Note) Ag Battery: =VSS1, Li Battery: =VSS2

Operation from Ag Battery [Static]

Absolute Maximum Ratings at $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=0\text{V}$

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}	$V_{SS2}=V_{SS3}$	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1-4, M1-4, K1-4, P1-4, TEST-3, 10P, OSCIN, INT, RES (M1-4, P1-4: Input mode)	$V_{SS1}-0.3$ to 0.3	V
	V_{OUT1}	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)	$V_{SS1}-0.3$ to 0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1	$V_{SS2}-0.3$ to 0.3	V
Operating Temperature	T_{opr}		-20 to +65	$^\circ\text{C}$
Storage Temperature	T_{stg}		-30 to +125	$^\circ\text{C}$

Allowable Operating Conditions at $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=0\text{V}$

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}	$V_{SS2}=V_{SS3}$	-3.3		-2.4	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES, (M1-4, P1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		$V_{SS1}+0.2$	V
Operating Frequency	fopg	$T_a=-20$ to $+65^\circ\text{C}$	32		33	kHz

Electrical Characteristics at $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=0\text{V}$

			min	typ	max	unit
Input Resistance	R_{IN1A}	$V_{SS1}=-1.55\text{V}$, $V_{IL}=V_{SS1}+0.2\text{V}$, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	R_{IN1B}	$V_{SS1}=-1.55\text{V}$, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	R_{IN2A}	$V_{SS1}=-1.55\text{V}$, $V_{IL}=V_{SS1}+0.2\text{V}$, input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	R_{IN2B}	$V_{SS1}=-1.55\text{V}$, input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	R_{IN3}	$V_{SS1}=-1.55\text{V}$, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	$V_{SS1}=-1.55\text{V}$, $I_{OH}=-0.4\mu\text{A}$, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	$V_{SS1}=-1.55\text{V}$, $I_{OL}=0.4\mu\text{A}$, SEGOUT			$V_{SS2}+0.2$	V
"H"-Level Output Voltage	V_{OH2}	$V_{SS1}=-1.55\text{V}$, $I_{OH}=-4\mu\text{A}$, COM1	-0.2			V
"L"-Level Output Voltage	V_{OL2}	$V_{SS1}=-1.55\text{V}$, $I_{OL}=4\mu\text{A}$, COM1			$V_{SS2}+0.2$	V
"H"-Level Output Voltage	V_{OH3}	$V_{SS1}=-1.35\text{V}$, $I_{OH}=-250\mu\text{A}$, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	$V_{SS1}=-1.35\text{V}$, $I_{OL}=250\mu\text{A}$, ALM, LIGHT, CNT1, CNT2			$V_{SS1}+0.65$	V
"H"-Level Output Voltage	V_{OH4}	$V_{SS1}=-1.55\text{V}$, $I_{OH}=-20\mu\text{A}$, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	$V_{SS1}=-1.55\text{V}$, $I_{OL}=20\mu\text{A}$, M1-4, P1-4 (M1-4, P1-4: Output mode)			$V_{SS1}+0.2$	V
Output Voltage (doubler)	V_{SS2}	$V_{SS1}=-1.35\text{V}$, $C1=C2=0.1\mu\text{F}$, fopg=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	I_{DD1}	$V_{SS1}=-1.55\text{V}$, standard watch/clock operation, $C1=C2=0.1\mu\text{F}$, $C_o=C_g=20\text{pF}$, $C_I=25\text{kohm}$, Fig. 2		2.0		μA
Oscillation Start Voltage	V_{stt}	$C_o=C_g=20\text{pF}$, $C_I=25\text{kohm}$, Fig. 3	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	$V_{BAK}=V_{SS1}$, $C_o=C_g=20\text{pF}$, $C_I=25\text{kohm}$, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	$V_{SS}=-1.35\text{V}$, $C_o=C_g=20\text{pF}$, $C_I=25\text{kohm}$, Fig. 3			10	s
Oscillation Correction	10P	External pin	8	10	12	pF
Capacitance	20P	OSCOUT	16	20	24	pF

Operation from Li Battery [Static]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

				unit
Maximum Supply Voltage	VSS1	VBAK=VSS1 or VSS2	-4.0 to +0.3	V
	VSS2	VSS2=VSS3, VBAK=VSS1 or VSS2	-4.0 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3	VBAK-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)	VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT	VBAK-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)	VSS2-0.3 to 0.3	V
Operating Temperature	Topr		-20 to +65	°C
Storage Temperature	Tstg		-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Supply Voltage	VBAK		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	VIH	S1-4, K1-4, M1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	VIL	" "	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, VIL=VSS2+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	RIN1B	VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	RIN2A	VSS2=-2.9V, VIL=VSS2+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	RIN2B	VSS2=-2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4µA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4µA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4µA, COM1	-0.2			V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4µA, COM1			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250µA, ALM, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250µA, ALM, CNT1, CNT2			VSS2+0.65	V
"H"-Level Output Voltage	VOH4	VSS2=-2.4V, IOH=-150µA, LIGHT	-1.5			V
"L"-Level Output Voltage	VOL4	VSS2=-2.4V, IOL=150µA, LIGHT			VSS2+1.5	V
"H"-Level Output Voltage	VOH5	VSS2=-2.9V, IOH=-40µA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL5	VSS2=-2.9V, IOL=40µA, M1-4, P1-4 (M1-4, P1-4: Output mode)			VSS2+0.4	V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10µA	-1	-0.3		V
"L"-Level Output Voltage	VOL6	VSS2=-2.4V, IOL=40µA			VSS2+0.3 VSS2+1	V
"H"-Level Output Voltage	VOH7	VSS2=-2.4V, IOH=-5µA	-1	-0.3		V
"L"-Level Output Voltage	VOL7	VSS2=-2.4V, IOL=20µA			VSS2+0.3 VSS2+1	V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10µA	-1	-0.3		V
Output OFF Leakage Current	IOFF	VSS2=-2.6V, VOUT=VSS2			1	µA

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			min	typ	max	unit
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz			-1.35	V
Current Dissipation	I _{DDI}	VSS2=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kohm, Fig. 5		1.0		V
Oscillation Start Voltage	V _{stt}	VSS1=VSS2, Co=Cg=20pF, CI=25kohm, Fig. 6			-1.35	V
Oscillation Hold Voltage	V _{HOLD}	V _{BAK} =VSS1≅VSS2/2, Co=Cg=20pF, CI=25kohm, Fig. 5			-2.6	V
Oscillation Start Time	t _{stt}	VSS1=VSS2=-2.9V, Co=Cg=20pF, CI=25kohm, Fig. 6			10	s
Oscillation Correction	10P	External pin	8	10	12	pF
Capacitance	20P	OSCOUT	16	20	24	pF

Operation from EXTV [Static]

Absolute maximum Ratings at Ta=25±2°C, VDD=0V

					unit
Maximum Supply Voltage	VSS2	VSS2=VSS3		-4.0 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3		VSS1-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)		VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT		VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2-0.3 to 0.3	V
Operating Temperature	T _{opr}			-20 to +65	°C
Storage Temperature	T _{stg}			-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typz	max	unit
Supply Voltage	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	V _{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES, (M1-4, P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V _{IL}	" "	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, V _{IL} =VSS2+0.4, "L"-level hold tr., *1, Fig. 13	50		500	kohm
	RIN1B	VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 13	200		2000	kohm
	RIN2A	VSS2=-2.9V, V _{IL} =VSS2+0.4V, input mode, "L"-level hold tr., *2, Fig. 13	50		500	kohm
	RIN2B	VSS2=-2.9V, input mode, "L"-level tr., *2, Fig. 13	200		2000	kohm
	RIN3	VSS2=-2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, I _{OH} =-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, I _{OL} =0.4μA, SEGOUT		VSS2+0.2		V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, I _{OH} =-4μA, COM1	-0.2			V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, I _{OL} =4μA, COM1		VSS2+0.2		V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, I _{OH} =-250μA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, I _{OL} =250μA, ALM, LIGHT, CNT1, CNT2		VSS2+0.65		V
"H"-Level Output Voltage	VOH4	VSS2=-2.9V, I _{OH} =-40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL4	VSS2=-2.9V, I _{OL} =40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2+0.4		V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, I _{OH} =-10μA	-1	-0.3		V
"L"-Level Output Voltage	VOL6	VSS2=-2.4V, I _{OL} =40μA		VSS2+0.3	VSS2+1	V

Segment (output port)
PAD No. 14 to 22,
57 to 64
QIP80 pin No.
3 to 11, 43 to 50

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			min	typ	max	unit
"H"-Level Output Voltage	VOH7	VSS2=-2.4V, IOH=-5μA	-1	-0.3		V
"L"-Level Output Voltage	VOL7	VSS2=-2.4V, IOL=20μA		VSS2+0.3	VSS2+1	V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA	-1	-0.3		V
Output OFF Leakage Current	IOFF	VSS2=-2.6V, VOUT=VSS2			1	μA
Current Dissipation	IDD	VSS2=-2.9V, standard watch/clock operation, Co=Cg=20pF, CI=25kohm, Fig. 14		5.0		μA
Oscillation Start Voltage	Vstt	VSS1=VSS2, Co=Cg=20pF, CI=25kohm, Fig. 15	-2.2			V
Oscillation Hold Voltage	VHOLD	VBAK=VSS2, Co=Cg=20pF, CI=25kohm, Fig. 14			-2.0	V
Oscillation Start Time	tstt	VSS1=VSS2=-2.9V, Co=Cg=20pF, CI=25kohm, Fig. 15			10	s
Oscillation Correction Capacitance	10P 20P	External pin OSCOUT	8 16	10 20	12 24	pF pF

Operation from Ag Battery [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

				unit
Maximum Supply Voltage	VSS1		-4.0 to +0.3	V
	VSS2	VSS=VSS3	-4.0 to +0.3	V
Maximum Input Voltage	VIN1	S1-4, M1-4, K1-4, P1-4, TEST1-3, 10P OSCIN, INT, RES (M1-4, P1-4: Input mode)	VSS1-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)	VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1-2, CUP1	VSS2-0.3 to 0.3	V
Operating Temperature	Topr		-20 to +65	°C
Storage Temperature	Tstg		-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Supply Voltage	VSS1		-1.65		-1.30	V
	VSS2	VSS2=VSS3	-3.3		-2.4	V
"H"-Level Input Voltage	VIH	S1-4, M1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	VIL	" "	VSS1		VSS1+0.2	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS1=-1.55V, VIL=VSS1+0.2V, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	RIN1B	VSS1=-1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	RIN2A	VSS1=-1.55V, VIL=VSS1+0.2V input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	RIN2B	VSS1=-1.55V, input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	RIN3	VSS1=-1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS1=-1.55V, IOH=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS1=-1.55V, IOL=0.4μA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS1=-1.55V, IOH=-4μA, COM1-2	-0.2			V
"M"-Level Output Voltage	VOM	VSS1=-1.55V, IOH=-4μA, IOL=4μA, COM1-2	VSS1-0.2		VSS1+0.2	V
"L"-Level Output Voltage	VOL2	VSS1=-1.55V, IOL=4μA, COM1-2			VSS2+0.2	V

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			min	typ	max	unit
"H"-Level Output Voltage	VOH3	VSS1=-1.35V, IOH=-250μA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS1=-1.35V, IOL=250μA, ALM, LIGHT, CNT1, CNT2		VSS1+0.65		V
"H"-Level Output Voltage	VOH4	VSS1=-1.55V, IOH=-20μA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	VOL4	VSS1=-1.55V, IOL=20μA, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS1+0.2		V
Output Voltage (doubler)	VSS2	VSS1=-1.35V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	IDD1	VSS1=-1.55V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kohm, Fig. 2		2.0		μA
Oscillation Start Voltage	Vstt	Co=Cg=20pF, CI=25kohm, Fig. 3	-1.35			V
Oscillation Hold Voltage	VHOLD	VBAK=VSS1, Co=Cg=20pF, CI=25kohm, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	tstt	VSS1=-1.55V, Co=Cg=20pF, CI=25kohm, Fig. 3			10	s
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Li Battery [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

					unit
Maximum Supply Voltage	VSS1	VBAK=VSS1 or VSS2		-4.0 to +0.3	V
	VSS2	VSS2=VSS3, VBAK=VSS1 or VSS2		-4.0 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3		VBAK-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)		VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT		VBAK-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1-2, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2-0.3 to 0.3	V
Operating Temperature	Topr			-20 to +65	°C
Storage Temperature	Tstg			-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Supply Voltage	VBAK		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	VIH	S1-4, K1-4, M1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	VIL	" "		VSS2	VSS2+0.4	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, VIL=VSS2+0.4, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	RIN1B	VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	RIN2A	VSS2=-2.9V, VIL=VSS2+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	RIN2B	VSS2=-2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
	RIN3	VSS2=-2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4μA, SEGOUT		VSS2+0.2		V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4μA, COM1-2	-0.2			V
"M"-Level Output Voltage	VOM	VSS2=-2.9V, IOH=-4μA, VSS2/2-0.2 IOL=4μA, COM1-2		VSS2/2+0.2		V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4μA, COM1-2		VSS2+0.2		V

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			min	typ	max	unit
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250μA, ALM, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250μA, ALM, CNT1, CNT2		VSS2+0.65		V
"H"-Level Output Voltage	VOH4	VSS2=-2.4V, IOH=-150μA, LIGHT	-1.5			V
"L"-Level Output Voltage	VOL4	VSS2=-2.4V, IOL=150μA, LIGHT		VSS2+1.5		V
"H"-Level Output Voltage	VOH5	VSS2=-2.9V, IOH=-40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL5	VSS2=-2.9V, IOL=40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2+0.4		V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA, Segment (output port) PAD No. 14 to 22, 57 to 64, QIP80 pin No. 3 to 11, 43 to 50	-1	-0.3		V
"L"-Level Output Voltage	VOL6	VSS2=-2.4V, IOL=40μA, Segment (output port) PAD No. 14 to 22, 57 to 64, QIP80 pin No. 3 to 11, 43 to 50		VSS2+0.3	VSS2+1	V
"H"-Level Output Voltage	VOH7	VSS2=-2.4V, IOH=-5μA, Segment (output port) PAD No. 23 to 34, 65 to 77, QIP80 pin No. 12 to 23, 51 to 63	-1	-0.3		V
"L"-Level Output Voltage	VOL7	VSS2=-2.4V, IOL=20μA, Segment (output port) PAD No. 23 to 34, 65 to 77, QIP80 pin No. 12 to 23, 51 to 63		VSS2+0.3	VSS2+1	V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA, Segment PAD No. 14 to 22, 57 to 64, QIP80 pin No. 3 to 11, 43 to 50	-1	-0.3		V
Output OFF Leakage Current	IOFF	VSS2=-2.6V, VOUT=VSS2, 57 to 64, QIP80 pin No. 3 to 11, 43 to 50			1	μA
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			-1.35	V
Current Dissipation	IDD1	VSS2=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		1.0		μA
Oscillation Start Voltage	Vstt	VSS1≅VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 6	-1.35			V
Oscillation Hold Voltage	VHOLD	VBAK=VSS1=VSS2/2, Co=Cg=20pF, Cl=25kohm, Fig. 5			-2.6	V
Oscillation Start Time	tstt	VSS1=VSS2=-2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	s
Oscillation Correction Capacitance	10P 20P	External pin OSCOUT	8 16	10 20	12 24	pF pF

Operation from EXTV [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

					unit
Maximum Supply Voltage	VSS1			-4.0 to +0.3	V
	VSS2	VSS2=VSS3		-4.0 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3		VSS1-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)		VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT		VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1-2, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2-0.3 to 0.3	V
Operating Temperature	Topr			-20 to +65	°C
Storage Temperature	Tstg			-30 to +125	°C

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Allowable Operating Conditions at Ta=25±2°C, VDD=0V				min	typ	max	unit
Supply Voltage	VSS1			-3.6		-1.3	V
	VSS2	VSS2=VSS3		-3.6		-2.0	V
"H"-Level Input Voltage	V _{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)		-0.4		0	V
"L"-Level Input Voltage	V _{IL}	" "		VSS2		VSS2+0.4	V
Operation Frequency	f _{opg}	Ta=-20 to 65°C		32		33	kHz
Electrical Characteristics at Ta=25±2°C, VDD=0V				min	typ	max	unit
Input Resistance	R _{IN1A}	VSS2=-2.9V, V _{IL} =VSS2+0.4V, "L"-level hold tr., *1, Fig. 4		50		500	kohm
	R _{IN1B}	VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 4		200		2000	kohm
	R _{IN2A}	VSS2=-2.9V, V _{IL} =VSS2+0.4V, input mode, "L"-level hold tr., *2, Fig. 4		50		500	kohm
	R _{IN2B}	VSS2=-2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4		200		2000	kohm
	R _{IN3}	VSS2=-2.9V, TEST1, 2, RES		10		300	kohm
"H"-Level Output Voltage	V _{OH1}	VSS2=-2.9V, I _{OH} =-0.4μA, SEGOUT		-0.2			V
"L"-Level Output Voltage	V _{OL1}	VSS2=-2.9V, I _{OL} =0.4μA, SEGOUT				VSS2+0.2	V
"H"-Level Output Voltage	V _{OH2}	VSS2=-2.9V, I _{OH} =-4μA, COM1-2		-0.2			V
"M"-Level Output Voltage	V _{OM}	VSS2=-2.9V, I _{OH} =-4μA, I _{OL} =4μA, COM1-2	VSS2/2-0.2			VSS2/2+0.2	V
"L"-Level Output Voltage	V _{OL2}	VSS2=-2.9V, I _{OL} =4μA, COM1-2				VSS2+0.2	V
"H"-Level Output Voltage	V _{OH3}	VSS2=-2.4V, I _{OH} =-250μA, ALM, LIGHT, CNT1, CNT2		-0.65			V
"L"-Level Output Voltage	V _{OL3}	VSS2=-2.4V, I _{OL} =250μA, ALM, LIGHT, CNT1, CNT2				VSS2+0.65	V
"H"-Level Output Voltage	V _{OH4}	VSS2=-2.9V, I _{OH} =-40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)		-0.4			V
"L"-Level Output Voltage	V _{OL4}	VSS2=-2.9V, I _{OL} =40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)				VSS2+0.4	V
"H"-Level Output Voltage	V _{OH6}	VSS2=-2.4V, I _{OH} =-10μA	Segment ^(output port) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	-1	-0.3		V
"L"-Level Output Voltage	V _{OL6}	VSS2=-2.4V, I _{OL} =40μA		VSS2+0.3	VSS2+1		V
"H"-Level Output Voltage	V _{OH7}	VSS2=-2.4V, I _{OH} =5μA	Segment ^(output port) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	-1	-0.3		V
"L"-Level Output Voltage	V _{OL7}	VSS2=-2.4V, I _{OL} =20μA		VSS2+0.3	VSS2+1		V
"H"-Level Output Voltage	V _{OH6}	VSS2=-2.4V, I _{OH} =-10μA	Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	-1	-0.3		V
Output OFF Leakage Current	I _{OFF}	VSS2=-2.6V, V _{OUT} =VSS2					1
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, f _{opg} =32.768kHz, Fig. 5				-1.35	V
Current Dissipation	I _{DDI}	VSS2=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kohm, Fig. 5				5.0	μA
Oscillation Start Voltage	V _{stt}	VSS1=VSS2, Co=Cg=20pF, CI=25kohm, Fig. 6		-2.2			V
Oscillation Hold Voltage	V _{HOLD}	V _{BAK} =VSS2, Co=Cg=20pF, CI=25kohm, Fig. 5				-2.0	V
Oscillation Start Time	t _{stt}	VSS1=VSS2=-2.9V, Co=Cg=20pF, CI=25kohm, Fig. 6				10	s
Oscillation Correction Capacitance	10P	External pin		8	10	12	pF
	20P	OSCOU		16	20	24	pF

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Operation from Ag Battery [1/2 bias, 1/3 duty]

Absolute Maximum ratings at $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=0\text{V}$

				unit
Maximum Supply Voltage	VSS1		-4.0 to +0.3	V
	VSS2	VSS2=VSS3	-4.0 to +0.3	V
Maximum Input Voltage	VIN1	S1-4, M1-4, K1-4, P1-4, TEST1-3, 10P, OSCIN, INT, RES (M1-4, P1-4: Input mode)	VSS1-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)	VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1-3, CUP1	VSS2-0.3 to 0.3	V
Operating Temperature	Topr		-20 to +65	$^\circ\text{C}$
Storage Temperature	Tstg		-30 to +125	$^\circ\text{C}$

Allowable Operating Conditions at $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=0\text{V}$

			min	typ	max	unit
Supply Voltage	VSS1		-1.65		-1.30	V
	VSS2	VSS2=VSS3	-3.3		-2.4	V
"H"-Level Input Voltage	VIH	S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	VIL	" "		VSS1	VSS1+0.2	V
Operating Frequency	fopg	$T_a=-20$ to $+65^\circ\text{C}$	32		33	kHz

Electrical Characteristics at $T_a=25\pm 2^\circ\text{C}$, $V_{DD}=0\text{V}$

			min	typ	max	unit
Input Resistance	RIN1A	VSS1=-1.55V, VIL=VSS1+0.2V, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	RIN1B	VSS1=-1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	RIN2A	VSS1=-1.55V, VIL=VSS1+0.2V, input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	RIN2B	VSS1=-1.55V, input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	RIN3	VSS1=-1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS1=-1.55V, IOH=-0.4 μA , SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS1=-1.55V, IOL=0.4 μA , SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS1=-1.55V, IOH=-4 μA , COM1-3	-0.2			V
"M"-Level Output Voltage	VOM	VSS1=-1.55V, IOH=-4 μA , IOL=4 μA , COM1-3	VSS1-0.2		VSS1+0.2	V
"L"-Level Output Voltage	VOL2	VSS1=-1.55V, IOL=4 μA , COM1-3			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS1=-1.35V, IOH=-250 μA , ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS1=-1.35V, IOL=250 μA , ALM, LIGHT, CNT1, CNT2			VSS1+0.65	V
"H"-Level Output Voltage	VOH4	VSS1=-1.55V, IOH=-20 μA , M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	VOL4	VSS1=-1.55V, IOL=20 μA , M1-4, P1-4 (M1-4, P1-4: Output mode)			VSS1+0.2	V
Output Voltage (doubler)	VSS2	VSS1=-1.35V, C1=C2=0.1 μF , fopg=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	I _{DDI}	VSS1=-1.55V, standard watch/clock operation, C1=C2=0.1 μF , Co=Cg=20pF, CI=25kohm, Fig. 2		2.0		μA
Oscillation Start Voltage	V _{stt}	Co=Cg=20pF, CI=25kohm, Fig. 3	-1.35			V
Oscillation Hold Voltage	V _{HOLD}	VBAK=VSS1, Co=Cg=20pF, CI=25kohm, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	t _{stt}	VSS1=-1.35V, Co=Cg=20pF, CI=25kohm, Fig. 3			10	s
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

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Operation from Li Battery [1/2 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

				unit
Maximum Supply Voltage	VSS1	VBAK=VSS1 or VSS2	-4.0 to +0.3	V
	VSS2	VSS2=VSS3, VBAK=VSS1 or VSS2	-4.0 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3	VBAK-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)	VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT	VBAK-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1-3, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)	VSS2-0.3 to 0.3	V
Operation Temperature	Topr		-20 to +65	°C
Storage Temperature	Tstg		-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Supply Voltage	VBAK		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	VIH	S1-4, K1-4, M1-4, P1-4, INT RES (M1-4, P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	VIL	" "	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, VIL=VSS2+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	RIN1B	VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	RIN2A	VSS2=-2.9V, VIL=VSS2+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	RIN2B	VSS2=-2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
	RIN3	VSS2=-2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4µA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4µA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4µA, COM1-3	-0.2			V
"M"-Level Output Voltage	VOM	VSS2=-2.9V, IOH=-4µA, IOL=4µA, COM1-3	VSS2/2-0.2		VSS2/2+0.2	V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4µA, COM1-3			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250µA, ALM, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250µA, ALM, CNT1, CNT2			VSS2+0.65	V
"H"-Level Output Voltage	VOH4	VSS2=-2.4V, IOH=-150µA, LIGHT	-1.5			V
"L"-Level Output Voltage	VOL4	VSS2=-2.4V, IOL=150µA, LIGHT			VSS2+1.5	V
"H"-Level Output Voltage	VOH5	VSS2=-2.9V, IOH=-40µA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL5	VSS2=-2.9V, IOH=40µA, M1-4, P1-4 (M1-4, P1-4: Output mode)			VSS2+0.4	V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10µA, Segment (output port) PAD No. 14 to 22, QIP80 pin No. 3 to 11, 43 to 50	-1	-0.3		V
"L"-Level Output Voltage	VOL6	VSS2=-2.4V, IOL=40µA, Segment (output port) PAD No. 23 to 34, QIP80 pin No. 12 to 23, 51 to 63			VSS2+0.3 VSS2+1	V
"H"-Level Output Voltage	VOH7	VSS2=-2.4V, IOH=-5µA, Segment (output port) PAD No. 23 to 34, QIP80 pin No. 12 to 23, 51 to 63	-1	-0.3		V
"L"-Level Output Voltage	VOL7	VSS2=-2.4V, IOL=20µA, Segment (output port) PAD No. 23 to 34, QIP80 pin No. 12 to 23, 51 to 63			VSS2+0.3 VSS2+1	V

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"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA	Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	-1	-0.3		V
Output OFF Leakage Current	IOFF	VSS2=-2.6V, VOUT=VSS2				1	μA
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz				-1.35	V
Current Dissipation	I _{DDI}	VSS2=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5			1.0		μA
Oscillation Start Voltage	V _{stt}	VSS1=VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 6		-1.35		V	
Oscillation Hold Voltage	V _{HOLD}	VBAK=VSS1=VSS2/2, Co=Cg=20pF, Cl=25kohm, Fig. 5			-2.6	V	
Oscillation Start Time	t _{stt}	VSS1=VSS2=-2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	s	
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF	
	20P	OSCOUT	16	20	24	pF	

Operation from EXTV [1/2 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

					unit
Maximum Supply Voltage	VSS1			-4.0 to +0.3	V
	VSS2	VSS2=VSS3		-4.0 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3		VSS1-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)		VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT		VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1-3, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2-0.3 to 0.3	V
Operating Temperature	Topr			-20 to 65	°C
Storage Temperature	Tstg			-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Supply Voltage	VSS1		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	V _{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V _{IL}	" "	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Input Resistance	R _{IN1A}	VSS2=-2.9V, V _{IL} =VSS2+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R _{IN1B}	VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	R _{IN2A}	VSS2=-2.9V, V _{IL} =VSS2+0.4V, input mode, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R _{IN2B}	VSS2=-2.9V, input mode, "L"-level tr., *1, Fig. 4	200		2000	kohm
	R _{IN3}	VSS2=-2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4μA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4μA, COM1-3	-0.2			V
"M"-Level Output Voltage	VOM	VSS2=-2.9V, IOH=-4μA, IOL=4μA, COM1-3	VSS2/2-0.2		VSS2/2+0.2	V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4μA, COM1-3			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250μA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250μA ALM, LIGHT, CNT1, CNT2			VSS2+0.65	V

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			min	typ	max	unit
"H"-Level Output Voltage	VOH4	VSS2=-2.9V, IOH=-40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL4	VSS2=-2.9V, IOL=40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS2+0.4		V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA, Segment (output port) PAD No. 14 to 22,	-1	-0.3		V
"L"-Level Output Voltage	VOL6	VSS2=-2.4V, IOL=40μA, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	VSS2+0.3	VSS2+1		V
"H"-Level Output Voltage	VOH7	VSS2=-2.4V, IOH=-5μA, Segment (output port) PAD No. 23 to 34,	-1	-0.3		V
"L"-Level Output Voltage	VOL7	VSS2=-2.4V, IOL=20μA, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	VSS2+0.3	VSS2+1		V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA, Segment PAD No. 14 to 22,	-1	-0.3		V
Output OFF Leakage Current	I _{OFF}	VSS2=-2.6V, V _{OUT} =VSS2, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50			1	μA
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz			-1.35	V
Current Dissipation	I _{DDI}	VSS2=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		5.0		μA
Oscillation Start Voltage	V _{stt}	VSS1=VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 6	-2.2			V
Oscillation Hold Voltage	V _{HOLD}	VBAK=VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 6			-2.0	V
Oscillation Start Time	t _{stt}	VSS1=VSS2=-2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	s
Oscillation Correction Capacitance	10P 20P	External pin OSCOUT	8 16	10 20	12 24	pF pF

Operation from Ag Battery [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V

					unit
Maximum Supply Voltage	VSS1			-4.0 to +0.3	V
	VSS2			-4.0 to +0.3	V
	VSS3			-5.5 to +0.3	V
Maximum Input Voltage	VIN1	S1-4, M1-4, K1-4, P1-4, TEST1-3, 10P, OSCIN, INT, RES (M1-4, P1-4: Input mode)		VSS1-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4: Output mode)		VSS1-0.3 to 0.3	V
	VOUT2	SEGOUT, COM1, COM2, COM3, CUP1		VSS3-0.3 to 0.3	V
Operating Temperature	T _{opr}			-20 to +65	°C
Storage Temperature	T _{stg}			-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, VDD=0V

			min	typ	max	unit
Supply Voltage	VSS1		-1.65		-1.30	V
	VSS2		-3.3		-2.4	V
	VSS3		-4.95		-3.7	V
"H"-Level Input Voltage	V _{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	V _{IL}	" "	VSS1	VSS1+0.2		V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

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Electrical Characteristics at Ta=25±2°C, VDD=0V			min	typ	max	unit
Input Resistance	RIN1A	VSS1=-1.55V, VIL=VSS1+0.2V, "L"-level hold tr., *1, Fig. 7	50		500	kohm
	RIN1B	VSS1=-1.55V, "L"-level pull-in tr., *1, Fig. 7	200		2000	kohm
	RIN2A	VSS1=-1.55V, VIL=VSS1+0.2V, input mode, "L"-level hold tr., *2, Fig. 7	50		500	kohm
	RIN2B	VSS1=-1.55V, input mode, "L"-level pull-in tr., *2, Fig. 7	200		2000	kohm
	RIN3	VSS1=-1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	VOH1	VSS1=-1.55V, IOH=-0.4μA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	VOM1-1	VSS1=-1.55V, IOH=-0.4μA,)	VSS1-0.2		VSS1+0.2	V
"M2"-Level Output Voltage	VOM2-1	IOH=0.4μA, SEGOUT	VSS2-0.2		VSS2+0.2	V
"L"-Level Output Voltage	VOL1	VSS1=-1.55V, IOL=-0.4μA, SEGOUT	VSS3-0.2		VSS3+0.2	V
"H"-Level Output Voltage	VOH2	VSS1=-1.55V, IOH=-4μA, COM1, COM2, COM3	-0.2			V
"M1"-Level Output Voltage	VOM1-2	VSS1=-1.55V, IOL=4μA,)	VSS1-0.2		VSS1+0.2	V
"M2"-Level Output Voltage	VOM2-2	IOH=-4μA, COM1, COM2, COM3	VSS2-0.2		VSS2+0.2	V
"L"-Level Output Voltage	VOL2	VSS1=-1.55V, IOL=4μA, COM1-3			VSS3+0.2	V
"H"-Level Output Voltage	VOH3	VSS1=-1.35V, IOH=-250μA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	VOL3	VSS1=-1.35V, IOL=250μA, ALM, LIGHT CNT1, CNT2			VSS1+0.65	V
"H"-Level Output Voltage	VOH4	VSS1=-1.55V, IOH=-20μA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	VOL4	VSS1=-1.55V, IOL=20μA, (M1-4, P1-4: Output mode)			VSS1+0.2	V
Output Voltage	VSS2	(VSS1=-1.35V, C1 to C3=0.1μF, fopg=32.768kHz, Fig. 8)			-2.5	V
	VSS3				-3.75	V
Current Dissipation	IIDD1	VSS1=-1.55V, standard watch/clock operation, C1 to C3=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 8		3.5		μA
Oscillation Start Voltage	Vstt	Co=Cg=20pF, Cl=25kohm, Fig. 9	-1.35			V
Oscillation Hold Voltage	VHOLD	VBAK=VSS1, Co=Cg=20pF, Cl=25kohm, Fig. 8	-1.65		-1.30	V
Oscillation Start Time	tstt	VSS1=-1.35V, Co=Cg=20pF, Cl=25kohm, Fig. 9			10	s
Oscillation Correction	10P	External pin	8	10	12	pF
Capacitance	20P	OSCOUT	16	20	24	pF

Operating from Li Battery [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, VDD=0V						unit
Maximum Supply Voltage	VSS1	VBAK=VSS1 or VSS2			-4.0 to +0.3	V
	VSS2	VBAK=VSS1 or VSS2			-4.0 to +0.3	V
	VSS3	VBAK=VSS1 or VSS2			-5.5 to +0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN, TEST3			VBAK-0.3 to 0.3	V
	VIN2	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4: Input mode)			VSS2-0.3 to 0.3	V
Maximum Output Voltage	VOUT1	TEST3, OSCOUT			VBAK-0.3 to 0.3	V
	VOUT2	ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4, CUP2 (M1-4, P1-4: Output mode)			VSS2-0.3 to 0.3	V
	VOUT3	SEGOUT 1-64, COM1 to COM3, CUP1			VSS3-0.3 to 0.3	V
Operating Temperature	Topr				-20 to +65	°C
Storage Temperature	Tstg				-30 to +125	°C

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Allowable Operating Conditions at Ta=25±2°C, VDD=0V,		min	typ	max	unit
Supply Voltage	VBAK	-3.6		-1.3	V
	VSS2	-3.6		-2.0	V
	VSS3	-5.0		-3.9	V
"H"-Level Input Voltage	VIH	-0.4		0	V
					VSS3≡VSS2+VSS1 S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4: Input mode)
"L"-Level Input Voltage	VIL	VSS2		VSS2+0.4	V
Operating Frequency	fopg	32		33	kHz
					Ta=-20 to +65°C
Electrical Characteristics at Ta=25±2°C, VDD=0V		min	typ	max	unit
Input Resistance	RIN1A	50		500	kohm
					VSS2=-2.9V, VIL=VSS2+0.4V, "L"-level hold tr., *1, Fig. 10
	RIN1B	200		2000	kohm
					VSS2=-2.9V, "L"-level pull-in tr., *1, Fig. 10
	RIN2A	50		500	kohm
					VSS2=-2.9V, VIL=VSS2+0.4V, input mode, "L"-level hold tr., *2, Fig. 10
	RIN2B	200		2000	kohm
					VSS2=-2.9V, input mode, "L"-level pull-in tr., *2, Fig. 10
	RIN3	10		300	kohm
					VSS2=-2.9V, TEST1, 2, RES
"H"-Level Output Voltage	VOH1	-0.2			V
					VSS2=-2.9V, IOH=-0.4μA, SEGOUT
"M1"-Level Output Voltage	VOM1-1	1/2VSS2-0.2		1/2VSS2+0.2	V
					VSS2=-2.9V, IOH=-0.4μA,)
"M2"-Level Output Voltage	VOM2-1	VSS2-0.2		VSS2+0.2	V
					IOH=0.4μA, SEGOUT
"L"-Level Output Voltage	VOL1			VSS3+0.2	V
					VSS2=-2.9V, IOL=0.4μA, SEGOUT
"H"-Level Output Voltage	VOH2	-0.2			V
					VSS2=-2.9V, IOH=-4μA, COM1-3
"M1"-Level Output Voltage	VOM1-2	1/2VSS2-0.2		1/2VSS2+0.2	V
					VSS2=-2.9V, IOH=-4μA)
"M2"-Level Output Voltage	VOM2-2	VSS2-0.2		VSS2+0.2	V
					IOH=4μA, COM1, COM2, COM3)
"L"-Level Output Voltage	VOL2			VSS3+0.2	V
					VSS2=-2.9V, IOL=4μA, COM1-3
"H"-Level Output Voltage	VOH3	-0.65			V
					VSS2=-2.4V, IOH=-250μA, ALM, CNT1, CNT2
"L"-Level Output Voltage	VOL3			VSS+0.65	V
					VSS2=-2.4V, IOL=250μA, ALM, CNT1, CNT2
"H"-Level Output Voltage	VOH4	-1.5			V
					VSS2=-2.4V, IOH=-150μA, LIGHT
"L"-Level Output Voltage	VOL4			VSS2+1.5	V
					VSS2=-2.4V, IOL=150μA, LIGHT
"H"-Level Output Voltage	VOH5	-0.4			V
					VSS2=-2.9V, IOH=-40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)
"L"-Level Output Voltage	VOL5			VSS2+0.4	V
					VSS2=-2.9V, IOL=40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)
"H"-Level Output Voltage	VOH6	-1	-0.3		V
					VSS2=-2.4V, Segment (output port) IOH=-10μA PAD No. 14 to 22,
"L"-Level Output Voltage	VOL6			VSS2+0.3	V
					VSS2=-2.4V, 57 to 64 IOL=40μA QIP80 pin No. 3 to 11, 43 to 50
"H"-Level Output Voltage	VOH7	-1	-0.3		V
					VSS2=-2.4V, Segment (output port) IOH=-5μA PAD No. 23 to 34,
"L"-Level Output Voltage	VOL7			VSS2+0.3	V
					VSS2=-2.4V, 65 to 77 IOL=20μA QIP80 pin No. 12 to 23, 51 to 63
"H"-Level Output Voltage	VOH6	-1	-0.3		V
					VSS2=-2.4V, Segment IOH=-10μA PAD No. 14 to 22,
Output OFF Leakage Current	IOFF			1	μA
					VSS2=-2.6V, 57 to 64 VOUT=VSS2 QIP80 pin No. 3 to 11, 43 to 50
Output Voltage	VSS1			-1.35	V
					(VSS2=-2.9V, C1 to C4=0.1μF,)
	VSS3			-4.1	V
					fopg=32.768kHz, Fig. 11
Current Dissipation	IIDD		2.0		μA
					VSS2=-2.9V, standard watch/clock operation, C1 to C4=0.1μF, Co=Cg=20pF, CI=250kohm, Fig. 11
Oscillation Start Voltage	Vstt	-1.35			V
					VSS1=VSS2, Co=Cg=20pF, CI=250kohm, Fig. 12

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Continued from preceding page.			min	typ	max	unit
Oscillation Hold Voltage	V _{HOLD}	V _{BAK} =V _{SS1} =V _{SS2} /2, Co=Cg=20pF, CI=250kohm, Fig. 11			-2.6	V
Oscillation Start Time	t _{stt}	V _{SS2} =-2.9V, V _{SS1} =V _{SS2} , Co=Cg=20pF, CI=25kohm, Fig. 12			10	s
Oscillation Correction Capacitance	10P 20P	External pin OSCOUT	8 16	10 20	12 24	pF pF

Operation from EXTV [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

					unit
Maximum Supply Voltage	V _{SS1} V _{SS2} V _{SS3}			-4.0 to +0.3 -4.0 to +0.3 -5.5 to +0.3	V V V
Maximum Input Voltage	V _{IN1} V _{IN2}	10P, OSCIN, TEST3 S1-4, M1-4, K1-4, P1-4, TEST1, 2, INT, RES (M1-4, P1-4: Input mode)		V _{SS1} -0.3 to 0.3 V _{SS1} -0.3 to 0.3	V V
Maximum Output Voltage	V _{OUT1} V _{OUT2} V _{OUT3}	TEST3, OSCOUT ALRM, LIGHT, CNT1, CNT2, M1-4, P1-4, CUP2 (M1-4, P1-4: Output mode) SEGOUT1-64, COM1 to COM3, CUP1		V _{SS1} -0.3 to 0.3 V _{SS2} -0.3 to 0.3 V _{SS3} -0.3 to 0.3	V V V
Operating Temperature	T _{opr}			-20 to +65	°C
Storage Temperature	T _{stg}			-30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V,

			min	typ	max	unit
Supply Voltage	V _{SS1} V _{SS2} V _{SS3}	V _{SS3} =V _{SS2} +V _{SS1}	-3.6 -3.6 -5.0		-1.3 -2.0 -3.9	V V V
"H"-Level Input Voltage	V _{IH}	S1-4, M1-4, K1-4, INT, RES (M1-4, P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V _{IL}	" "	V _{SS2}		V _{SS2} +0.4	V
Operating Frequency	f _{opg}	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R _{IN1A} R _{IN1B} R _{IN2A} R _{IN2B} R _{IN3}	V _{SS2} =-2.9V, V _{IL} =V _{SS2} +0.4V, "L"-level hold tr., *1, Fig. 10 V _{SS2} =-2.9V, "L"-level pull-in tr., *1, Fig. 10 V _{SS2} =-2.9V, V _{IL} =V _{SS2} +0.4V, input mode, "L"-level hold tr., *2, Fig. 10 V _{SS2} =-2.9V, input mode, "L"-level pull-in tr., *2, Fig. 10 V _{SS2} =-2.9V, TEST1, 2, RES	50 200 50 200 10		500 2000 500 2000 300	kohm kohm kohm kohm kohm
"H"-Level Output Voltage	V _{OH1}	V _{SS2} =-2.9V, I _{OH} =-0.4μA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	V _{OM1-1}	V _{SS2} =-2.9V, I _{OH} =-0.4μA, I _{OL} =0.4μA, SEGOUT	1/2V _{SS2} -0.2		1/2V _{SS2} +0.2	V
"M2"-Level Output Voltage	V _{OM2-1}		V _{SS2} -0.2		V _{SS2} +0.2	V
"L"-Level Output Voltage	V _{OL1}	V _{SS2} =-2.9V, I _{OL} =0.4μA, SEGOUT			V _{SS3} +0.2	V
"H"-Level Output Voltage	V _{OH2}	V _{SS2} =-2.9V, I _{OH} =-4μA, COM1, COM2, COM3	-0.2			V
"M1"-Level Output Voltage	V _{OM1-2}	V _{SS2} =-2.9V, I _{OH} =-4μA, I _{OL} =4μA, COM1, COM2, COM3	1/2V _{SS2} -0.2		1/2V _{SS2} +0.2	V
"M2"-Level Output Voltage	V _{OM2-2}		V _{SS2} -0.2		V _{SS2} +0.2	V
"L"-Level Output Voltage	V _{OL2}	V _{SS2} =-2.9V, I _{OL} =4μA, COM1, COM2, COM3			V _{SS2} +0.2	V
"H"-Level Output Voltage	V _{OH3}	V _{SS2} =-2.4V, I _{OH} =-250μA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	V _{OL3}	V _{SS2} =-2.4V, I _{OL} =250μA, ALM, LIGHT, CNT1, CNT2			V _{SS2} +0.65	V
"H"-Level Output Voltage	V _{OH4}	V _{SS2} =-2.9V, I _{OH} =-40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	V _{OL4}	V _{SS2} =-2.9V, I _{OL} =40μA, M1-4, P1-4 (M1-4, P1-4: Output mode)			V _{SS2} +0.4	V

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			min	typ	max	unit
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA	-1	-0.3		V
"L"-Level Output Voltage	VOL6	VSS2=-2.4V, IOL=40μA	VSS2+0.3	VSS2+1		V
"H"-Level Output Voltage	VOH7	VSS2=-2.4V, IOH=-5μA	-1	-0.3		V
"L"-Level Output Voltage	VOL7	VSS2=-2.4V, IOL=20μA	VSS2+0.3	VSS2+1		V
"H"-Level Output Voltage	VOH6	VSS2=-2.4V, IOH=-10μA	-1	-0.3		V
Output OFF Leakage Current	I _{OFF}	VSS2=-2.6V, V _{OUT} =VSS2			1	μA
Output Voltage	VSS1 VSS3	(VSS2=-2.9V, C1 to C4=0.1μF, f _{opg} =32.768kHz, Fig. 11)			-1.35 4.1	V V
Current Dissipation	I _{DDI}	VSS2=-2.9V, standard watch/clock operation, C1 to C4=0.1μF, Co=Cg=20pF, Cl=250kohm, Fig. 11		5.0		μA
Oscillation Start Voltage	V _{stt}	VSS1=VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 12	-2.2			V
Oscillation Hold Voltage	V _{HOLD}	V _{BAK} =VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 11			-2.0	V
Oscillation Start Time	t _{stt}	VSS2=-2.9V, VSS1=VSS2, Co=Cg=20pF, Cl=25kohm, Fig. 12			10	s
Oscillation Correction Capacitance	10P 20P	External pin OSCOUT	8 16	10 20	12 24	pF pF

*1 S1·S2·S3·S4·INT·K1·K2·K3·K4

*2 M1·M2·M3·M4·P1·P2·P3·P4

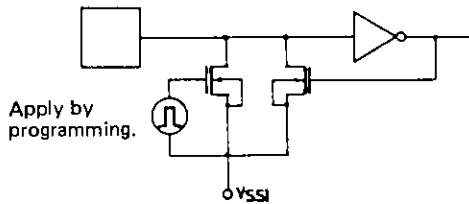


Fig. 1 Input configuration of S1-4, M1-4, K1-4, P1-4, INT

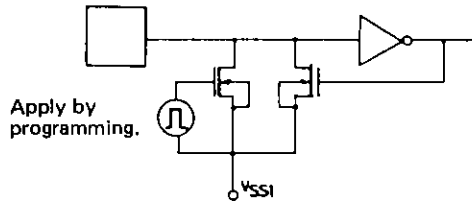


Fig. 7 Input configuration of S1-4, M1-4, K1-4, P1-4, INT

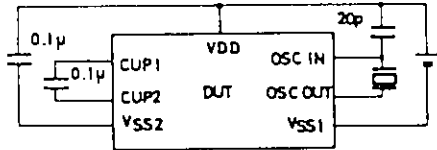


Fig. 2 Output voltage, current dissipation, oscillation hold voltage test circuit

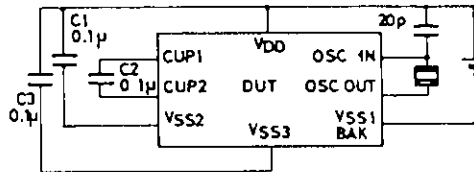


Fig. 8 Output voltage, current dissipation, oscillation hold voltage test circuit

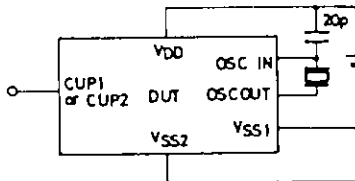


Fig. 3 Oscillation start voltage, oscillation start time, frequency stability test circuit

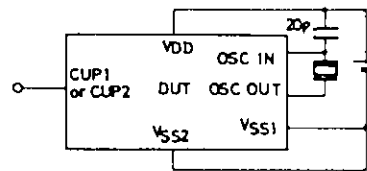


Fig. 9 Oscillation start voltage, oscillation start time, frequency stability test circuit

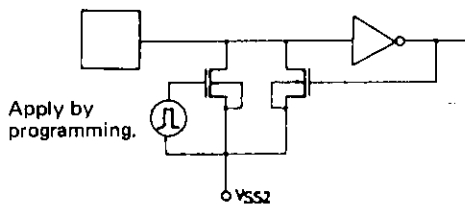


Fig. 4 Input configuration of S1-4, M1-4, K1-4, P1-4, INT

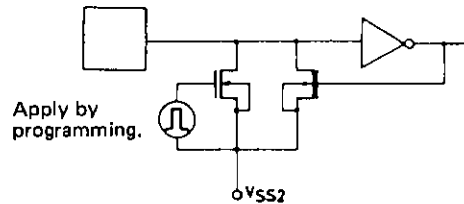


Fig. 10 Input configuration of S1-4, M1-4, K1-4, P1-4, INT

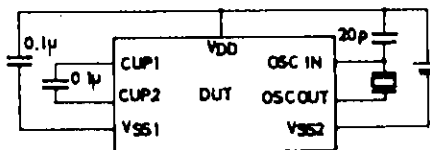


Fig. 5 Output voltage, current dissipation, oscillation hold voltage test circuit

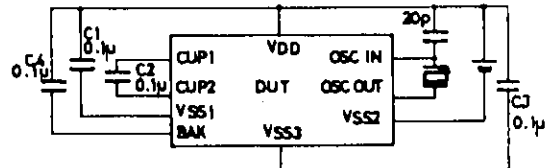


Fig. 11 Output voltage, current dissipation, oscillation hold voltage test circuit

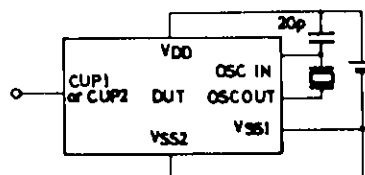


Fig. 6 Oscillation start voltage, oscillation start time, frequency stability test circuit

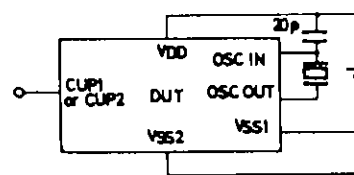


Fig. 12 Oscillation start voltage, oscillation start time, frequency stability test circuit

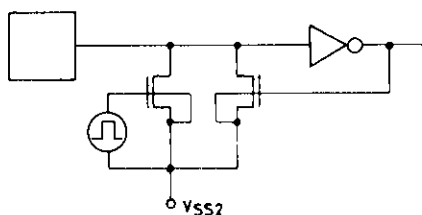


Fig. 13 Input configuration of S1-4, M1-4, K1-4, P1-4, INT

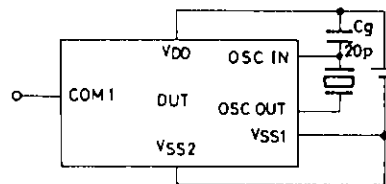


Fig. 15 Oscillation start voltage, oscillation start time, frequency stability test circuit

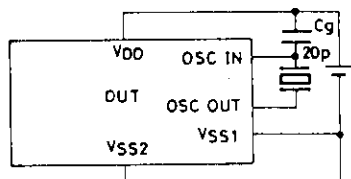


Fig. 14 Output voltage, current dissipation, oscillation hold voltage test circuit

Unit (capacitance: F)

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INSTRUCTION SET OF LC5805

Summary of LC5805 Instructions

Symbol	Description	Symbol	Description	Symbol	Description
AC	: Accumulator	E/S F	: Interrupt/switch select flag	CSTF	: Chrono start flag
ACn	: Accumulator	BCF	: Backup flag	CMF	: Chrono mode flag
CF	: Carry flag	SCFn	: Start condition flag n	CDF	: Chrono data decoder flag
DP	: Data Pointer	PDF	: Pull-down flag	TM	: Timer
DPF	: Data pointer flag	HQF	: Halt request flag	L	: LCD latch
SP	: Strobe pointer	HEFn	: Halt release enable flag	()	: Contents
PC	: Program counter	HRFn	: Halt release request flag	←	: Transfer direction, result
[P()]	: Contents of port ()	CC	: Chrono counter	∧	: AND
Rx	: Memory of address x	LSF	: Lap sample flag	∨	: OR
Rxn	: Memory-bit n of address x	LPF	: Lap mode flag	⊕	: Exclusive OR
IEFn	: Interrupt enable flag n				

Instruction group	Mnemonic	Instruction code								Function	Description	Status flag to be affected	
		D15	D14	D13	D12	D11	D10	D9	D8				
		D7	D6	D5	D4	D3	D2	D1	D0				
Accumulator manipulation instructions - memory manipulation instructions	CLA	Clear AC	0	1	0	1	1	0	1	0	AC ← 0	The AC contents are cleared.	
	RCF	Reset CF	1	1	1	0	1	1	0	0	CF ← 0	The CF contents are cleared.	CF
			0	0	0	0	0	0	0	1	≡ RF1 _L 1		
	SCF	Set CF	1	1	1	0	1	0	0	0	CF ← 1	The CF is set.	CF
			0	0	0	0	0	0	0	1	≡ SF1 _L 1		
	MRW Y, X	Move Rx to Working Register Ry	0	1	1	0	0	0	Y ₂	Y ₁	AC, Ry ← (Rx)	The memory (Rx) contents are loaded to the AC and working register (Ry).	
			Y ₀	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	MWR X, Y	Move Working Register Ry to Rx	0	1	1	0	0	1	Y ₂	Y ₁	AC, Rx ← (Ry)	The working register (Ry) contents are loaded to the AC and memory (Rx).	
			Y ₀	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	SR0 X	Shift Right Rx & MSB=0	0	1	1	0	1	0	0	0	Rxn, ACn ← (Rxn+1)	The memory (Rx) contents are shifted right and 0 is loaded to the MSB. The same contents are loaded to the AC.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Rx3, AC3 ← 0		
	SRI X	Shift Right Rx & MSB=1	0	1	1	0	1	0	0	1	Rxn, ACn ← (Rxn+1)	The memory (Rx) contents are shifted right and 1 is loaded to the MSB. The same contents are loaded to the AC.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Rx3, AC3 ← 1		
	SLO X	Shift Left Rx & LSB=0	0	1	1	0	1	0	1	0	Rxn, ACn ← (Rxn-1)	The memory (Rx) contents are shifted left and 0 is loaded to the LSB. The same contents are loaded to the AC.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Rx0, AC0 ← 0		
SLI X	Shift Left Rx & LSB=1	0	1	1	0	1	0	1	1	Rxn, ACn ← (Rxn-1)	The memory (Rx) contents are shifted left and 1 is loaded to the LSB. The same contents are loaded to the AC.		
		0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Rx0, AC0 ← 1			
RAR X	Rotate Right Rx	0	1	1	0	1	1	0	0	Rxn, ACn ← (Rxn+1)	The memory (Rx) contents are rotated right. The same contents are loaded to the AC.		
		0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Rx3, AC3 ← Rx0			
RAL X	Rotate Left Rx	0	1	1	0	1	1	1	0	Rxn, ACn ← (Rxn-1)	The memory (Rx) contents are rotated left. The same contents are loaded to the AC.		
		0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Rx0, AC0 ← Rx3			
MAF X	Move CF & WRF to AC & Rx	0	1	1	1	0	1	0	0	AC, Rx ← (CF)	The CF, contents are loaded to the AC and memory (Rx).		
		0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀				
MRA X	Move Rx to CF & WRF	0	0	0	0	1	1	1	1	CF ← (Rx)	The memory (Rx) contents are loaded to the CF. Bit has the same correspondence as for MAF X.		
		1	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀				
Operation instructions	ADC X	Add AC to Rx with CF	0	1	0	0	0	0	0	0	AC ← (Rx)+(AC)	The memory (Rx), AC, CF contents are binary-added and the result is loaded to the AC.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	+ (CF)		
	ADC* X	Add AC to Rx with CF	0	1	0	0	0	0	0	1	AC, Rx ← (Rx)+(AC)	The memory (Rx), AC, CF contents are binary-added and the result is loaded to the AC, Rx.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	+ (CF)		
	SBCX	Subtract AC from Rx with CF	0	1	0	0	0	0	1	0	AC, ← (Rx)+(AC)	The AC, CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	+ (CF)		
	SBC* X	Subtract AC from Rx with CF	0	1	0	0	0	0	1	1	AC ← (Rx)+(AC)	The AC, CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	+ (CF)		

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Instruction group	Mnemonic	Instruction code								Function	Description	Status flag to be affected	
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈				
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
Operation instructions	ADD X	Add AC to Rx	0	1	0	0	0	1	0	0	$AC \leftarrow (Rx) + (AC)$	The memory (Rx), AC contents are binary-added and the result is loaded to the AC.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	ADD* X	Add AC to Rx	0	1	0	0	0	1	0	1	$AC, Rx \leftarrow (Rx) + (AC)$	The memory (Rx), AC contents are binary-added and the result is loaded to the AC, Rx.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	SUB X	Subtract AC from Rx	0	1	0	0	0	1	1	0	$AC \leftarrow (Rx) + (\overline{AC}) + 1$	The AC contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	SUB* X	Subtract AC from Rx	0	1	0	0	0	1	1	1	$AC, Rx \leftarrow (Rx) + (\overline{AC}) + 1$	The AC contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	ADN X	Add AC to Rx	0	1	0	0	1	0	0	0	$AC \leftarrow (Rx) + (AC)$	The memory (Rx), AC contents are binary-added and the result is loaded to the AC.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	ADN* X	Add AC to Rx	0	1	0	0	1	0	0	1	$AC, Rx \leftarrow (Rx) + (AC)$	The memory (Rx), AC contents are binary-added and the result is loaded to the AC, Rx.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	AND X	And AC to Rx	0	1	0	0	1	0	1	0	$AC \leftarrow (Rx) \wedge (AC)$	The memory (Rx) contents and AC contents are ANDed and the result is loaded to the AC.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	AND* X	And AC to Rx	0	1	0	0	1	0	1	1	$AC, Rx \leftarrow (Rx) \wedge (AC)$	The memory (Rx) contents and AC contents are ANDed and the result is loaded to the AC, Rx.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	EOR X	Exclusive or AC to Rx	0	1	0	0	1	1	0	0	$AC \leftarrow (Rx) \vee (AC)$	The memory (Rx), AC contents are exclusive-ORed and the result is loaded to the AC.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
	EOR* X	Exclusive or AC to Rx	0	1	0	0	1	1	0	1	$AC, Rx \leftarrow (Rx) \vee (AC)$	The memory (Rx), AC contents are exclusive-ORed and the result is loaded to the AC, Rx.	
			0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀			
OR X	OR AC to Rx	0	1	0	0	1	1	1	0	$AC \leftarrow (Rx) \vee (AC)$	The memory (Rx), AC contents are ORed and the result is loaded to the AC.		
		0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀				
OR* X	OR AC to Rx	0	1	0	0	1	1	1	1	$AC, Rx \leftarrow (Rx) \vee (AC)$	The memory (Rx), AC contents are ORed and the result is loaded to the AC, Rx.		
		0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀				
ADCI X, Y	Add Immediate data to Rx with CF.	0	1	0	1	0	0	0	0	$AC \leftarrow (Rx) + Y + (CF)$	The memory (Rx) contents, Y, CF contents are binary-added and the result is loaded to the AC. The relation between absolute address of data memory (Rx) and X is as follows: Absolute address=XH+70H	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ADCI* X, Y	Add Immediate data to Rx with CF	0	1	0	1	0	0	0	1	$AC, Rx \leftarrow (Rx) + Y + (CF)$	The memory (Rx) contents, Y are binary-added and the result is loaded to the AC, Rx.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
SBCI X, Y	Subtract Immediate data & CF from Rx	0	1	0	1	0	0	1	0	$AC \leftarrow (Rx) + \overline{Y} + (CF)$	Immediate data Y and the CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
SBCI* X, Y	Subtract Immediate data & CF from Rx	0	1	0	1	0	0	1	1	$AC, Rx \leftarrow (Rx) + \overline{Y} + (CF)$	Immediate data Y and the CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ADDI X, Y	Add Immediate data to Rx	0	1	0	1	0	1	0	0	$AC \leftarrow (Rx) + Y$	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ADDI* X, Y	Add Immediate data to Rx	0	1	0	1	0	1	0	1	$AC, Rx \leftarrow (Rx) + Y$	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC, Rx.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
SUBI X, Y	Subtract Immediate data from Rx	0	1	0	1	0	1	1	0	$AC \leftarrow (Rx) + \overline{Y} + 1$	Immediate data Y is binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
SUBI* X, Y	Subtract Immediate data from Rx	0	1	0	1	0	1	1	1	$AC, Rx \leftarrow (Rx) + \overline{Y} + 1$	Immediate data Y is binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF	
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ADNI X, Y	Add Immediate data to Rx	0	1	0	1	1	0	0	0	$AC \leftarrow (Rx) + Y$	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC.		
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ADNI* X, Y	Add Immediate data to Rx	0	1	0	1	1	0	0	1	$AC, Rx \leftarrow (Rx) + Y$	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC, Rx.		
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ANDI X, Y	And Immediate data to Rx	0	1	0	1	1	0	1	0	$AC \leftarrow (Rx) \wedge Y$	The memory (Rx) contents and Y are ANDed and the result is loaded to the AC.		
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
ANDI* X, Y	And Immediate data to Rx	0	1	0	1	1	0	1	1	$AC, Rx \leftarrow (Rx) \wedge Y$	The memory (Rx) contents and Y are ANDed and the result is loaded to the AC, Rx.		
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
EORI X, Y	Exclusive Or Y to Rx	0	1	0	1	1	1	0	0	$AC \leftarrow (Rx) \vee Y$	The memory (Rx) contents and Y are exclusive-ORed and the result is loaded to the AC.		
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				
EORI* X, Y	Exclusive Or Y to Rx	0	1	0	1	1	1	0	1	$AC, Rx \leftarrow (Rx) \vee Y$	The memory (Rx) contents and Y are exclusive-ORed and the result is loaded to the AC, Rx.		
		Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀				

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Instruction group	Mnemonic		Instruction code										Function	Description	Status flag to be affected						
			D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆				D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
			Y ₃	Y ₂	Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀	Y ₃	Y ₂				Y ₁	Y ₀	X ₃	X ₂	X ₁	X ₀
Operation instructions	ORI X, Y	Or Immediate data to Rx	0	1	0	1	1	1	1	1	0	AC ← (Rx)VY	The memory (Rx) contents and Y are ORed and the result is loaded to the AC.								
	ORI* X, Y	Or Immediate data to Rx	0	1	0	1	1	1	1	1	1	AC, Rx ← (Rx)VY	The memory (Rx) contents and Y are ORed and the result is loaded to the AC, Rx.								
Data pointer and Flag manipulation instructions	MDPL X	Move DPL to Rx	0	1	1	1	0	1	1	1	1	AC, Rx ← (DPL)	The DPL contents are loaded to the memory (Rx).								
	MDPH X	Move DPH to Rx	0	1	1	1	0	1	1	0	AC, Rx ← (DPH)	The DPH contents are loaded to the AC and memory (Rx).									
	MRDH X	Move Rx to DPH	0	1	1	0	1	0	1	1	1	DPH, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and DPH. (If the DPF is set with X=00H to 6FH, the memory (Rx) contents are not loaded to the DPH.)								
	MRDL X	Move Rx to DPL	0	1	1	0	1	0	0	0	1	DPL, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and DPL. (If the DPF is set with X=00H to 6FH, the memory (Rx) contents are not loaded to the DPL.)								
	MRSB X	Move Strobe Pointer	0	1	1	0	1	0	1	0	0	SP, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and SP.								
		SF1 X	Set Flag 1 Group	1	1	1	0	1	0	X ₉	X ₈		The flag corresponding to the data specified with X ₉ to X ₀ is set.	CF DPF							
			X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Data of X ₉ to X ₀	X ₀ =1	X ₁ =1		X ₂ =1						
											Instruction to be executed	SCH	SCEX		SCT1						
											Data of X ₉ to X ₀	X ₄ =1	X ₅ =1		X ₆ =1	X ₇ =1					
											Instruction to be executed	SFPD	COMD1	COMD2	SDPF						
			X ₉ =1, X ₈ =1	Used for test.																	
	RF1 X	Reset Flag 1 Group	1	1	1	0	1	1	X ₉	X ₈		Each flag is reset corresponding to SF1.	CF DPF								
			X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀											
	SF2 X	Set Flag 2 Group	1	1	1	1	0	0	X ₉	X ₈		The flag corresponding to the data specified with X ₉ to X ₀ is set.	BCF CMF CDF PDF HQP								
			X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Data of X ₉ to X ₀	X ₀ =1		X ₁ =1	X ₂ =1	X ₃ =1	X ₄ =1				
											Instruction to be executed	SCHF 1		SCHF 2	SBAK	LON	LON SLOT				
											Data of X ₉ to X ₀	X ₅ =1		X ₆ =1	X ₇ =1	X ₈ =1	X ₉ =1				
											Instruction to be executed	SPDF 1	SPDF 2	SPDF 4	SPDF 8	SCT 2					
	RF2 X	Reset Flag 2 Group	1	1	1	1	0	1	X ₉	X ₈		Each flag is reset corresponding to SF2.									
			X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀											
	SDPF	Set DPF	1	1	1	0	1	0	0	0	DPF ← 1	The DPF is set. The memory address is specified with the DP. If the instruction code address is 70H to 7FH, the instruction code address prevails.	DPF								
			1	0	0	0	0	0	0	0	≡SF1 80H										
	RDPF	Reset DPF	1	1	1	0	1	1	0	0	DPF ← 0	The DPF is reset.	DPF								
			1	0	0	0	0	0	0	0	≡RF1 80H										
Load/store instructions	STA X	Store AC to Rx	0	1	1	1	0	1	1	1	Rx ← (AC)	The AC contents are loaded to the memory (Rx).									
			1	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀											
	LDS X, D	Load AC with Data & Store AC to Rx	0	1	1	1	1	D ₃	D ₂	D ₁	AC, Rx ← D	Immediate data D is loaded to the AC and memory (Rx).									
			D ₀	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀											
	LDA X	Load AC from Rx	0	1	1	0	1	0	0	0	AC ← (Rx)	The memory (Rx) contents are loaded to the AC.									
			1	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀											
CPU control instructions	HALT	HALT	1	1	1	1	1	1	1	1		The operation of CPU is stopped. The following 3 conditions cause the halt mode to be released. 1) An interrupt is accepted. 2) The signal change specified by the SSW Instruction is applied to port S, K. 3) The halt release condition specified by the SIC instruction is met. When an interrupt is accepted to release the halt mode, the halt mode returns by executing the RTS instruction after completion of interrupt service.									
			0	0	0	0	0	0	0	0											

Instruction group	Mnemonic	Instruction code								Function	Description	Status flag to be affected									
		D15	D14	D13	D12	D11	D10	D9	D8												
		D7	D6	D5	D4	D3	D2	D1	D0												
CPU control instructions	SSW X	Set Switch State	1	1	1	0	0	0	0	0	0	0	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	The data specified by X causes the halt mode to be released. The signal change at port S, K is specified.		
													X ₀ ~X ₅	X ₀ =1	X ₁ =1	X ₂ =1	X ₃ =1				
													Signal change at input port	S ₁	S ₂	S ₃	S ₄				
													X ₀ ~X ₅	X ₄ =1		X ₅ =1					
													Signal change at input port		Fall signal at one of K1 to K4		Rise signal at one of K1 to K4				
	SIC X	Set/Reset Interrupt Enable Flag	1	1	1	1	1	0	1	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	X ₀ ~X ₈	Operation	IEF ₀ ~3 HEF ₀ ~3 E/SF
																			X ₀ =1	The IEF ₃ is set so that Interrupt 3 (overflow from the divider) is accepted.	The IEF ₀ to 3 are reset automatically when an interrupt is accepted.
																			X ₁ =1	The IEF ₂ is set so that Interrupt 2 (overflow from the CC) is accepted.	
																			X ₂ =1	The IEF ₁ is set so that interrupt 1 (underflow from the TM) is accepted.	
																			X ₃ =1	The IEF ₀ is set so that interrupt 0 (mode shown below) is accepted. 1) Signal change at port S specified by the SSW. 2) Signal change at port K specified by the SSW. 3) Rise signal change at external interrupt pin INT. Refer to the operation for X ₈ =1 also.	
																		X ₄ =1	The HEF ₃ is set so that overflow from the divider causes the halt mode to be released.		
																		X ₅ =1	The HEF ₂ is set so that overflow from the CC causes the halt mode to be released.		
																		X ₆ =1	The HEF ₁ is set so that underflow from the TM causes the halt mode to be released.		
																		X ₇ =1	The HEF ₀ is set so that the halt mode is released when the rise signal change is applied to INT. In this case X ₈ must be 0.		
																		X ₈ =1	For X ₃ =1, port S/K is selected at X ₈ =1 (E/SF set); INT is selected at X ₈ =0 (E/SF reset). In the case of X ₇ =1, X ₈ must be 1.		
	SIC* X		1	1	1	1	1	1	0	0	0	0	0	X ₃	X ₂	X ₁	X ₀		Only X ₀ to X ₃ of the SIC instruction are significant. X ₄ to X ₈ remain unaffected.		
	MSB X	Move SCF & BCF to AC & Rx	0	1	1	1	0	1	0	1	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	AC, Rx ~ SCF ₁ ~3 BCF	The SCF ₁ to 3 and BCF contents are loaded to the AC and memory (Rx).		
																			The AC contents and the meaning of bit after execution of this instruction are as follows: Bit 0 ---- BCF: "1" at the backup mode Bit 1 ---- SCF ₁ : "1" when the halt mode is released by the signal change at port K Bit 2 ---- SCF ₂ : "1" when the halt mode is released by the SCF ₄ to 7 Bit 3 ---- SCF ₃ : "1" when the halt mode is released by the signal change at port S		
	MSC X	Move SCF to AC & Rx	0	1	1	1	0	1	1	0	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	AC, Rx ~ SCF ₄ ~7	The SCF ₄ to 7 contents are loaded to the AC and memory (Rx).		
																			The AC contents and the meaning of bit after execution of this instruction are as follows: Case where the corresponding bit is "1". Bit 0 ---- SCF ₄ : The halt mode is released by overflow from the divider. Bit 1 ---- SCF ₅ : The halt mode is released by overflow from the CC. Bit 2 ---- SCF ₆ : The halt mode is released by underflow from the TM. Bit 3 ---- SCF ₇ : The halt mode is released by the signal change at INT.		
																			The SIC instruction is used to specify that the INT/port S, K, TM, CC, divider should be specified for interrupt service, halt release, or no operation.		

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Instruction group	Mnemonic	Instruction code										Function	Description	Status flag to be affected						
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6				D5	D4	D3	D2	D1	D0
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6				D5	D4	D3	D2	D1	D0
CPU control instructions	NOP	No Operation	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	LON	Light ON	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Set Light & HQF ≡ SF2 18H	The Light Out pin is made active and the halt request flag (HRQ) is set to cause the halt mode to be entered.	HQF
	LOFF	Light OFF	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Reset Light & HQF ≡ RF2 18H	The Light Out pin is made nonactive and the HRQ is reset.	HQF
	SBAK	Set Back-up Mode	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	≡ SF2 4	V _{SS2} is applied to the logic unit at the Li battery power supply mode. The inverter size of the oscillator is approximately doubled at the Ag, Li battery, EXTV power supply mode.	BCF
	RBAK	Reset Back-up Mode	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	≡ RF2 4	The backup mode is released.	BCF
Chrono instructions	MCD X	Move Chrono Counter Data to AC & Rx	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	AC, Rx ← (CC)	The CC contents are loaded to the AC and memory (Rx).	
	MCF X	Move Chrono Flag to AC & Rx	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	AC, Rx ← CMF, CSTF	The contents of each flag are loaded to the AC and memory (Rx).	
																		The AC contents after execution of this instruction are as follows: Bit 0 ---- LSF: "1" at the CC overflow mode at LPF=1. Bit 1 ---- LPF: "1" at the lap mode. Bit 2 ---- CSTF: "1" at the chrono start mode. Bit 3 ---- CMF: "1" at the chrono mode.		
	CCC	Clear CC	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	CC ← 0 LSF ← 0		LSF
	RLP	Reset LPF	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	LPF ← 0 PLC 040H	The lap mode is released.	LPF
	CSP	Chrono Stop	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	CSTF ← 0 PLC 080H	1/100 second pulse is inhibited from being applied to the CC.	CSTF
	CST	Chrono Start	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	CSTF + 1 ≡ PLC 100H	1/100 second pulse is applied to the CC.	
	SCEX	Set CC External Input Mode	1	1	1	0	1	0	0	0	0	0	0	1	0	0	0	≡ SF1 2	The CC input connected to K4 pin, instead of 1/100 pulse. At the initial mode the CC input is connected to 1/100 pulse.	
	RCEX	Reset CC External Input Mode	1	1	1	0	1	1	0	0	0	0	0	1	0	0	0	≡ RF1 2	The CC input is connected to 1/100 pulse.	
	SCHF X	Set Chrono Flag	1	1	1	1	0	0	0	0	0	0	X ₁	X ₀	0	0	0	CMF ← 1 (at X ₀ =1) CDF ← 1 (at X ₁ =1) ≡ One of SF2	The CMF and CDF are set. When the CMF is set, the chrono start/stop, lap/lap release mode can be controlled by the signal at port S or the dedicated instruction. When the CDF is set, the date decoder is connected to the CC.	CMF CDF At the initial mode the CMF and CDF are reset.
RCHF X	Reset Chrono Flag	1	1	1	1	0	1	0	0	0	0	X ₁	X ₀	0	0	0	CMF ← 0 (at X ₀ =1) CDF ← 0 (at X ₁ =1) ≡ One of RF2	The CMF and CDF are reset.	CMF CDF	

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Instruction group	Mnemonic	Instruction code								Function	Description	Status flag to be affected					
		D15	D14	D13	D12	D11	D10	D9	D8								
		D7	D6	D5	D4	D3	D2	D1	D0								
Input/output instructions	IPP X	Input Port P to AC & Rx	0	1	1	1	0	0	0	1	Rx, AC ← [P(P)]	The input data at input/output port P is loaded to the AC and memory (Rx).					
	IPS X	Input Port S to AC & Rx	0	1	1	1	0	0	0	0	Rx, AC ← [P(S)]	The input data at input port S is loaded to the AC and memory (Rx).					
	IPM X	Input Port M to AC & Rx	0	1	1	1	0	0	0	0	Rx, AC ← [P(M)]	The input data at input/output port M is loaded to the AC and memory (Rx).					
	IPK X	Input Port K to AC & Rx	0	1	1	1	0	0	0	1	Rx, AC ← [P(K)]	The input data at input port K is loaded to the AC and memory (Rx).					
	OPP X	Output Rx to Port P	0	0	0	0	0	0	0	0	[P(P)] ← Rx	The memory (Rx) contents are loaded to input/output port P.					
	OPM X	Output Rx to Port M	0	0	0	0	1	1	1	1	[P(M)] ← Rx	The memory (Rx) contents are loaded to input/output port M.					
	SCT1	Set CNT OUT 1	1	1	1	0	1	0	0	0	≡SF1 4	The CNT1 OUT pin is made active (ON).					
	RCT1	Reset CNT OUT 1	1	1	1	0	1	1	0	0	≡RF1 4	The CNT1 OUT pin is made nonactive (OFF).					
	SCT2	Set CNT OUT 2	1	1	1	1	0	0	1	0	≡SF2 200H	The CNT2 OUT pin is made active (ON).					
	RCT2	Reset CNT OUT 2	1	1	1	1	0	1	1	0	≡RF2 200H	The CNT2 OUT pin is made nonactive (OFF).					
	SLGT	Set Light	1	1	1	1	0	0	0	0	≡SF2 10H	The LIGHT OUT pin is made active (ON). (Refer to the LON instruction.)					
	RLGT	Reset Light	1	1	1	1	0	1	0	0	≡RF2 10H	The LIGHT OUT pin is made nonactive (OFF). (Refer to the LOFF instruction.)					
	SAS X	Set Alarm Sound	1	1	1	1	1	0	0	X ₈	The waveform specified by X ₈ to X ₀ is delivered at the Alarm Out pin.						
			X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	X ₇ ~X ₀	X ₀ =1	X ₁ =1	X ₂ =1	X ₃ =1	X ₄ =1	
											Enable Signal	32Hz	16Hz	8Hz	4Hz	2Hz	
											X ₇ ~X ₀	X ₅ =1	X ₆ X ₇ =1	X ₆ X ₇ =1	X ₆ X ₇ =1	X ₆ X ₇ =1	
											Enable Signal	1Hz	1kHz	2kHz	4kHz	DC	
											At X ₈ =1 the signal specified by X ₆ , X ₇ is enabled.						
RAS	Reset Alarm Sound	1	1	1	1	1	0	0	0	≡SAS 0	The Alarm Out pin is made nonactive (OFF).						
COMD X	Change to Output Mode	1	1	1	0	1	0	0	0	≡One of SF1	Input/output port M or P is changed to the output mode. At the initial mode the port is in the input mode. X=1, X=2, X=3 correspond to port M, port P, port M, P respectively.	COMD					
CIMD X	Change to Input Mode	1	1	1	0	1	1	0	0	≡One of RF1	Input/output port M or P is changed to input port.	COMD					
SPDF X	Set PDF	1	1	1	1	0	0	0	X ₃	PDF ← 1	The pull-down MOS transistor at the corresponding input port is turned ON.	PDF					
		X ₂	X ₁	X ₀	0	0	0	0	0	≡One of SF2							
										X ₀ ~X ₃	X ₀ =1	X ₁ =1	X ₂ =1	X ₃ =1			
										Corresponding port	S	M	K, INT	P			
RPDF X	Reset PDF	1	1	1	1	0	1	0	X ₃	PDF ← 0		PDF					
		X ₂	X ₁	X ₀	0	0	0	0	0	≡One of RF2							

Instruction group	Mnemonic	Instruction code										Function	Description	Status flag to be affected						
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6				D5	D4	D3	D2	D1	D0
		Y0	X6	X5	X4	X3	X2	X1	X0	Y0	X6				X5	X4	X3	X2	X1	X0
Input/output instructions	WRT Y, X Write Rx to LCD Latch (Ly)	0	0	0	0	Y4	Y3	Y2	Y1	Y0	X6	X5	X4	X3	X2	X1	X0	Y=00H, 01H, 1EH, 1FH causes a different instruction to occur. For input/output of the data decoder, refer to page 60.	The memory (Rx) contents are loaded to the LCD latch (Ly) through the data decoder. For DPF=1, X=00H to 6FH, the address of Rx is specified by DP; the address of Ly is specified by SP.	
	WRB Y, X Write Rx to LCD Latch (Ly)	0	0	0	1	Y4	Y3	Y2	Y1	Y0	X6	X5	X4	X3	X2	X1	X0	Same as above.	Same as WRT X, Y. Output data "a" to "h" corresponding to input data of the data 0 decoder are all 0.	
	WRC Y, X Write Rx to LCD Latch (Ly)	0	0	1	0	Y4	Y3	Y2	Y1	Y0	X6	X5	X4	X3	X2	X1	X0	For input/output of the data decoder, refer to page 60.	Same as WRT X, Y except input/output of the data decoder.	
	WRP Y, X Write Rx to LCD Latch (Ly)	0	0	1	1	Y4	Y3	Y2	Y1	Y0	X6	X5	X4	X3	X2	X1	X0	For input/output of the data decoder, refer to page 60.	Same as WRT X, Y except input/output of the data decoder.	
Jump instructions	JMP X Jump	1	1	0	0	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0	The data specified by X10 to X0 is loaded to the PC to produce an unconditional jump.	
	BAB0 X Branch on AC bit 0 High	1	0	0	0	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if AC0='1,	If bit 0 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB1 X Branch on AC bit 1 High	1	0	0	0	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if AC1='1,	If bit 1 of the AC is "1", a jump occurs. If "0" the PC is incremented +1.	
	BAB2 X Branch on AC bit 2 High	1	0	0	1	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if AC2='1,	If bit 2 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB3 X Branch on AC bit 3 High	1	0	0	1	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if AC3='1,	If bit 3 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BANZ X Branch on AC not Zero	1	0	1	0	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if AC≠0	If the AC is not "0", a jump occurs. If "0", the PC is incremented +1.	
	BAZ X Branch on AC Zero	1	0	1	1	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if AC=0	If the AC is "0", a jump occurs. If not "0", the PC is incremented +1.	
	BCNH X Branch on CF not High	1	0	1	0	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if CF≠1	If the CF is "0", a jump occurs. If "1", the PC is incremented +1.	
	BCH X Branch on CF High	1	0	1	1	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PC10~PC0 - X10~X0 if CF=1	If the CF is "1", a jump occurs. If "0", the PC is incremented +1.	
	Subroutine instructions	CALL X Call Subroutine	1	1	0	0	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	STACK - (PC)+1 PC10~PC0 - X10~X0	A subroutine is called.
RTS Return from Subroutine		1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	PC - (STACK)	A return from a subroutine occurs.	
POP POP the stack		1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0		The stack pointer is popped -1.	

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Instruction group	Mnemonic	Instruction code										Function	Description	Status flag to be affected						
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6				D5	D4	D3	D2	D1	D0
		X7	X6	X5	X4	X3	X2	X1	X0	X7	X6				X5	X4	X3	X2	X1	X0
Other instructions	STM X	Set Timer	1	1	1	0	0	1	X ₉	X ₈	For the relation between X data and time setting, refer to page .		The date specified by X ₉ to X ₀ is loaded to the TM to start the TM.							
	RTM	Reset Timer	1	1	1	1	1	1	0	0	≡PLC 4	The TM stops operating. When using the TM to release the halt mode, this instruction is executed to stop the TM and to reset the halt release request signal. When the timer interrupt is accepted, the TM stops operating automatically.								
	SFPD	Set High Frequency Pre-Divider Over Flow Mode	1	1	1	0	1	0	0	0	≡SF1 10H	Overflow signal from the divider is changed from 2Hz to 4Hz. When watch count is based on this 2Hz/4Hz signal, this instruction must be executed so that no error occurs in watch operation.								
	RFPD	Reset High Frequency Pre-Divider Over Flow Mode	1	1	1	0	1	1	0	0	≡RF1 10H	Overflow signal from the divider is changed from 4Hz to 2Hz. At the initial mode 2Hz is set.								
	PLC X	Pulse Control	1	1	1	1	1	1	0	X ₈		The pulse corresponding to the data specified by X ₀ to X ₈ is generated.	HRF ₀₋₃							
		X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	X ₀ ~X ₈	Mode after execution of instruction									
										X ₀ =1	Halt release request flag HRF3 caused by overflow from the divider is reset.									
										X ₁ =1	Halt release request flag HRF2 caused by overflow from the CC is reset.									
										X ₂ =1	Halt release request flag HRF1 caused by overflow from the TM is reset.									
										X ₃ =1	Halt release request flag HRF0 caused by the signal at input port S, K or INT is reset.									
										X ₄ =1	The last 5 bits of the divider (15 bits) are reset. When executing this instruction, X ₀ must be set to "1".									
										X ₅ =1	The CC and LSF are cleared. When executing this instruction, X ₁ must be set to "1". Same as the CCC instruction.									
										X ₆ =1	Same as the RLP instruction.									
										X ₇ =1	Same as the CSP instruction.									
										X ₈ =1	Same as the CST instruction.									

Note) 4Hz of the SFPD, RFPD instructions is for the chip (LC5805F/5899F) whose cycle time is 244μs.
8Hz is for the chip (LC5805G/5899G) whose cycle time is 122μs.

Input/Output of data decoder at WRT instruction execution mode

Input data	Output data							
	a	b	c	d	e	f	g	h
0	1	1	1	1	1	1	0	0
1	0	1	1	0	0	0	0	0
2	1	1	0	1	1	0	1	0
3	1	1	1	1	0	0	1	0
4	0	1	1	0	0	1	1	0
5	1	0	1	1	0	1	1	0
6	1	0	1	1	1	1	1	0
7	1	1	1	0	0	0	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	0	1	1	0
A/B	1	0	0	1	1	1	1	0
C/D	0	0	0	0	0	0	1	0
E/F	0	0	0	0	0	0	0	0

Input/output of data decoder at WRC instruction execution mode

Input data	Output data							
	a	b	c	d	e	f	g	h
0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0
2	0	0	0	1	0	0	0	0
3	0	0	1	0	0	0	0	0
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	1	0
6	0	0	0	0	1	0	0	0
7	1	0	0	0	0	0	0	0
8 ~ F	0	0	0	0	0	0	0	0

Input/output of data decoder WRP instruction execution mode

Input data	(Rx0)	(Rx1)	(Rx2)	(Rx3)	(AC0)	(AC1)	(AC2)	(AC3)
Output data	a	b	c	d	e	f	g	h

Data specified by X9 to X0 and set time at STM instruction execution mode

Set value										Set time (μ s)
X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	
0	0	0	0	0	0	0	0	0	0	244
0	0	0	0	0	0	0	0	0	1	488
0	0	0	0	0	0	0	0	1	0	732
}		}				}				}
1	1	1	1	1	1	1	1	0	1	249512
1	1	1	1	1	1	1	1	1	0	249756
1	1	1	1	1	1	1	1	1	1	250000

Note) The set time is for the chip (LC5805F/5899F) whose cycle time is 244 μ s.
 For the chip (LC5805G/5899G) whose cycle time is 122 μ s, the set time is halved.