LSI/CSI

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ISO 9001 UL REGISTERED FIRM A3800

LS7566R

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24-BIT x 4-AXES QUADRATURE COUNTER

FEATURES:

- Read/write registers for count and I/O modes.
  Count modes include: non-quadrature (Up/Down), Quadrature (x1, x2, x4), Free-run, Non-recycle, Modulo-n and Range limit
- Separate mode-control registers for each axis
- Interrupt output and interrupt mask register
- 40 MHz count frequency, 5V
  20 MHz count frequency, 3V
- Sets of 24-bit counters, preset registers, comparators and output latches and 8-bit status registers for each axis
- Digital filtering of the input quadrature clocks for noise immumity.
- 3-state Octal I/O bus
- 3V to 5.5V operating voltage range
- LS7566R-TS (TSSOP) - **See Figure 1** -

GENERAL DESCRIPTION:

The LS7566R consists of four identical modules of 24-bit programmable counters with direct interface to incremental encoders. The modules can be configured to operate as quadrature-clock counters or non-quadrature up/down counters. In both quadrature and non-quadrature modes, the modules can be further configured into free-running, non-recycle, modulo-n and range-limit count modes. The mode configuration is made through two 8-bit read/write addressable control registers, MDR0 and MDR1. Data can be ported to a 24-bit preset register PR, organized in directly addressable (write-only) byte0 [PR0], byte1 [PR1] and byte2 [PR2] segments. PR can be transferred to the 24-bit counter CNTR, either by instruction to MDR1 or by hardware input control. A 24-bit digital comparator perpetually checks for the equality of the CNTR and the PR and can be used to set an output flag when the equality occurs. For reading the CNTR, its instantaneous value can be transferred to a 24-bit output latch OL, either by instruction to MDR1 or by hardware input control. The OL in turn can be read in directly addressable (read-only) byte0 [OL0], byte1 [OL1] and byte2 [OL2] segments. An addressable (read-only) Octal status register STR, stores the count related status information such as CNTR overflow, underflow, count direction, etc. Data communication for read/write is performed through an Octal 3-state parallel I/O bus.

REGISTER DESCRIPTION:

Following is a list of the hardware registers. There are four sets of registers, with name prefixes x0 through x3 to refer to axes x0 through x3.

PIN ASSIGNMENT - Top View

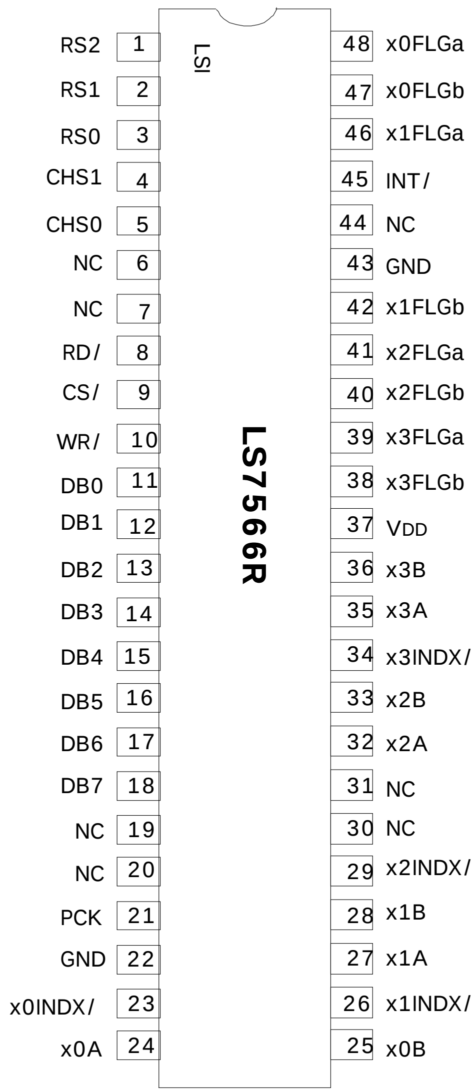


FIGURE 1

PR (x0PR, x1PR, x2PR, x3PR)

The PR is a 24-bit data register directly addressable for write in individual segments of byte0 [PR0], byte1 [PR1] and byte2 [PR2]. The PR serves as the input portal for the counter (CNTR), since the CNTR is not directly addressable for either read or write. In order to preset the CNTR to any desired value the data is first written into the PR and then transferred into the CNTR.

B23---B0

	PR2	PR1	PR0
PR:	B7----------------B0	B7-------------B0	B7--------------B0

In **mod-n** and **range-limit** count modes the PR serves as the repository for the division factor n and the count range-limit, respectively. The PR can also be used to hold the compare data for the CNTR wherein the equality PR = CNTR sets an output flag.

CNTR (x0CNTR, x1CNTR, x2CNTR, x3CNTR):

The CNTR is a 24-bit up/down counter which counts the up/down pulses resulting from tthe quadrature clocks applied at A and B inputs or alternatively, in non-quadrature mode, pulses applied at the A input. The CNTR is not directly accessible for read or write; instead it can be preloaded with data from the PR or it can port its own data out to the OL which in turn can be accessed by read operation. In both quadrature and non-quadrature modes, the CNTR can be further configured into either free-running or single-cycle or mod-n or range-limit mode.

OL (x0OL, x1OL, x2OL, x3OL):

The OL is a 24-bit register directly addressable for read in individual segments of byte0 [OL1], byte1 [OL1] and byte2 [OL2]. OL serves as the output portal for the CNTR. Snapshot of the CNTR data can be loaded in the OL without interfering with the counting process, which then can be accessed by read.

B23--B0

	OL2	OL1	OL0
OL:	B7----------------B0	B7-------------B0	B7--------------B0

STR (x0STR, x1STR, x2STR, x3STR):

The STR is an 8-bit status register indicating count related status.

	CY	BW	CMP	IDX	CEN	0	U/D	S
STR:	B7	B6	B5	B4	B3	B2	B1	B0

An individual STR bit is set to 1 when the bit related event has taken place. The STR is cleared to 0 at power-up. The STR can also be cleared through the control register CMR with the exception of bit1 (U/D) and bit3 (CEN). These two STR bits always indicate the instantaneous status of the count_direction and count_enable assertion/de-assertion. The STR bits are described below:

B7 (CY): Carry; set by CNTR overflow
B6 (BW): Borrow; set by CNTR underflow
B5 (CMP): Set when CNTR = PR
B4 (IDX): Set when INDX input is at active level
B3 (CEN): Set when counting is enabled, reset when counting is disabled
B2 (0): Always 0
B1 (U/D): Set when counting up, reset when counting down
B0 (S): Sign of count value; set when negative, reset when positive

IMR:

The IMR is a trans-axis global register used for masking out the interrupt function of individual axes. It is a 4-bit read/write register with the following bit assignments.

IMR:	B3	B2	B1	B0

B0 = 0: disable axis 0 interrupt
= 1: enable axis 0 interrupt
B1 = 0: disable axis 1 interrupt
= 1: enable axis 1 interrupt
B2 = 0: disable axis 2 interrupt
= 1: enable axis 2 interrupt
B3 = 0: disable axis 3 interrupt
= 1: enable axis 3 interrupt

A write to IMR places the lower nibble of the databus into the IMR with identical bit map. A read of IMR produces a joint read of IMR and ISR (interrupt status register), with IMR occupying the lower nibble and ISR occupying the upper nibble of the databus.

ISR:

The ISR is a trans-axis global register used to hold the interrupt assertion status of all the axes. It is a 4-bit read-only register with the following bit assignment.

ISR:

B3	B2	B1	B0

B0 = 0: axis_0 interrupt cleared
= 1: axis_0 interrupt asserted
B1 = 0: axis_1 interrupt cleared
= 1: axis_1 interrupt asserted
B2 = 0: axis_2 interrupt cleared
= 1: axis_2 interrupt asserted
B3 = 0: axis_3 interrupt cleared
= 1: axis_3 interrupt asserted

An ISR bit gets set when the FLGa output of the associated axis switches low. For this reason, in order for the interrupt to be enabled for any axis, its associated FLGa output must be enabled. In addition, the associated IMR bit must also be set for the interrupt to be enabled.
An individual ISR bit can be cleared through its axis relevant CMR register. The ISR is cleared upon power-up.
A read of ISR produces a joint read of ISR and IMR (interrupt mask register) with ISR occupying the upper nibble and IMR occupying the lower nibble of the databus.

CMR (x0CMR, x1CMR, x2CMR, x3CMR):
The CMR is a write only register, which when written into, generates transient signals to perform load and reset operations as described below:

CMR:

B7	B6	B5	B4	B3	B2	B1	B0

B0 = 0: Nop
= 1: Reset CNTR and sign to 0. (Should not be combinedwith load_CNTR operation).
B1 = 0: Nop
= 1: Load CNTR from PR. Affects all 24 bits. (Should not be combined with reset_CNTR operation)
B2 = 0: Nop
= 1: Load OL from CNTR. Affects all 24 bits.
B3 = 0: Nop
= 1: Reset STR. Affects status bits corresponding to carry, borrow, compare and index. Status bits corresponding to count_enable, count direction and sign are not affected.
B4 = 0: Nop.
1: Master reset. Resets MDR0, MDR1, STR, CNTR, PR, OL, ISR and IMR
B5 = 0: Nop
1: Set sign bit
B6 = 0: Nop
1: Reset sign bit
B7 = 0: Nop.
1: Reset ISR bit for the selected axis

MDR0 (x0MDR0, x1MDR0, x2MD0, x3MDR0): The MDR0 is an 8-bit read/write register which configures the counting modes and the index input functionality. Upon power-up, the MDR0 is cleared to zero.

MDR0:	B7	B6	B5	B4	B3	B2	B1	B0

B1B0 = 00: Non-quadrature count mode (A = clock, B = direction).
= 01: x1 quadrature count mode (one count per quadrature cycle).
= 10: x2 quadrature count mode (two counts per quadrature cycle).
= 11: x4 quadrature count mode (four counts per quadrature cycle).
B3B2 = 00: **Free-running** count mode.
= 01: **Single-cycle** count mode (CNTR disabled with **carry** and **borrow**, re-enabled with **reset** or **load**)
= 10: **Range-limit** count mode (up and down count ranges are limited between PR and zero, respectively. Counting freezes at these limits but resumes when the direction is reversed)
= 11: **Modulo-n** count mode (input count clock frequency is divided by a factor of [n+1], where n = PR. In up direction, the CNTR is **cleared** to 0 at CNTR = PR and up count continues. In down direction, the CNTR is **preset** to the value of PR at CNTR = 0 and down count continues. A mod-n rollover marker pulse is generated at each limit at the FLGa output).
B5B4 = 00: Disable INDX/ input.
= 01: Configure INDX/ input as the load CNTR input (transfers PR to CNTR).
= 10: Configure INDX/ as the reset _CNTR input (clears CNTR to 0).
= 11: Configure INDX/ as the load_OL input (transfers CNTR to OL).
B6 = 0: Asynchronous INDX/ input
= 1: Synchronous INDX/ input (overridden in non-Quadrature Mode)
B7 = 0: Input filter clock (PCK) division factor = 1. Filter clock frequency = f_{PCK}.
= 1: Input filter clock division factor = 2. Filter clock frequency = $f_{PCK}/2$.

MDR1 (x0MDR1, x1MDR1, x2MD1, x3MDR1): The MDR1 is an 8-bit read/write register which configures the FLGa and FLGb output functionality. In addition, the MDR1 can be used to enable/disable counting.Upon power-up, the MDR1 is cleared to zero:

MDR1:	B7	B6	B5	B4	B3	B2	B1	B0

B0 = 1: Enable Carry on FLGa (flags CNTR overflow; latched or unlatched logic low on carry).
B1 = 1: Enable Borrow on FLGa (flags CNTR underflow, latched or unlatched logic low on borrow).
B2 = 1: Enable Compare on FLGa (In free-running count mode a latched or unlatched logic low is generated in both up and down count directions at CNTR = PR. In contrast, in range-limit and mod-n count modes a latched or unlatched low is generated at CNTR = PR in the up-count direction only.
B3 = 1: Enable index on FLGa (flags index, latched or unlatched logic low when INDX/ input is at active level)
B5B4 = 00: FLGb disabled (fixed high)
= 01: FLGb = **Sign**, high for negative signifying CNTR underflow, low for positive.
= 10: FLGb = **Up/Down** count direction, high in count-up, low in count-down.
B6 = 0: Enable counting.
= 1: Disable counting.
B7 = 0: FLGa is latched.
= 1: FLGa is non-latched and instantaneous.

NOTE: Carry, Borrow, Compare and Index can all be simultaneously enabled on FLGa.

I/O PINS: The following is a description of the input/out pins.

RSO(Pin 3)**, RS1** (Pin 2)**, RS2** (Pin1).
Inputs. These three inputs select the hardware registers for read/write access according to Table 1.

TABLE 1

CS/	RS2	RS1	RS0	RD/	WR/	SELECTED REGISTER	OPERATION
1	x	x	x	x	x	none	none
x	x	x	x	0	0	none	none
x	x	x	x	1	1	none	none
0	0	0	0	0	1	[ISR:IMR]	READ (NOTE 2)
0	0	0	1	0	1	MDR0	READ
0	0	1	0	0	1	MDR1	READ
0	0	1	1	0	1	STR	READ
0	1	0	0	0	1	OL0	READ
0	1	0	1	0	1	OL1	READ
0	1	1	0	0	1	OL2	READ
0	1	1	1	0	1	none	none
0	0	0	0	1	0	IMR	WRITE
0	0	0	1	1	0	MDR0	WRITE
0	0	1	0	1	0	MDR1	WRITE
0	0	1	1	1	0	none	none
0	1	0	0	1	0	PR0	WRITE
0	1	0	1	1	0	PR1	WRITE
0	1	1	0	1	0	PR2	WRITE
0	1	1	1	1	0	CMR	WRITE

Note 1. x indicates don't care case.
Note 2. DB0 through DB3 contain IMR B0 through B3; DB4 through DB7 contain ISR B0 through B3.

CHS0 (Pin 5), **CHS1** (Pin 4) .
Inputs. These two inputs select one of four axes for read/write access according to the following table. The registers within the axis are selected according to Table 1.

TABLE 2

CHS1	CHS0	AXIS
0	0	x0
0	1	x1
1	0	x2
1	1	x3

RD/ (Pin 8) Input. A low on RD/ input accesses an addressed register for read and places the data on the octal databus, DB<7:0>. The register selection is made according to Table 1.

CS/ (Pin 9) Input. A low on the CS/ input enables the chip for read or write operation. When the CS/ input is high, read and write operations are disabled and the databus, DB<7:0> is placed in a high impedance state.

WR/ (Pin 10) Input. A low pulse on the WR/ input writes the data on the databus, DB<7:0> into the addressed register according to Table 1. The write operation is completed at the trailing edge of the WR/ pulse.

DB<7:0> (Pin 18 thru Pin 11) Input/Output.
The octal databus DB<7:0> is the input/output portal for write and read data transfers between LS7566R and the outside world. During a read operation, when both CS/ and the RD/ inputs are low, DB<7:0> are outputs. During a write operation, when both CS/ and WR/ are low, DB<7:0> are inputs. When CS/ is high, DB<7:0> are in high impedance state independent of the states of RD/ and WR/.

PCK (Pin21) Input. A clock applied at PCK input is used for validating the logic states of the A and B quadrature clocks and the INDX/ input.
The PCK input frequency, f_{PCK} is divided down by a factor of 1 or 2 according to bit7 of MDR0. The resultant clock is used to sample the logic levels of the

A, the B and the INDX/ inputs. If a logic level at any of these inputs remains stable for a minimum of two filter clock periods, it is validated as a correct logic state.
The PCK input is common to all four axes, but the filter clock frequency for any axis is set by its associated MDR0 register.
In non-quadrature mode no filter clock is used and the PCK input should be tied to either VDD or GND.

x0A (pin 24), **x0B** (Pin 25) Inputs. These are the A and B count inputs in axis x0. These inputs can configured to function either in quadrature mode or in non-quadrature mode. The configuration is made through MDR0. In quadrature mode, A and B clocks are 90 degrees out of phase. When A leads B in phase, the CNTR counts up and when B leads A in phase, the CNTR counts down.

In non-quadrature mode, A is the count input and B is the count direction control input. When B is **high**, positive transitions at the A input causes the CNTR to count **up**. Conversely, when B is **low**, the positive transition at the A input causes the CNTR to count **down**.

In quadrature mode, A and B inputs are sampled by an internal filter clock generated from the PCK input. In non-quadrature mode A and B inputs are not sampled and the count clocks are applied to the CNTR bypassing the filter circuit.

x1A (Pin 27), **x1B** (Pin 28), **x2A** (Pin 32), **x2B** (Pin33), **x3A** (Pin 35), **x3B** (Pin36)
These are the A and B inputs corresponding to axes x1, x2 and x3. Functionally, they are identical with the A and B inputs of axis x0.

x0INDX/ (Pin 23) Input. The INDX/ input in axis x0. The INDX/ input can be configured by MDR0 to function as load_CNTR or reset_CNTR or load_OL input. In quadrature mode, the INDX/ input can be configured to function in either synchronous or asynchronous mode. In synchronous mode, the INDX/ input is sampled with the same filter clock used for sampling the A and the B inputs and must satisfy the phase relationship with A and B in which INDX/ is at the active level during a minimum of quarter cycle of both A and B high or both A and B low.

In asynchronous mode the INDX/ input is not sampled and can be applied in any phase relationship with respect to the A and B inputs.

The INDX/ input can be either enabled or disabled in both synchronous and asynchronous modes.

x1INDX/ (Pin 26), **x2INDX/** (Pin 29), **x3INDX/** (Pin 34)
These are the INDX inputs corresponding to axes x1, x2 and x3. Functionally, they are identical with the INDX input of axis x0.

INT/ (Pin 45) **Output**
The INT/ output is the common interrupt output for all the axes. When any of the ISR bits gets set, INT/ switches low indicating an asserted interrupt. The axis generating the interrupt can then be identified by reading the ISR register.

x0FLGa (Pin 48) Output. The FLGa output in axis x0. The FLGa output is configured by MDR1 register to function as either Carry or Borrow or Compare flag. A Carry flag is generated when the CNTR overflows, a Borrow flag is generated when the CNTR underflows and a Compare flag is generated by the condition, CNTR=PR. The FLGa can be configured to produce outputs in either latched mode or instantaneous mode. In the latched mode when the selected event of Carry or Borrow or Compare has taken place, the FLGa switches low and remains low until the status register, STR is cleared. In the instantaneous mode a negative pluse is generated instantaneously when the event takes place. The FLGa output can be disabled to remain at a fixed logic high.

x1FLGa (Pin 46), **x2FLGa** (Pin 41), **x3FLGa** (Pin 39)
These outputs are the FLGa outputs corresponding to axes x1, x2 and x3 respectively. Functionally, they are identical with the FLGa output of axis x0.

x0FLGb (Pin 47) Output. The FLGb output in axis x0. The FLGb output is configured by MDR1 to function as either Index or Sign or Up/Down status indicator. When configured as Index, the FLGb output switches low when the INDX input is enabled and at active level.

When configured as Sign, the FLGb output remains high when CNTR is in an underflow state (caused by down counts at or below zero), indicating a negative number. When the CNTR counts up past zero, FLGb switches low, indicating a positive number.

When configured as Up/Down indicatior, a high at the FLGb indicates that the current count direction is up (incremental) whereas a low indicates that the direction is down (decremental).

The FLGb can be configured to function in either latched or instantaneous mode, although the latched mode has no impact on FLGb when it is configured as either Sign or Up/Down Indicator. The Sign and the Up/Down signal are always instantaneous as described above. If configured as Index, in the latched mode, the FLGb output switches low when the INDX/ input switches to the active level. It remains low until the STR register is cleared In the instantaneous mode, the FLGb output produces a negative pulse when the INDX/ input becomes active.

The FLGb output can be disabled to remain at a fixed logic high.

x1FLGb (Pin42), **x2FLGb** (Pin 40) **x3FLGb** (Pin 38)
These are the FLGb outputs corresponding to axes x1, x2 and x3 respectively. Functionally, they are identical with the FLGb output of x0.

Absolute Maximum Ratings:

Parameter	Symbol	Values	Unit
Voltage at any input	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Supply Voltage	V_{DD}	+7.0	V
Operating Temperature	T_A	-25 to +85	^oC
Storage Temperature	T_{STG}	-65 to +150	^oC

DC Electrical Characteristics. (T_A = -25˚C to +85˚C, V_{DD} = 3V to 5.5V)

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Supply Voltage	V_{DD}	3.0	5.5	V	-
Supply Current	I_{DD}	-	800	µA	All clocks off
Input Logic Low	V_{IL}	-	0.15V_{DD}	V	-
Input Logic High	V_{IH}	0.5V_{DD}	-	V	-
Output Low Voltage	V_{OL}	-	0.5	V	I_{OSNK} = 5mA, V_{DD} = 5V
Output High Voltage	V_{OH}	V_{DD} - 0.5	-	V	I_{OSRC} = 1mA, V_{DD} = 5V
Input Leakage Current	I_{ILK}	-	30	nA	-
Data Bus Leakage Current	I_{DLK}	-	60	nA	Data bus off
Data Bus Source Current	I_{OSRC}	3.0	-	mA	V_O = V_{DD} - 0.5V, V_{DD} = 5V
Data Bus Sink Current	I_{OSNK}	8.0	-	mA	V_O = 0.5V, V_{DD} = 5V
FLGa, FLGb, INT/ Source	I_{OSRC}	1.0	-	mA	V_O = V_{DD} - 0.5V, V_{DD} = 5V
FLGa, FLGb, INT/ Sink	I_{OSNK}	6.0	-	mA	V_O = 0.5V, V_{DD} = 5V

Transient Characteristics. (T_A = -25˚ to +85˚C)

For V_{DD} = 3V to 5.5V

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Read Cycle (See Fig. 2)					
RD/ Pulse Width	t_{r1}	80	-	ns	-
CS/ Set-up Time	t_{r2}	80	-	ns	-
CS/ Hold Time	t_{r3}	0	-	ns	-
RS<2:0> Set-up Time	t_{r4}	80	-	ns	-
RS<2:0> Hold Time	t_{r5}	10	-	ns	-
CHS<1:0> Set-up Time	t_{r6}	80	-	ns	-
CHS<1:0> Hold Time	t_{r7}	10	-	ns	-
DB<7:0> AccessTime	t_{r8}	80	-	ns	Access starts when both RD/ and CS/ are low.
DB<7:0> Release Time	t_{r9}	-	35	ns	Release starts when either RD/ or CS/ is terminated.
Back to Back Read delay	t_{r10}	10	-	ns	-
Write Cycle (See Fig. 3)					
WR/ Pulse Width	t_{w1}	45	-	ns	-
CS/ Set-up Time	t_{w2}	45	-	ns	-
CS/ Hold Time	t_{w3}	0	-	ns	-
RS<2:0> Set-up Time	t_{w4}	45	-	ns	-
RS<2:0> Hold Time	t_{w5}	10	-	ns	-
CHS<1:0> Set-up Time	t_{w6}	45	-	ns	-
CHS<1:0> Hold Time	t_{w7}	10	-	ns	-
DB<7:0> Set-up Time	t_{w8}	45	-	ns	-
DB<7:0> Hold Time	t_{w9}	10	-	ns	-
Back to Back Write Delay	t_{w10}	90	-	ns	-

For VDD = 3.3V ±10%

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Quadrature Mode (See Fig. 4-6)					
PCK High Pulse Width	t_1	24	-	ns	-
PCK Low Pulse Width	t_2	24	-	ns	-
PCK Frequency	f_{PCK}	-	20	MHz	-
Filter Clock(ff)Period	t_3	50	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> =0
	t_3	100	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> =1
Filter clock frequency	f_f	-	20	MHz	$f_f = 1/ t_3$
Quadrature Separation	t_4	52	-	ns	$t_4 > t_3$
Quadrature Clock Pulse Width	t_5	105	-	ns	$t_5 > 2t_3$
Quadrature Clock frequency	f_{QA}, f_{QB}	-	4.5	MHz	$f_{QA} = f_{QB} < 1/4t_3$
Quadrature Clock to Count Delay	t_{Q1}	$4t_3$	5t3	-	-
X1/X2/X4 Count Clock Pulse Width	t_{Q2}	25	-	ns	$t_{Q2} = t_3/2$
Quadrature Clock to FLGa delay	t_{fda}	$4.5t_3$	5.5t3	ns	-
Quadrature Clock to FLGb delay	t_{fdb}	$3t_3$	4t3	ns	-
FLGa to INT/ delay	t_{nt}	0	-	ns	-
INDX/ Input Pulse Width (Synchronous)	t_{id}	60	-	ns	$t_{id} > t_4$
INDX/ set-up time (Synchronous)	t_{is}	10	-	ns	-
INDX/ hold time (Synchronous)	t_{ih}	10	-	ns	-
FLGa Output Width	t_{fw}	50	-	ns	$t_{fw} \approx t_4$
Non-Quadrature Mode (See Fig. 7-8)					
Clock A - High Pulse Width	t_6	24	-	ns	-
Clock A - Low Pulse Width	t_7	24	-	ns	-
Direction Input B Set-up Time	t_{8s}	24	-	ns	-
Direction Input B Hold Time	t_8	20	-	ns	-
Clock Frequency	f_A	-	20	MHz	$f_A = (1/ (t_6 + t_7))$
Clock to FLGa Out Delay	t_9	-	40	ns	-
FLGa Out Pulse Width	t_{10}	24	-	ns	$t_{10} = t_7$
INDX/ Pulse Width (Asynchronous)	t_{11}	30	-	ns	-

For VDD = 5V ±10%

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Quadrature Mode (See Fig. 4-6)					
PCK High Pulse Width	t_1	12	-	ns	-
PCK Low Pulse Width	t_2	12	-	ns	-
PCK Frequency	f_{pCK}	-	40	MHz	-
Filter Clock(f_f)Period	t_3	25	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> =0
	t_3	50	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> =1
Filter clock frequency	f_f	-	40	MHz	-
Quadrature Separation	t_4	26	-	ns	$t_4 > t_3$
Quadrature Clock Pulse Width	t_5	52	-	ns	$t_5 > 2t_3$
Quadrature Clock frequency	f_{QA}, f_{QB}	-	9.6	MHz	$f_{QA} = f_{QB} < 1/4t_3$
Quadrature Clock to Count Delay	t_{Q1}	$4t_3$	5t3	-	-
x1 / x2 / x4 Count Clock Pulse Width	t_{Q2}	12	-	ns	$t_{Q2} = t_3/2$
Quadrature Clock to FLGa delay	t_{fda}	$4.5t_3$	5.5t3	ns	-
Quadrature Clock to FLGb delay	t_{fdb}	$3t_3$	4t3	ns	-
FLGa to INT/ delay	t_{nt}	0	-	ns	-
INDX/ Input Pulse Width (Synchronous)	t_{id}	32	-	ns	$t_{id} > t_4$
INDX/ set-up time (Synchronous)	t_{is}	5	-	ns	-
INDX/ hold time (Synchronous)	t_{ih}	5	-	ns	-
FLGa Output Width	t_{fw}	24	-	ns	$t_{fw} \approx t_4$
Non-Quadrature Mode (See Fig. 7-8)					
Clock A - High Pulse Width	t_6	12	-	ns	-
Clock A - Low Pulse Width	t_7	12	-	ns	-
Direction Input B Set-up Time	t_8	12	-	ns	-
Direction Input B Hold Time	t_8	10	-	ns	-
Clock Frequency	f_A	-	40	MHz	$f_A = (1/ (t_6 + t_7))$
Clock to FLGa Out Delay	t_9	-	20	ns	-
FLGa Out Pulse Width	t_{10}	12	-	ns	$t_{10} = t_7$
INDX/ Pulse Width (Asynchronous)	t_{11}	15	-	ns	-

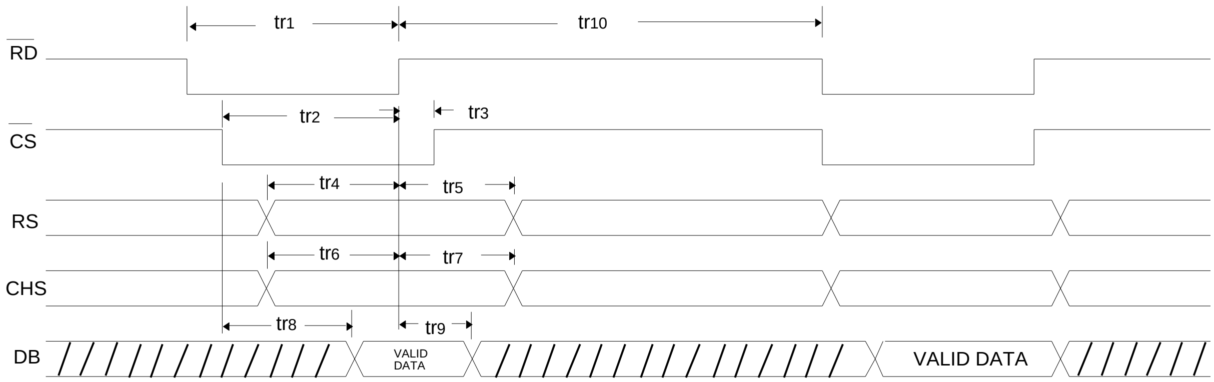


FIGURE 2. READ CYCLE

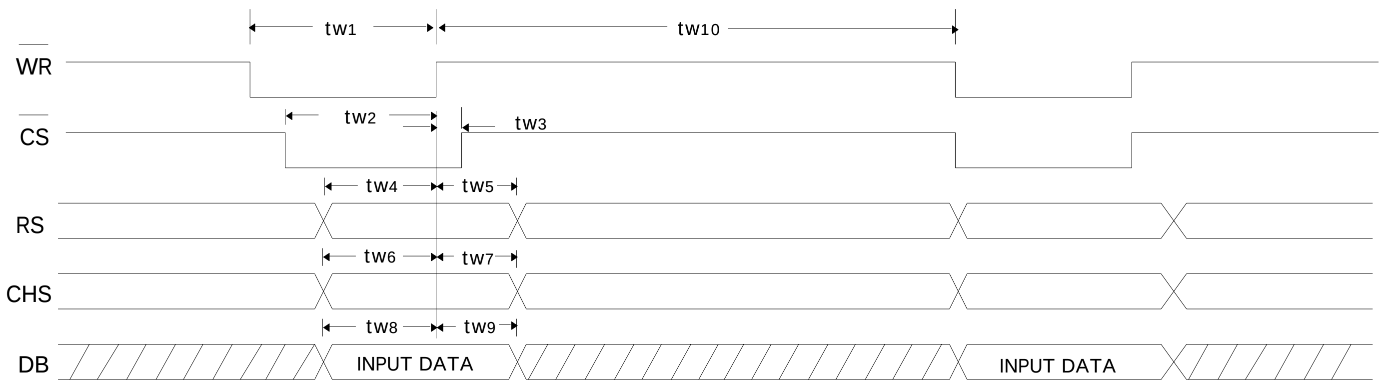
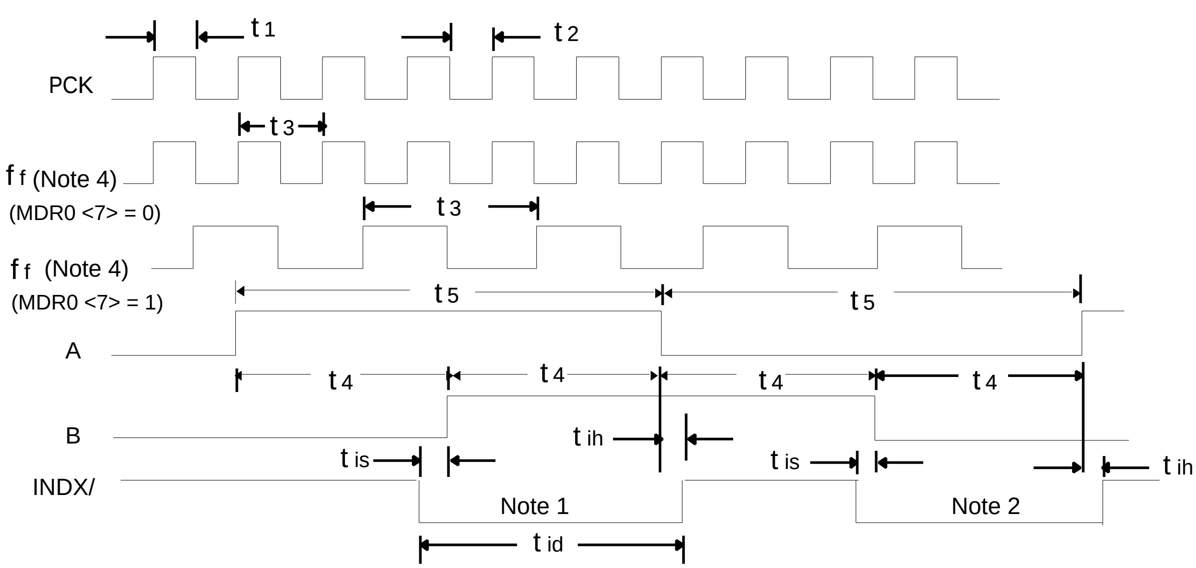
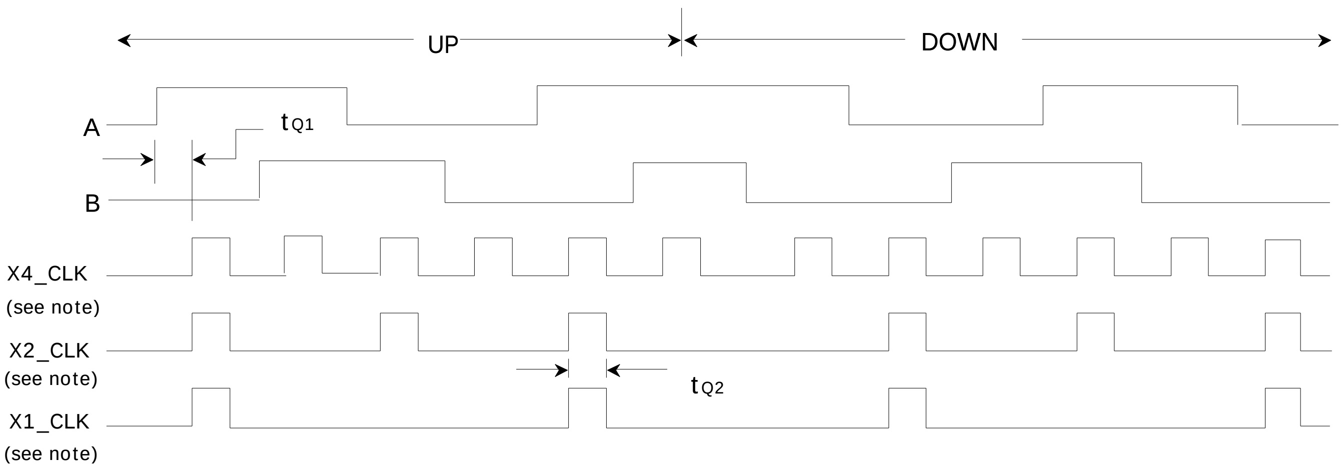


FIGURE 3. WRITE CYCLE



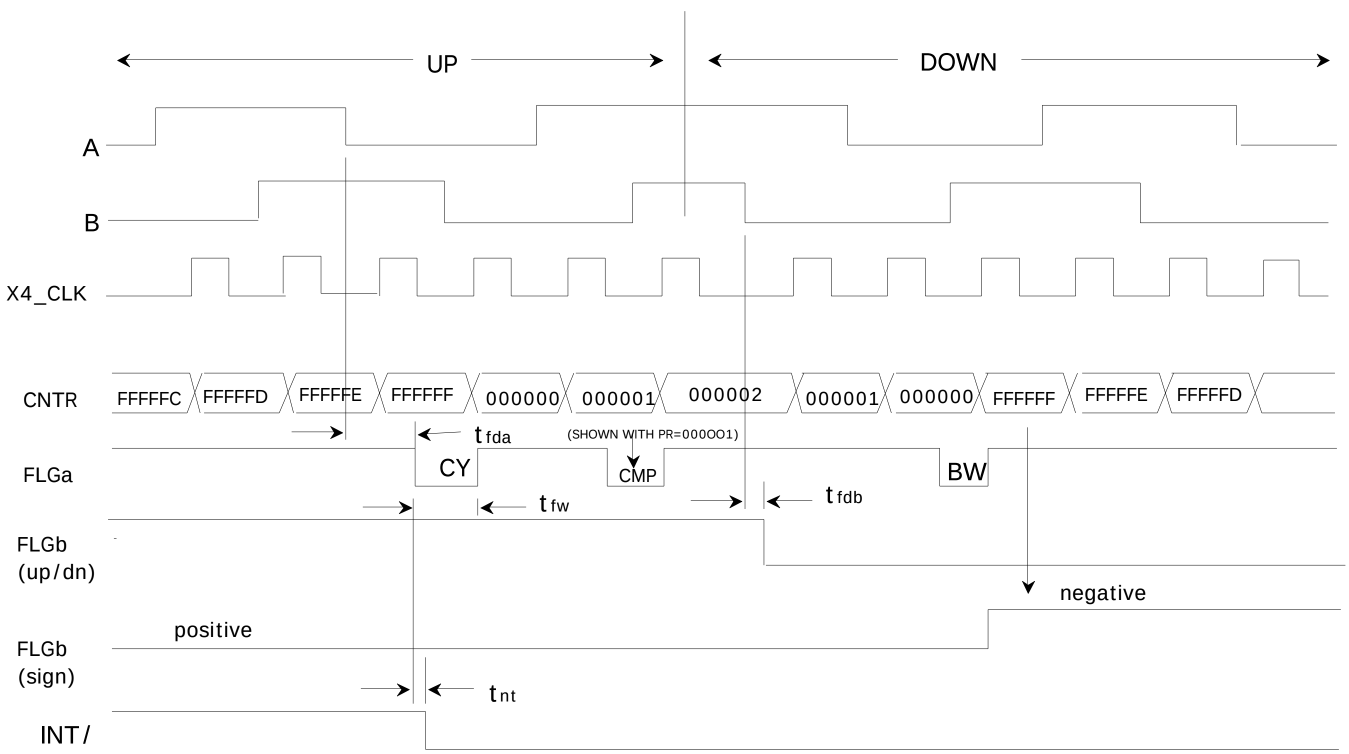
Note 1. Synchronous index coincident with both A and B high.
Note 2. Synchronous index coincident with both A and B low.
Note 3. f_F is the internal effective filter clock.

FIGURE 4. PCK, A, B and INDX



NOTE. x1, x2 and x4 CLKs are internal Up/Down clocks derived from filtered and decoded quadrature clocks.

FIGURE 5. A/B QUADRATURE CLOCKS vs INTERNAL COUNT CLOCKS



NOTE. FLGa is in non-latched mode.

FIGURE 6. QUADRATURE CLOCKS vs FLGa, FLGb and INT/ OUTPUTS

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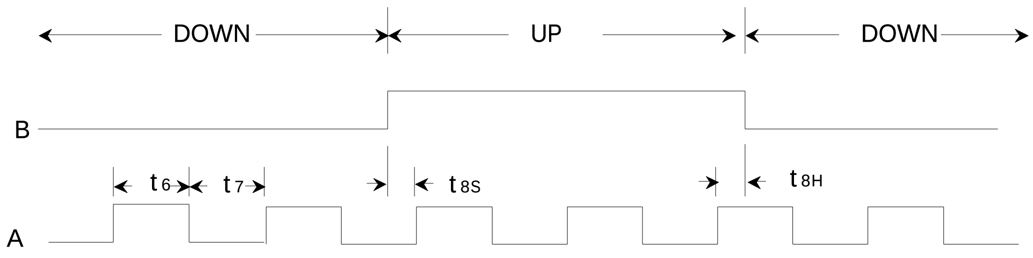

FIGURE 7. COUNT (A) and DIRECTION (B) INPUTS IN NON-QUADRATURE MODE

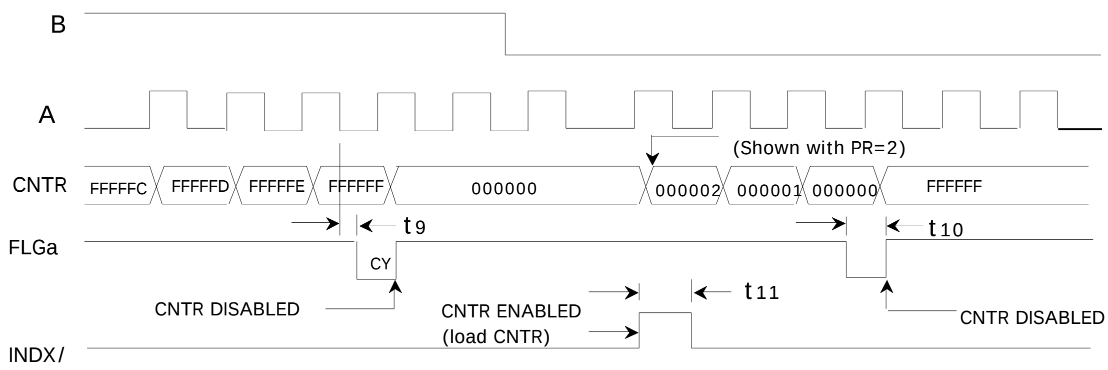

FIGURE 8. SINGLE-CYCLE, NON-QUADRATURE

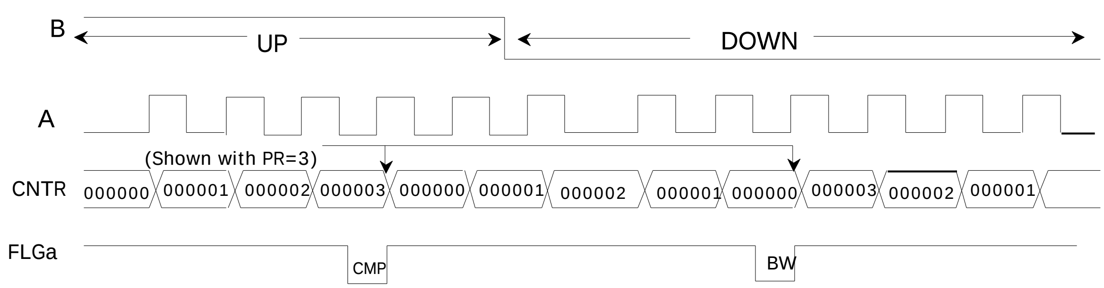

FIGURE 9. MODULO-N, NON-QUADRATURE

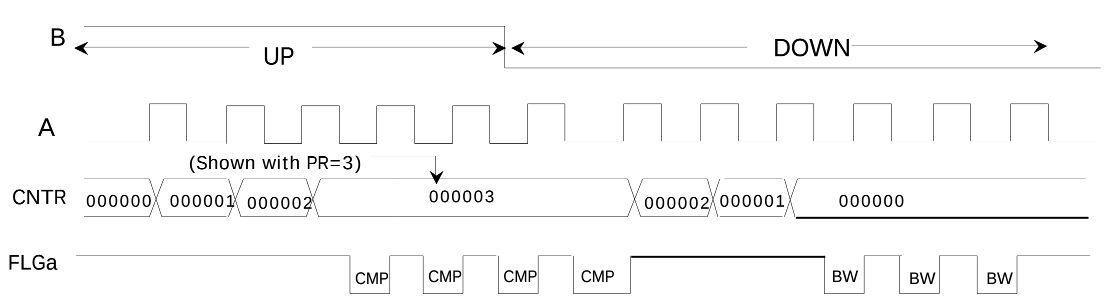

FIGURE 10. RANGE-LIMIT, NON-QUADRATURE

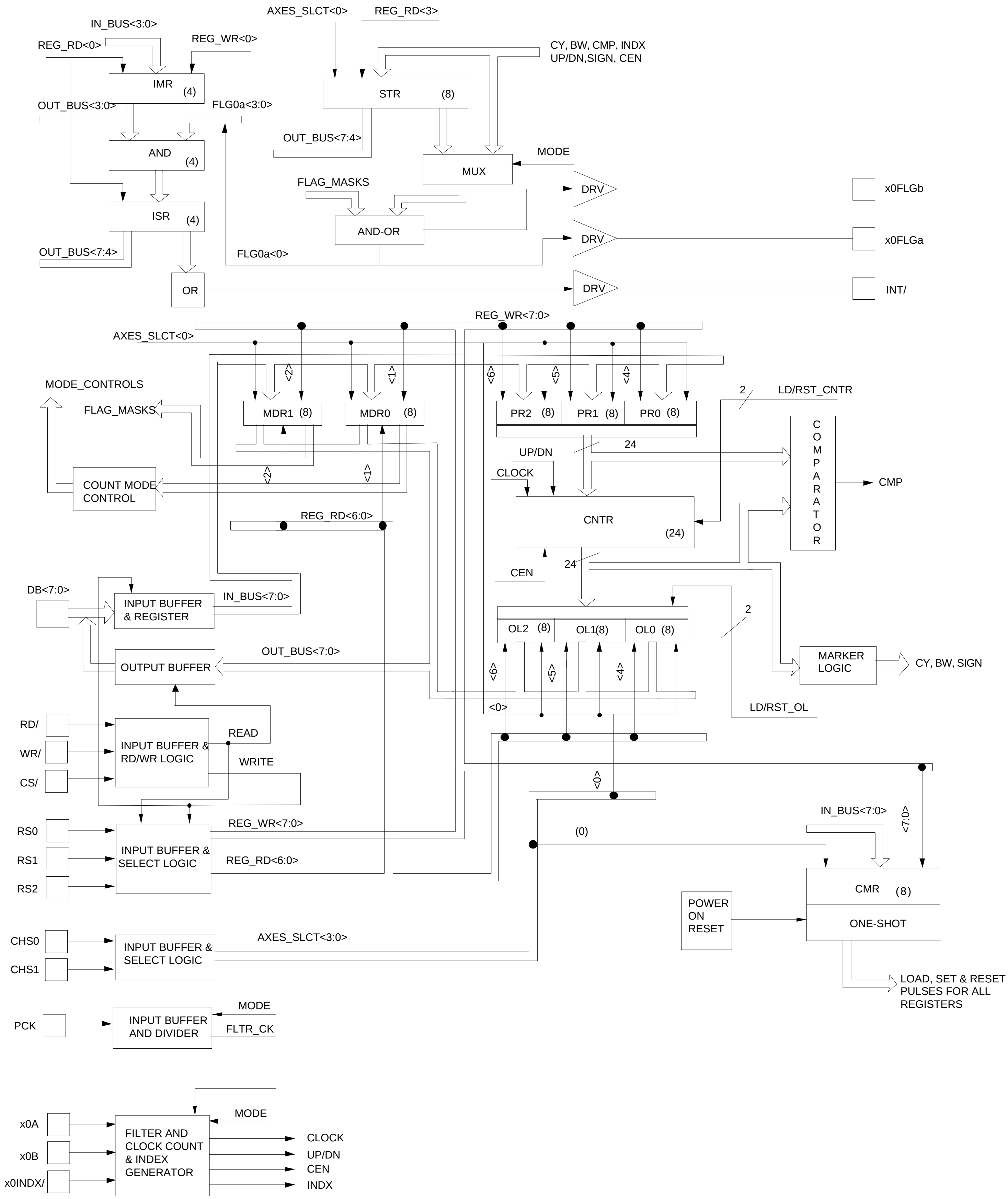

FIGURE 11. LS7566R BLOCK DIAGRAM

NOTE : For Clarity, only Axis0 is included

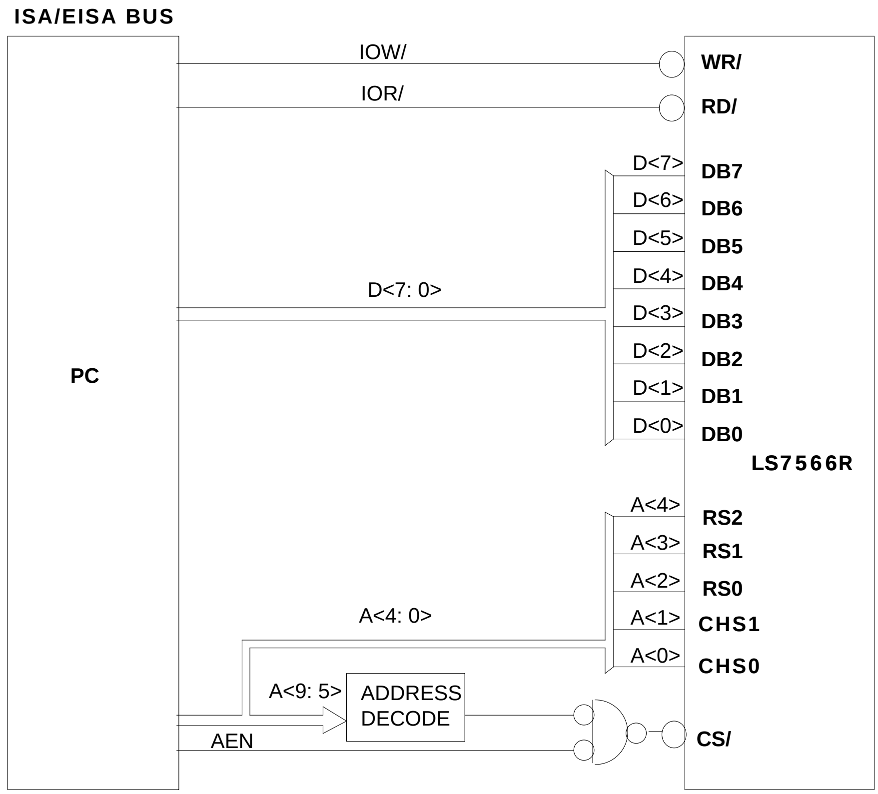

FIGURE 12. LS7566R TO ISA/EISA INTERFACE

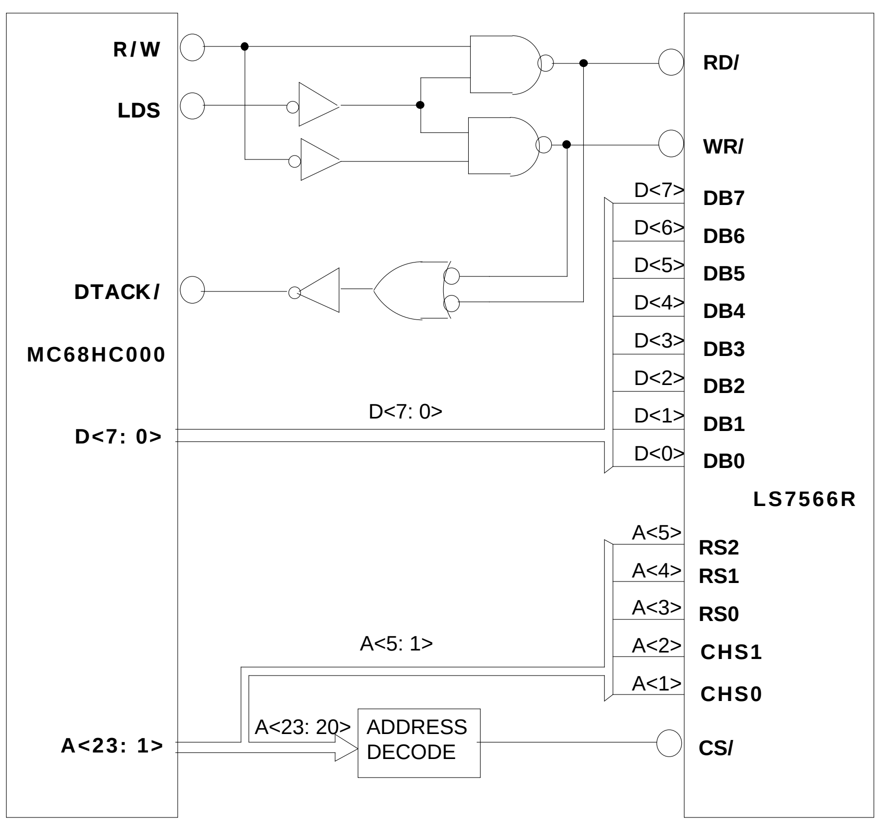

FIGURE 13. LS7566R TO MC68HC000 INTERFACE