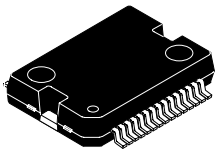
Document Number: MC33899
Rev. 2.0, 6/2007

RoHS

Programmable H-Bridge Power IC

33899

PROGRAMMABLE H-BRIDGE POWER IC



VW SUFFIX (Pb-FREE)
98ASH70693A
30-PIN HSOP

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33899VW/R2	-40°C to 125°C	30 HSOP

The 33899 is designed to drive a DC motor in both forward and reverse shaft rotation under pulse-width modulation (PWM) control of speed and torque. A current mirror output provides an analog feedback signal proportional to the load current. A serial peripheral interface (SPI) is used to select slew rate control, current compensation limits and to read diagnostic status (faults) of the H-Bridge drive circuits. SPI diagnostic reporting includes open circuit, short circuit to VIGNP, short circuit to ground, die temperature range, and undervoltage on VIGNP.

Features

- Drives Inductive Loads in a Full H-Bridge Configuration
- Current Mirror Output Signal (Gain Selectable via External Resistor)
- Short Circuit Current Limiting
- Thermal Shutdown (Outputs Latched Off Until Reset via SPI)
- Internal Charge Pump Circuit for the Internal High-Side MOSFETs
- SPI-Selectable Slew Rate Control and Current Limit Control
- Overtemperature Shutdown
- Outputs Can Be Disabled to High-Impedance State
- PWM-able up to 11 kHz @ 3.0 A
- Synchronous Rectification Control of the High-Side MOSFETs
- Low RDS(ON) Outputs at High Junction Temperature (< 165 mΩ @ TA = 125°C, VIGNP = 6.0 V)
- Outputs Survive Shorts to -1.0 V
- Pb-Free Packaging Designated by Suffix Code VW

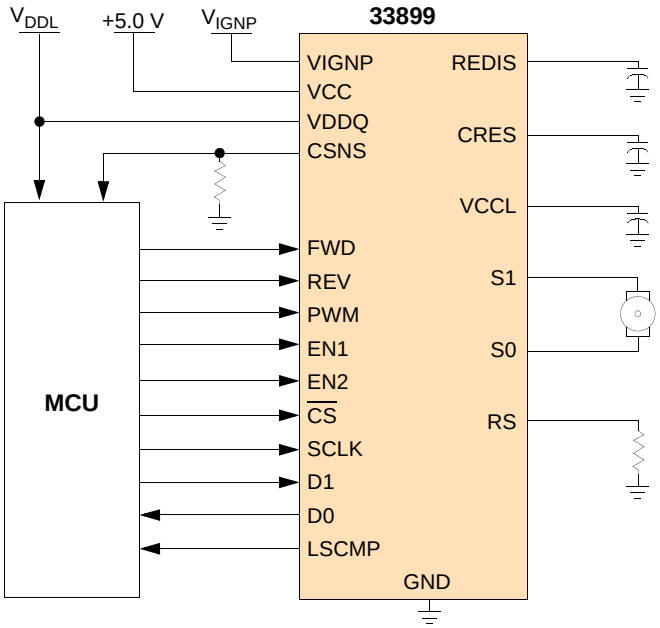


Figure 1. 33899 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

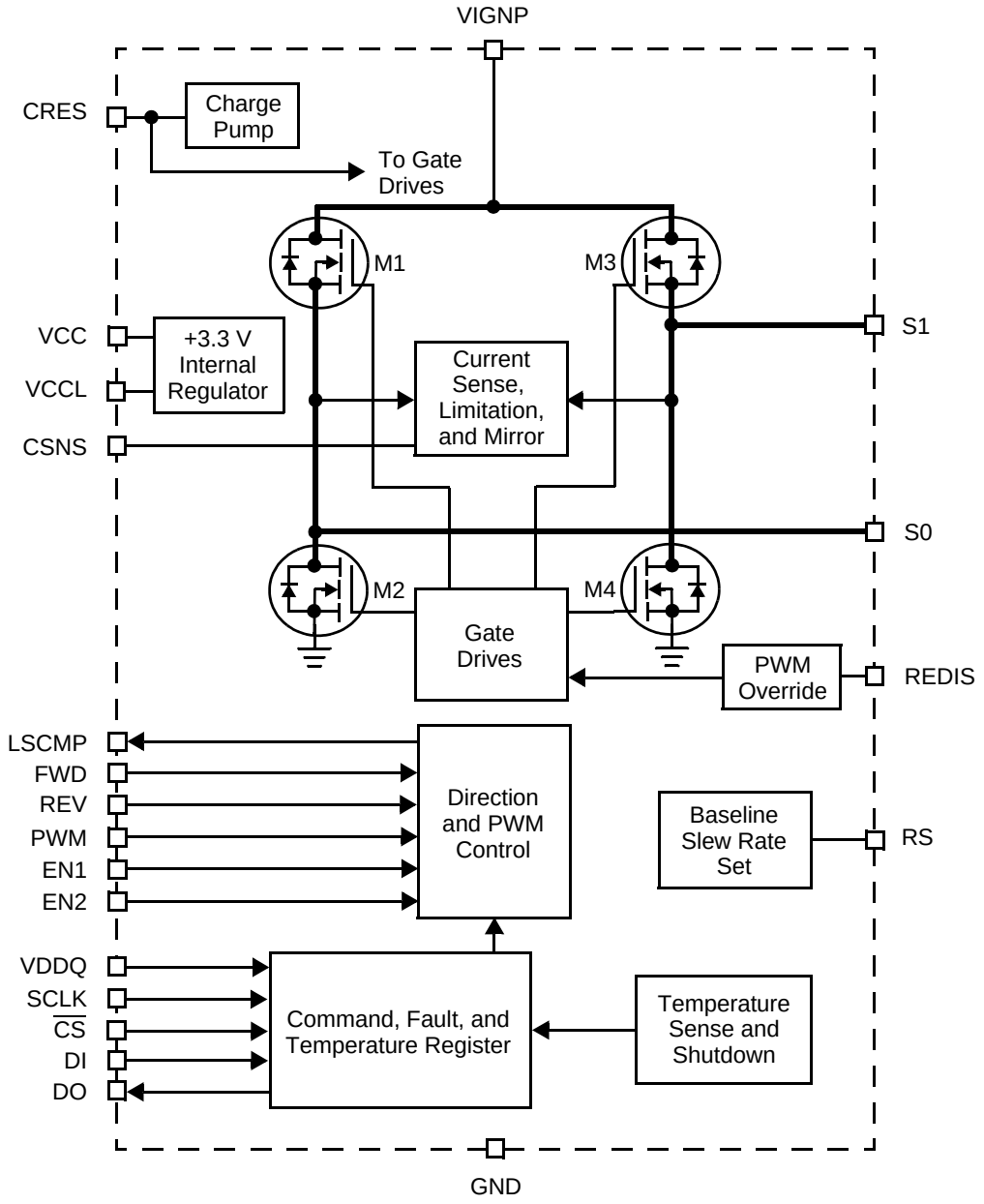


Figure 2. 33899 Simplified Internal Block Diagram

PIN CONNECTIONS

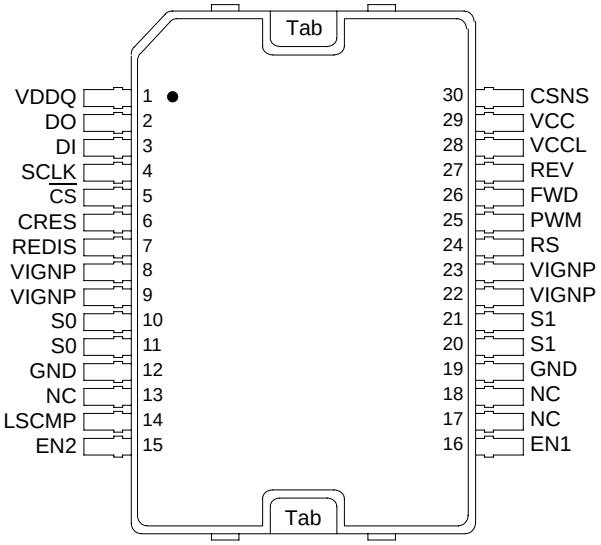


Figure 3. 33899 Pin Connections

Table 1. 33899 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 12.

Pin Number	Pin Name	Formal Name	Definition
1	VDDQ	Logic Level Output Bias	Sets V_{OH} level of DO output and LSCMP.
2	DO	SPI Data Out	SPI control data output pin from the IC to the MCU.
3	DI	SPI Data In	SPI control data input pin from the MCU to the IC.
4	SCLK	SPI Serial Clock Input	The SCLK input is the clock signal input for synchronization of serial data transfer.
5	$\overline{CS}$	Chip Select (Active Low)	This pin is an input connected to a chip select output of an MCU.
6	CRES	Charge Pump	This pin connects an external capacitor, which is the storage reservoir for the internal charge pump.
7	REDIS	Automatic Output Re-Enable Disable	This input pin is a connection to a capacitor that determines the default time the output will be turned off when the low-side current comparator is tripped, if PWM has not commanded it. The typical value with a 0.1 μF is 100 μs. If shorted, the feature is disabled.
8, 9, 22, 23	VIGNP	Protected Ignition Voltage	This input pin is the primary H-Bridge power input. **Note:** Not reverse voltage protected.
10, 11	S0	Bridge Output 0 to Load	These output pins drive the bi-directional motor and must be connected together on the PC board.
12, 19	GND	Ground	These pins must be connected on the PC board to the exposed pad.
13, 17, 18	NC	No Connect	These pins have no internal connections.
14	LSCMP	Low-Side Comparator	This output pin pulses high anytime the low-side current comparator is tripped.
15 16	EN2 EN1	Master Enable 2 Master Enable 1	These input pins determine the mode of the IC; namely, sleep, standby, and run.
20, 21	S1	Bridge Output 1 to Load	These output pins drive the bi-directional motor and must be connected together on the PC board.

Table 1. 33899 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 12.

Pin Number	Pin Name	Formal Name	Definition
24	RS	Slew Rate Control	This input pin is connected to a resistor that sets slew timing.
25	PWM	PWM Input	This input pin is used to set the motor switching and frequency duty cycle.
26	FWD	Forward Input	This input pin, along with the reverse input pin REV, determines the direction of current flow in the H-Bridge.
27	REV	Reverse Input	This input pin, along with the forward input pin FWD, determines the direction of current flow in the H-Bridge.
28	VCCL	3.3 V Input	3.3 V input source.
29	VCC	5.0 V Input	5.0 V input source.
30	CSNS	Current Sense	Output of current amplifier.
Tab/Pad	Thermal Interface/ GND	Exposed Pad Thermal Interface	The exposed pad, a thermal interface for sinking heat from the device, is a high-current GND connection and must be connected to GND (pins 12 and 19).

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Protected Power Supply Voltage	V_{IGNP}	-0.3 to 40	V
Logic Supply Voltage	V_{CC}	-0.3 to 7.0	V
Logic Output Bias Voltage	V_{DDQ}	-0.3 to 7.0	V
VCCL Supply Voltage	V_{CCL}	-0.3 to 5.0	V
Input/Output Voltage (FWD, REV, EN1, EN2, PWM, $\overline{CS}$, DI, SCLK, DO, CSNS, LSCMP, RS, REDIS)	$V_{I/O}$	-0.3 to 7.0	V
Motor Outputs	V_{S0}, V_{S1}	-0.5 to 40	V
Charge Pump Voltage	V_{CRES}	-0.3 to 50	V
ESD Voltage [1] Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
THERMAL RATINGS			
Operating Temperature[2] Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Thermal Resistance, Junction to Ambient[3]	$R_{\theta JA}$	18	°C/W
Thermal Resistance, Junction to Case (Exposed Pad)	$R_{\theta JC}$	<0.5	°C/W
Peak Package Reflow Temperature During Solder Mounting [4]	T_{SOLDER}	220	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
2. The junction temperature is the primary limiting parameter. The module thermal design must provide a low enough thermal impedance to keep the junction temperature within limits for all anticipated power levels and ambient temperatures.
3. $R_{\theta JA}$ is referenced to JEDEC standard 2s2p thermal evaluation board at 1W total device power dissipation in still air. Deviations from this standard will produce corresponding changes in the actual thermal performance.
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics at -40°C ≤ T_J ≤ +150°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 3.14 V ≤ V_{CCL} ≤ 3.47 V, 2.97 V ≤ V_{DDQ} ≤ 5.25 V, 6.0 V ≤ V_{IGNP} ≤ 26.5 V unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
V_{IGNP} Operating Voltage	V_{IGNP}	6.0	–	26.5	V
V_{IGNP} Operating Current V_{IGNP} = 14.5 V, H-Bridge Disabled, EN1 = EN2 = 5.0 V	I_{VIGNP}	–	–	10	mA
V_{IGNP} Sleep Current EN1 = EN2 = 0 V	I_{VIGNP}	–	–	145	µA
Undervoltage Shutdown Threshold	$V_{IGNP\ UV}$	3.4	–	4.2	V
Overvoltage Shutdown Threshold	$V_{IGNP\ OV}$	27	–	32	V
V_{CC} Operating Voltage	V_{CC}	4.75	–	5.25	V
V_{CC} Operating Current @ 5.0 V	I_{VCC}	–	–	5.0	mA
V_{CC} Sleep Current EN1 = EN2 = 0 V	I_{VCC}	–	–	25	µA
V_{CCL} Operating Voltage	V_{CCL}	3.14	–	3.47	V
V_{CCL} Operating Current @ 3.3 V	I_{VCCL}	–	–	3.0	mA
V_{CCL} Sleep Current EN1 = EN2 = 0 V	I_{VCCL}	–	–	2.0	µA
V_{DDQ} Operating Voltage	V_{DDQ}	2.97	–	5.25	V
V_{DDQ} Operating Current	I_{VDDQ}	–	–	200	µA
V_{DDQ} Sleep Current EN1 = EN2 = 0 V	I_{VDDQ}	–	–	50	µA
POWER-ON RESET					
Power-ON Reset Threshold V_{CC} Rising	V_{CCPOR}	3.9	–	4.7	V
Power-ON Reset Threshold V_{CCL} Rising	V_{CCLPOR}	2.50	–	2.95	V
Power-ON Reset Hysteresis	$V_{POR\ HYS}$	0.2	–	0.5	V
CHARGE PUMP					
C_{RES} Voltage (MOSFETs 1 and 3 or 2 and 4 ON) I_{CRES} = -0.1 mA V_{IGNP} = 6.0 V 9.5V ≤ V_{IGNP} ≤ 26.5 V	V_{CRES}	14 V_{IGNP} + 10	– –	– 45	V
CONTROL INPUTS					
Input Low Voltage EN1, EN2, PWM, $\overline{CS}$, SCLK, DI, FWD, REV	V_{IL}	–	–	0.8	V
Input High Voltage EN1, EN2, PWM, $\overline{CS}$, SCLK, DI, FWD, REV	V_{IH}	2.0	–	–	V

Table 3. Static Electrical Characteristics (continued)

Characteristics at -40°C ≤ T_J ≤ +150°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 3.14 V ≤ V_{CCL} ≤ 3.47 V, 2.97 V ≤ V_{DDQ} ≤ 5.25 V, 6.0 V ≤ V_{IGNP} ≤ 26.5 V unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INPUTS (CONTINUED)					
Input Leakage Current—Digital Inputs SCLK, DI: V_{IN} = 0 V	I_{IN}	 -5.0	 –	 5.0	µA
Input Bias Current EN1, EN2, FWD, REV, PWM: V_{IN} = 5.0 V $\overline{CS}$: V_{IN} = 0 V	 I_{DWN} I_{UP}	 27 -70	 – –	 70 -27	µA
DATA OUTPUT					
Data Output Low Voltage I_{OL} = 1.6 mA	V_{DO_OL}	 –	 –	 0.4	V
Data Output High Voltage I_{OH} = -800 µA	V_{DO_OH}	 V_{DDQ} - 0.5	 –	 –	V
Data Out Tri-State Leakage	I_{LEAK}	-5.0	–	5.0	µA
POWER OUTPUT					
Breakdown Voltage S0, S1, V_{IGNP}: I = 100 µA	V_{BVDS}	 40	 –	 –	V
ON-Resistance (Each Output FET) I_{OUT} = 3.5 A, V_{IGNP} = 6.0 V	$R_{DS(ON)}$	 –	 –	 165	mΩ
Body Diode Forward Voltage (All 4 Output Diodes) (6) ENx = 0 V, I_{OUT} = 3.0 A, T_J = 150°C ENx = 0 V, I_{OUT} = 3.0 A, T_J = 23°C ENx = 0 V, I_{OUT} = 3.0 A, T_J = -40°C	V_F	 – – –	 – – –	 1.0 1.4 1.8	V
OFF-State Output Bias VCC = 5.0 V, EN1 = EN2 = 0 V, S0 Shorted to S1 (Through Motor)	V_{BIAS}	 0.2 V_{CC}	 –	 0.6 V_{CC}	V
OFF-State Output Leakage (between SO and S1) V_{CC} = 0 V, EN1 = EN2 = 0 V, R_L = 600 Ω, V_{IGN} = 16 V V_{CC} = 5.0 V, EN1 = EN2 = 0 V, R_L = 600 Ω, V_{IGN} = 18 V	I_{LEAK}	 – –	 – –	 100 100	µA
Fault Threshold (OFF State) (EN1 = EN2 = 0 V) Measured at S1 Measured at S0	 V_{FAULT_THR1} V_{FAULT_THR2}	 0.65 V_{CC} 0.15 V_{CC}	 – –	 0.85 V_{CC} 0.35 V_{CC}	V
CURRENT SENSE					
Current Sense Zero FWD = 5.0 V, REV = 0 V; Then FWD = 0 V, REV = 5.0 V, $I_{S1/S0}$ = 0 A	I_{CSZ}	–	–	0.2	mA
Current Sense Ratio: k_{CSNS} = $I_{S1/S0}$ / I_{CS} (FWD = 5.0 V, REV = 0 V; Then FWD = 0 V, REV = 5.0 V) $I_{S1/S0}$ = -0.4 A $I_{S1/S0}$ = -1.6 A $I_{S1/S0}$ = -6.0 A (7)	 k_{CSNS} k_{CSNS} k_{CSNS}	 250 340 –	 – – 400	 500 435 –	

Table 3. Static Electrical Characteristics (continued)

Characteristics at -40°C ≤ T_J ≤ +150°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 3.14 V ≤ V_{CCL} ≤ 3.47 V, 2.97 V ≤ V_{DDQ} ≤ 5.25 V, 6.0 V ≤ V_{IGNP} ≤ 26.5 V unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE (CONTINUED)					
Current Sense Saturation Voltage FWD = 5.0 V, REV = 0 V; Then FWD = 0 V, REV = 5.0 V, R_{CSNS}= 10 kΩ	V_{CSNS_SAT}	V_{CC} - 0.2	–	V_{CC} + 0.2	V
High-Side Current Limit	I_{HSLIM}				A
DI Bit 4 and Bit 3 = 00		5.8	–	10.2	
DI Bit 4 and Bit 3 = 01		7.2	–	11.9	
DI Bit 4 and Bit 3 = 10 (5)		8.0	–	13.5	
DI Bit 4 and Bit 3 = 11 (5)		10.0	–	17.9	
Low-Side Current Limit	I_{LSLIM}				A
DI Bit 4 and Bit 3 = 00		5.3	–	8.6	
DI Bit 4 and Bit 3 = 01		6.4	–	10.0	
DI Bit 4 and Bit 3 = 10		7.4	–	11.0	
DI Bit 4 and Bit 3 = 11		10.0	–	15.0	
Low-Side Current Limit Comparator	I_{LSCMP}				A
DI Bit 4 and Bit 3 = 00		3.2	–	5.2	
DI Bit 4 and Bit 3 = 01		4.2	–	6.4	
DI Bit 4 and Bit 3 = 10		5.0	–	7.5	
DI Bit 4 and Bit 3 = 11		7.5	–	10.6	
Current Limit Current Comparator Differential	I_{CURLIM}-				A
DI Bit 4 and Bit 3 = 00	I_{LSCMP}	1.0	3.0	–	
DI Bit 4 and Bit 3 = 01		1.0	3.0	–	
DI Bit 4 and Bit 3 = 10		1.0	3.0	–	
DI Bit 4 and Bit 3 = 11		1.0	3.0	–	
LSCMP Output Voltage					V
I_{OL} = 100 μA	V_{LSCMP_OL}	–	–	0.1	
I_{OH} = -100 μA	V_{LSCMP_OH}	V_{DDQ}-0.5	–	V_{DDQ}	
REDIS Current					
Pullup Current Source	I_{REDIS_sc}	-160	–	-70	μA
Pulldown Current Sink	I_{REDIS_sk}	1.0		5.0	mA
REDIS Threshold	V_{REDIS_THR}				V
Voltage Where Low-Side MOSFET Turns On		3.6	–	4.4	
Voltage Where Low-Side MOSFET Turns Off		3.35	–	4.15	
Hysteresis		0.15	–	0.35	
THERMAL					
Thermal Shutdown (6), SPI Bits = 11	T_{LIM}	157.5	–	172.5	°C
Thermal Hysteresis (6)	T_{HYS}	3.0	–	10	°C
Temperature Warning (6), SPI Bits = 01	T_{WARN}	132.5	–	147.5	°C
Temperature Warning Hysteresis (6)	$T_{WARN(HYS)}$	3.0	–	10	°C

Notes

5. Production test at 125°C is at V_{IGNP} ≤ 18 V. Operation to 26.5V is guaranteed by design.
6. Guaranteed by characterization in the development phase. Parameter not tested.
7. Design Information, not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics at -40°C ≤ T_A ≤ 125°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 6.0 V ≤ V_{IGNP} ≤ 26.5 V unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PWM Frequency (8)	f_{PWM}	–	–	11	kHz
PWM/Output Duty Cycle Accuracy Frequency = 10 kHz, RS = 10 kΩ, Slew Time = 1X, Duty cycle = 50%	OUT_{ACC}	-4.5	–	4.5	%
Short Circuit Filter (S0 and S1)	t_{SCF}	5.0	–	11	µs
Minimum PWM Low Pulse Width (8)	PWM_{MIN}	–	–	0.2	µs
Low-Side Comparator One Shot Pulse Duration After a Low-Side Comparator Trip	t_{LSC}	5.0	–	10	µs
Low-Side Comparator Blank Time Blanking Time After a Low-Side Comparator Pulse	t_{LSCB}	5.0	–	10	µs
Overtemperature Shutdown Filter (time before Die Temp bit is set), (8)	t_{OTF}	5.0	–	13.5	µs
Enable Lead Time (8)	t_{LEAD}	140	–	–	ns
Enable Lag Time (8)	t_{LAG}	50	–	–	ns
Delay Until Output Shuts Off Short Circuit Detection or EN1 Falling or EN2 Falling Until H-Bridge Disables	t_{SODLY}	–	–	5.0	µs
Dead Timer (9) Time Between High-Side MOSFET and Low-Side MOSFET Transition	t_{DEAD}	1.0	–	3.0	µs
Open Load Fault Delay Duration of Fault Condition Until Fault Gets Latched In	t_{FDO}	200	–	400	µs
Overvoltage Shutdown Filter Time from VIGNP > V_{OV} to MOSFET Output Disable	t_{OVS}	100	–	200	µs
Sleep Recovery Time(8)(9)(10)	t_{SLEEP}	–	150	–	µs
Slew Time S0 and S1(11) (Output Load = 5.0 mH and 1.6 Ω, 30% to 70%, V_{IGNP} = 14.5 V)	$S0/S1_{RS}$				µs
Slew Mode = 1X					
RS= 50 kΩ		1.6	–	3.2	
RS = 10 kΩ, Short		0.2	–	0.8	
Slew Mode = 2X					
RS = 50 kΩ		2.8	–	6.3	
RS = 10 kΩ, Short		0.5	–	1.5	
Slew Mode = 4X					
RS = 50 kΩ		5.0	–	12.8	
RS = 10 kΩ, Short		1.2	–	3.0	

Notes

8. Design information.
9. Guaranteed by characterization in the development phase. Parameter not tested.
10. Sleep recovery time is the time from EN going high until the outputs are ready to respond to input. This time is dependent on the recovery time of V_{CCL} and V_{CCL_POR}. The recommended value for the V_{CCL} capacitor is designed to permit initialization of internal logic prior to clearing of the POR condition (See +3.3 V Input (V_{CCL}) on page 12).
11. By design, if the RS input is left open, the slew time is the same as when shorted to GND. However, this is a high-impedance input and will be susceptible to external noise sources unless terminated appropriately. It is highly recommended to terminate this pin with either a ground or one of the program resistors .

Table 4. Dynamic Electrical Characteristics

Characteristics at -40°C ≤ T_A ≤ 125°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 6.0 V ≤ V_{IGNP} ≤ 26.5 V unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI CHARACTERISTICS (12)					
Transfer Frequency (13)	f_{OP}	dc	–	6.25	MHz
SCLK Period (13)	t_{SCLK}	160	–	–	ns
SCLK High Time (13)	t_{SCLK_HS}	56	–	–	ns
SCLK Low Time (13)	t_{SCLK_LS}	56	–	–	ns
DI Input Setup Time (13)	$t_{DI(SU)}$	16	–	–	ns
DI Input Hold Time (13)	$t_{DI(HOLD)}$	20	–	–	ns
DO Access Time	$t_{DO(ACC)}$	–	–	116	ns
DO Disable Time (14)	$t_{DO(DIS)}$	–	–	100	ns
DO Output Valid Time	$t_{DO(VALID)}$	–	–	116	ns
DO Output Hold Time (13) No Capacitor on DO	$t_{DO(HOLD)}$	0	20	–	ns
Rise Time (14)	t_R	–	–	60	ns
Fall Time (14)	t_F	–	–	30	ns
$\overline{CS}$ Negated Time (13)	$t_{\overline{CSN}}$	500	–	–	ns
Input Pins Input Capacitance (8) DI SCLK	C_{IN}	 – –	 – –	 20 20	pF

Notes
12. All SPI timing is performed with a 100 pF load on DO unless otherwise noted.
13. Design information.
14. Guaranteed by characterization.

TIMING DIAGRAMS

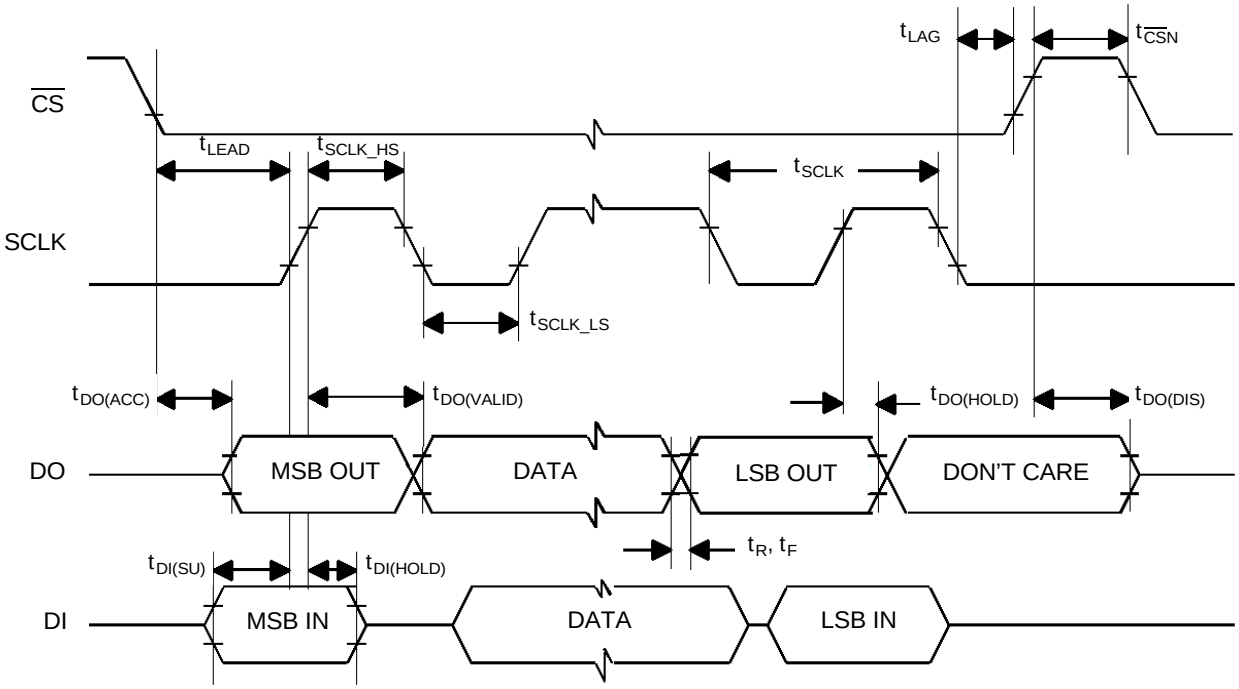


Figure 4. SPI Timing Diagram

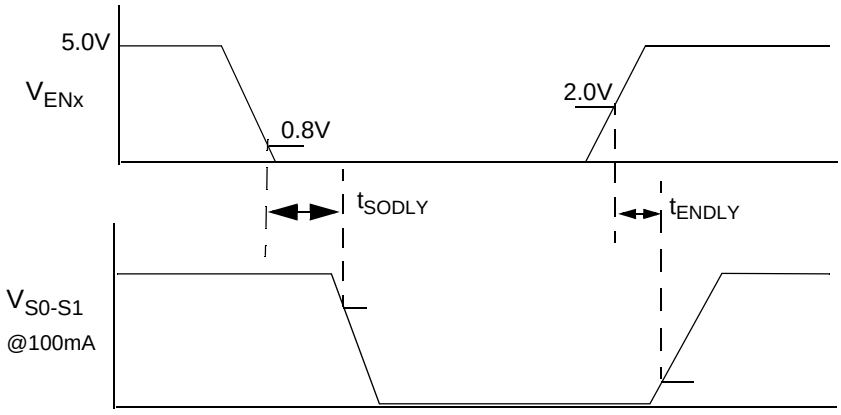


Figure 5. Shut Off and Enable Delay

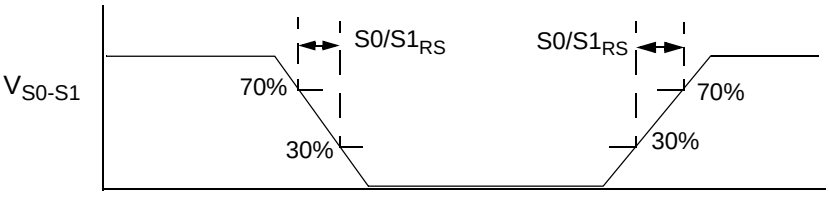


Figure 6. Slew Time Measurement

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33899 is a programmable H-Bridge, power integrated circuit (IC) designed to drive DC motors or bi-directional solenoid controlled actuators, such as throttle control or exhaust gas recirculation actuators. It is particularly well suited for the harsh environment found in automotive power train systems.

The key characteristic of this versatile driver is configurability. The selectable slew rate permits the customer to choose the slew rate needed for performance and noise suppression. The Serial Peripheral Interface (SPI) allows the system microprocessor to clear the fault register, select a programmable current limit and select the slew rate. A unique fault restart feature allows the part to be configured to maintain limited functionality even in the presence of some faults.

The 33899 is designed to drive a bi-directional DC motor using pulse-width modulation (PWM) for speed and torque control. A current mirror output provides an analog feedback signal proportional to the load current. SPI diagnostic reporting includes open circuit, short-to-battery, short-to-ground, die temperature range and under voltage.

FUNCTIONAL PIN DESCRIPTION

VIGNP INPUT (VIGNP)

VIGNP is the primary power input for the H-Bridge. The input voltage is 0 V to 26.5 V (40 V during a load dump transient). This pin must be externally protected against application of a reverse voltage (through an external inverted N-channel MOSFET, diode, or switched relay).

+5.0 V INPUT (VCC)

+5.0 V power input is required to power the internal analog circuitry and the +3.3 V internal regulator.

+3.3 V INPUT (VCCL)

A +3.3 V internal regulator powers the internal digital circuitry. The internal supply cannot be used as a power source by any other IC in the system. This output can be overdriven by an external supply. The internal supply requires a 0.47 μF capacitor on this output to insure proper startup sequencing when coming out of sleep mode.

LOGIC BIAS INPUT (VDDQ)

VDDQ supplies the level shifted bias voltage for the logic level outputs designed to be read by the microprocessor. This pin will apply the logic supply voltage to DO and LSCMP making the output logic levels compliant to logic systems from 3V to over 5V.

OUTPUTS (S1 AND S0)

The S1 and S0 outputs drive the bi-directional DC motor. Each output has two internal N-channel MOSFETs connected a half-bridge configuration between VIGNP and ground. Only one internal MOSFET is on at any one time for each output. The FWD, REV, and PWM inputs control the state of the H-Bridge. The turn on/off slew times are determined by the selected RS resistor value and the SPI slew time register contents (refer to Table 8, page 22).

OUTPUT POLARITY CONTROL (FWD/REV INPUTS)

The FWD and REV inputs determine the direction of current flow in the H-Bridge by directing the PWM input to one of the low-side MOSFETs (refer to Table 5). When a change in the current direction is commanded via the microprocessor, the PWM must switch from one low-side MOSFET to the other without shoot-through current in the H-Bridge. The gate voltage of the low-side MOSFETs must drop below and remain below the gate threshold voltage for the “dead time” before either of the high-side MOSFETs is commanded on. At no time are the high-side and low-side MOSFETs simultaneously on at the same side of the H-Bridge. The FWD and REV inputs have 50 μA pull-downs to ground that disable all the outputs should an open circuit condition occur.

Table 5. FWD/REV Truth Table

FWD	REV	Current Direction
0	0	Off
0	1	Reverse
1	0	Forward
1	1	Off

ENABLE INPUTS (EN1, EN2)

Logic [0] in either of the Enables (EN1 or EN2) disables all four of the output drivers (refer to Table 6). While either EN1 or EN2 is at logic [1], the 33899 is still capable of detecting open circuit and short circuit faults on all of the outputs interfacing with the external load(s). The EN1 and EN2 inputs have 50 μA pull-downs to ground that disable the outputs when open circuit conditions occur.

Table 6. Enable Truth Table

EN1	EN2	Status
0	0	Disabled (Sleep Mode)

EN1	EN2	Status
0	1	Disabled (Standby Mode)
1	0	Disabled (Standby Mode)
1	1	Enabled (Run Mode)

INPUT CONTROL OF H-BRIDGE (PWM)

The PWM input pin controls the sequencing of the PWM'ing high-side and low-side MOSFETs. A logic [1] commands the appropriate low-side MOSFET (M2 or M4) ON and the appropriate high-side MOSFET (M1 or M3) OFF. A logic [0] commands the appropriate low-side MOSFETs (M2 or M4) OFF and the appropriate high-side MOSFETs (M1 or M3) ON. The high- and low-side MOSFETs that are PWM'ed are determined by the commanded direction (FWD or REV).

If a shorted condition exists, the particular output MOSFET will be latched off after 5.0 μs to 10 μs. Subsequent PWM edges will retry to turn on the same MOSFET. Only when a thermal fault is reached are all outputs latched off until the clear fault bit is set by the microprocessor. Any PWM high-to-low-to-high pulse that is shorter than 500 ns keeps the low-side MOSFET from starting to turn off. The rising edge of this short pulse re-enables the low-side MOSFET if the pulse width is at least 200 μs long (if a short circuit latch-off had occurred during the previous positive PWM pulse). The PWM input has a 50 μA pull-down to ground that disables all the outputs should an open circuit condition occur.

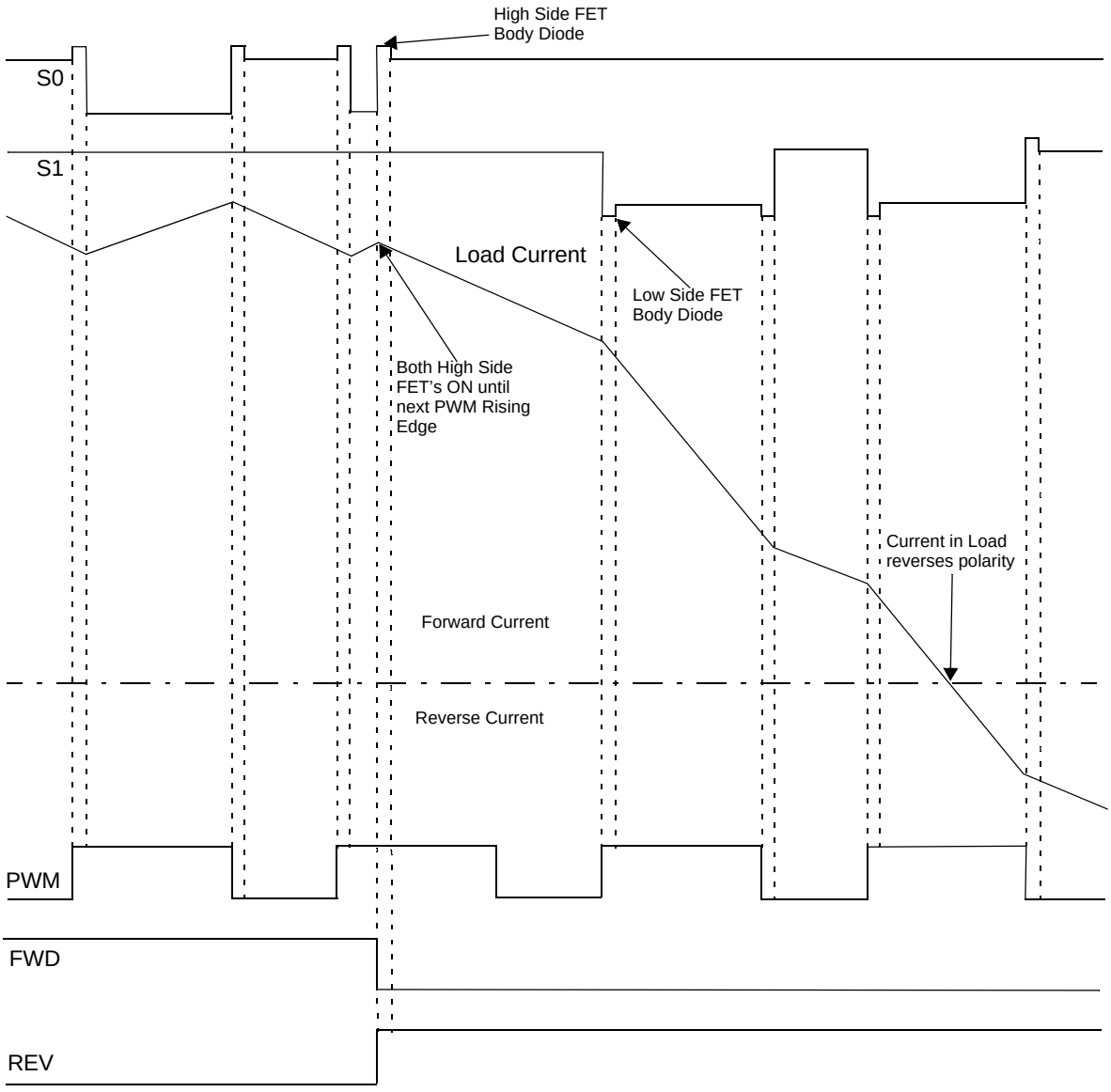


Figure 7. 33899 Operation in Current Reversal

LOAD CURRENT FEEDBACK (CSNS)

The load current sense circuit mirrors a sample of the load current back to the microcontroller via the CSNS pin. It supplies a current that is 1/400th of the load current (see Equation 1). An analog multiplexer routes the enabled high-side current to the CSNS pin. An external resistor connected to the CSNS pin (R_{CSNS}) sets current to voltage gain. The circuit operates properly in the presence of high-frequency noise. An external capacitor may be necessary to provide filtering.

$$V_{CSNS} = \frac{I_{OUT}}{400} \cdot R_{CSNS} \qquad \textbf{Eq. 1}$$

Note This output is clamped so that it will not exceed V_{CC}.

CHARGE PUMP RESERVOIR CAPACITOR (CRES)

The charge pump provides an output voltage over the full operating VIGNP range that is sufficient to drive the output MOSFETs and ensure that the output $R_{DS(ON)}$ specifications are met. An external reservoir capacitor of 0.1 μF is recommended. The charge pump operates at approximately 2.0 MHz to 4.0 MHz in order to prevent interference with AM entertainment radio.

HIGH-SIDE AND LOW-SIDE SLEW TIME CONTROL (RS)

The turn-on and the turn-off slew times on S0 and S1 (both low- and high-side drive outputs) are adjustable from 5.0 μs (50 kΩ RS) to 1.0 μs (10 kΩ RS) to reduce high-frequency harmonic energy in the vehicle's wiring harness. In addition, slew time control is programmable to be either 1X, 2X, or 4X (via the SPI) to lower power dissipation at elevated die temperatures. The characteristics of the turn-on and turn-off voltage are linear, with no discontinuities, during the output driver state transitions. If the RS pin detects an impedance of less than 5.0 kΩ to ground or greater than 1.0 MΩ to ground, it defaults to the fastest slew time of 1.0 μs.

LOW-SIDE COMPARATOR ONE SHOT OUTPUT (LSCMP)

The LSCMP output pin pulses high for 5 μs to 10 μs any time the low-side comparator is tripped. Then the output goes low during a 5 μs to 10 μs blanking time. If another low-side comparator trip event is detected during the blanking time, another 5 μs to 10 μs pulse high occurs immediately after the blanking interval.

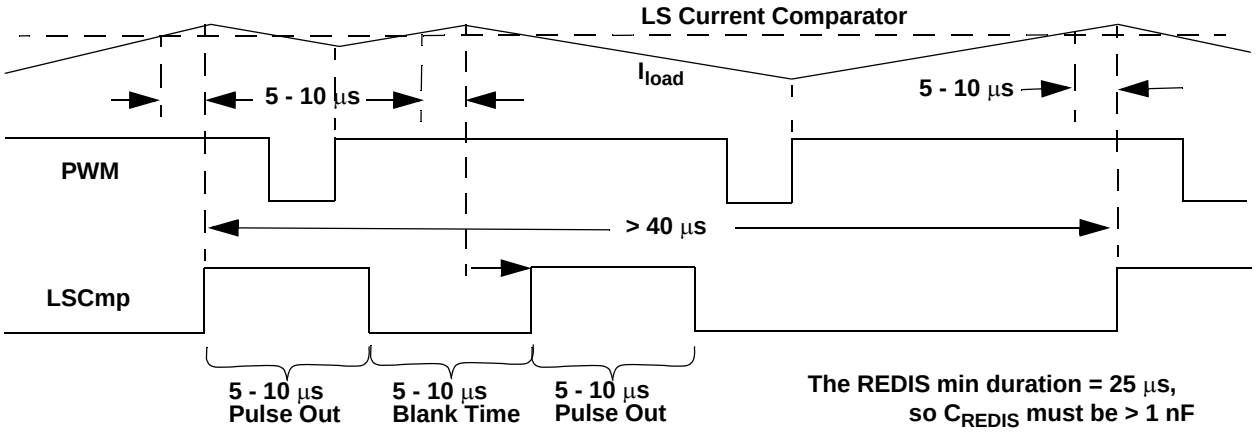


Figure 8. LS Current Comparator One Shot

AUTOMATIC OUTPUT RE-ENABLE DISABLE (REDIS)

The REDIS input pin automatically re-enables the low-side MOSFET once the REDIS input voltage exceeds 4.0 V. An external capacitor (C_{REDIS}) determines the time interval (see Equation 2). Once a low-side current comparator is tripped, a 120 μA current source linearly charges the capacitor until either the next rising edge of PWM or the 4.0 V trip level is achieved. This re-enables the low-side output MOSFET and discharges the capacitor to 0 V. This feature is disabled by grounding this input.

$$dt = \frac{C_{REDIS} \cdot dv}{I} = \frac{C \cdot 4.0\ V}{120\ \mu A} \qquad \textbf{Eq. 2}$$

As per the above equation, a 2.2 nF capacitor will provide a nominal 75 μs time interval.

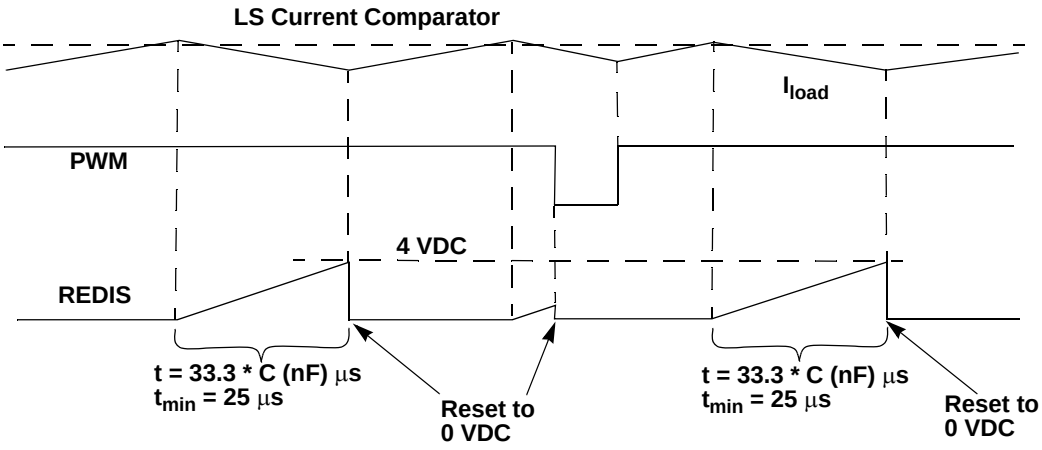


Figure 9. Re-enable after a Low Side Current Comparator Trip

LOW-SIDE CURRENT COMPARATOR VS. CURRENT LIMIT LEVELS

There are two different current limit thresholds for the low-side MOSFETs: current comparator and current limit. Current comparator is the normal commanded switching current. Current limit is for fault protection.

The inductance of the load results in just the current comparator tripping. Once the low-side current comparator has tripped and filter time expired, the low-side MOSFET turns off and the high-side MOSFET subsequently turns on for normal current re-circulation in the load. If an actual hard short to either VIGNP or ground on the S0/S1 outputs is encountered, the current limit kicks in and prevents large current spikes from VIGNP (or to ground) to occur. The threshold level of the current comparator vs. the high- and low-side current limits is given in the Static Electrical Characteristics table, page 8.

As backup protection, there is a linear overcurrent controller to limit current spike during timer operations.

SERIAL PERIPHERAL INTERFACE (SPI)

The 33899 has a serial peripheral interface consisting of Chip Select ($\overline{CS}$), Serial Clock (SCLK), Serial Data Out (DO), and Serial Data In (DI). This device is configured as a SPI slave and is daisy-chainable (single $\overline{CS}$ for multiple SPI slaves).

CHIP SELECT ($\overline{CS}$)

The $\overline{CS}$ is a low = true input that selects this device for serial transfers. On the falling edge of $\overline{CS}$, the DO pin is released from tri-state mode, and all status information is latched in the SPI shift register. While $\overline{CS}$ is asserted, register data is shifted into the DI pin and shifted out of the DO pin on each subsequent SCLK. On the rising edge of $\overline{CS}$, the DO pin is placed in a high impedance state and the Fault register reloaded (latched) with the current filtered status data. To allow sufficient time to reload the Fault register, the $\overline{CS}$ pin must remain low for a minimum of t_{CSN} prior to going high again.

By design, the $\overline{CS}$ input is immune to spurious pulses of 50 ns or shorter. (DO may come out of tri-state, but no status bits are cleared and no control bits are changed.)

The $\overline{CS}$ input has a 50 µA current source to VCC, which pulls this pin to V_{CC} if an open circuit condition occurs. This pin has TTL-level compatible input voltages, which allows proper operation with microprocessors using a 3.0 V to 5.0 V supply.

SERIAL CLOCK (SCLK)

The SCLK input is the clock signal input for synchronization of serial data transfer. This pin has TTL-level compatible input voltages, which allow proper operation with microprocessors using a 3.3 V to 5.0 V supply.

When $\overline{CS}$ is asserted, both the microprocessor and the 33899 latch input data on the rising edge of SCLK. The SPI master typically shifts data out on the falling edge of SCLK, while the 33899 shifts data out on the falling edge of SCLK to allow more time to drive the DO pin to the proper level.

SERIAL DATA OUTPUT (DO)

The DO is the SPI data out pin. When $\overline{CS}$ is asserted (low), the MSB is the first bit of the word transmitted on DO and the LSB is the last bit of the word transmitted on DO. After all 8 bits of the fault register are transmitted, the DO output sequentially transmits the digital data that was just received on the DI pin. This allows the processor to distinguish a shorted DI pin condition. The DO output continues to transmit

the input data from the DI input until $\overline{CS}$ eventually transitions from a logic [0] to a logic [1].

The DO output pin is in a high impedance condition unless $\overline{CS}$ is low, at least one enable pin is high and VCC and VCCL are within the normal operating range. When active, the output is “rail to rail”, depending on the voltage at the VDDQ pin.

SERIAL DATA INPUT (DI)

The DI input takes data from the microprocessor while $\overline{CS}$ is asserted (low). The MSB is the first bit of each word received on DI and the LSB is the last bit of each word received on DI. The 33899 serially wraps around the DI input bits to the DO output after the DO output transmits its fault flag bits. The first 8 bits before $\overline{CS}$ goes high are latched into the Control register. Any bytes transmitted before the last 8 bits are just wrapped around to the DO output and are not used by the 33899 (see Figure 10).

This pin has TTL-level compatible input voltages, which allow proper operation with microprocessors using a 3.3 V to 5.0 V supply.

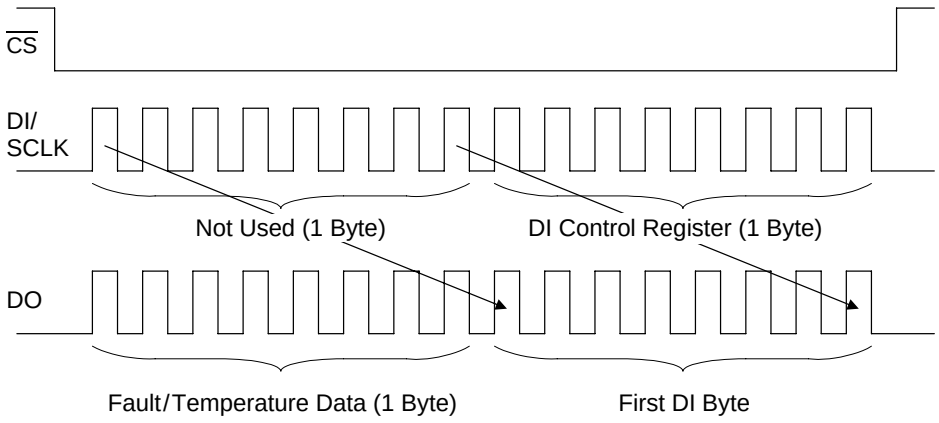


Figure 10. SPI Operation with Extended $\overline{CS}$

LOGIC OUT BIAS (VDDQ)

The VDDQ input pin provides the bias voltage for the data out buffer and LS Comparator. It must be connected to the same power supply that is used by the microprocessor’s SPI I/O.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

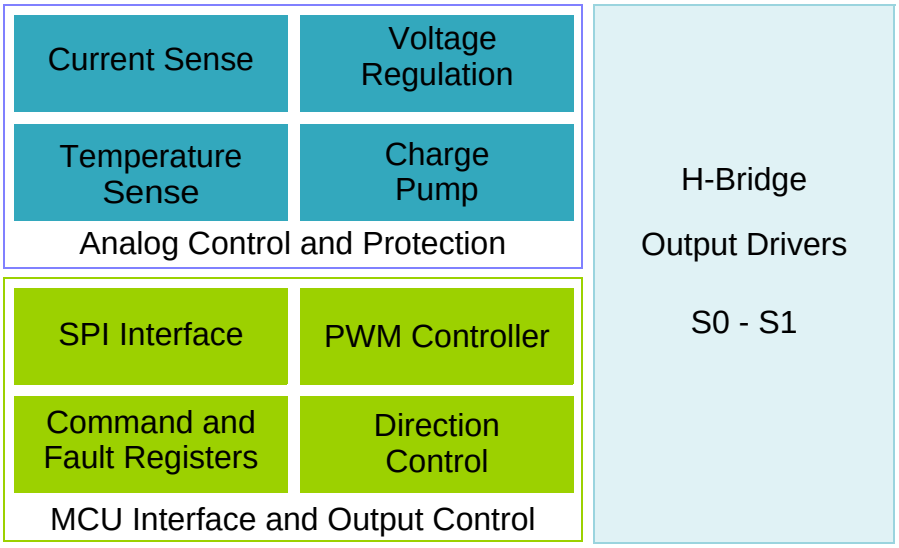


Figure 11. Functional Block Diagram

INTRODUCTION

H-BRIDGE OUTPUT DRIVERS (S0 AND S1)

The 33899 Power IC provides the means to efficiently drive a DC motor in both forward and reverse shaft rotation via a monolithic H-Bridge comprising low $R_{DS(ON)}$ N-channel MOSFETs and integrated control circuitry. The switching action of the H-Bridge can be pulse-width modulated to obtain both torque and speed control, with PWM frequencies up to 11 kHz supported with minimal switching losses.

The outputs comprise four Power MOSFETs configured as a standard H-Bridge, controlled by the PWM input and the FWD and REV inputs.

ANALOG CONTROL AND PROTECTION

The 33899 has integrated voltage regulators which supply the logic and protection functions internally. This reduces the requirements for external supplies and insures the device is safely controlled at all times when battery voltage is applied.

An integrated charge pump provides the required bias levels to insure the output MOSFETs turn fully ON when commanded.

Each MOSFET provides feedback to the protection circuitry by way of a current sensor. Each sense signal is compared with programmable over-current levels and produces an immediate shutdown in case of a high current short circuit. The low-side current sense is also capable of producing a current limiting PWM to reduce overload conditions as determined by the programmable limits. The high-side current sense is available to the MCU as an analog current proportional to the load current.

Each MOSFET has over-temperature protection circuitry that disables the device. A thermal warning sets a flag in the SPI register when the device is approaching a protection limit.

MCU INTERFACE AND OUTPUT CONTROL

The SPI and control logic signals are compatible with both 5V and 3.3V logic systems.

The SPI provides programmable control of output slew rate and current limits. The status register makes detailed diagnostics available for protective and warning functions.

The output drivers are controlled by the input signals EN1, EN2, FWD, REV, and PWM.

The low-side and high-side MOSFETs connected to S0 are controlled by the PWM input when FWD is a logic [1] and REV is a logic [0]. The low-side MOSFET connected to S1 is idle in this state. The high-side MOSFET connected to S1 is statically ON in the forward direction. The low-side and high-side MOSFETs connected to S1 are controlled by the PWM input when FWD is a logic [0] and REV is a logic [1]. The low-side MOSFET connected to S0 is idle in this state. The high-side MOSFET connected to S0 is statically ON in the reverse direction. To reduce power during the recirculation period, the upper recirculation MOSFET is turned on synchronously with the OFF-time of the low-side MOSFET.

The PWM input is connected to the system microprocessor and provides for control of the four MOSFET outputs. The PWM duty cycle range is 0% to 100%; however, open load detection circuits require a minimum off-time.

The 33899 holds all outputs off if both FWD and REV are either logic [0]s or logic [1]s. Figure 12 depicts inputs versus outputs in forward mode operation.

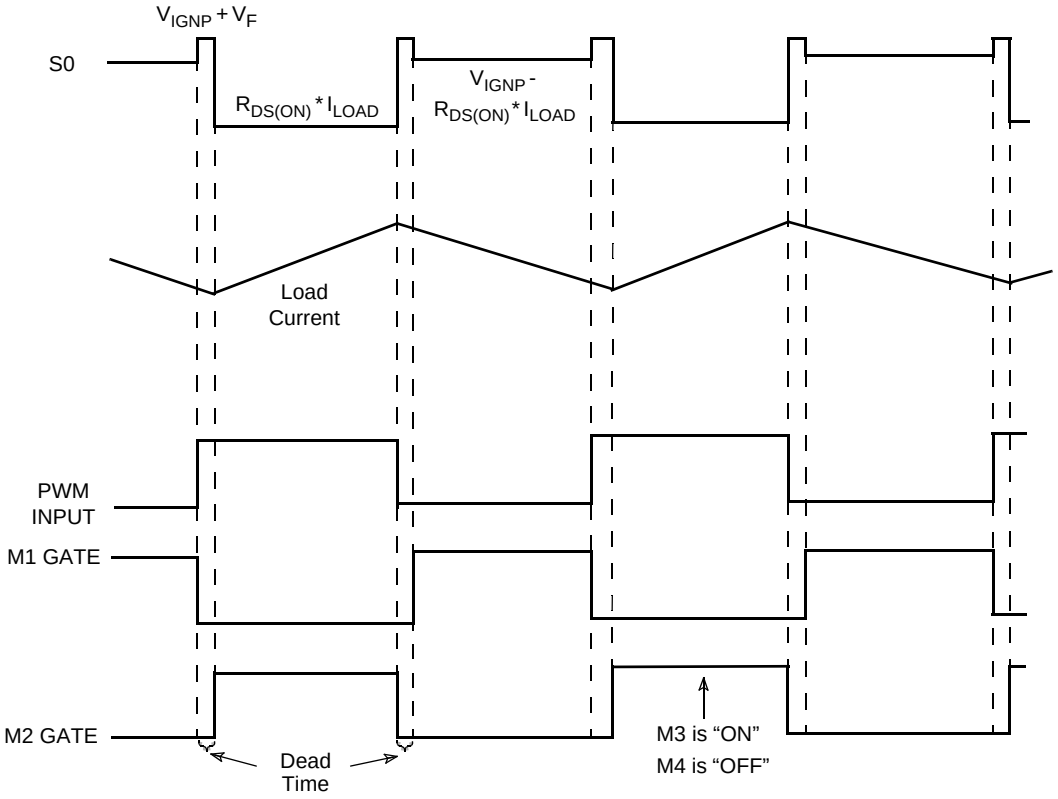


Figure 12. 33899 Operation in Forward Mode

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

Short-to-GND or Short-to-VIGNP Fault Filtering

The 33899 has a short-to-GND and short-to-VIGNP digital fault filter. After a single fault occurrence, another 7 shorts consecutive with PWM must be detected before the bit is latched into the fault register.

Short to -1.0 V on Output Devices

The 33899 can survive a short to -1.0 V through a 300 mΩ impedance (10 kHz to 1000 kHz) and a direct short to -0.5 V on all I/Os that exit the module. A shorted output to these voltages does not impact correct fault diagnostics for the effected channel or any other normal operation of the 33899. This feature applies to the SO and S1 outputs as well.

Loss of Module Ground

Loss of ground condition at the parts level denotes that all pins of the 33899 see very low impedance to ignition. In the application, a loss of ground condition results in all I/O pins floating to ignition voltage V_{IGNP}, while all externally referenced I/O pins are at worst case pulled to ground.

Loss of Module Ignition Supply

Loss of ignition condition at the parts level denotes that the power input pins of the 33899 see infinite impedance to the ignition supply voltage (depending on the application) but there is some undefined impedance from these pins to ground.

Output Driver Load(s)

The 33899 is capable of driving any PWM'ed inductive load of up to 3.5 A of continuous average current (at a maximum frequency of 11 kHz) with current feedback capability. The 33899 drives ETC (Electronic Throttle Control) motors. The typical characteristics of the ETC motor are as follows:

- **Resistance** 1.25 Ω to 2.4 Ω (lumped resistance due to actuator, harness, and connectors) over the temperature range.
- **Inductance** 800 μH at 1000 Hz over the temperature range.

Output Power Density

The die area for the output MOSFETs provides an adequate thermal resistance to limit junction temperature to 150°C when the device is operated at 11 kHz, 3.5 A continuous average current, and a 2.0 ms nominal transition time. This applies to FR4 PC board with a metal pedestal under the device, which provides a thermal path to the case of the module.

Output Synchronous Rectification Control

The 33899 uses synchronous rectification to reduce the power dissipation during the recirculation period. In order to prevent shoot-through current, the 33899 has a dead time circuit that turns on the upper recirculation MOSFET after the lower gate voltage falls below the threshold voltage and turns it off before the lower gate voltage rises above the threshold voltage.

Output Overvoltage Shutdown

The 33899 disables all MOSFET outputs when V_{IGNP} is above the overvoltage shutdown threshold for a time period greater than t_{OVS} (refer to Dynamic Electrical Characteristics table, page 9).

Output Avalanche Protection

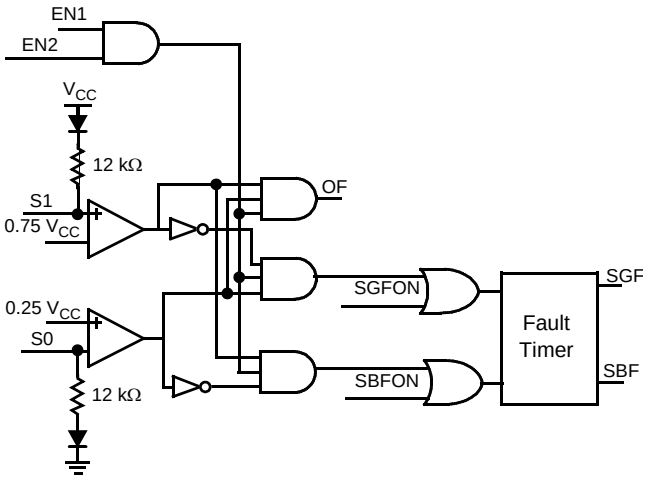
An inductive fly-back event, namely when the outputs are suddenly disabled and V_{IGNP} is lost, could result in electrical overstress of the drivers. To prevent this the V_{IGNP} input to the 33899 should not exceed 40 V during a fly-back condition. A zener clamp and/or an appropriately valued capacitor are common methods of limiting the transient.

Power-ON Reset (POR)

On power-up, the VCC and VCCL supplies to the 33899 typically increase to 5.0 V and 3.3 V, respectively, within 0.3 ms to 3.0 ms. The 33899 has power-ON reset (POR) circuitry that monitors both the VCC and VCCL voltages. When either voltage falls below its POR threshold, the S0 and S1 outputs are driven to the inactive state. When both voltages rise above the POR threshold, the outputs are enabled. During POR none of the outputs momentarily glitches ON. The contents of all SPI registers (both DI and DO) are cleared on each power-ON reset cycle. See +3.3 V Input (V_{CCL}) on page 12 for part requirements to guarantee normal operation.

Fault Detection

Open load detection is performed in the OFF state, and short circuit fault detection is performed while the H-Bridge circuit(s) are enabled (see Figure 13, page 20). However, the user can determine whether an open circuit has caused the output current to go to 0 A via the CSNS output. All valid faults are latched into the SPI Fault register and cleared when a logic [1] is written to the FLTCLR bit by the system microprocessor (refer to Table 8, page 22).



Note SGFON and SBFON are ON-State Fault.

Figure 13. OFF-State Fault Detection Diagram

In the full or half H-Bridge mode an open, short to ignition, or short to GND latches the appropriate SPI fault bits until the FLTCLR bit is set. Any additional faults that occur prior to setting FLTCLR will be ignored.

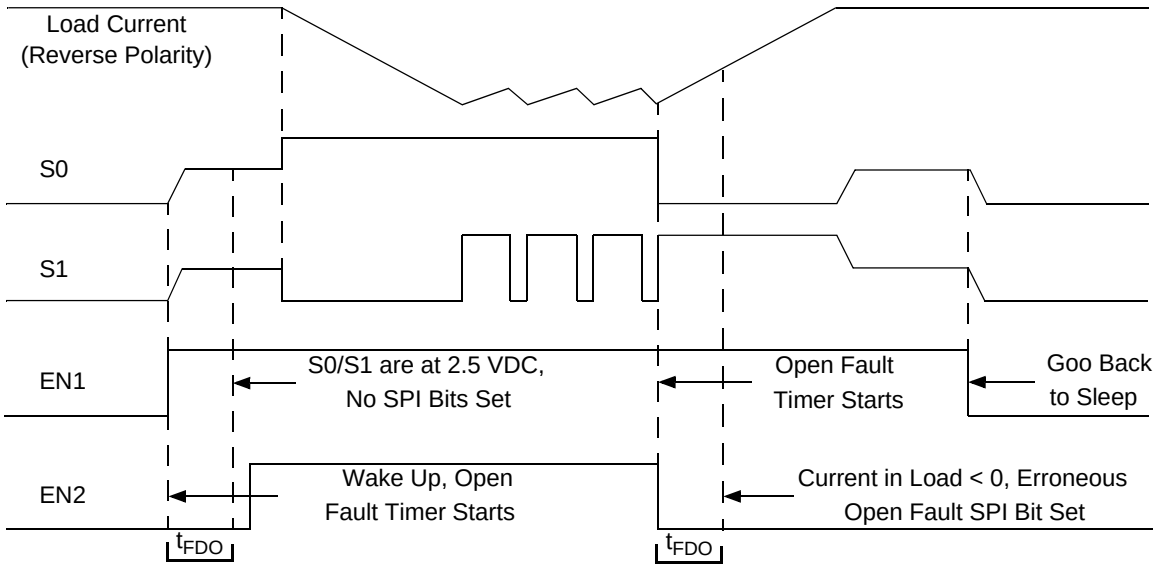
Fault Detection During OFF State

Fault detection for both the high-side and low-side outputs is done during the OFF state, when either the EN1 or EN2 pin is a logic [1], by analyzing the states of both the high-side and low-side outputs interacting to the external load. S1 is pulled up internally via a high-impedance pullup to V_{CC}, while S0 is pulled down internally to ground. In a normal load state, the low impedance (relative to the internal pull-ups/pull-downs) will force both load connections to about 0.5 V_{CC}. S1 is compared with an internal reference of 0.75 V_{CC} nominally, while S0 is compared to an internal reference of 0.25 V_{CC} nominally. Table 7 indicates what status the load will be in based on the combination of the outputs of these two comparators.

Table 7. OFF-State Fault Detection

S1	S0	Load Status
<0.75 V_{CC}	>0.25 V_{CC}	Normal Load
<0.75 V_{CC}	<0.25 V_{CC}	Short to Ground
>0.75 V_{CC}	<0.25 V_{CC}	Open Load
>0.75 V_{CC}	>0.25 V_{CC}	Short to VIGNP

Once any of the above faults are indicated for a period of time exceeding the OFF-state fault timer, the fault bit will be latched into the SPI Fault register. The OFF-state fault timer is started when either the EN1 or EN2 pin transitions from a logic [1] to a logic [0] (both inputs previously logic [1]) or from a logic [0] to a logic [1] (both inputs previously logic [0]). The OFF-state filter time is substantially longer than the ON-state to allow energy in the load to dissipate. False open state faults may be set when the outputs are shut down and the load current (reverse polarity only) takes more than the OFF-state filter time to decay to zero. The microprocessor should clear the open state fault SPI bit and read the Fault register again under this condition.



Fault Detection During ON State

While the H-Bridge circuit is in operation (i.e., when a high-side MOSFET is ON), the 33899 is capable of detecting both shorts to VIGNP and shorts to ground. A short will cause the appropriate MOSFETs to current limit. The current limit is active for numerous retry periods until an overtemperature condition is reached, at which time all outputs are turned OFF.

All ON-state faults must be present for a period of time that exceeds the fault time before the 33899 will consider them valid. Once they are valid, they are latched until the SPI has reported these faults to the microcontroller via the DO pin and a logic [1] is written to the FLTCLR bit.

In order for the user to be certain that all detectable ON-state faults have been reported, a minimum ON time is required for the low-side MOSFET. For example, if the PWM frequency is 11 kHz, ON-state fault detection would not be guaranteed for duty cycles of less than 11%.

Thermal Shutdown

The H-Bridge has thermal protection circuitry. A thermal fault sets the thermal shutdown bits (and any other faults that may be present at that time) and latches off. The H-Bridge will remain disabled until the microprocessor sets the FLTCLR bit (refer to Table 8, page 22).

LOGIC COMMANDS AND REGISTERS

SPI INTERFACE AND REGISTER DESCRIPTION

SPI Control Register Definition

An 8-bit SPI allows the system microprocessor to clear the Fault register, select a programmable current limit, and select a 1X, 2X, or 4X slew rate. The SPI Control Register bit definitions are shown in Table 8.

Note At POR, all bits in the register are cleared to 0s.

Table 8. SPI Control Register Bit Definitions

8 (MSB)	7	6	5	4	3	2	1 (LSB)
FLTCLR	Not Used	Not Used	Not Used	Current Limit	Current Limit	Slew Time	Slew Time

Bit 8: FLTCLR: 0 = Retain faults; 1 = Clear faults
Bit 7: Not used
Bit 6: Not used
Bit 5: Not used
Bits 4–3: Set Low Side Current Comparator Limits
00 = 4.0 A
01 = 5.0 A
10 = 6.0 A
11 = 8.5 A
Bits 2–1: Slew Time
00 = 1X
01 = 2X
10 = 4X
11 = 4X

SPI Fault Register Definition

The fault diagnostic capability consists of one internal 8-bit Fault register. Table 9 shows the content of the Fault register. The output load status of the H-Bridge circuit is reported via the output DO SPI bits. In addition to output fault information, die temperature warnings and overtemperature conditions are reported.

An SPI read cycle is limited by a $\overline{CS}$ logic [1] to logic [0] transition, followed by 8 SCLK cycles to shift the fault register bits out the DO pin. The rising edge of $\overline{CS}$ sets DO in a high impedance mode and clears the fault latches if the FLTCLR bit is set. The thermal fault is immediately set again if the fault condition is still present. Accurate fault reporting can only be obtained by reading the DO line at intervals greater than the fault timer. A thermal fault will be latched as soon as it occurs.

Note At POR, all bits in the register are cleared to 0s.

Table 9. SPI Fault Register Bit Definitions

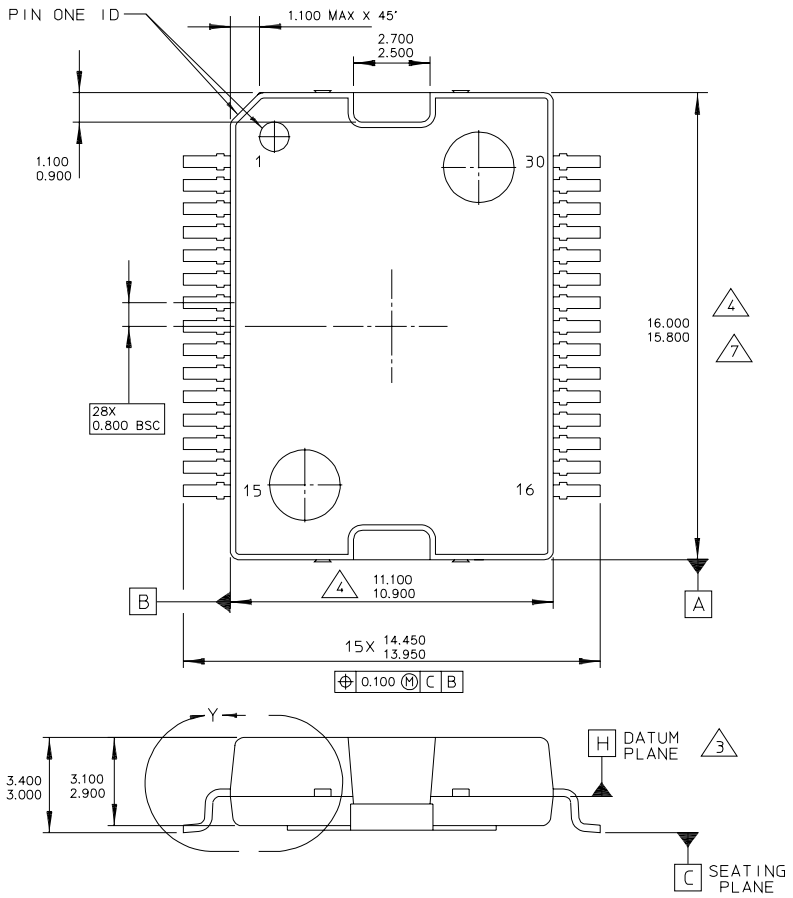
8 (MSB)	7	6	5	4	3	2	1 (LSB)
ShVIGNP	ShGnd	Open Fault	Overvoltage or Undervoltage	LS Comparator	EN1, EN2 Status	Die Temp	Die Temp

Bit 8: Short to VIGNP: 0 = No fault; 1 = S1 or S0 shorted to VIGNP (Low-Side Linear Current Limit has tripped)
Bit 7: Short to Ground: 0 = No fault; 1 = S1 or S0 shorted to GND (High-Side Linear Current Limit has tripped)
Bit 6: Open Fault: 0 = No fault; 1 = S1 or S0 is Open Circuited
Bit 5: Overvoltage or Undervoltage: 0 = No fault; 1 = Overvoltage/undervoltage fault
Bit 4: Low-Side Comparator: 0 = No trip; 1 = Tripped
Bit 3: XOR function of EN1, EN2 inputs. 0 = (EN1 same logic level as EN2). 1 = (EN1 not same logic level as EN2).
Bits 2–1: Die Temperature
00 = T < 140°C
01 = 140°C < T < Overtemperature Shutdown
10 = Not Defined
11 = Overtemperature Shutdown (Latched Off)

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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	CASE NUMBER: 979B-02	09 MAR 2005
	STANDARD: NON-JEDEC	

VW SUFFIX
30-PIN HSOP
98ASH70693A
ISSUE A

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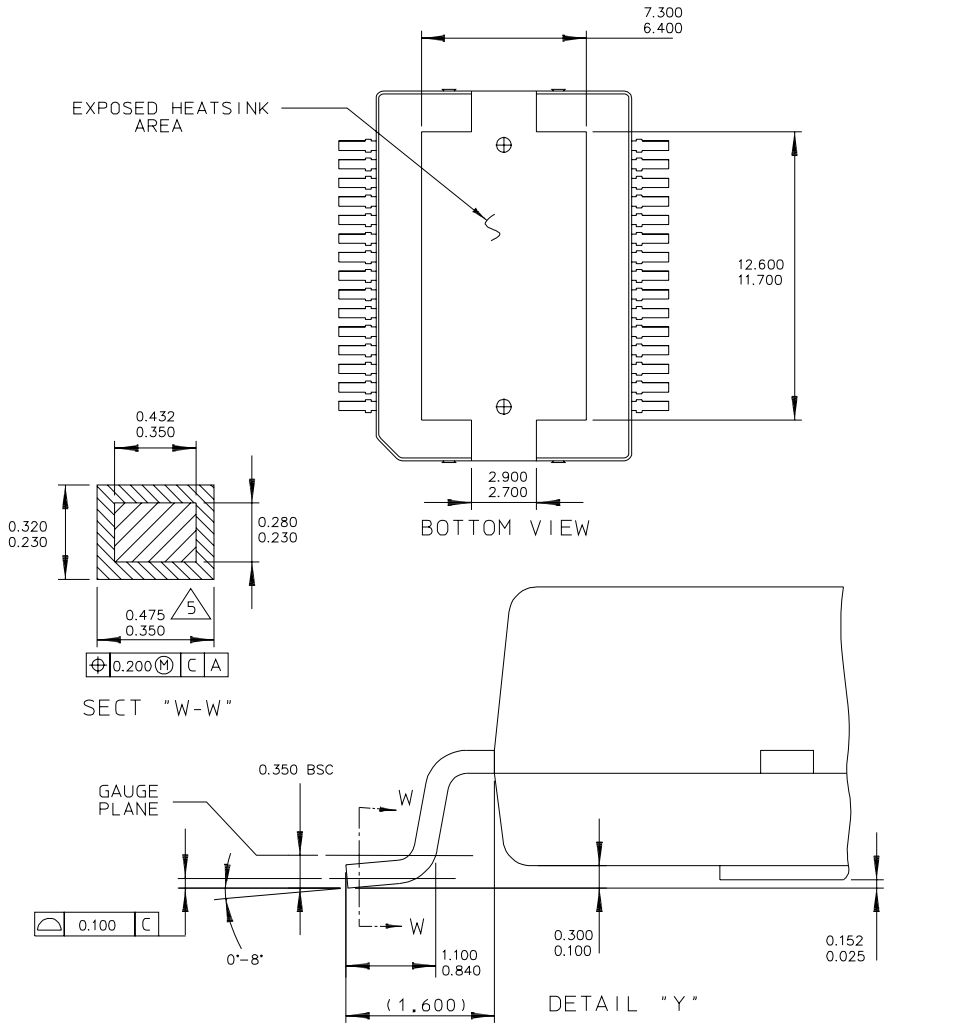

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	CASE NUMBER: 979B-02	09
	STANDARD: NON-JEDEC	

VW SUFFIX
30-PIN HSOP
98ASH70693A
ISSUE A

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	6/2006	• Initial Release

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www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
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Tai Po, N.T., Hong Kong
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MC33899
Rev. 2.0
6/2007

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