



# OKI Semiconductor

## FEDR27V12800J-02-06

Issue Date: Jul. 9, 2004

## MR27V12800J

 $8M-Word \times 16$ -Bit or  $16M-Word \times 8$ -Bit P2ROM

#### **FEATURES**

- $\cdot 8,388,608$ -word  $\times$  16-bit/16,777,216-word  $\times$  8-bit electrically switchable configuration
- · 3.0 V to 3.6 V power supply
- · Access time 80 ns MAX (MR27V12800J-xxxTN) 100 ns MAX(MR27V12800J-xxxTNE)
- · Operating current 25 mA MAX(5MHz)
- · Standby current 10 µA MAX
- · Input/Output TTL compatible
- · Three-state output

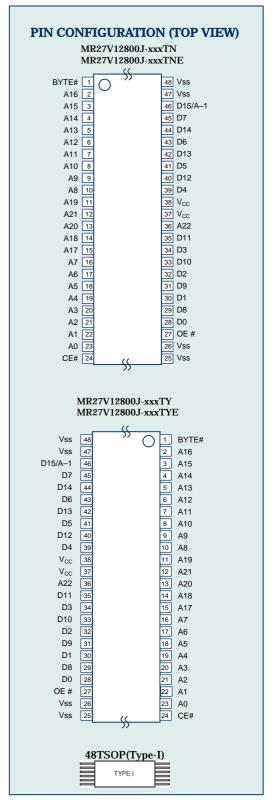
#### **PACKAGES**

- · MR27V12800J-xxxTN, MR27V12800J-xxxTNE 48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)
- · MR27V12800J-xxxTY, MR27V12800J-xxxTYE 48-pin plastic TSOP (TSOP I 48-P-1220-0.50-L)

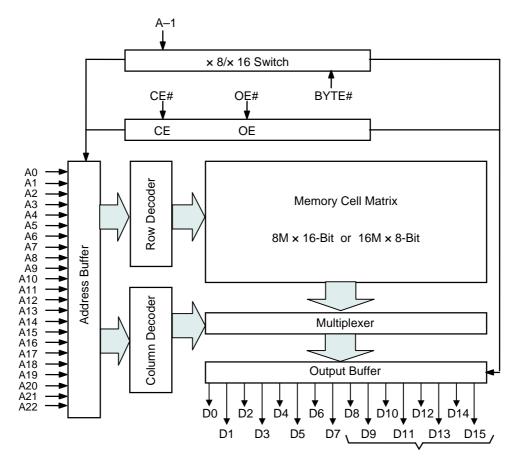
#### P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- Short lead time, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- No mask charge, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- No additional programming charge, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- Custom Marking is available at no additional charge.
- · Pin Compatible with Mask ROM



## **BLOCK DIAGRAM**



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

## PIN DESCRIPTIONS

Pin name	Functions			
D15 / A-1	Data output / Address input			
A0 to A22	Address inputs			
D0 to D14	Data outputs			
CE#	Chip enable input			
OE#	Output enable input			
BYTE#	Word / Byte select input			
Vcc	Power supply voltage			
V <sub>SS</sub>	Ground			

## **FUNCTION TABLE**

Mode	CE#	OE#	BYTE#	V <sub>CC</sub>	D0 to D7	D8 to D14	D15/A-1
Read (16-Bit)	L	L	Н			D <sub>OUT</sub>	
Read (8-Bit)	L	L	L	201/	D <sub>OUT</sub>	Hi–Z	L/H
Outrast districts			Н	3.0 V		Hi–Z	
Output disable	able L H —		L	to 3.6 V		*	
Standby	Н	*	Н	3.0 V		LI: 7	
			L		Hi–Z		*

<sup>\*:</sup> Don't Care (H or L)

#### **ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Та		0 to 70	°C
Storage temperature	Tstg	_	-55 to 125	°C
Input voltage	Vı		-0.5 to V <sub>CC</sub> +0.5	V
Output voltage	Vo	relative to V <sub>SS</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Power supply voltage	V <sub>CC</sub>		–0.5 to 5	V
Power dissipation per package	P <sub>D</sub>	Ta = 25°C	1.0	W
Output short circuit current	los	_	10	mA

#### RECOMMENDED OPERATING CONDITIONS

 $(Ta = 0 \text{ to } 70^{\circ}C)$ 

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
V <sub>CC</sub> power supply voltage	V <sub>cc</sub>		3.0	_	3.6	V
Input "H" level	V <sub>IH</sub>	$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$	2.2	_	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>		-0.5**	_	0.6	V

### Voltage is relative to $V_{\text{SS}}$ .

- \* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
- \*\*: -1.5V(Min.) when pulse width of undershoot is less than 10ns.

#### PIN CAPACITANCE

 $(V_{CC} = 3.0 \text{ V}, Ta = 25^{\circ}\text{C}, f = 1 \text{ MHz})$ 

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input	C <sub>IN1</sub>	V <sub>1</sub> = 0 V	_	_	8	
BYTE#	C <sub>IN2</sub>	V <sub>1</sub> = 0 V	_	_	200	pF
Output	C <sub>OUT</sub>	$V_O = 0 V$	_	_	10	

#### **ELECTRICAL CHARACTERISTICS**

#### **DC** Characteristics

 $(V_{CC} = 2.7 \text{ to } 3.6 \text{ V}, \text{Ta} = 0 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_I = 0$ to $V_{CC}$	_		5	μА
Output leakage current	I <sub>LO</sub>	$V_O = 0$ to $V_{CC}$	_	_	5	μА
V <sub>CC</sub> power supply current	I <sub>ccsc</sub>	CE# = V <sub>CC</sub>	_	_	10	μА
(Standby)	Iccst	CE# = V <sub>IH</sub>	_	_	1	mA
V <sub>CC</sub> power supply current	1	CE# = V <sub>IL</sub> , OE# = V <sub>IH</sub>			25	Λ
(Read)	I <sub>CCA</sub>	f=5MHz			25	mA
Input "H" level	V <sub>IH</sub>	_	2.2	_	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>	_	-0.5**	_	0.6	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> = −1 mA	2.4	_	_	V
Output "L" level	V <sub>OL</sub>	$I_{OL} = 2 \text{ mA}$	_	_	0.4	V

#### Voltage is relative to V<sub>SS</sub>.

- \* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
- \*\*: -1.5V(Min.) when pulse width of undershoot is less than 10ns.

#### **AC Characteristics**

Note 1  $\rightarrow$  MR27V12800J-xxxTN, MR27V12800J-xxxTY

Note 2  $\rightarrow$  MR27V12800J-xxxTNE, MR27V12800J-xxxTYE

 $(V_{CC} = 3.0 \text{ to } 3.6 \text{ V}, Ta = 0 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min.	Max.	Unit
Address avalatima	4 -		80 (Note 1)		200
Address cycle time	t <sub>C</sub>	_	100 (Note 2)	_	ns
A alabana a a a a a a a 4 i a a a		OF# OF# V		80 (Note 1)	ns
Address access time	t <sub>ACC</sub>	CE# = OE# = V <sub>IL</sub>	_	100 (Note 2)	
OF# time	t <sub>CE</sub>	OE# = V <sub>IL</sub>		80 (Note 1)	
CE# access time			_	100 (Note 2)	ns
OE# access time	t <sub>OE</sub>	CE# = V <sub>IL</sub>	_	30	ns
Output diaable time	t <sub>CHZ</sub>	OE# = V <sub>IL</sub>	0	20	ns
Output disable time	t <sub>OHZ</sub>	CE# = V <sub>IL</sub>	0	20	ns
Output hold time	t <sub>OH</sub>	CE# = OE# = V <sub>IL</sub>	0	_	ns

#### Measurement conditions

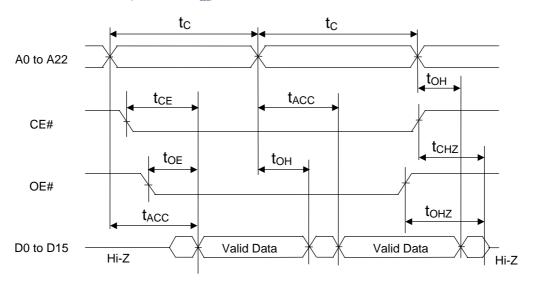
Input signal level ------0 V/3 V Input timing reference level------50 pF Output timing reference level -------1/2Vcc

#### Output load

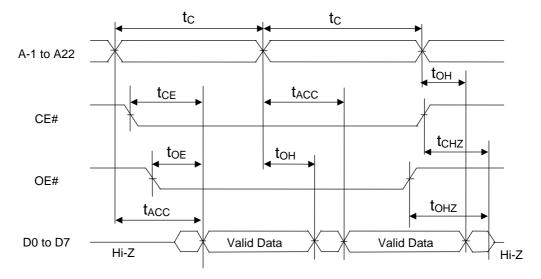


## TIMING CHART (READ CYCLE)

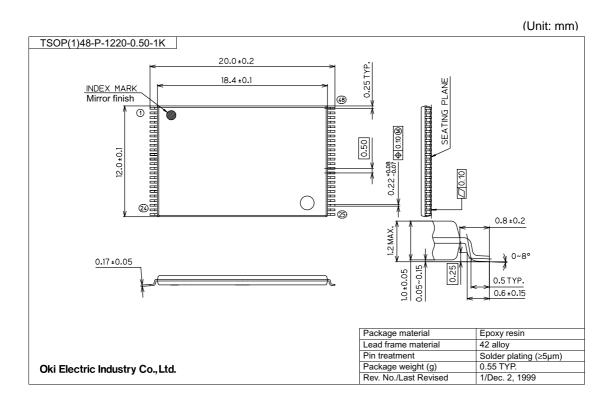
## 16-Bit Read Mode (BYTE# = $V_{IH}$ )



## 8-Bit Read Mode (BYTE# = $V_{IL}$ )



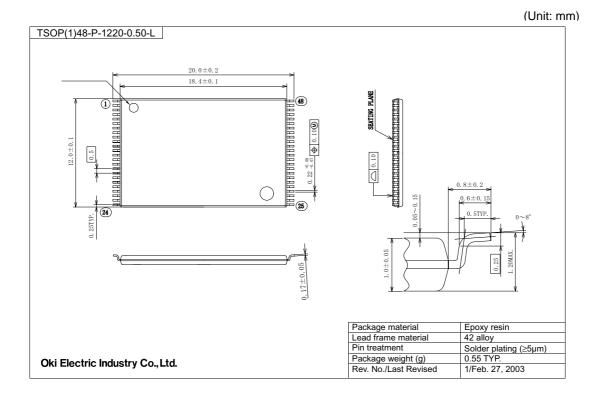
#### PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



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## **REVISION HISTORY**

Document		Page		
No.	Date	Previous Edition	Current Edition	Description
FEDR27V12800J-02-01	July. 2002	_	ı	Final edition 1
FEDR27V12800J-02-02	Jan. 2003	1, 4	1, 4	Change tC, tACC, tCE to 100ns
FEDR27V12800J-02-03	Jan. 2003	1	1	Change P/N to MR27V12800J-xxxTNE
FEDR27V12800J-02-04	Mar. 10, 2003	1, 4	1, 4	Added MR27V12800J-xxxTN
FEDR27V12800J-02-05	Jun. 6, 2003	1, 3, 4	1, 3, 4	Change Ta to 0°C     Added MR27V12800J-xxxTY,TYE
FEDR27V12800J-02-06	Jul. 9, 2004	3	3	Add P <sub>D</sub> condition and I <sub>OS</sub> = 10mA

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