

OKI semiconductor

MSC23B136D-xxBS4/DS4

1,048,576 Word By 36 Bit DYNAMIC RAM MODULE : FAST PAGE MODE

GENERAL DESCRIPTION

The Oki MSC23B136D-xxBS4/DS4 is a fully decoded, 1,048,576 word X 36 bit CMOS dynamic random access memory composed of two 16Mb(1Mx16) DRAMs and two 2Mb(1Mx2) DRAMs in SOJ.

The mounting of four DRAMs together with decoupling capacitors on a 72-pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required.

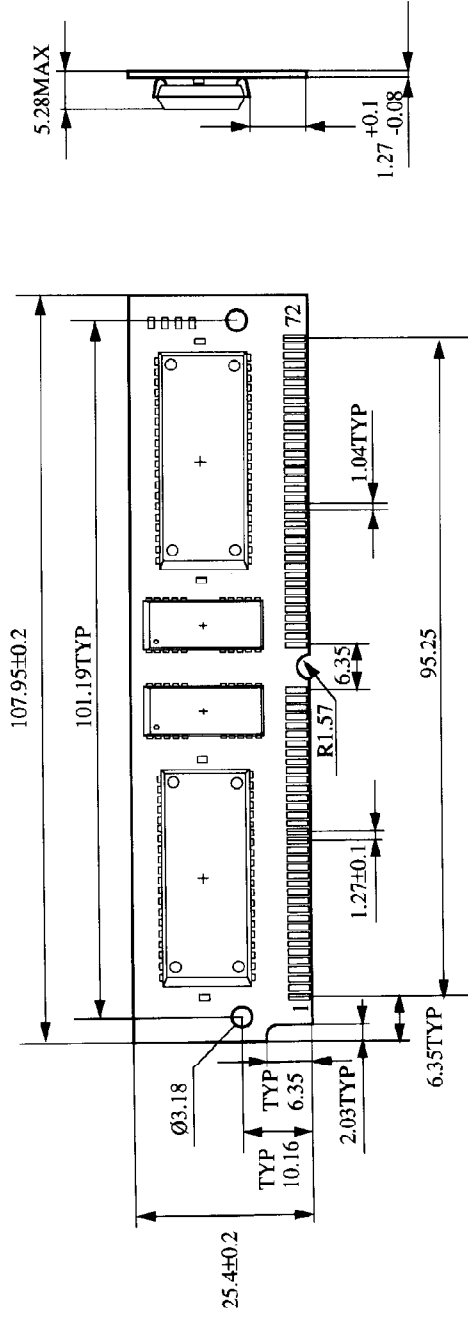
FEATURES

- 1,048,576 word X 36 bit organization
- 72-pin socket insertable module
 - MSC23B136D-xxBS4 : Gold tab
 - MSC23B136D-xxDS4 : Solder tab
- Single +5 V supply $\pm 10\%$ tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 1024 cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ only refresh capability

FAMILY ORGANIZATION

| FAMILY | ACCESS TIME (MAX) | | | Cycle Time (MAX) | Power Dissipation | |
|----------------------|-------------------|-----------------|------------------|------------------|-------------------|---------------|
| | t _{RAC} | t _{AA} | t _{CAC} | | Operating (MAX) | Standby (Max) |
| MSC23B136D-60BS4/DS4 | 60ns | 30ns | 15ns | 110ns | 2256mW | 22mW |
| MSC23B136D-70BS4/DS4 | 70ns | 35ns | 20ns | 130ns | 2036mW | |

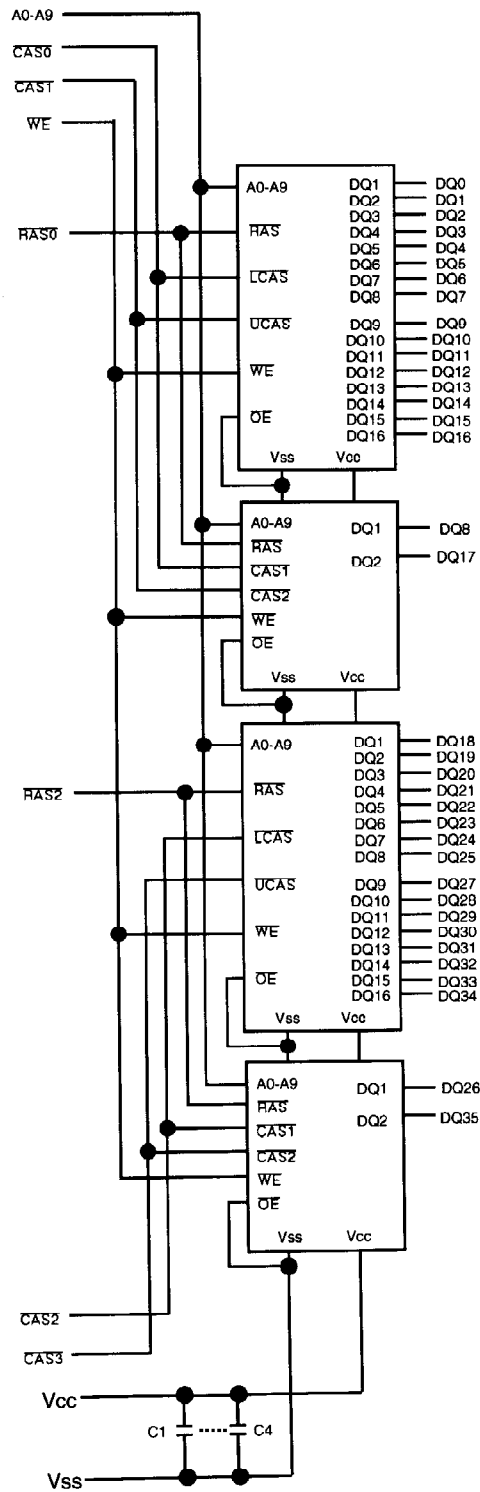
MSC23B136D-xxBS4/DS4



*1 The common size difference of the board width 12.5mm of its height is specified as ± 0.2 . The value above 12.5mm is specified as ± 0.5 .

FUNCTIONAL BLOCK DIAGRAM

MSC23B136D-xxBS4/DS4



PIN CONFIGURATION

MSC23B136D-xxBS4/DS4

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | Vss | 19 | NC | 37 | DQ17 | 55 | DQ12 |
| 2 | DQ0 | 20 | DQ4 | 38 | DQ35 | 56 | DQ30 |
| 3 | DQ18 | 21 | DQ22 | 39 | Vss | 57 | DQ13 |
| 4 | DQ1 | 22 | DQ5 | 40 | CAS0 | 58 | DQ31 |
| 5 | DQ19 | 23 | DQ23 | 41 | CAS2 | 59 | Vcc |
| 6 | DQ2 | 24 | DQ6 | 42 | CAS3 | 60 | DQ32 |
| 7 | DQ20 | 25 | DQ24 | 43 | CAS1 | 61 | DQ14 |
| 8 | DQ3 | 26 | DQ7 | 44 | RAS0 | 62 | DQ33 |
| 9 | DQ21 | 27 | DQ25 | 45 | NC | 63 | DQ15 |
| 10 | Vcc | 28 | A7 | 46 | NC | 64 | DQ34 |
| 11 | NC | 29 | NC | 47 | WE | 65 | DQ16 |
| 12 | A0 | 30 | Vcc | 48 | NC | 66 | NC |
| 13 | A1 | 31 | A8 | 49 | DQ9 | 67 | PD1 |
| 14 | A2 | 32 | A9 | 50 | DQ27 | 68 | PD2 |
| 15 | A3 | 33 | NC | 51 | DQ10 | 69 | PD3 |
| 16 | A4 | 34 | RAS2 | 52 | DQ28 | 70 | PD4 |
| 17 | A5 | 35 | DQ26 | 53 | DQ11 | 71 | NC |
| 18 | A6 | 36 | DQ8 | 54 | DQ29 | 72 | Vss |

PRESENCE DETECT PINS

| Pin No. | Pin name | -60 | -70 |
|---------|----------|-----|-----|
| 67 | PD1 | Vss | Vss |
| 68 | PD2 | Vss | Vss |
| 69 | PD3 | NC | Vss |
| 70 | PD4 | NC | NC |

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|------------------------------------|---------------|------|
| Voltage on any pin relative to V _{SS} | V _{IN} , V _{OUT} | - 1.0 ~ + 7.0 | V |
| Voltage V _{CC} supply relative to V _{SS} | V _{CC} | - 1.0 ~ + 7.0 | V |
| Short circuit output current | I _{OS} | 50 | mA |
| Power dissipation | P _D | 4 | W |
| Operating temperature | T _{OPR} | - 0 ~ + 70 | °C |
| Storage temperature | T _{STG} | - 40 ~ + 125 | °C |

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted within the limits as specified in this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | MIN | TYPE | MAX | UNIT | Operating temperature 0 °C ~ + 70 °C |
|--------------------|-----------------|------|------|-----|------|---|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V | |
| | V _{SS} | 0 | 0 | 0 | V | |
| Input high voltage | V _{IH} | 2.4 | - | 6.5 | V | |
| Input low voltage | V _{IL} | -1.0 | - | 0.8 | V | |

CAPACITANCE

| Parameter | Symbol | Typ. | MAX | Unit |
|-------------------------------|------------------|------|-----|------|
| Input Capacitance(A0-A9) | C _{IN1} | - | 29 | pF |
| Input Capacitance(WE) | C _{IN2} | - | 35 | pF |
| Input Capacitance(RAS0, RAS2) | C _{IN3} | - | 20 | pF |
| Input Capacitance(CAS0-CAS3) | C _{IN4} | - | 20 | pF |
| I/O Capacitance(DQ0-DQ35) | C _{DQ} | - | 13 | pF |

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim +70^\circ C$)

| Parameter | Symbol | Condition | MSC23B136D-60BS4/DS4 | | MSC23B136D-70BS4/DS4 | | Unit | Note | |
|---|-----------|--|----------------------|----------|----------------------|----------|---------|------|--|
| | | | Min | Max | Min | Max | | | |
| Input Leakage Current | I_{LI} | $0V \leq V_{in} \leq 6.5V$: All other pins not under test = $0V$ | -40 | 40 | -40 | 40 | μA | | |
| Output Leakage Current | I_{LO} | Data out is disable $0V \leq V_{out} \leq 5.5V$ | -10 | 10 | -10 | 10 | μA | | |
| Output High Voltage | V_{OH} | $I_{OH} = -5.0mA$ | 2.4 | V_{CC} | 2.4 | V_{CC} | V | | |
| Output Low Voltage | V_{OL} | $I_{OL} = 4.2mA$ | 0 | 0.4 | 0 | 0.4 | V | | |
| Average power supply current (Operating) | I_{CC1} | RAS cycling, CAS cycling $t_{RC} = \min$ | - | 410 | - | 370 | mA | 1,2 | |
| Power supply current (Standby) | I_{CC2} | RAS = V_{IH} CAS = V_{IH} | TTL | - | 8 | - | 8 | mA | |
| | | MOS | - | 4 | - | 4 | mA | | |
| Average power supply current (RAS only refresh) | I_{CC3} | RAS cycling, CAS = V_{IL} $t_{RC} = \min$ | - | 410 | - | 370 | mA | 1 | |
| Average power supply current (CAS before RAS refresh) | I_{CC6} | $t_{RC} = \min$. | - | 410 | - | 370 | mA | 1 | |
| Average power supply current (Fast page) | I_{CC7} | RAS = V_{IL} , CAS cycling $t_{PC} = \min$. | - | 370 | - | 340 | mA | 1,3 | |

NOTE:

1. I_{CC} is dependent on output loading and cycles rates. Specified values are obtained with the output open.
2. Address can be changed once or less while RAS = V_{IL}
3. Address can be changed once or less while CAS = V_{IH}

AC CHARACTERISTIC

(V_{CC} = 5V ± 10%, T_a = 0 ~ 70 °C)

NOTE 1.2.3

| Parameter | Symbol | MSC23B136D-60BS4/DS4 | | MSC23B136D-70BS4/DS4 | | UNIT | NOTE |
|--|-------------------|----------------------|------|----------------------|------|------|-------|
| | | MIN | MAX | MIN | MAX | | |
| Random read or write cycle time | t _{RC} | 110 | - | 130 | - | ns | |
| Fast page mode cycle time | t _{PC} | 40 | - | 45 | - | ns | |
| Access time from $\overline{\text{RAS}}$ | t _{RAC} | - | 60 | - | 70 | ns | 4,5,6 |
| Access time from $\overline{\text{CAS}}$ | t _{CAC} | - | 15 | - | 20 | ns | 4,5 |
| Access time from column address | t _{AA} | - | 30 | - | 35 | ns | 4,6 |
| Access time from $\overline{\text{CAS}}$ precharge | t _{CPA} | - | 35 | - | 40 | ns | 4,11 |
| $\overline{\text{CAS}}$ to output in Low-Z | t _{CLZ} | 0 | - | 0 | - | ns | 4 |
| Output buffer turn-off delay | t _{OFF} | 0 | 15 | 0 | 20 | ns | 7 |
| Transition time | t _T | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh period | t _{REF} | - | 16 | - | 16 | ms | |
| $\overline{\text{RAS}}$ precharge time | t _{RP} | 40 | - | 50 | - | ns | |
| $\overline{\text{RAS}}$ pulse width | t _{RAS} | 60 | 10K | 70 | 10K | ns | |
| $\overline{\text{RAS}}$ pulse width (Fast page mode) | t _{RASP} | 60 | 100K | 70 | 100K | ns | |
| $\overline{\text{RAS}}$ hold time | t _{RSH} | 15 | - | 20 | - | ns | |
| $\overline{\text{CAS}}$ precharge time | t _{CP} | 10 | - | 10 | - | ns | 13 |
| $\overline{\text{CAS}}$ pulse width | t _{CAS} | 15 | 10K | 20 | 10K | ns | |
| $\overline{\text{CAS}}$ hold time | t _{CSH} | 60 | - | 70 | - | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | t _{CRP} | 5 | - | 5 | - | ns | 11 |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge | t _{RHCP} | 35 | - | 40 | - | ns | 11 |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | t _{RCD} | 20 | 45 | 20 | 50 | ns | 5 |
| $\overline{\text{RAS}}$ to column address delay time | t _{RAD} | 15 | 30 | 15 | 35 | ns | 6 |
| Row address set-up time | t _{ASR} | 0 | - | 0 | - | ns | |
| Row address hold time | t _{RAH} | 10 | - | 10 | - | ns | |
| Column address set-up time | t _{ASC} | 0 | - | 0 | - | ns | 10 |
| Column address hold time | t _{CAH} | 15 | - | 15 | - | ns | 10 |
| Column address to $\overline{\text{RAS}}$ load time | t _{RAL} | 30 | - | 35 | - | ns | |

AC CHARACTERISTICS (Continued)
(V_{CC} = 5V ± 10%, T_a = 0 ~70 °C)

| Parameter | Symbol | MSC23B136D-60BS4/DS4 | | MSC23B136D-70BS4/DS4 | | UNIT | NOTE |
|--|-------------------|----------------------|-----|----------------------|-----|------|------|
| | | MIN | MAX | MIN | MAX | | |
| Read command set-up time | t _{RCS} | 0 | - | 0 | - | ns | 10 |
| Read command hold time | t _{RCH} | 0 | - | 0 | - | ns | 8,10 |
| Read command hold time reference to RAS | t _{RRH} | 0 | - | 0 | - | ns | 8 |
| Write command set-up time | t _{WCS} | 0 | - | 0 | - | ns | 10 |
| Write command hold time | t _{WCH} | 10 | - | 15 | - | ns | 10 |
| Write command pulse width | t _{WP} | 10 | - | 10 | - | ns | |
| Write command to RAS read time | t _{RWL} | 15 | - | 20 | - | ns | |
| Write command to CAS read time | t _{CWL} | 15 | - | 20 | - | ns | 12 |
| Data-in set-up time | t _{DS} | 0 | - | 0 | - | ns | 9,10 |
| Data-in hold time | t _{DH} | 15 | - | 15 | - | ns | 9,10 |
| CAS precharge WE delay time | t _{CPWD} | 60 | - | 70 | - | ns | |
| CAS active delay time from RAS precharge | t _{RPC} | 5 | - | 5 | - | ns | 10 |
| RAS to CAS set-up time (CAS before RAS) | t _{CSR} | 10 | - | 10 | - | ns | 10 |
| CAS hold time (CAS before RAS) | t _{CHR} | 10 | - | 10 | - | ns | 11 |

- NOTES:
- 1) An initial pause of 200 μ s is required after power-up followed by a minimum of 8 initialization cycles (examples: $\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 - 2) The AC measurements assume the transition time (t_T) = 5 ns.
 - 3) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL} .
 - 4) Measured by using an equivalent load circuit of 2 TTL loads and 100 pF.
 - 5) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC} .
 - 6) Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA} .
 - 7) The t_{OFF} (max.) spec. defines at which time the output data achieves a high impedance state and is not referenced to output voltage levels.
 - 8) Either the t_{RRH} or the t_{RCH} spec. must be satisfied for proper read cycle.
 - 9) These parameters are referenced to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ leading edge in an early write cycle.
 - 10) These parameters are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 - 11) These parameters are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 - 12) t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 - 13) t_{CP} is determined by the time of both $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ are high.