FEATURES

- Precision 1:2, 400mV LVPECL fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - > 6GHz f_{MAX} clock
  - < 80ps t_r/t_f times
  - < 250ps t_{pd}
  - < 15ps max. skew
- Low jitter performance:
  - < 10ps$_{PP}$ total jitter (clock)
  - < 1ps$_{RMS}$ random jitter (data)
  - < 10ps$_{PP}$ deterministic jitter (data)
- Accepts an input signal as low as 100mV
- Unique input termination and V_T pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS and CML
- 400mV LVPECL compatible outputs
- Power supply 2.5V ±5% and 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 16-pin (3mm × 3mm) MLF® package

APPLICATIONS

- All SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplanes
- Data distribution: OC-48, OC-48+FEC, XAUI
- High-end, low-skew, multiprocessor synchronous clock distribution

Precision Edge®

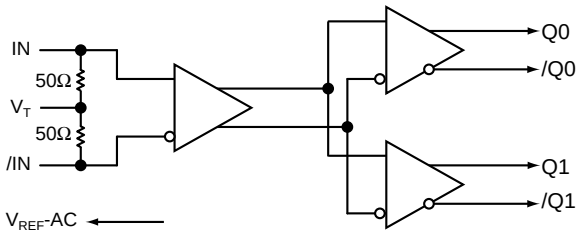
DESCRIPTION

The SY58013U is a 2.5V/3.3V precision, high-speed, fully differential 1:2 LVPECL fanout buffer. Optimized to provide two identical output copies with less than 15ps of skew and less than 10ps$_{(pk-pk)}$ total jitter, the SY58013U can process clock signals as fast as 6GHz or data patterns up to 10.7Gbps.

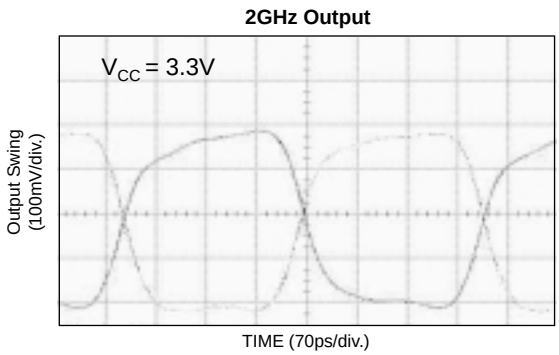
The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS, and CML differential signals, (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the V_T pin. The outputs are 400mV LVPECL compatible, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY58013U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require greater output swing or CML compatible outputs, consider the SY58012U 1:2 fanout buffer with 800mV LVPECL outputs, or the SY58011U 1:2 fanout buffer with 400mV CML outputs. The SY58013U is part of Micrel's high-speed, Precision Edge® product line. Datasheets and support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM

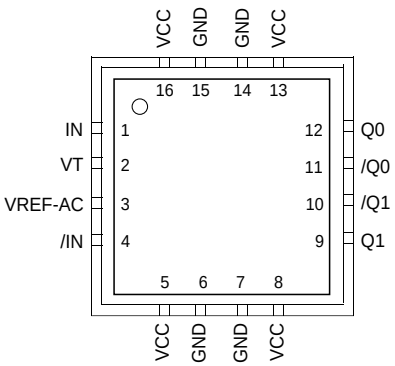


TYPICAL PERFORMANCE



2GHz with 100mV Input

PACKAGE/ORDERING INFORMATION



16-Pin MLF®

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58013UMI	MLF-16	Industrial	013U	Sn-Pb
SY58013UMITR[2]	MLF-16	Industrial	013U	Sn-Pb
SY58013UMG[3]	MLF-16	Industrial	013U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58013UMGTR[2, 3]	MLF-16	Industrial	013U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. Each pin is internally terminated with 50Ω to the V_T pin. Note that this input will default to an indeterminate state if left open. See *"Input Interface Applications"* section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The V_T pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} –1.2V. It is used for AC-coupled inputs (IN, /IN). Connect V_{REF-AC} directly to the V_T pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum curent source or sink is 0.5mA. See *"Input Interface Applications"* section.
5, 8, 13, 16	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
6, 7, 14, 15	GND, (Exposed Pad)	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
12, 11 9, 10	Q0, /Q0, Q1, /Q1	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400mV. Unused output pairs may be left floating with no impact on jitter. See "*LVPECL Output Termination*" section.

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CC}) ..... –0.5V to+4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
V_T Current
  Source or sink current on V_T pin ..... ±100mA
Input Current
  Source or sink current on (IN, /IN) ..... ±50mA
V_{REF} Current
  Source or sink current on V_{REF}-AC, **Note 4** ..... ±1.5mA
Soldering, (20 sec.) ..... 260°C
Storage Temperature Range (T_{STORE}) ..... –65 to +150°C

Operating Ratings(Note 2)

Power Supply Voltage (V_{CC}) ..... +2.375V to +3.60V
Operating Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance, **Note 3**
  MLF® (θ_{JA})
    Still-Air ..... 60°C/W
    500lpfm ..... 54°C/W
  MLF® (ψ_{JB}) ..... 33°C/W

DC ELECTRICAL CHARACTERISTICS(Note 5)

T_A= –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.375		3.60	V
I_{CC}	Power Supply Current	Max. V_{CC}, no load		75	90	mA
V_{IH}	Input HIGH Voltage	IN, /IN	V_{CC}–1.2		V_{CC}	V
V_{IL}	Input LOW Voltage	IN, /IN	0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing	IN, /IN; see Figure 1a	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage	IN, /IN; see Figure 1b	0.2		3.4	V
R_{IN}	In to V_T Resistance		40	50	60	Ω
V_{REF}-AC	Output Reference Voltage		V_{CC} –1.3	V_{CC} –1.2	V_{CC} –1.1	V
IN to V_T					1.28	V

LVPECL DC ELECTRICAL CHARACTERISTICS(Note 5)

V_{CC} = 3.3V ±10% or V_{CC} = 2.5 ±5%; R_L= 50Ω to V_{CC}–2V; T_A= –40°C to 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	Q0, /Q0, Q1, /Q1	V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage	Q0, /Q0, Q1, /Q1	V_{CC}–1.545	V_{CC}–1.420	V_{CC}–1.295	V
V_{OUT}	Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1a	200	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1b	400	800		mV

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Note 4. Due to the limited drive capability, use for input of the same package only.

Note 5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[Note 7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data		10		Gbps
		$V_{OUT} \geq$ 200mV Clock	6			GHz
t_{pd}	Propagation Delay	$V_{IN} \geq$ 100mV	100	180	250	ps
t_{CHAN}	Channel-to-Channel Skew	**Note 8**		4	15	ps
t_{SKEW}	Part-to-Part Skew	**Note 9**			100	ps
t_{JITTER}	Data Random Jitter (RJ)	**Note 10**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 11**			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	**Note 12**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 13**			10	ps_{PP}
t_r, t_f	Output Rise/Fall Time	20% to 80%, at full output swing	20	50	80	ps

Note 7. High frequency AC electricals are guaranteed by design and characterization.

Note 8. Skew is measured between outputs of the same bank under identical transitions.

Note 9. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

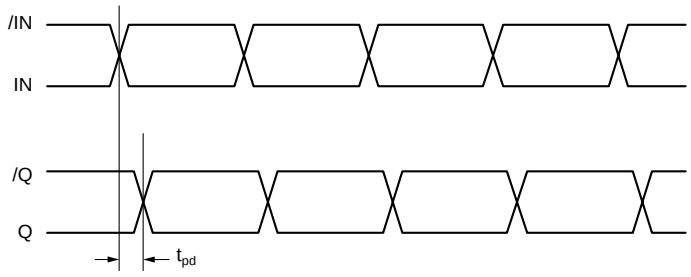
Note 10. RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.

Note 11. DJ is measured at 10.7Gbps and 2.5Gbps/3.2Gbps with both K28.5 and 2^{23}–1 PRBS pattern

Note 12. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.

Note 13. Total jitter definition: With an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TIMING DIAGRAM



SINGLE-ENDED AND DIFFERENTIAL SWINGS

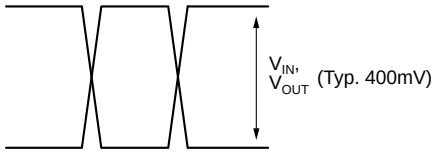


Figure 1a. Single-Ended Voltage Swing

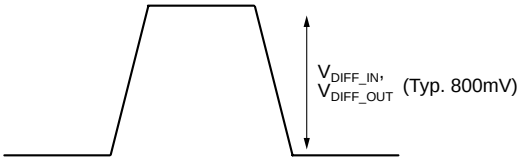
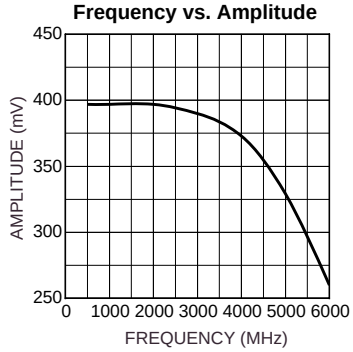


Figure 1b. Differential Voltage Swing

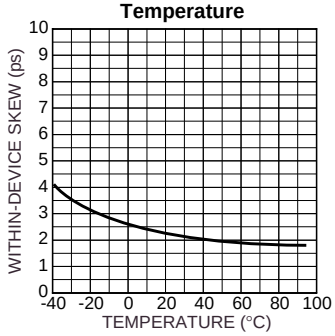
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

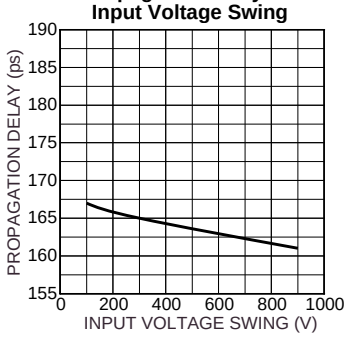
Frequency vs. Amplitude



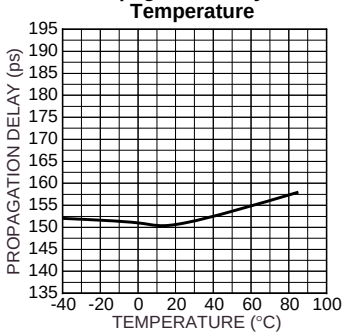
Within-Device Skew vs. Temperature



Propagation Delay vs. Input Voltage Swing



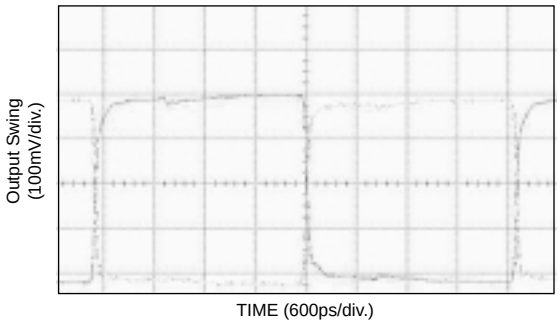
Propagation Delay vs. Temperature



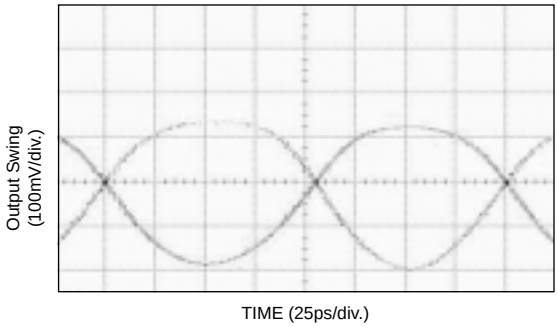
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} = 0V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

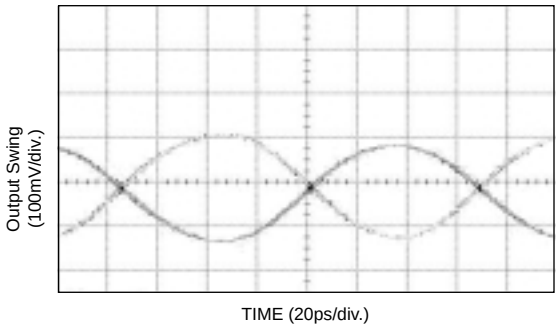
200MHz Output



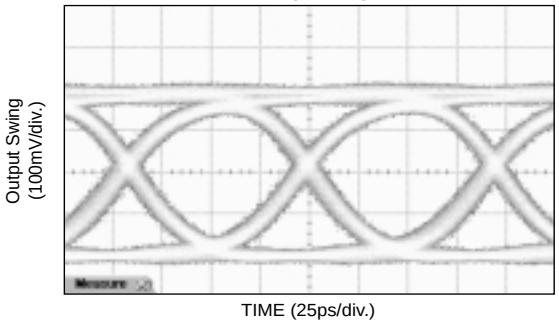
5GHz Output



7GHz Output



10.7Gbps Output



(2^{23}–1 PRBS Pattern)

INPUT STAGE

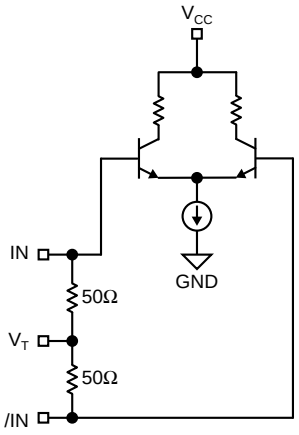


Figure 2. Simplified Differential Input Buffer

INPUT INTERFACE APPLICATIONS

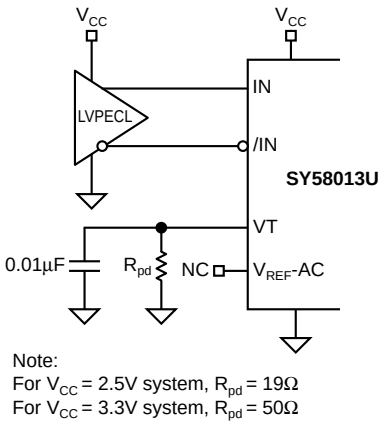


Figure 3a. DC-Coupled LVPECL Input Interface

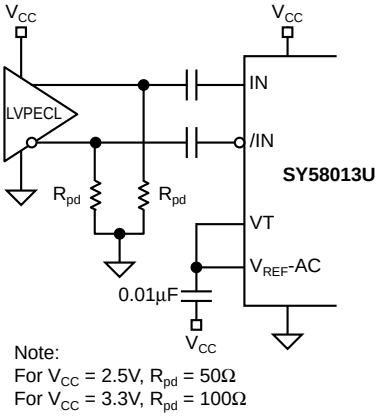


Figure 3b. AC-Coupled LVPECL Input Interface

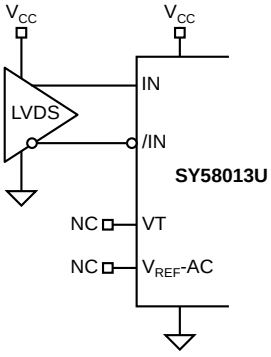


Figure 3c. LVDS Input Interface

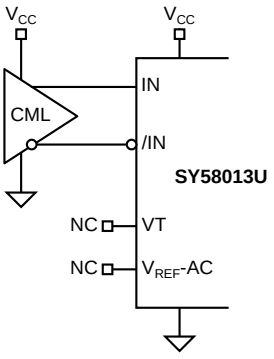


Figure 3d. DC-Coupled CML Input Interface
(option: may connect V_T to V_{CC})

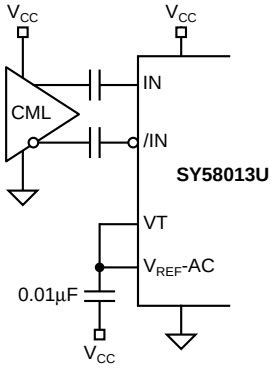


Figure 3e. AC-Coupled CML Input Interface

OUTPUT TERMINATION RECOMMENDATIONS

LVPECL outputs have very low output impedance (open emitter), and small signal swing which results in low EMI (electro-magnetic interference). The LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. In addition, LVPECL is compatible for driving standard PECL inputs since PECL inputs require only 100mV input swing. Further, there are several techniques in terminating the LVPECL outputs, as shown in Figure 5 through 7.

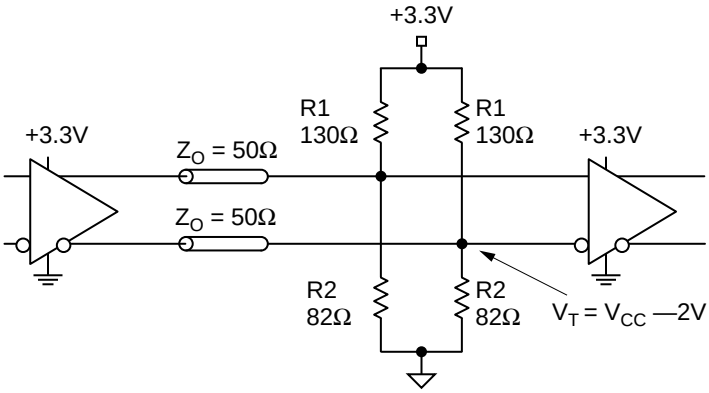


Figure 5. Parallel Termination–Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω
Note 2. For +3.3V systems: R1 = 130Ω, R2 = 82Ω

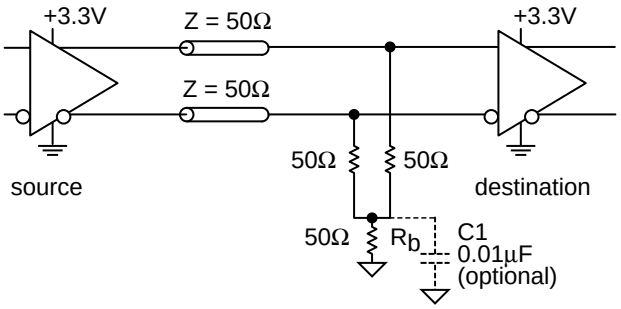


Figure 6. Three-Resistor "Y–Termination"

Note 1. Power-saving alternative to Thevenin termination.
Note 2. Place termination resistors as close to destination inputs as possible.
Note 3. R_b resistor sets the DC bias voltage, equal to V_T.
For +2.5V systems R_b = 39Ω.
For +3.3V systems R_b = 46Ω to 50Ω.
Note 4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

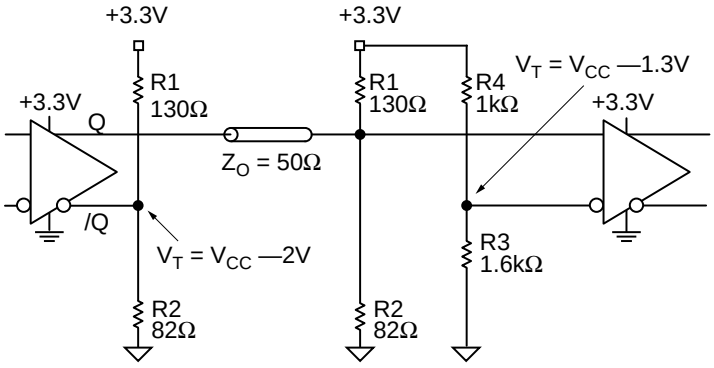


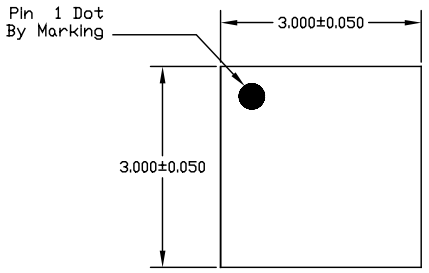
Figure 7. Terminating Unused I/O

Note 1. Unused output (/Q) must be terminated to balance the output.
Note 2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.
For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1kΩ, R4 = 1.6kΩ.
Note 3. Unused output pairs (Q and /Q) may be left floating.

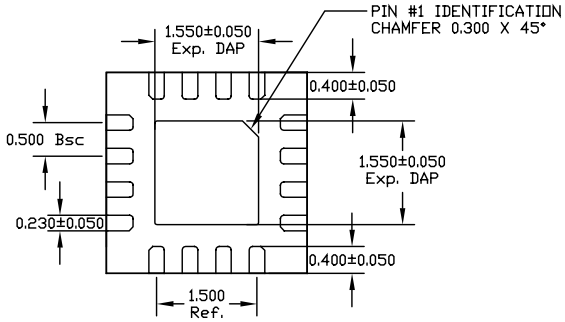
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58011U	7GHz, 1:2 CML Fanout Buffer/Translator With Internal I/O Termination	http://www.micrel.com/product-info/prod/ucts/sy58011u.shtml
SY58012U	5GHz, 1:2 LVPECL Fanout Buffer/Translator With Internal Input Termination	http://www.micrel.com/product-info/products/sy58012u.shtml
SY58013U	6GHz, 1:2 Fanout Buffer/Translator w/400mV LVPECL Outputs and Internal Input Termination	http://www.micrel.com/product-info/products/sy58013u.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
M-0317	HBW Solutions	http://www.micrel.com/product-info/as/solutions.shtml

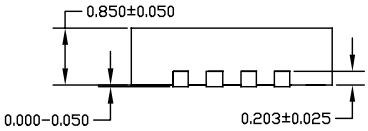
16-PIN *Micro*LeadFrame® (MLF-16)



TOP VIEW

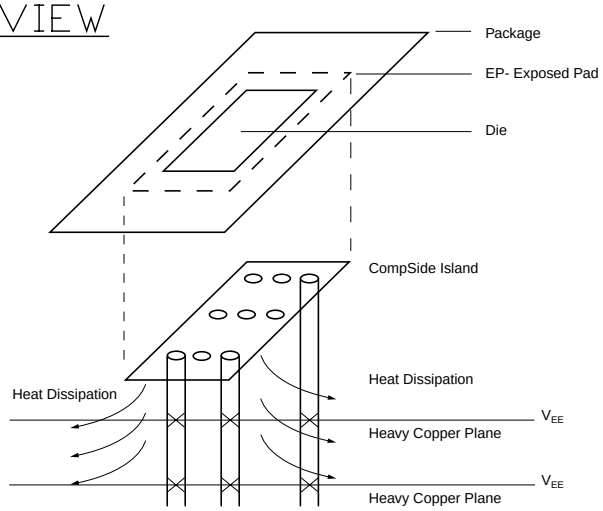


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com