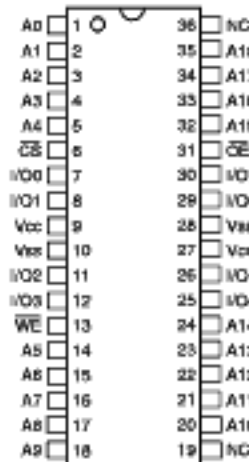




512Kx8 SRAM

PRELIMINARY *

PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A0-13	Address Inputs
I/O0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground
NC	No Connect

PLASTIC PLUS™ FEATURES

- Access Times of 15, 20, 25ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard 36 pin Plastic SOJ Package
- Electrical and Speed Characteristics for:
 - Military Temperature (-55°C to +125°C)
 - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 512K x 8
- Center Power/Ground Pins (Revolutionary)
- 5 Volt Power Supply
- Low Power ("L") Version Available
- Battery Back-Up Operation
- Reliability Test Data Available:
 - High Temperature Operating Life
 - High Temperature Storage
 - Pressure Cooker Test
 - Wet High Temperature Operating Life
 - Thermal Shock
 - Temperature Cycling

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

PLASTIC PLUS SRAM

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T _A	-55	+125	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to V _{SS}	V _G	-0.5	V _{CC} + 0.5	V
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O Pin	V _{CC} Current
H	X	X	Power Down	High-Z	I _{SB}
L	H	H	Out Disable	High-Z	I _{CC}
L	H	L	Read	DOUT	I _{CC}
L	L	X	Write	DIN	I _{CC}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T _A	-55	+125	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	6	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = V _{SS} to V _{CC}		10	μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = V _{SS} to V _{CC}		10	μA
Operating Supply Current	I _{CC}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		180	mA
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		15	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V**DATA RETENTION CHARACTERISTICS**(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions				Units
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		0.5	8	mA
Low Power Data Retention (L)	I _{CCDR1}	V _{CC} = 3V		300	800	μA



AC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-15*		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	15		20		25		ns
Address Access Time	t _{AA}		15		20		25	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		15		20		25	ns
Output Enable to Output Valid	t _{OE}		8		10		12	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		7		8		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		7		8		10	ns

* 15ns not available in the lower power option.
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol	-15*		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	15		20		25		ns
Chip Select to End of Write	t _{CW}	12		13		15		ns
Address Valid to End of Write	t _{AW}	12		13		15		ns
Data Valid to End of Write	t _{DW}	8		9		10		ns
Write Pulse Width	t _{WP}	12		13		15		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	0		0		0		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		8		10	ns
Data Hold Time	t _{DH}	0		0		0		ns

* 15ns not available in the lower power option.
1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

The diagram shows a diamond-shaped load circuit. The top and bottom nodes are connected to current sources labeled I_{OL} and I_{OH} respectively. The left node is connected to a D.U.T. (Device Under Test) which has an effective capacitance C_{eff} = 50 pf. The right node is connected to a bipolar supply V_Z ≈ 1.5V.

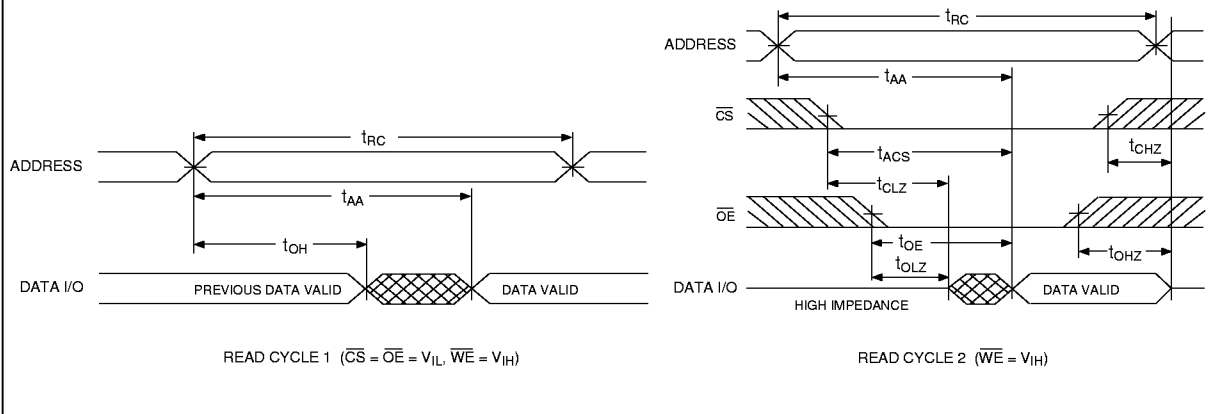
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

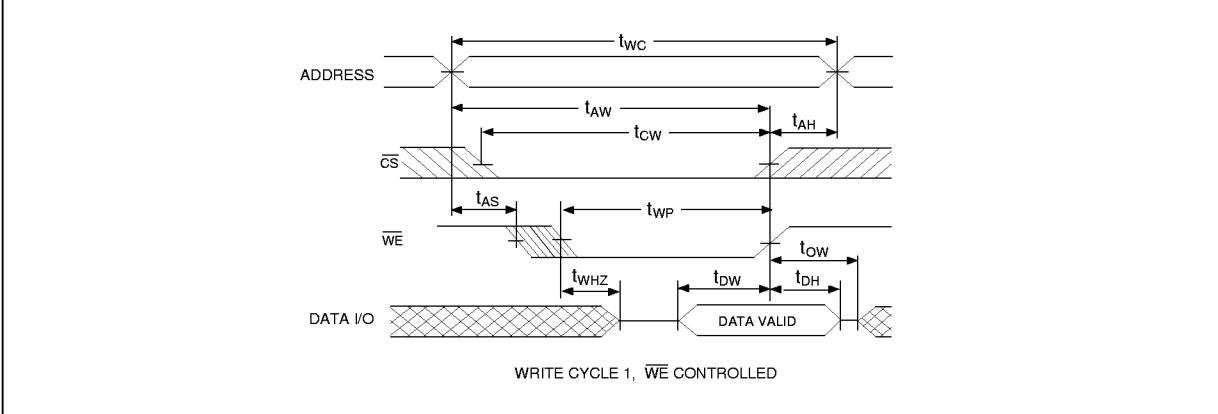
NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



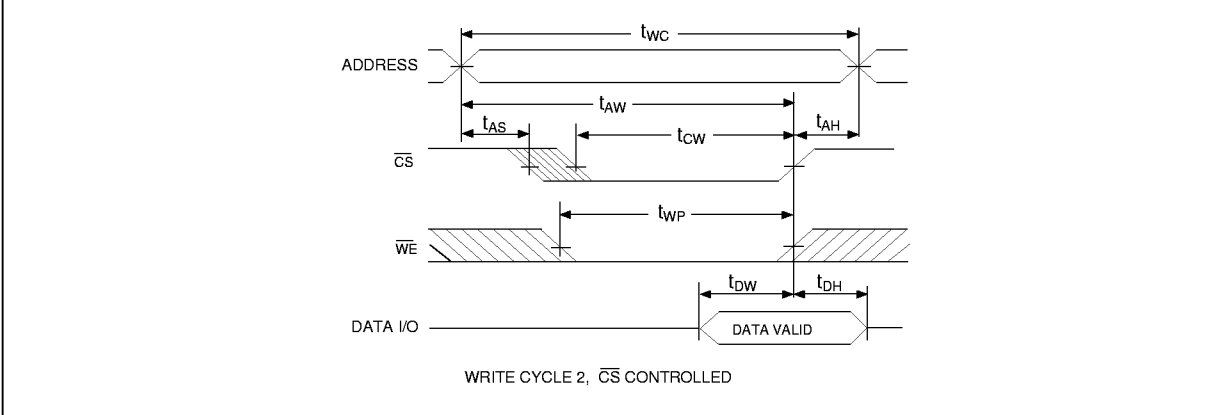
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

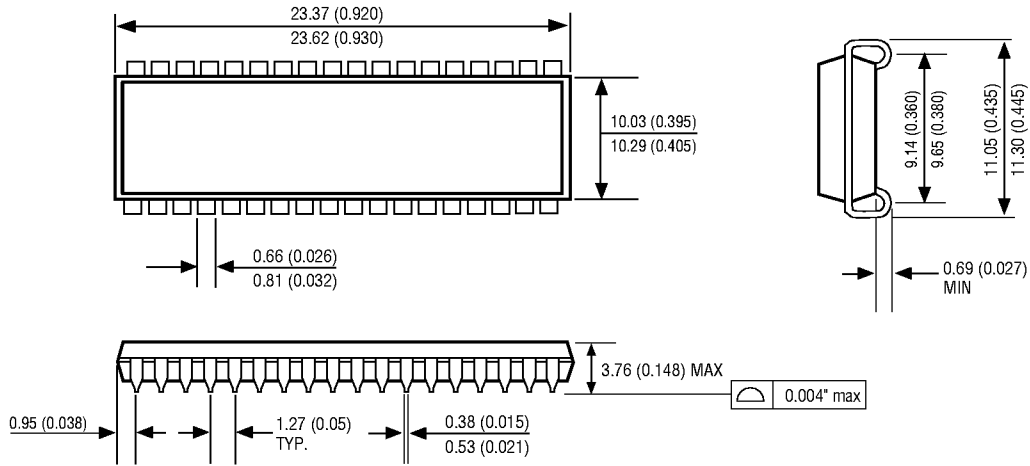


WRITE CYCLE - \overline{CS} CONTROLLED





PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION

W P S 512K 8 X X - XXX R J X X

SPECIAL PROCESS:

- Blank = CMOS
- B = Bi CMOS

DEVICE GRADE:

- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:

- RJ = Revolutionary SOJ

ACCESS TIME (ns)

IMPROVEMENT MARK

- B = Burn-in
- T = Temperature Cycling
- C = Burn-in and Temperature Cycle

Blank = Standard Power

L = Low Power

ORGANIZATION, 512K x 8

SRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS