AK2308LV
SPEECH CODEC for Digital Key telephone

GENERAL DISCREPTION

AK2308LV is an integrated LSI with PCM CODEC, Voice path control, MIC amplifier and Handset driver suitable for PBX/KTS digital key telephone, VoIP Telephone Analog Interface.

PCM CODEC is compliant to ITU G.711 G.712 specification, very low noise, and low power dissipation CODEC. A-law and u-law selectable through Serial I/F register. PCM I/F provides Long/Short frame format. The output is 8bit compressed data along with 16bit linear format. FS must be 8kHz clock that is synchronized with BCLK.

Voice path block consists of TX analog inputs, output for handset receiver, output for the hands-free speaker, volume for the TX and RX respectively, and the path control switches. Side tone can be added internally and its volume is controlled through serial CPU I/F.

FEATURES

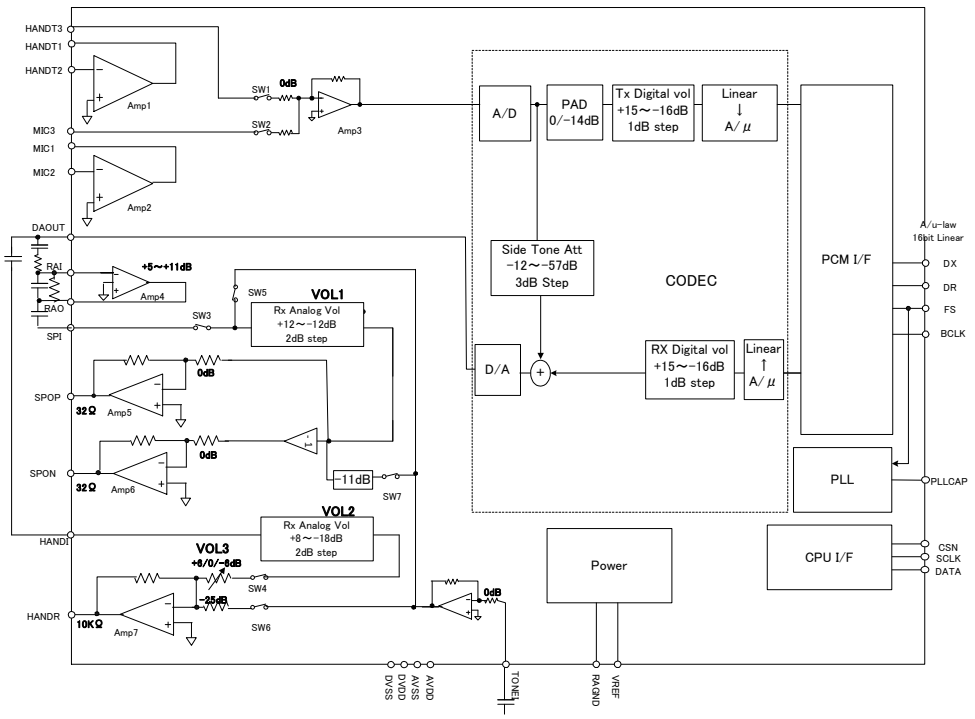
- 2 MIC AMP for the handset and microphone are integrated.
- Differential driver for the 32ohm speaker and 10k ohm driver for the handset receiver.
- Path control and volume control via serial CPU I/F
- 3.3V+/-0.3V single power supply
- Low noise, low power consumption

Package

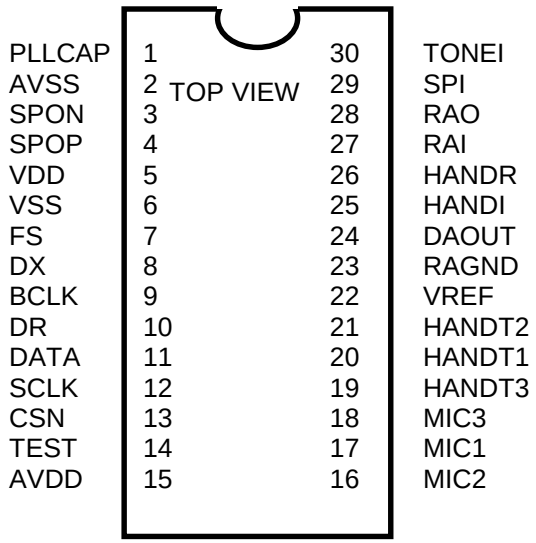
30pin VSOP package

- Package size; 9.7*7.6mm(pin to pin)
- Pin pitch; 0.65mm

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN CONDITIONS

Pin types;
DIN: Input
DOUT: Output
AIN: Analog Input
AOUT: Analog Output
I/O: Input/ Tri-state output
TOUT: Tri-state output
AOUT: Analog output
PWR: Power supply

Table 1

Pin #	Name	Type	Pin function	Max Cap load	Mln Res load	comment
21	HANDT2	AIN	Analog input for handset microphone			
19	HANDT3	AIN	Analog input for handset microphone			
20	HANDT1	AOUT	Amplifier output for handset microphone	20pF	5kΩ	
26	HANDR	AOUT	Analog output for handset receiver	20pF	10kΩ	
25	HANDI	AIN	Analog input for handset receiver			
18	MIC3	AIN	Analog input for external microphone			
16	MIC2	AIN	Analog input for external microphone			
17	MIC1	AOUT	Amplifier output for external microphone	20pF	5kΩ	
24	DAOUT	AOUT	Analog output of D/A converter	20pF	8kΩ	
27	RAI	AIN	Amplifier input for level adjustment			
28	RAO	AOUT	Amplifier output for level adjustment	20pF	12kΩ	
29	SPI	AIN	Analog input for speaker			
4	SPOP	AOUT	Analog output of the speaker driver (+)	1000pF between	32Ω	
3	SPON	AOUT	Analog output of the speaker driver (–)			
30	TONEI	AIN	Input for the external tone signal			
11	DATA	I/O	Serial data I/O for the internal register access	50pF		
12	SCLK	DIN	Serial data clock for the internal register access			
13	CSN	DIN	Chip select negative input for the internal register access			
10	DR	DIN	RX PCM data serial input			
8	DX	TOUT	TX PCM data serial output	50pF		
9	BCLK	DIN	Bit clock input for the PCM I/F			
7	FS*	DOUT	8KHz frame sync signal input for the PCM I/F			
6	VSS	PWR	Power supply for the digital block:0V			
5	VDD	PWR	Power supply for the digital block: 3.3V			
2	AVSS	PWR	Power supply for the analog block:0V			
15	AVDD	PWR	Power supply for the analog block: 3.3V			
1	PLLCAP	AOUT	Output to connect the PLL loop filter capacitance			1.0uF external capacitance
23	RAGND	AOUT	Analog ground output for the RX side			1.0uF external capacitance
22	VREF	AOUT	Voltage reference output			1.0uF external capacitance
14	TEST	DIN	Test pin			Tied to VSS

*FS must be 8kHz clock that is synchronized with BCLK.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Power Supply Voltages Analog/Digital Power Supply	VDD	-0.3	6.5	V
VSS Voltage	VSS	0	0	V
Digital Input Voltage	V_{TD}	-0.3	VDD+0.3	V
Analog Input Voltage	V_{TA}	-0.3	VDD+0.3	V
Input current (except power supply pins)	I_{IN}	-10	10	mA
Storage Temperature	Tstg	-55	125	°C

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies Analog/Digital power supply	VDD	3.0	3.3	3.6	V
Ambient Operating Temperature	Ta	-10		70	°C

Note) All voltages reference to ground : VSS=0V

1. CPU INTERFACE

The internal registers can be read/written via serial CPU interface which consists of SCLK, DATA, and CSN pin.
1 word consists of 16bits. The first 3bits are the instruction code which specifies read or write.
The following 4bits specify the address. The rest of 8bits are the data stored in the internal registers.

Table1-A CPU I/F ADDRESS/DATA STRUCTURE

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
I2	I1	I0	A3	A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
Instruction code (3 bit)			Address (4bit)				*	Data for internal registers (8bit)							

*)Dummy bit for adjusting the I/O timing when reading register.

Table1-B INSTRUCTION CODE

I2	I1	I0	Read/Write
1	1	0	Read
1	1	1	Write
Others			No action

1-2 Timing of the CPU Interface

SCLK and DATA timing in WRITE/READ operation

(1) Input data are loaded into the internal shift register at the rising edge of SCLK.
(2) The rising edge of SCLK is counted after the falling edge of CSN.
(3) When CSN is “L” and more than 16 SCLK pulses:
[WRITE] Data are loaded into the internal register at the rising edge of the SCLK 16th pulse.
[READ] DATA pin becomes an input pin at the falling edge of the SCLK 16th pulse.

CSN timing and WRITE/READ CANCELLATION

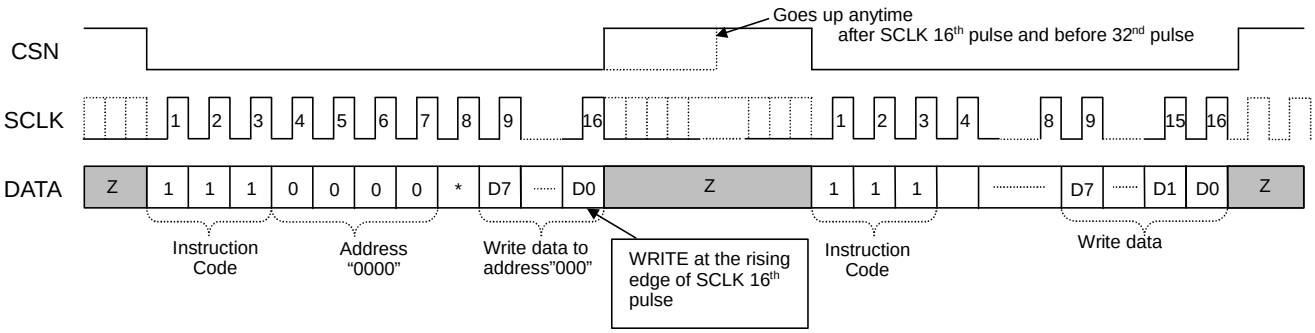
(1) WRITE is cancelled when CSN goes up before the rising edge of the SCLK 16th pulse.
(2) READ is cancelled when CSN goes up before the falling edge of the SCLK 16th pulse.

SERIAL WRITE/READ ACCESS timing (SERIAL ACCESS MODE)

(1) Serial write and read operation will be done by feeding the another 16 SCLK pulse and data after 1st write or read operation.
(2) It is not necessary to make CSN high between 1st operation and 2nd operation.

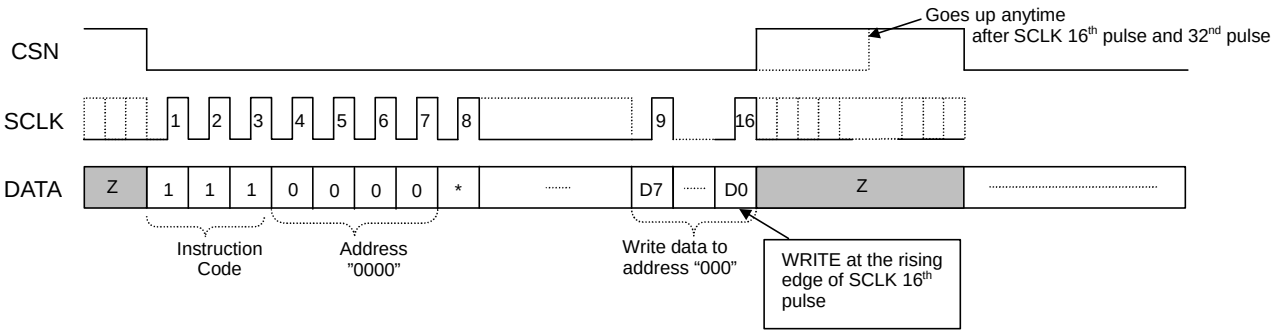
WRITE

Continuous SCLK

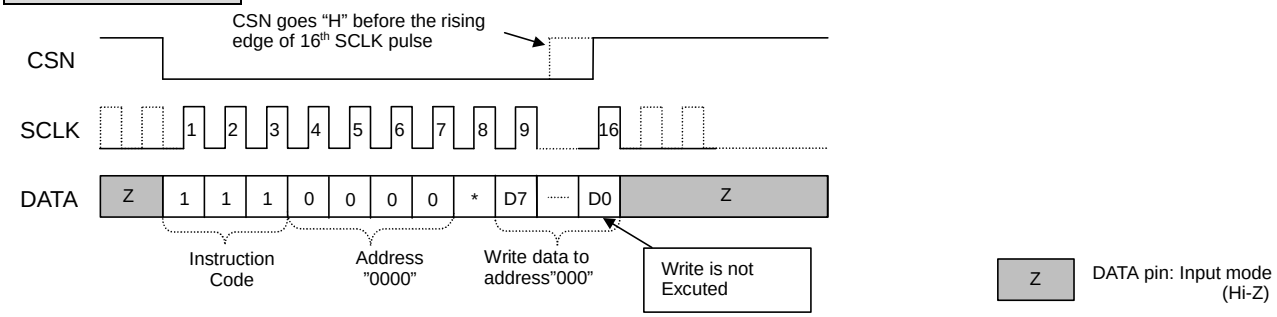


Burst SCLK

SCLK can be stoped at "H" level or "L" level at anytime during the write cycle. After resuming the SCLK, write cycle is retrieved normally.

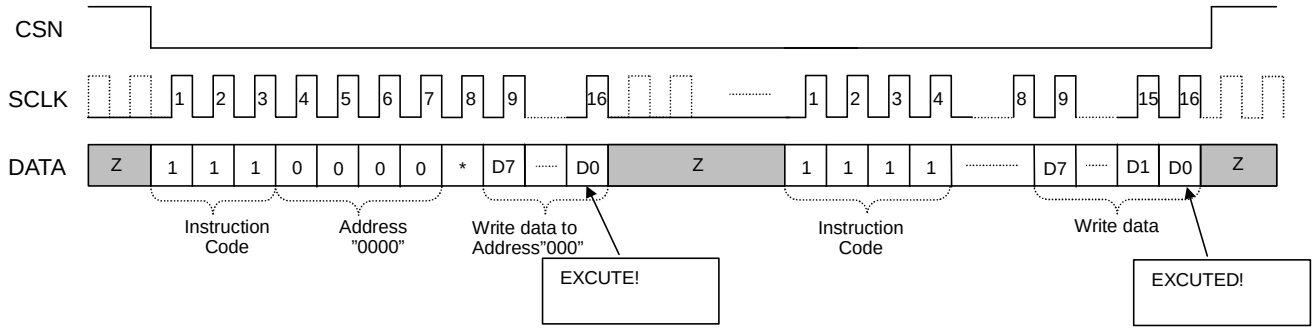


CANCELLATION



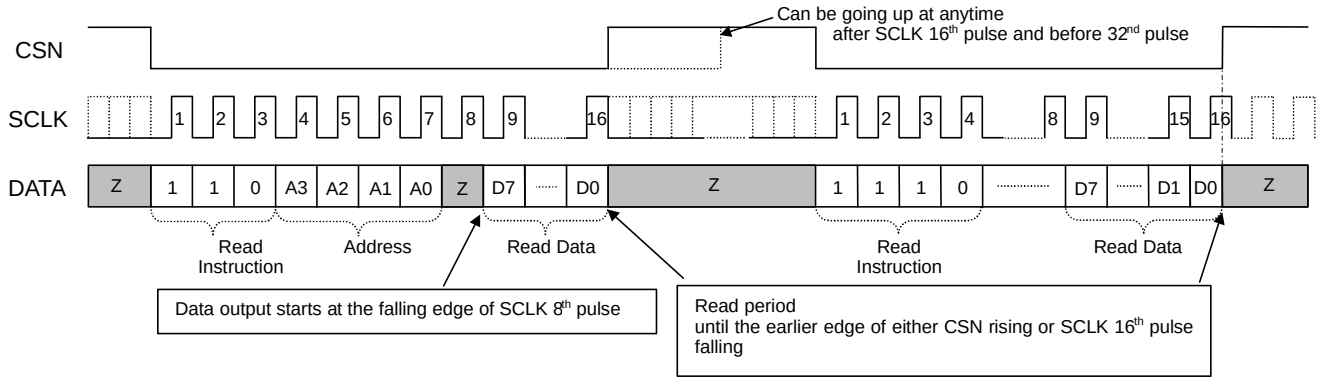
SERIAL ACCESS

Serial access can be done by CSN staying “L” during the serise of write cycle.

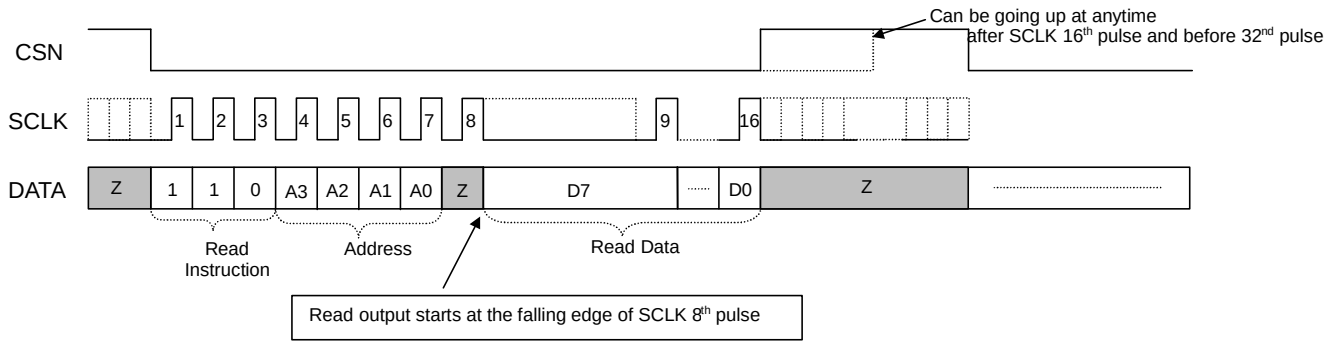


READ

Continuous SCLK

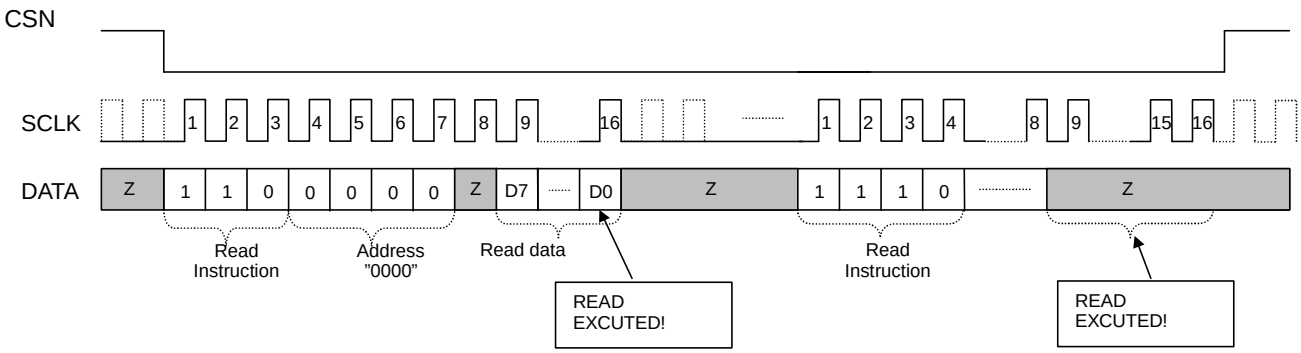


Burst SCLK

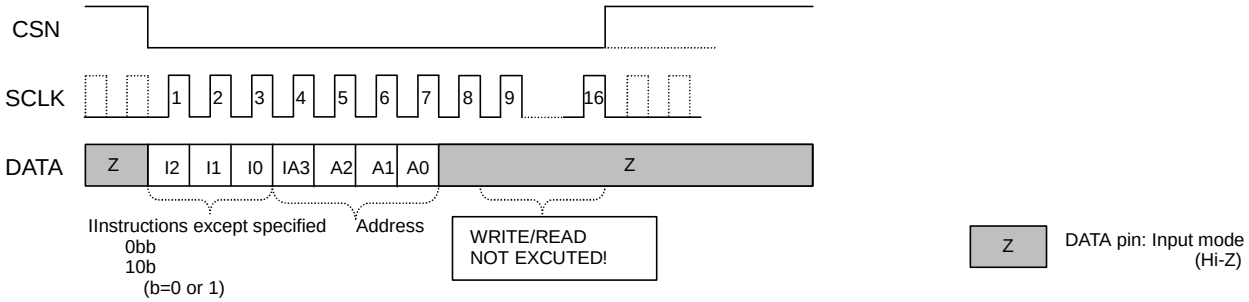


SERIAL ACCESS

Serial access can be done by CSN staying "L" during the serise of read cycle



DISCORD OF INSTRUCTION CODE



Register Map

Register Type : Read/ Write

Add (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Register Name (Functions)
0	-	SW7	SW6	SW5	SW4	SW3	SW2	SW1	Path Control
1	-	-	-	-	-	PCM_1	PCM_0	u/A-law	PCM Control
2	-	-	-	Side Tone	Side Tone Attenuator				Side Tone Control Side Tone Digital Attenuator Gain
3	-	-	TX_pad	TX Digital Volume					TX Voice Path Gain Control
4	-	-	-	RX Digital Volume					RX Digital Volume Control
5	-	-	-	-	VOL 1				RX Speaker Volume Control
6	-	-	VOL 3		VOL 2				RX Handset Volume Control
7 – F	-	-	-	-	-	-	-	-	Reserved for test use

•Address "1" ; PCM_0/1 ---- Selection of the PCM interface Mode(Long/Short frame, AK130-1,AK130-2, 16bit linear)

•Bits with "-" in the flame are for test mode activation. Please fill the data "0" for the normal operation.
These bits are for test use so that cannot write the data from CPU interface and read operation, data "0" are read from CPU interface.

•Each bit is set as "Default value" written in the following related sections after power on reset.

•Explanatory of each bits are described in following pages.

2. PCM Data Interface

AK2308LV supports 4 PCM data interface modes.

- **A/u-Law PCM data mode(Long or Short frame)**
  This mode is for interface of 64kbps PCM data which are compressed /extended by A -law or u-law. Both Long frame and short frame format are acceptable. The PCM data occupies the first time slot of the PCM data bus which is specified by the frame sync signal. Please refer to the format diagram. A -law or u-law is selectable via CPU register.
- **16 bit Linear data Mode**
  This mode is for the interface the 16 bit linear PCM data. PCM CODEC of AK2308LV operates at 14 bit accuracy. The 2 bits of the LSB are fixed in the 16 bit data stream.
- **AK130 B1 Mode**
  This mode provides the PCM data Interface to AK130, the TCM transceiver for PBX/KTS system. PCM data format is 64kbps A-law or u-law data. The timing between data and FS is different from the A/u-Law PCM data mode written above. In this mode the PCM data are transmitted/received via B1 channel , one of the PCM data channel of the AK130.
- **AK130 B2 Mode**
  This mode provides the PCM data interface to AK130 B2 channel in the same manner as AK130 B1 Mode.

In every mode, the digital voice data are in and out from DR and DX pin, respectively, and the bit clock and the 8KHz frame sync signal will be fed via BCLK and FS. And FS must be 8kHz clock that is synchronized with BCLK. The order of PCM and linear data is MSB first.

Table 2-A Summary of PCM interface modes

Mode	**PCM data format**	**BCLK rate**	**frame signal**	**Time slot**
A/u-Law PCM data mode	A/u-Law	64K x N (N: 1 to 32)	LF/SF auto select	1st Time slot
16bit Linear data mode	16bit Linear	64K x N (N: 2 to 32)	SF only	first 16 bit after FS signal
AK130 B1 mode	A/u-Law	2.048MHz	AK130 FS signal	B1 channel of AK130
AK130 B2 mode	A/u-Law	2.048MHz	AK130 FS signal	B2 channel of AK130

2-1. Selection of the interface mode

These four interface modes are selectable through the CPU register which specified below.
A/u-Law is also selectable from the same CPU register and it is effective in the A/u -law PCM interface mode and AK130 B1/B2 modes.

PCM Control

Register Type : Read Write[Address:0001 D2-D0:(PCM_1-0, u/A-law)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
1	-	-	-	-	-	**PCM_1**	**PCM_0**	**u/A law**
Default	0	0	0	0	0	**0**	**0**	**0**

PCM_1、0 ; PCM interface mode select

PCM_1	**PCM_0**	Mode
0	0	A/u-Law PCM data mode
0	1	16bit Linear interface mode
1	0	AK130 B1 mode
1	1	AK130 B2 mode

u/A-law ; PCM compress/Extend format select

A/u-law	Compress/Extend
0	u-law
1	A-law

2-2 Timing and format of the PCM interface

2-2-1 u/A-Law PCM data Mode

8 bits PCM data is accommodated in 1 frame(125us) defined by 8kHz frame sync signal.
Although there are 32 time slots at maximum in 8kHz frame(when BCK=2.048MHz), PCM data for AK2308LV occupies the first time slot as is indicated in figures below.

2-2-1-a Signals

- Frame Sync signal (FS)
8kHz reference signal. This signal indicated the timing and the frame position of 8kHz PCM interface. All the internal clock of the LSI is generated based on this FS signal.

- Bit Clock (BCLK)
BCLK defines the PCM data rate. BCLK can be varied from 64kHz to 2.048MHz by 64kHz step.

- PCM data output (DX)
DX is an output signal of 64Kbps PCM u/A-law data. The data is synchronized to the BCLK which determines the data rate. In the period in which the PCM data is not occupied, the DX pin turns to Hi-impedance. In the long frame mode, the LSB bit turns to Hi-impedance at the faster edge of either FS falling edge or 9th rising edge of BCLK.

- PCM data input (DR)
DR is an input signal of 64Kbps PCM u/A-law data. The data is clocked by the falling edge of the BCLK and fed into the D/A block.

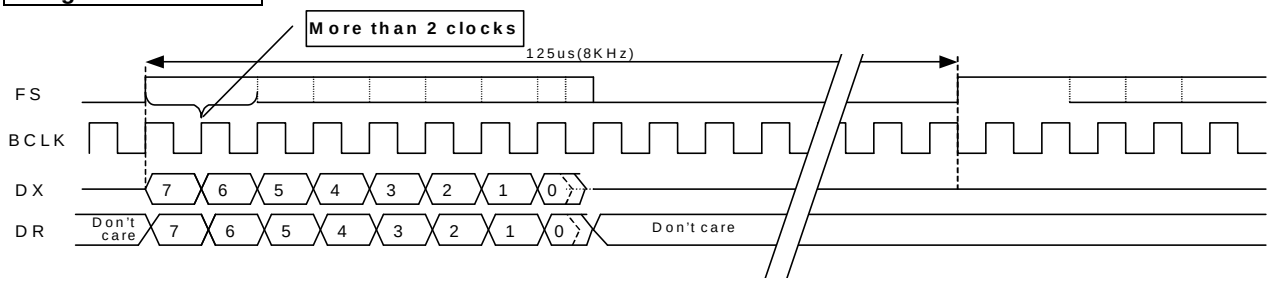
2-2-1-b LONG FRAME(LF) / SHORT FRAME (SF) Automatic selection

AK2308LV monitors the duration of the "H" level of FS and automatically selects LF or SF interface format.

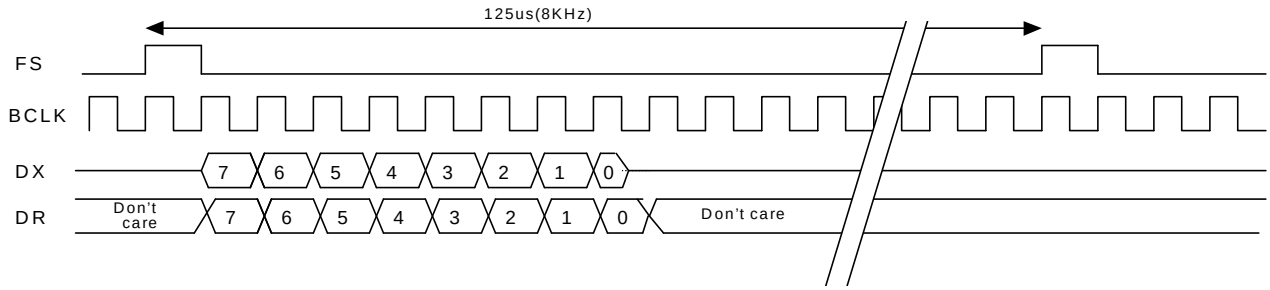
Period of FS="H"	Interface format
More than 2 clocks of BCLK	LF
1 clock of BCLK	SF

2-2-1-c Frame format of the interface

Long Frame format



Short Frame format



Notice FS must be 8kHz clock that is synchronized with BCLK.

2-2-2 16 bit Linear PCM data mode

In this mode the 16 bit linear PCM data are interfaced to the outside. This mode is useful to compress/extend the PCM data using much higher compress rate algorithm than u/A-law algorithm by the external DSP. The AK2308LV CODEC operates at 14bit accuracy, thus the least 2 bits are output as fixed value.

2-2-2-a Signals

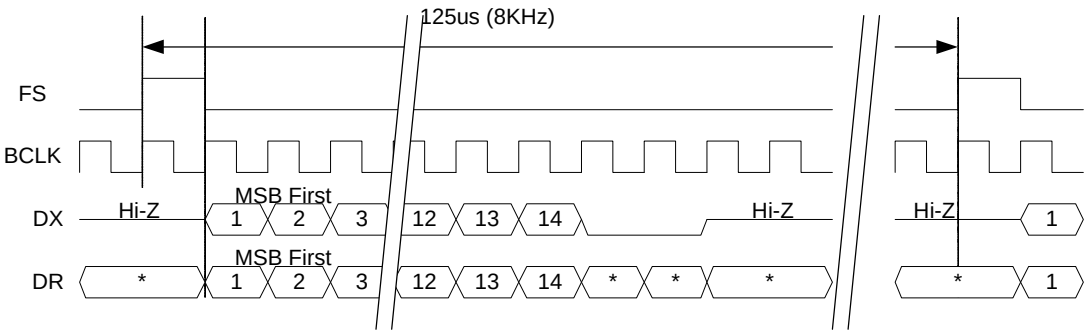
- Frame Sync signal (FS)
8kHz reference signal which is as same as in u/A-law PCM data mode. "H" level pulse width of the FS should be 1 clock period as same as in the short frame PCM mode.

- Bit Clock (BCLK)
BCLK defines the PCM data rate. BCLK can be varied from **128kHz to 2.048MHz by 64kHz step** which is different from in the u/A-law PCM data mode.

- PCM data output (DX)
DX is an output signal of 128Kbps linear PCM data. The data is synchronized to the BCLK which determines the data rate. In the period which the PCM data is not occupied, the DX pin turns to Hi-impedance output.

- PCM data input (DR)
DR is an input signal of 128Kbps linear PCM data. The data is clocked by the falling edge of the BCLK and fed into the D/A block.

16bti Linear Frame format



2-2-3 AK130 B1/B2 Mode

These modes are for connecting the PCM interface to AK130, AKM's TCM(ping-pong) transceiver for PBX/KTS system.
The PCM data format is A-law or u-law which can be selected by the register. The AK130 B1 mode interfaces the data to B1 channel, one of the B channel which AK130 provides, and the AK130 B2 mode interfaces the data to B2 channel.

2-2-3-a Signals

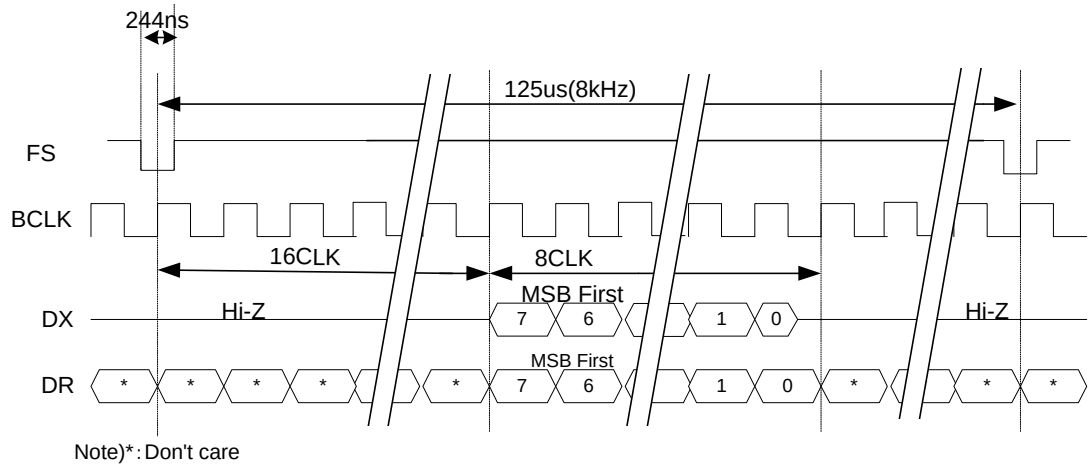
- Frame Sync signal (FS)
Please feed the FS signal which is generated by AK130.($\overline{F0o}$, pin#3)

- Bit Clock (BCLK)
BCLK defines the PCM data rate. Please use 2.048MHz clock which is generated by AK130.(E2o,pin#5)

- PCM data output (DX)
DX is an output signal of 128Kbps linear PCM data. Please connect to the PCM data input pin of AK130. (DSTi,pin#11)

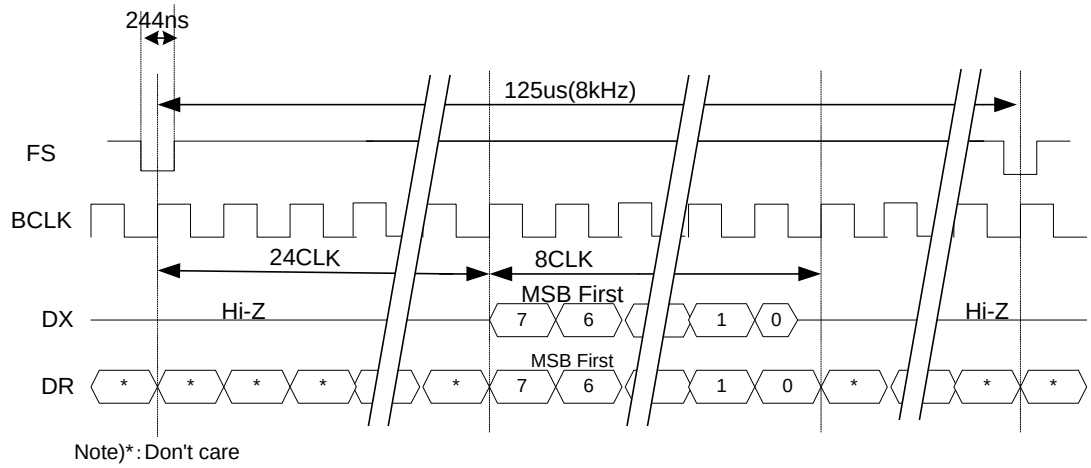
- PCM data input (DR)
DR is an input signal of 128Kbps linear PCM data. The data is clocked by the falling edge of the BCLK and fed into the D/A block. Please connect to the PCM data output pin of AK130. (DSTo,pin#6)

AK130 B1 Mode



Note)* : Don't care

AK130 B2 Mode



Note)* : Don't care

3. Path and Gain Controls

The voice path gain of both RX and TX side, and the tone path gain are controlled from the CPU registers.

3-1. Voice Path control switches;

AK2308LV has 7 analog switches to control the RX, TX analog path and Tone path. These switches are controlled from following "Path Control" register.

Path Control

Register Type : Read Write[Address:0000 D6-D0:(SW7-SW1)]

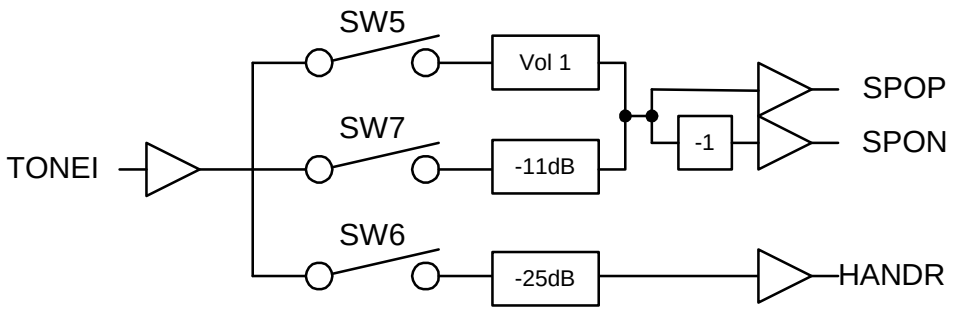
ADD	D7	D6	D5	D4	D3	D2	D1	D0
0	-	SW7	SW6	SW5	SW4	SW3	SW2	SW1
Default	0	0	0	0	0	0	0	0

Table3-a Switch function

SW Name	Function	Polarity
SW7	Speaker Tone enable 2	1: Tone output ON 0: Tone output OFF
SW6	Handset Tone select	1: Tone output ON 0: Tone output OFF
SW5	Speaker Tone enable 1	1: Tone output ON 0: Tone output OFF
SW4	RX Voice path enable for Handset	1: Voice path ON 0: Voice path OFF
SW3	RX speaker path enable	1: Speaker path ON 0: Speaker path OFF
SW2	TX MIC path enable	1: MIC path ON 0: MIC path OFF
SW1	TX Handset path enable	1: Handset path ON 0: Handset path OFF

Tone Path

When the tone signal is applied, please input the tone signal first, and then turn on the switches (SW7~5). Also when you want to stop the tone signal, please turn off the switches before stopping the tone signal. This is to prevent the pop noise when tone is turned off & on.



Notice

Please do not turn on the SW5 and SW7 simultaneously.

3-2 Voice path gain Controls

AK2308LV provides the RX and TX voice gain control functions both in analog domain and in digital domain. These gain can be controlled from following five registers.

3-2-1. RX voice path gain controls

RX side voice path has three gain control blocks. These gain stages are controlled through following three registers, “RX Digital Volume Control”, “RX Handset Volume Control” and “RX Speaker Control”.

RX Digital Volume Control

Register Type : Read Write[Address:0100 D4-D0(VRX4-VRX0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
4	-	-	-	VRX4	VRX3	VRX2	VRX1	VRX0
Default	0	0	0	0	0	0	0	0

VRX[4-0]; RX side digital volume from +15dB to –16dB by 1dB step.

VRX4	VRX3	VRX2	VRX1	VRX0	RX digital Attenuator	Comment
0	0	0	0	0	-16dB	default
0	0	0	0	1	-15dB	
0	0	0	1	0	-14dB	
0	0	0	1	1	-13dB	
0	0	1	0	0	-12dB	
0	0	1	0	1	-11dB	
0	0	1	1	0	-10dB	
0	0	1	1	1	-9dB	
0	1	0	0	0	-8dB	
0	1	0	0	1	-7dB	
0	1	0	1	0	-6dB	
0	1	0	1	1	-5dB	
0	1	1	0	0	-4dB	
0	1	1	0	1	-3dB	
0	1	1	1	0	-2dB	
0	1	1	1	1	-1dB	
1	0	0	0	0	0dB	
1	0	0	0	1	+1dB	
1	0	0	1	0	+2dB	
1	0	0	1	1	+3dB	
1	0	1	0	0	+4dB	
1	0	1	0	1	+5dB	
1	0	1	1	0	+6dB	
1	0	1	1	1	+7dB	
1	1	0	0	0	+8dB	
1	1	0	0	1	+9dB	
1	1	0	1	0	+10dB	
1	1	0	1	1	+11dB	
1	1	1	0	0	+12dB	
1	1	1	0	1	+13dB	
1	1	1	1	0	+14dB	
1	1	1	1	1	+15dB	

RX Handset Volume Control (Vol 2), RX Handset Volume Control (Vol 3)

Register Type : Read Write [Address:0111 D4-D0(V2_3-V2_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
6	-	-	V3_1	V3_0	V2_3	V2_2	V2_1	V2_0
default	0	0	0	0	0	0	0	0

V2_[3-0]; Analog volume for the RX side handset output (precise). The gain is variable from +8dB to –18dB by 2 dB step. The total gain control is done with V3_[1:0].

V2_3	V2_2	V2_1	V2_0	VOL2	Comment
0	0	0	0	-18dB	defult
0	0	0	1	-16dB	
0	0	1	0	-14dB	
0	0	1	1	-12dB	
0	1	0	0	-10dB	
0	1	0	1	-8dB	
0	1	1	0	-6dB	
0	1	1	1	-4dB	
1	0	0	0	-2dB	
1	0	0	1	0dB	
1	0	1	0	+2dB	
1	0	1	1	+4dB	
1	1	0	0	+6dB	
1	1	0	1	+8dB	
1	1	1	0	Forbidden	
1	1	1	1	Forbidden	

V3_[1-0]; Analog volume for the RX side handset output (coarse). The gain is variable from +6dB to –6dB by 6 dB step.

V3_1	V3_0	VOL3	Comment
0	0	-6dB	defult
0	1	0dB	
1	0	+6dB	
1	1	Forbidden	

RX Speaker Volume Control (Vol 1)

Register Type : Read Write [Address:0101 D3-D0(V1_3-V1_0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
5	-	-	-	-	V1_3	V!_2	V1_1	V1_0
default	0	0	0	0	0	0	0	0

V1_[3-0]; Analog volume for the RX Speaker output. The gain is variable from +12dB to –12dB by 2 dB step.

V1_3	V1_2	V1_1	V1_0	VOL1	Comment
0	0	0	0	-12dB	defult
0	0	0	1	-10dB	
0	0	1	0	-8dB	
0	0	1	1	-6dB	
0	1	0	0	-4dB	
0	1	0	1	-2dB	
0	1	1	0	0dB	
0	1	1	1	+2dB	
1	0	0	0	+4dB	
1	0	0	1	+6dB	
1	0	1	0	+8dB	
1	0	1	1	+10dB	
1	1	0	0	+12dB	
1	1	0	1	Forbidden	
1	1	1	0	Forbidden	
1	1	1	1	Forbidden	

3-2-2. TX voice path gain controls

TX side voice path has two gain control blocks. One is a analog volume and the other is a digital attenuator after D/A converter. These voice path gains are controlled through the following register.

TX Voice Path Gain Control (TX digital Attenuator, VOL 1)

Register Type : Read Write[Address:0010 D5−D0: (TX_pad, VTX4−VTX0)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
3	-	-	Tx_pad	VTX4	VTX3	VTX2	VTX1	VTX0
default	0	0	1	0	0	0	0	0

VTX[4-0]; The digital attenuator for TX side voice path. The gain variation is from +15dB to –16dB by 1dB step.

VTX4	VTX3	VTX2	VTX1	VTX0	TX digital Attenuator	Comment
0	0	0	0	0	-16dB	default
0	0	0	0	1	-15dB	
0	0	0	1	0	-14dB	
0	0	0	1	1	-13dB	
0	0	1	0	0	-12dB	
0	0	1	0	1	-11dB	
0	0	1	1	0	-10dB	
0	0	1	1	1	-9dB	
0	1	0	0	0	-8dB	
0	1	0	0	1	-7dB	
0	1	0	1	0	-6dB	
0	1	0	1	1	-5dB	
0	1	1	0	0	-4dB	
0	1	1	0	1	-3dB	
0	1	1	1	0	-2dB	
0	1	1	1	1	-1dB	
1	0	0	0	0	0dB	
1	0	0	0	1	+1dB	
1	0	0	1	0	+2dB	
1	0	0	1	1	+3dB	
1	0	1	0	0	+4dB	
1	0	1	0	1	+5dB	
1	0	1	1	0	+6dB	
1	0	1	1	1	+7dB	
1	1	0	0	0	+8dB	
1	1	0	0	1	+9dB	
1	1	0	1	0	+10dB	
1	1	0	1	1	+11dB	
1	1	1	0	0	+12dB	
1	1	1	0	1	+13dB	
1	1	1	1	0	+14dB	
1	1	1	1	1	+15dB	

TX_pad: The digital attenuator for TX side voice path. The gain variation is 0dB or –14dB

TX_pad	TX digital pad	Comment
0	0dB	
1	-14dB	default

3-2-3. Side Tone path gain controls

AK2308LV provides the side tone pass from TX to RX in digital domain. The activation of this pass is set through “Side Tone” bit and the side tone attenuation is controlled through “Side Tone digital attenuator gain” register.

Side Tone Control, Side Tone digital attenuator gain

Register Type : Read Write[Address:0010 D4-D0:(Side_Tone, Side Tone digital attenuator gain)]

ADD	D7	D6	D5	D4	D3	D2	D1	D0
2	-	-	-	Side Tone	VSD_3	VSD_2	VSD_1	VSD_0
default	0	0	0	0	1	1	1	1

Side Tone; A pass enable of the side tone from TX to RX.

Name	Porarity		Comment
Side Tone	0	OFF	default
	1	ON	

VSD_[3-0]; Side tone digital Attenuator. The gain variation range is from –12dB to –57dB.

VSD_3	VSD_2	VSD_1	VSD_0	Side Tone digital Attenuator gain	Comment
0	0	0	0	-12dB	
0	0	0	1	-15dB	
0	0	1	0	-18dB	
0	0	1	1	-21dB	
0	1	0	0	-24dB	
0	1	0	1	-27dB	
0	1	1	0	-30dB	
0	1	1	1	-33dB	
1	0	0	0	-36dB	
1	0	0	1	-39dB	
1	0	1	0	-42dB	
1	0	1	1	-45dB	
1	1	0	0	-48dB	
1	1	0	1	-51dB	
1	1	1	0	-54dB	
1	1	1	1	-57dB	default

4. Power on Reset

Power on Reset
AK2308LV automatically generates the internal reset pulse wh ich resets all the circuit that is necessary to start the initialization after the power on reset. The CPU registers are set to the default value.

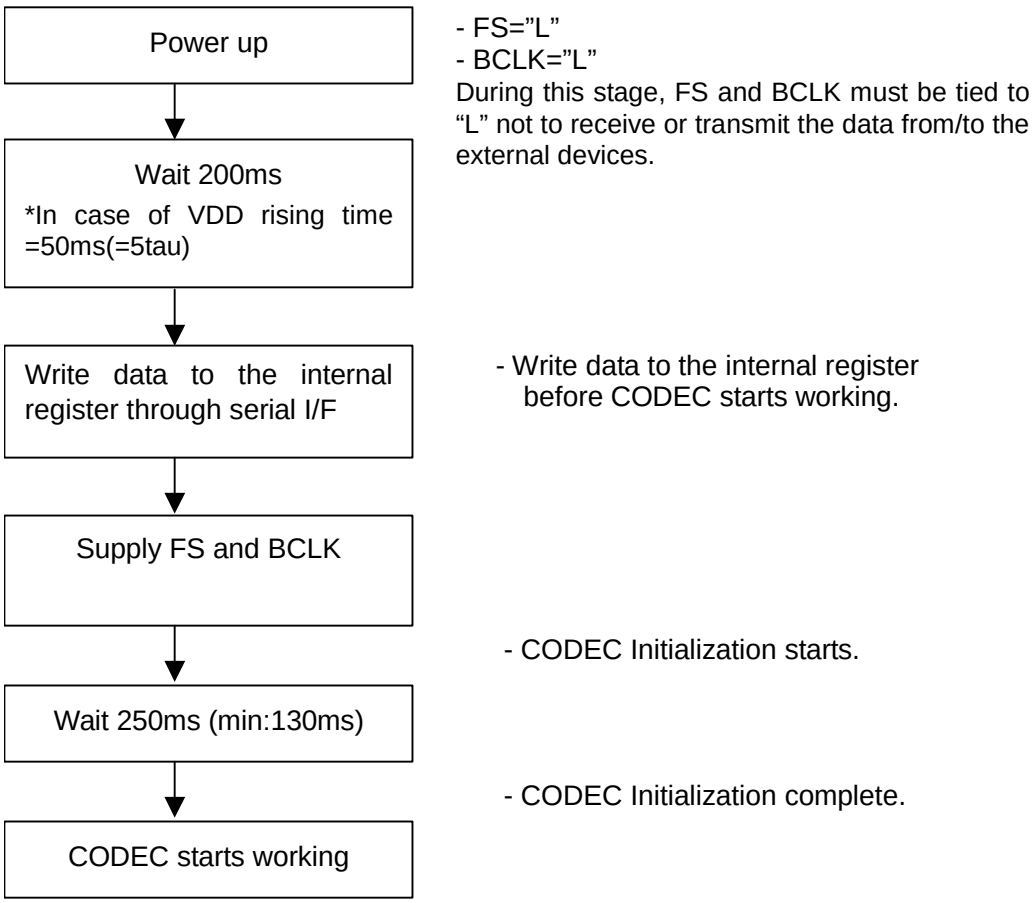
After the internal reset pulse is generated, CODEC starts the initialization procedure by being fed FS signa l, and it takes 150ms(typ.), 330ms(max) to complete the initialization after the detection of power on.

Power up slope to enable the Power-on Reset
When the power-up slope is no longer than 50ms(=5tau:tau is time constant), Power On Reset works normally.

When the slope is longer than 50ms, Power On Reset may not be activated and no internal registers are initialized. In this case all registers must be written through CPU interface.

NOTE) For the stable operation after power up, we recommend to write all register value through CPU interface in any case after the power up.

Recommended start up procedure
The following start up procedure is recommended when AK2308LV is going to power up.



ELECTRICAL CHARACTERISTICS

Unless otherwise noted, guaranteed for VDD=+3.3V+/-0.3V(AK2308LV), Ta = –10 ~ +85 °C, FS=8kHz.

♦DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Consumption BCLK=2048kHz	Idd	* Note1)	-	17	26	mA
Output High Voltage (CMOS level)	V_{OH}	I_{OH}=-1.6mA	VDD-0.5			V
Output Low Voltage (CMOS level)	V_{OL}	I_{OL}=1.0mA			0.4	V
Input High Voltage1 (CMOS level)	V_{IH1}		0.7VDD			V
Input Low Voltage1 (CMOS level)	V_{IL1}				0.3VDD	V
Analog Ground (RAGND) Output Voltage	VRG	Maximum output current ±100μA	1.4	1.5	1.6	V
Input Leakage Current	Ii		-10		+10	μA
Output Leakage Current	Io	Tri-state mode	-10		+10	μA

*Note1) All the output pins are unloaded. 1020Hz@0dBm0 sine wave from HANDT1,2, and A to A loop-backed to HANDR.
All the volume gains are set to 0dB. The handset mic and receiver paths are only active.

♦AC Characteristics

Note) Otherwise specified, Ta=-10℃～+70 degree, VDD=3.3V +/- 0.3V(AK2308LV), VSS=0V, FS=8kHz are assumed. All the timing parameters are measured at VOH=VDD-0.5, VOL=0.4V.

PCM Interface

u/A-law mode（Long Frame ,Short Frame） & Linear PCM mode

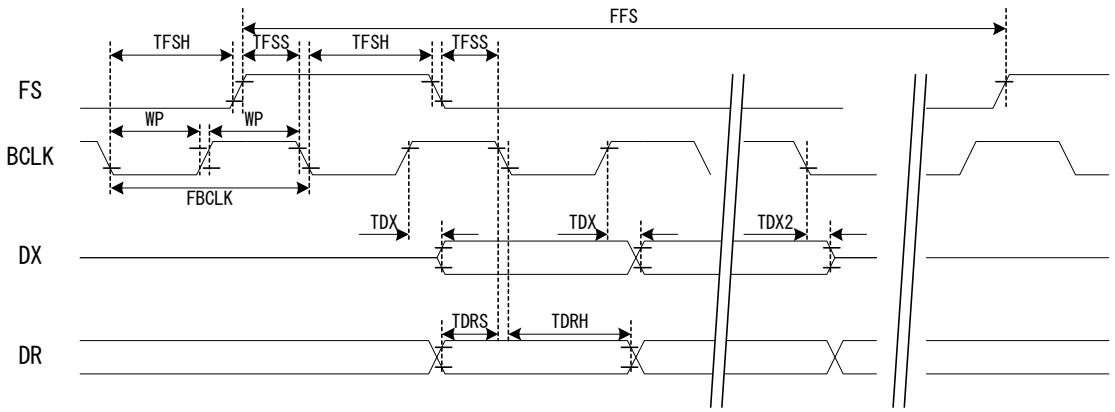
Items	Pin Name	Parm.	Conditions	MIN	TYP	MAX	Unit
FS frequency	FS	FFS	-	-	8	-	kHz
BCLK frequency Note1)	BCLK	FBCLK	-	-	64×N	-	kHz
Clock width	BCLK	WP	-	100	-	-	ns
Falling/rising time	FS,BCLK,DR	TD	-	-	-	40	ns
Output delay	DX	TDX	Cl=50pF	-	-	60	ns
	DX	TDX2	Cl=50pF	10	-	60	ns
Setup time	FS	TFSS	-	100	-	-	ns
	DR	TDRS	-	100	-	-	ns
Hold time	FS	TFSH	-	100	-	-	ns
	DR	TDRH	-	100	-	-	ns
FS Low level width	FS	TWLFS	-	1	-	-	BCLK

Note1） Short Frame, Long Frame:64 x N kHz (N=1 to 32), Linear mode:64 x N kHz(N=2 to 32)

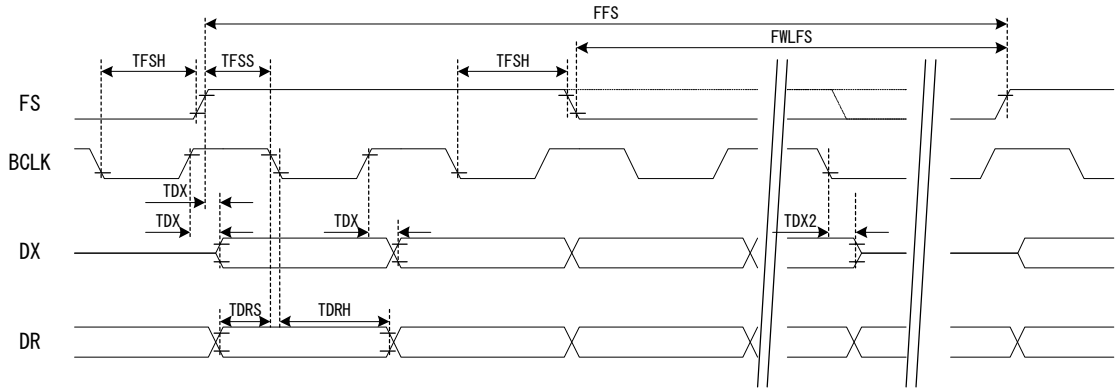
AK130 B1ch/B2ch mode

Items	Pin Name	Parm.	Conditions	MIN	TYP	MAX	Unit
FS frequency	FS	FFS	-	-	8	-	kHz
Clock frequency	BCLK	FBCLK	-	-	2.048	-	kHz
Pulse width	BCLK	WP	-	-	244	-	ns
Falling/Rising time	FS,BCLK,DR	TD	-	-	-	40	ns
Output delay	DX	TDX	CL=50pF	-	-	60	ns
	DX	TDX2	CL=50pF	10	-	60	ns
Setup time	FS	TFSS	-	100	-	-	ns
	DR	TDRS	-	100	-	-	ns
Hold time	FS	TFSH	-	100	-	-	ns
	DR	TDRH	-	100	-	-	ns

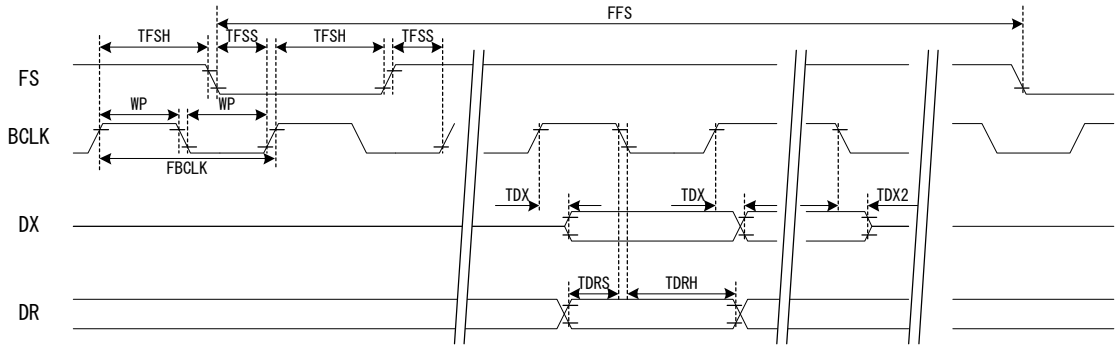
u/A-law PCM mode（Short Frame） & Linear PCM mode



u/A law PCM mode（Long Frame）



AK130 B1ch/B2ch mode

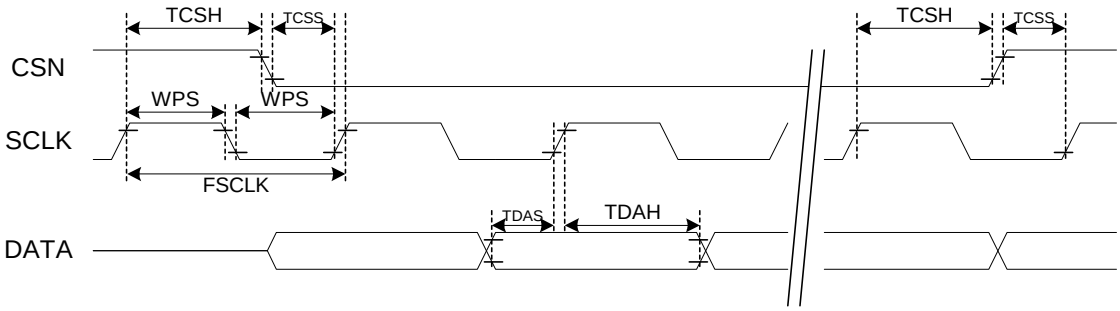


CPU I/F

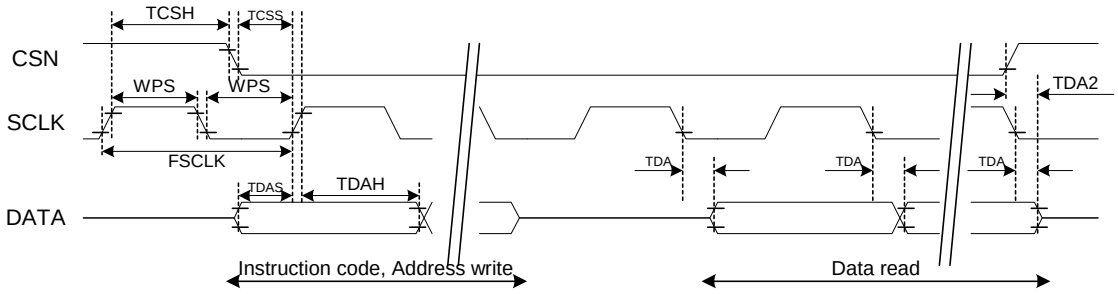
Items	Pin Name	Parm.	Conditions	MIN	TYP	MAX	Unit
SCLK pulse width*	SCLK	WPS	-	60	-	-	ns
Falling/rising time	CSN,SCLK	TD	-	-	-	40	ns
Output delay	DATA	TDA	CL=15pF	-	-	150	ns
	DATA	TDA2	CL=15pF	-	-	150	Ns
Setup time	CSN	TCSS	-	60	-	-	ns
	DATA	TDAS	-	60	-	-	ns
Hold time	CSN	TCSH	-	60	-	-	ns
	DATA	TDAH	-	60	-	-	ns

Note) ex; maximum SCLK=5. 0MHz(@50% duty), 4.34MHz(@40/60% duty)

Data write cycle



Data read cycle



♦CODEC

Absolute Gain (AK2308LV:VDD=3.3V +/-0.3V)

Parameter	Conditions		Min	Typ	Max	Units
Analog Input Level	HANDT3 to DX MIC3 to DX	1020Hz 0dBm0 input		0.101		Vrms
Absolute Transmit Gain	1020Hz dBm0 input	u/A-law	-1.5	-	+1.5	dB
Maximum input level		3.17dBm0(u-law) 3.14dBm0(A-law)		0.145		Vrms
Analog Output Level	DR to DAOUT 1020Hz 0dBm0 input			0.482		Vrms
Absolute Receive Gain			-1.5	-	+1.5	dB
Maximum Overload Level	DR to DAOUT +3.14dBm0 input			0.694		Vrms

Gain Tracking

Parameter	Conditions		Min	Typ	Max	Units
Transmit Gain Tracking Error	Reference Level:	-51dBm0 ~-46dBm0	-0.9	-	0.9	
(A to D)	-10dBm0	-46dBm0 ~-36dBm0	-0.6	-	0.6	dB
HANDT3 to DX, MIC3 to DX	1020Hz Tone	-36dBm0 ~ 0dBm0	-0.4	-	0.4	
Receive Gain Tracking Error	Reference Level:	-51dBm0 ~-46dBm0	-0.9	-	0.9	
(D to A)	-10dBm0	-46dBm0 ~-36dBm0	-0.6	-	0.6	dB
DR to DAOUT	1020Hz Tone	-36dBm0 ~ 0dBm0	-0.4	-	0.4	

The characteristics from MIC3 to DR path is guaranteed by the design.

Frequency Response

Parameter	Conditions		Min	Typ	Max	Units
Transmit Frequency Response	Relative to:	0.06kHz	24	-	-	
(A to D)	0dBm0@1020Hz	0.2kHz	0	-	2.5	
		0.3 ~3.0kHz	-0.3	-	0.3	dB
HANDT3 to DX		3.4kHz	0	-	0.8	
MIC3 to DX		3.78kHz	6.5	-	-	
Receive Frequency Response	Relative to:	0.3K ~3.0kHz	-0.3	-	0.3	
(D to A)	0dBm0@1020Hz	3.4kHz	0	-	0.8	dB
DR to DAOUT		3.78kHz	6.5	-	-	

Distortion

Parameter	Conditions		Min	Typ	Max	Units
Transmit Signal to Distortion	1020Hz Tone	-36dBm0 ~-41dBm0	24	-	-	
(D to A)		-26dBm0 ~-36dBm0	29	-	-	dB
HANDT3 to DX MIC3 to DX		0dBm0 ~-26dBm0	35	-	-	
Receive Signal to Distortion	1020Hz Tone	-36dBm0 ~-41dBm0	24	-	-	
(A to D)		-26dBm0 ~-36dBm0	29	-	-	dB
DR to DAOUT		0dBm0 ~-26dBm0	35	-	-	

Note) C-message Weighted for u-Law, Psophometric Weighted for A-Law

Noise

Parameter	Conditions	Min	Typ	Max	Units
Idle Channel Noise [1)] AtoD HANDT1,2 to DX MIC2 to DX	u-law, C-message	-	8	16	dBrnC0
	A-law, Psophometric	-	-82	-74	dBm0p
Idle Channel Noise [2)] DtoA DR to DAOUT	u-law, C-message	-	2	9	dBrnC0
	A-law, Psophometric	-	-88	-81	dBm0p
Idle Channel Noise [2)] DtoA DR to HANDR DR to SPOP/SPON	u-law, C-message	-	3	10	dBrnC0
	A-law, Psophometric	-	-87	-80	dBm0p

Note 1) Analog Input = Analog Ground. The gain of Handset MIC and MIC input is assumed as +25dB.
SCLK is not supplied.
Note 2) Digital Input(DR) = +0 Code

Interchannel Crosstalk

Parameter	Conditions	Min	Typ	Max	Units
Transmit to Receive HANDT3 to DAOUT MIC3 to DAOUT	0dBm0@HANDT4, Idle PCM code@DR	-	-70	-	dB
Receive to Transmit DX to DR	0dBm0 code@DR, HANDT4 = 0 Vrms	-	-70	-	dB

♦Voice Path

RX voice path Volume

Parameter	Volume	Conditions	Min	typ	max	Unit
Step margin	VOL1 +12to-12dB	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0*)	dB
	VOL2 +8to-12dB -14to-18dB	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0*)	dB
			-1.5	0	+1.5	
	VOL3 +6/0/-6dB	1020Hz 0dBm0 input at DR Relative to: 0dB	-1.0	0	+1.0	dB

*)Monotonus increase/decrease is guaranteed

RX Amp for Handset receiver

Parameter		Conditions	MIN	TYP	MAX	Unit
SINAD	HANDI to HANDR	1.0Vp-p@1020Hz input (0 to 30kHz)	40	-		dB
Gain error			-1.5	0	+1.5	
Gain error	TONEI to HANDR (-25dB gain)	1.0Vp-p@1020Hz input (0 to 30kHz)	-2	0	+2	
Signal attenuation of speaker mute	HANDI to HANDR	2.0Vp-p@1020Hz input SW4: 0 to 1	60	-	-	
	TONEI to HANDR	1.0Vp-p@1020Hz input SW6:0 to 1	40	-	-	

RX Amp for Speaker output

Parameter		Conditions	MIN	TYP	MAX	Unit
SINAD	SPI to SPOP/SPOP	1.0Vp-p@1020Hz input (0 to 30kHz)	40	-		dB
Gain error			-1.5	0	+1.5	
Gain error	TONEI to SPOP/SPON	1.0Vp-p@1020Hz input (0 to 30kHz)	-1.5	0	+1.5	
Signal attenuation of speaker mute	SPI to SPOP/SPON	2.0Vp-p@1020Hz input SW3: 0 to 1	60	-	-	
	TONEI to SPOP/SPON	1.0Vp-p@1020Hz input SW5:0 to 1, SW7: 0 to 1	60	-	-	

RX Amp

Parameter		Conditions	MIN	TYP	MAX	Unit
SINAD	RAI to RAO	0.564Vp-p@1020Hz input, +11dB setting (0 to 30kHz)	40	-		dB
Gain error			-1.5	0	+1.5	
gain		Invert amplifier	5	0	11	

TX Amp for Handset / MIC Amp

Parameter		Conditions	MIN	TYP	MAX	Unit
SINAD	HANDT2 to HANDT1, MIC2 to MIC1	0.023Vp-p@1020Hz input, +25dB setting (0 to 30kHz)	40	-		dB
Gain error			-1.5	0	+1.5	
gain		Invert amplifier	0	0	25	

TX path switching summing amplifier characteristics

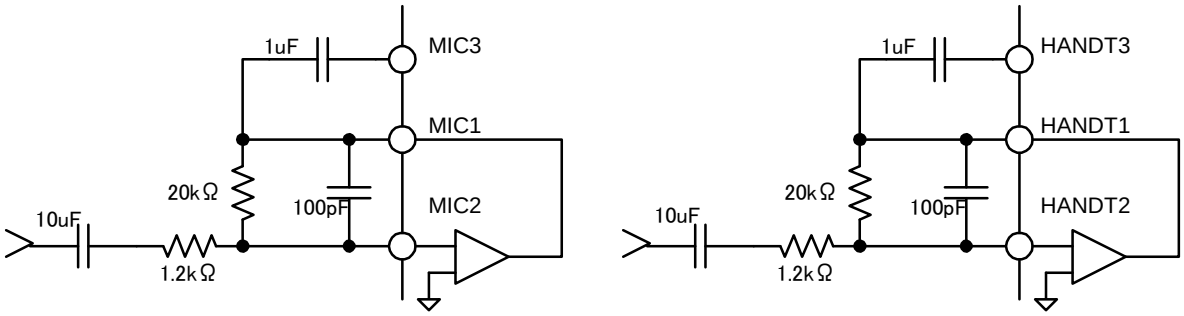
Parameter		Conditions	MIN	TYP	MAX	Unit
Signal attenuation of path switching	HANDT3 to DX	1020Hz@0dBm0 input SW1: 0 to 1	60	-	-	dB
	MIC3 to DX	1020Hz@0dBm0 input SW2: 0 to 1	60	-	-	

Input impedance

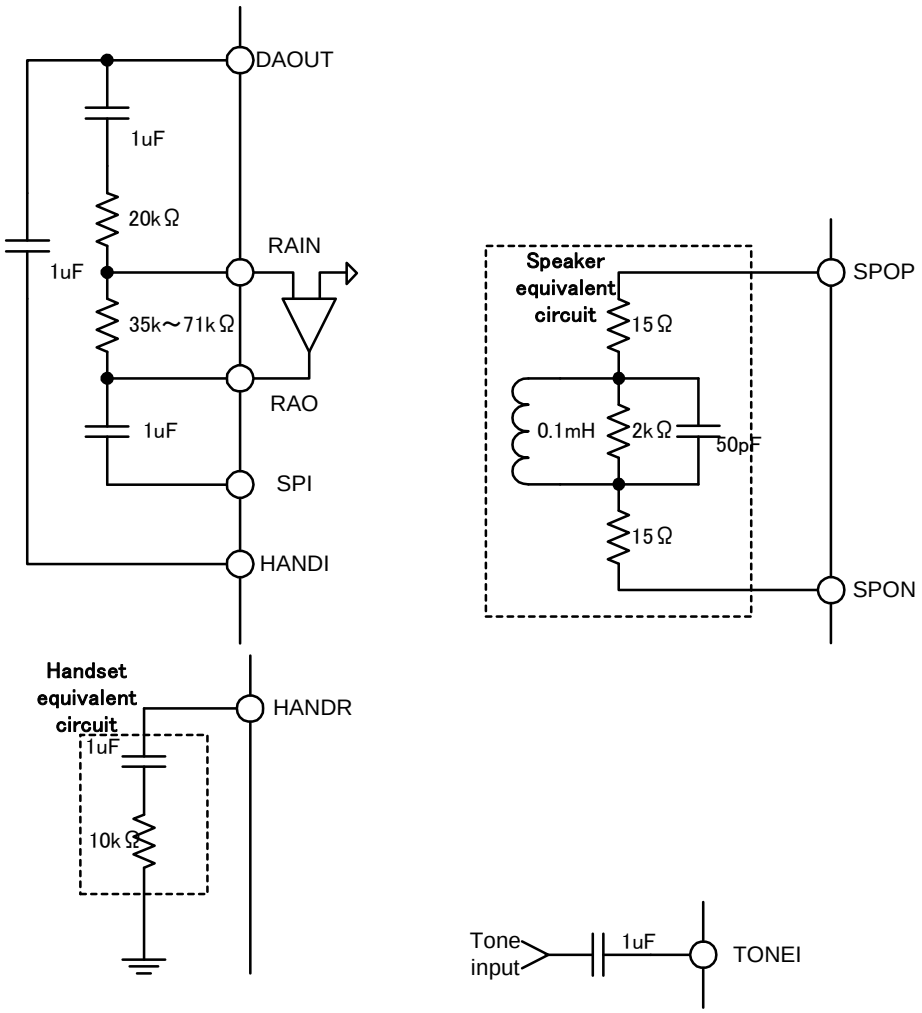
Parameter		Conditions	MIN	TYP	MAX	Unit
Input impedance	HANDT3		7	10	15	kΩ
	MIC3		7	10	15	kΩ
	RAI		1	-	-	MΩ
	SPI		52	75	113	kΩ
	HANDI		70	100	150	kΩ
	TONEI		70	100	150	kΩ

APPLICATION CIRCUIT EXAMPLE

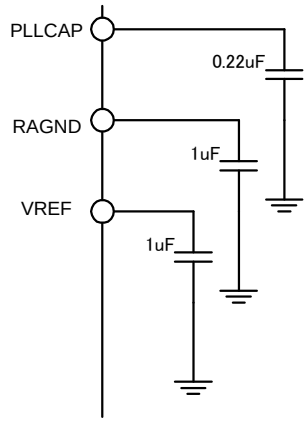
I Transmit side pins



I Receive side pins

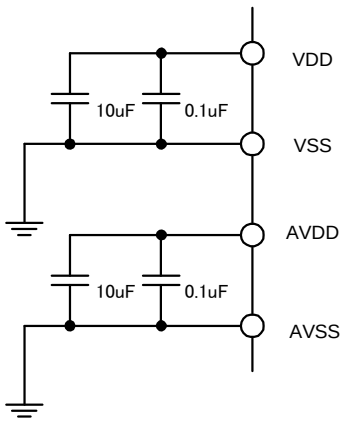


l Analog Ground, PLLCAP



Please place the capacitor closer to the pins.

l Power Supplies



Please adjust capacitors in response to the noise environment on the power source.

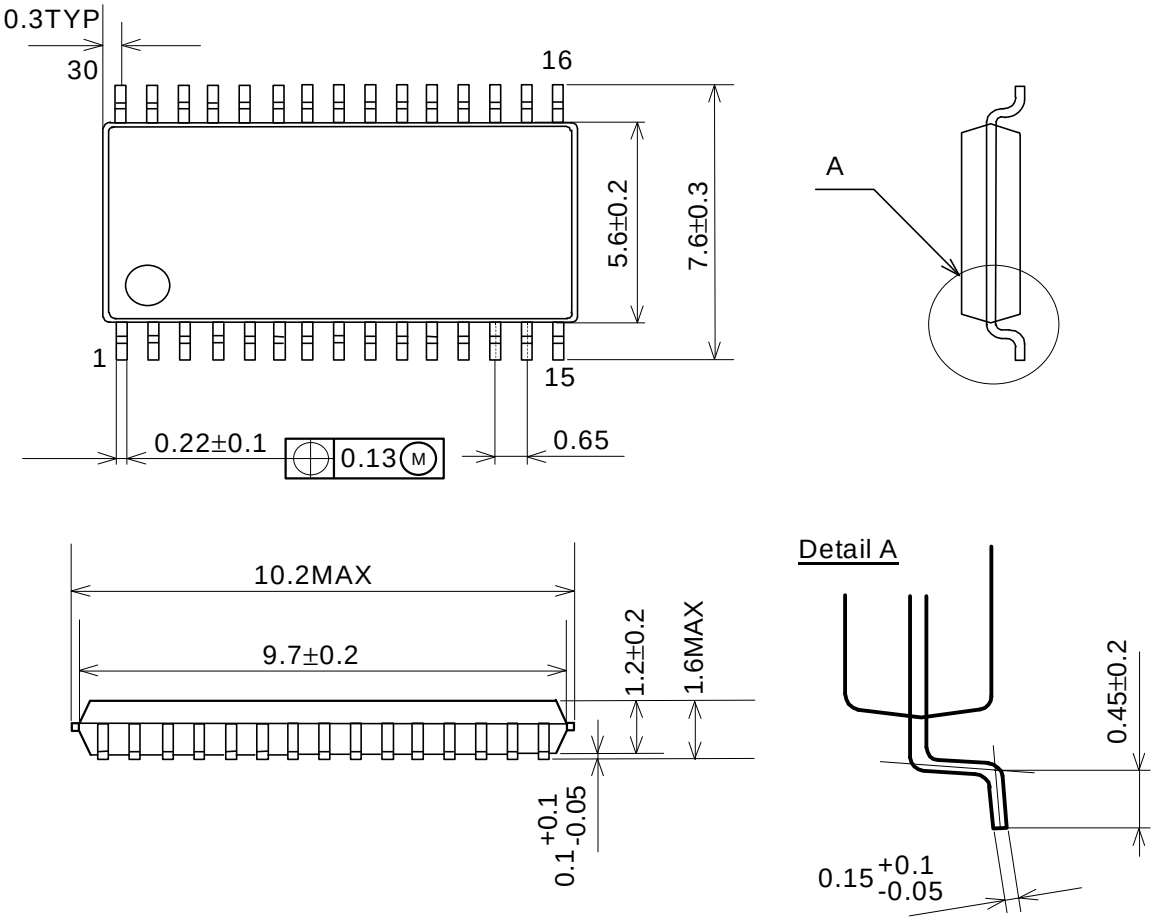
PACKAGE

30pin VSOP
Marking
(1) Pin#1 indicator
(2) Date code: XXXXXXX (7digit)
(3) Marketing code: AK2308LV
(4) AKM Logo

AK2308LV

Package dimensions

30pin VSOP (Unit: mm)



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