NEC ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD3575

1 024 BIT CCD LINEAR IMAGE SENSOR

The μPD3575D is a 1 024 bit linear image sensor capable of converting light into voltage. It is a charge coupled device (CCD). This product has a built-in driving circuit, as well as a 1 024-bit photo sensor array and two 525 bit CCD charge transfer registors to reduce peripheral circuits.

FEATURES

- Built-in driving circuit capable of directly driving TTL loads.
- Built-in output signal amplifier and sample hold circuit.
- High sensitivity: 10 times as sensitive as our conventional products (μPD795AD) under white fluorescent lighting.
- Peak sensitivity: green 550 nm.
- Data rate: capable of high-speed driving at a rate of 3 MHz.
- Capable of reading the shorter side of a B6 size sheet at a rate of 8 dots/mm.
- Driven by a single 12 volts power source.
- Pin-compatible with the μPD795AD.

ORDERING INFORMATION

Part Number	Package
μPD3575D	22 PIN Cer DIP (400 mil)

BLOCK DIAGRAM

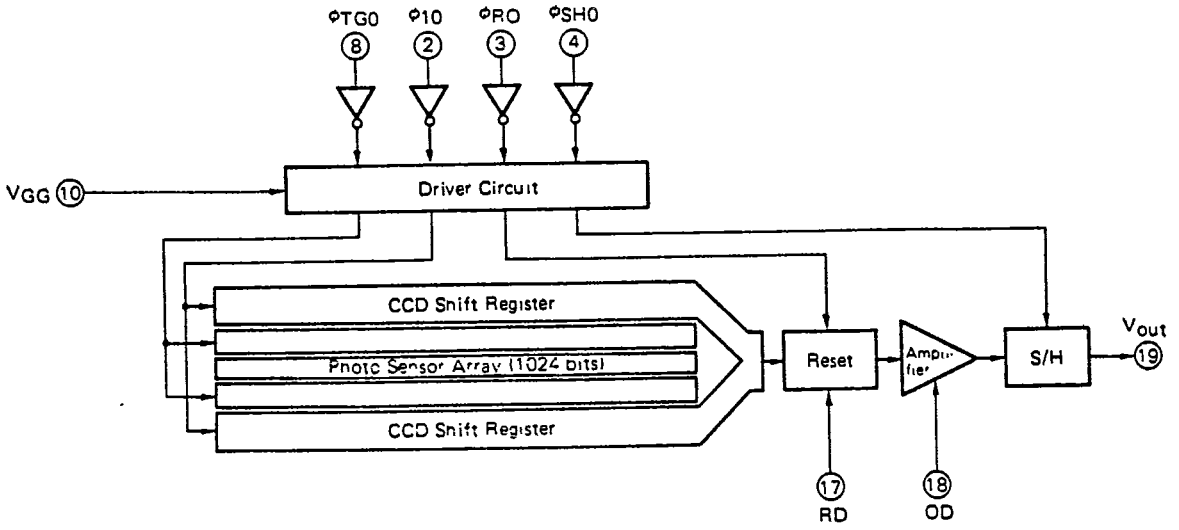
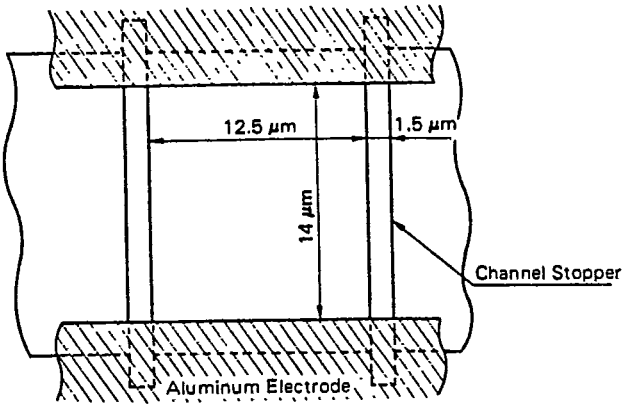
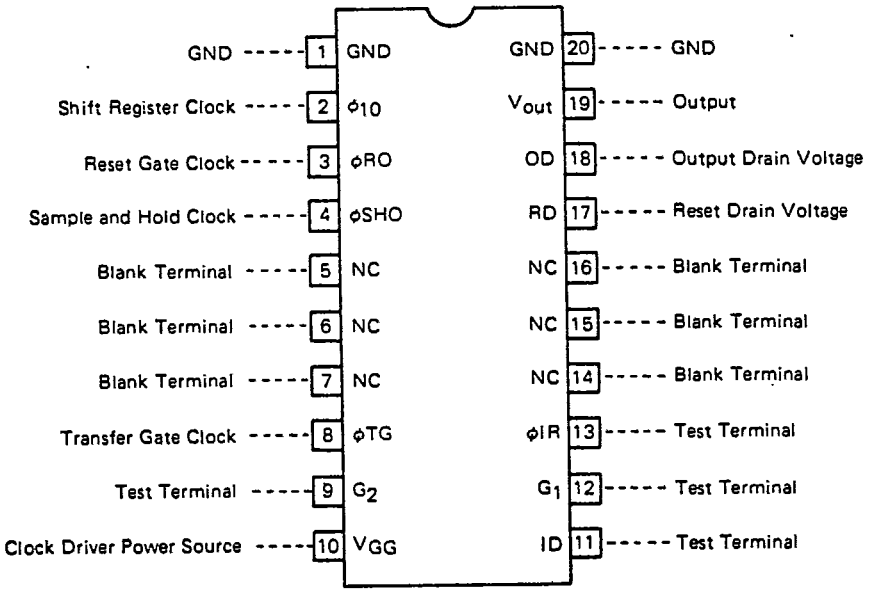


PHOTO ELEMENT CONFIGURATION DIAGRAM



TERMINAL CONNECTION DIAGRAM



T-41-55

ABSOLUTE MAXIMUM SPECIFICATIONS (T_a = 25 °C)

Output Drain Voltage	V_{OD}	−0.3 to +15	V
Reset Drain Voltage	V_{RD}	−0.3 to +15	V
Output Gate Bias Voltage	V_{OG}	−0.3 to +15	V
Driver Power Source Voltage	V_{GG}	−0.3 to +15	V
Shift Register Clock Signal Voltage	V_{10}	−0.3 to +15	V
Reset Signal Voltage	V_{R0}	−0.3 to +15	V
Sample and Hold Signal Voltage	V_{SH0}	−0.3 to +15	V
Transfer Gate Signal Voltage	V_{TG}	−0.3 to +15	V
Operational Temperature	T_{opt}	−25 to +55	°C
Storage Temperature	T_{stg}	−40 to +100	°C

RECOMMENDED OPERATION CONDITIONS (T_a = −25 ~ +55 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output Drain Voltage	V_{OD}	11.4	12.0	12.6	V
Reset Drain Voltage	V_{RD}	11.4	12.0	12.6	V
Test Terminal G_1 Voltage	V_{G1}		0		V
Test Terminal G_2 Voltage	V_{G2}		0		V
Test Terminal ID Voltage	V_{ID}		12.0		V
Test Terminal ϕ_{R1} Voltage	$V_{\phi R1}$		0		V
Shift Register Clock Signal High Level	$V_{\phi 10H}$	2.4	4.5	5.5	V
Shift Register Clock Signal Low Level	$V_{\phi 10L}$	−0.3	0	0.5	V
Reset Signal High Level	$V_{\phi ROH}$	2.4	4.5	5.5	V
Reset Signal Low Level	$V_{\phi ROL}$	−0.3	0	0.5	V
Sample and Hold Signal High Level	$V_{\phi SHOH}$	2.4	4.5	5.5	V
Sample and Hold Signal Low Level	$V_{\phi SHOL}$	−0.3	0	0.5	V
Transfer Gate Signal High Level	$V_{\phi TGH}$	2.4	4.5	5.5	V
Transfer Gate Signal Low Level	$V_{\phi TGL}$	−0.3	0	0.5	V
Driving Power Source Voltage	V_{GG}	11.4	12.0	12.6	V
Data Rate	$f_{\phi RO}$		1	3	MHz

ELECTRIC CHARACTERISTICS

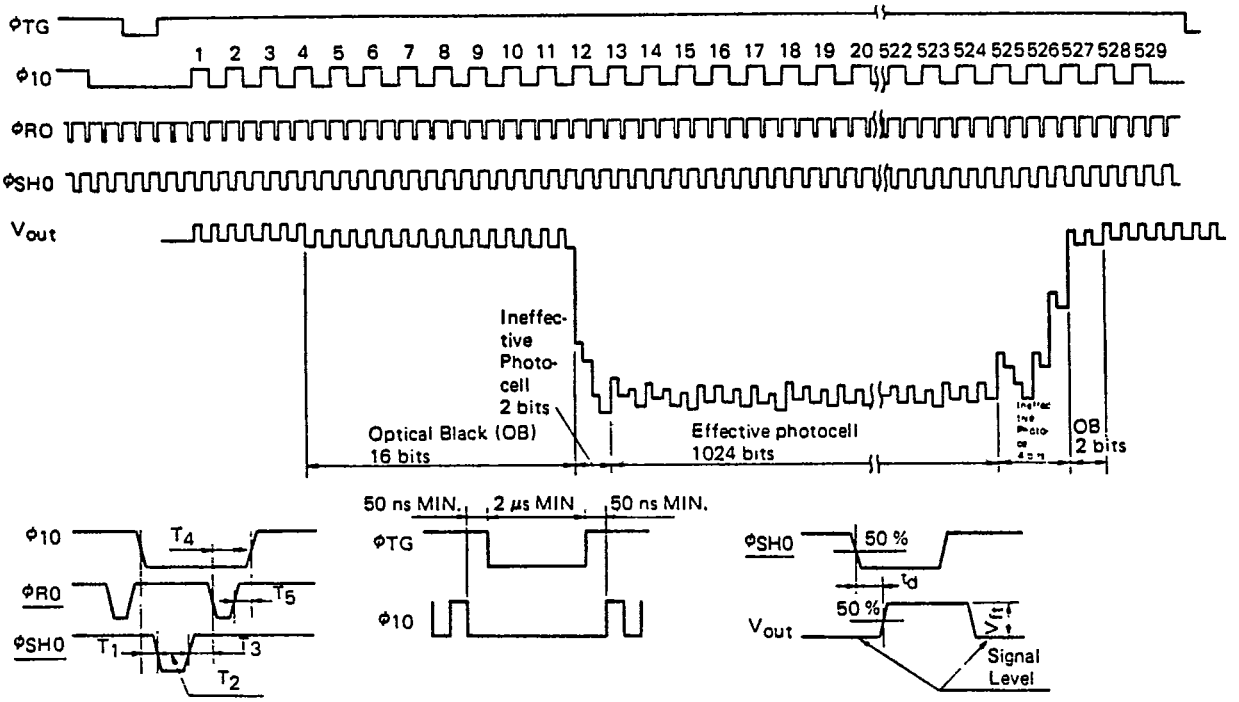
T-41-55

(T_a = 25 °C; V_{OD} = V_{RD} = V_{GG} = 12.0 V; $f_{\phi 10}$ = 250 kHz; Storage Time = 10 ms, $f_{\phi RO}$ = 500 kHz; Light Source: 2856 K Tungsten-Filament Lamp.)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Saturation Output Voltage	V_{sat}	1.5	2.3		V	
Saturation Exposure	SE		0.46		Lux·s	White Fluorescent Lamp
Photoresponse Non-uniformity	PRNU		±5	±10	%	V_{out}: 500 mV, White Fluorescent Lamp.
Average Dark Signal	ADS		0.5	10	mV	No exposure
Dark Signal Non-uniformity	DSNU		0.5	10	mV	No exposure
Power Consumption	P_W	50	100	200	mV	
Output Impedance	Z_O	0.5	1	2	kΩ	
Responsivity	R	9.8	14	18.2	V/Lux·s	2856 K Tungsten-Filament Lamp
	R	3.5	5	6.5	V/Lux·s	White Fluorescent Lamp
Peak Responsivity Wave Length			550		nm	
Offset Level	V_{OS}	4.0	7.0	8.5	V	
Shift Register Clock Terminal Input Capacity	$C_{\phi 10}$		5	10	pF	
Reset Terminal Input Capacity	$C_{\phi RO}$		5	10	pF	
Sample and Hold Terminal Input Capacity	$C_{\phi SHO}$		5	10	pF	
Transfer Gate Signal Terminal Input Capacity	$C_{\phi TG}$		5	10	pF	
Feed-through Level	V_{ft}		100	200	mV	
Output Rise Delay Time	t_d		50	100	ns	
Output Rise Time	t_r		50	100	ns	
Output Fall Time	t_f		50	100	ns	

T-41-55

TIMING CHART



Note: To operate this in the range of $f_{\phi RO}$ equal to or less than 1 MHz, use timing which equals or exceeds the TYP value.

	MIN.	TYP.
T_1	200	300
T_2	100	300
T_3	3	100
T_4	30	100
T_5	0	50

(ns)

T-41-55

DEFINITION OF CHARACTERISTICS

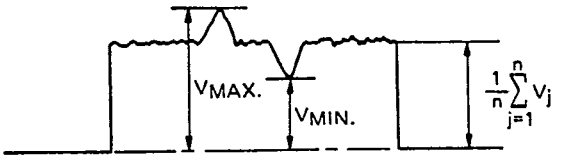
1. Saturation Voltage: V_{sat}
   The voltage at which the sensitivity is become nonlinear.

2. Saturation Exposure: SE
   The product of the illuminance (IX) and storage time (s) when the output saturates.

3. Photo Response Non-uniformity: PRNU
   The ratios of peak/bottom of the photo response to the average output voltage of all the effective bits which is given by the following equation:

$$PRNU\ (\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

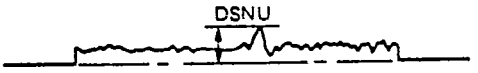
   n : Number of Effective Bits
   V_j : Output Voltage of the Respective Bit



4. Average Dark Signal: ADS
   The average output voltage with the light blocked; given by the following equation:

$$ADS\ (mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. Dark Signal Non-uniformity: DSNU
   The ratio of the peak output voltage to the invalid voltage when the light is blocked.



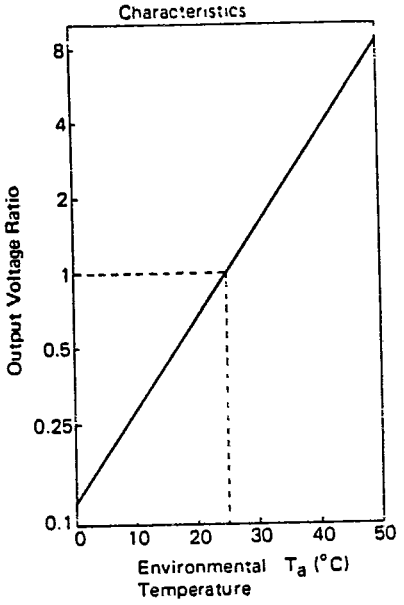
6. Output Impedance: Z_O
   The output terminal impedance (seen from outside).

7. Response: R
   The output voltage divided by the exposure (lx·s).
   The response differs from this when a light source other than that described in the electrical characteristics section is used.

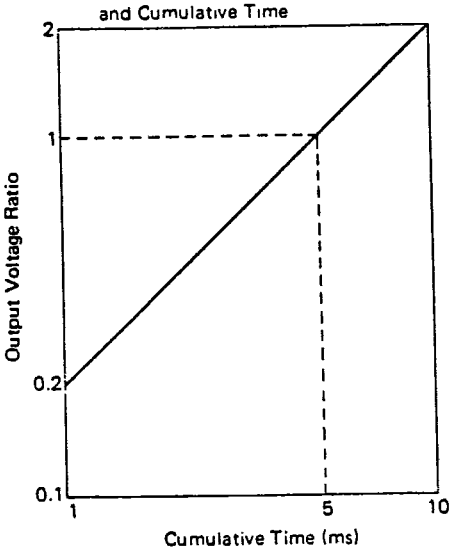
TYPICAL PERFORMANCE CHARACTERISTICS (T_a = 25 °C)

T-41-55

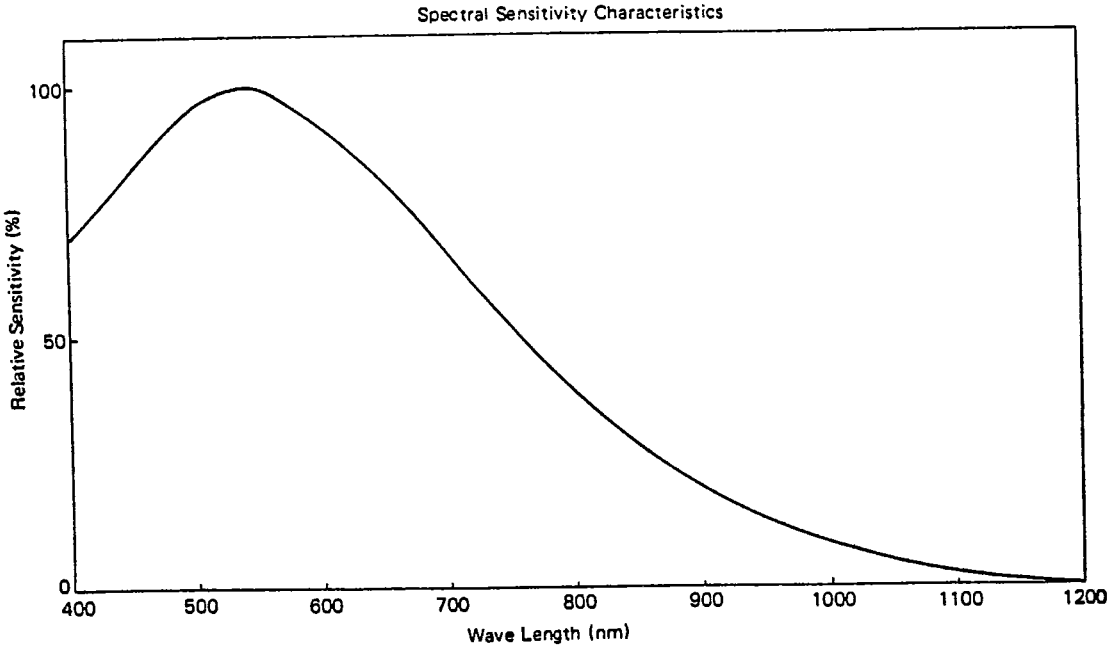
Dark Signal Temperature Characteristics



Output Voltage Characteristics and Cumulative Time

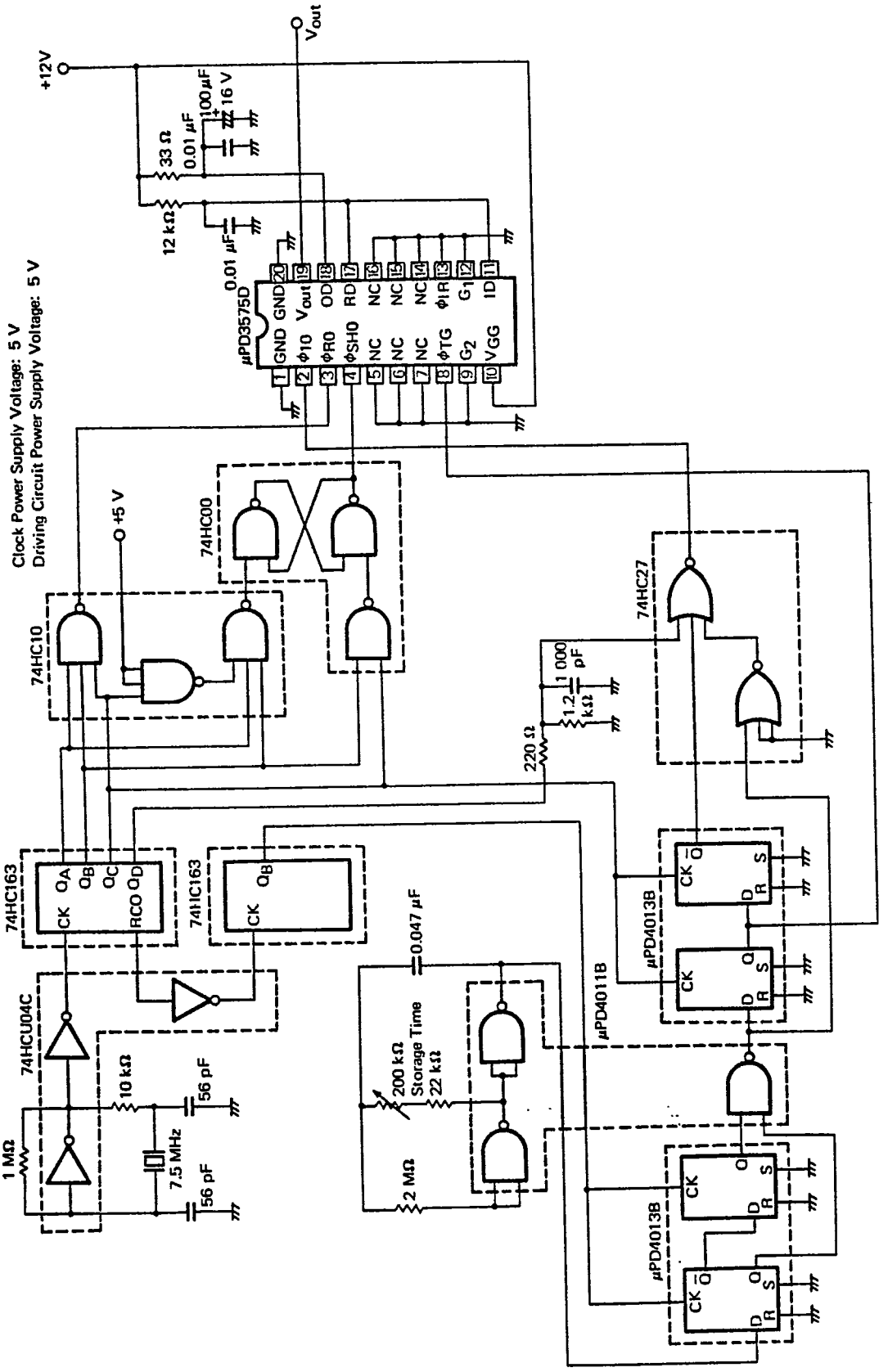


Spectral Sensitivity Characteristics



T-41-55

DRIVING CIRCUIT



EXTERIOR VIEW (Unit: mm)

T-41-55