PolarPAK Solder Joint Reliability Based on Thermal Fatigue IPC-9701

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ABSTRACT

PolarPAK, a thermally enhanced package from Vishay Intertechnology, facilitates MOSFET heat removal from an exposed top metal lead-frame connected to a drain surface in addition to a source lead-frame connected to a PCB. See Figures 1 and 2.

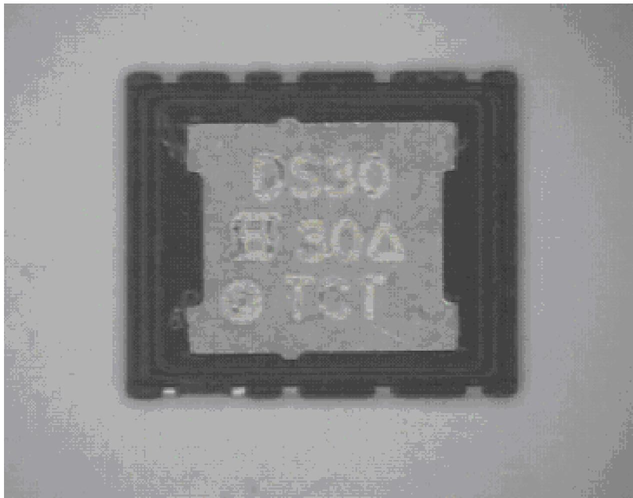


Figure 1: Top View of a PolarPAK

For a new-generation package like PolarPAK, it is imperative to examine solder joint reliability. IPC-9701[1] guidelines are implemented for PCB design and temperature cycling. The latter induces thermal fatigue on solder joints, which in turn enables the study of solder joint reliability.

The design of experiment (DOE) consists of two phases. The first phase is process development discussed in the application note titled "Development of Lead-free soldering profile for PolarPAK"[2] The application note describes PCB design, process variables, and process development methodology, and concludes by defining a recommended process.

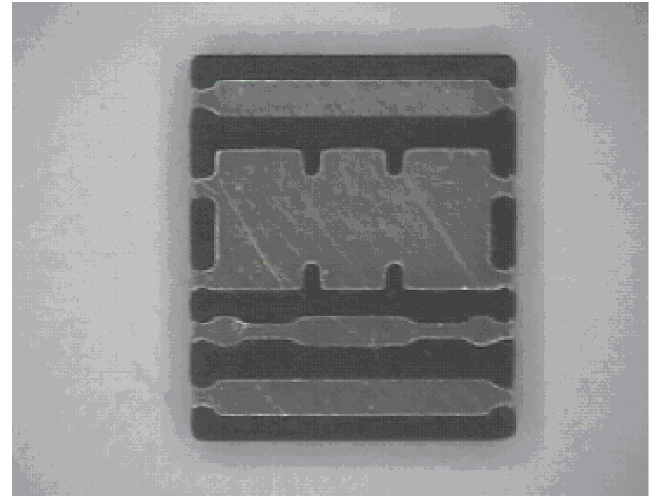


Figure 2: Bottom View of a PolarPAK

The second phase also follows IPC-9701 guidelines, comprising the assembling of device samples and the study of solder joints under thermal fatigue induced by a temperature cycling test.

The PCB assemblies were done at a third-party vendor, contract-manufacturing facility. Current industry-standard assembly practices and equipment setups were used for the development. This insures a smooth implementation of results in manufacturing practices. The assembly process recommendations derived in the aforesaid application note were used for lead-free solder paste. The latter includes other process variables such as stencil designs and parameters for solder paste applicator machines and part pick-and-place machines. Ramp-soak-spike (RSS) profiles for both varieties of solder pastes were used. First, a visual inspection was used to check for obviously faulty solder joints. Both 5DX laminography X-ray and 2DX transmission X-ray equipment were used for data collection and analysis.

The thermal fatigue DOE comprises 3,000 temperature cycles from 0 °C to 100 °C for a component sample size of 32+10 (re-work) as defined in IPC-9701. Event recording and monitoring of solder joint resistances of each daisy chain joint at the end of each cycle identifies a failure point for the solder joint. The primary benchmark as per IPC-9701 is if no failure occurs before 3,000 temperature cycles, in which case the part qualifies for solder joint reliability.

DOE PHASE (I):

a) PCB design: A worst-case PCB design was selected for this experiment, using a FR-4 board designed with 16 layers and 3.175-mm [0.125-in.] thickness as per IPC-9701 guidelines. Refer to the Figure 3 for more information. The layer stack comprised two outer copper layers of 35 µm [0.5 oz.] and 14 inner copper layers of 12 µm [0.5 oz.]. Each insulation layer of the FR-4 in between is 231 µm [7,709 µin.]. Appendix A covers the PCB specifications. For this experiment, an immersion silver board finish was used as per recommendations from external contract manufacturers.

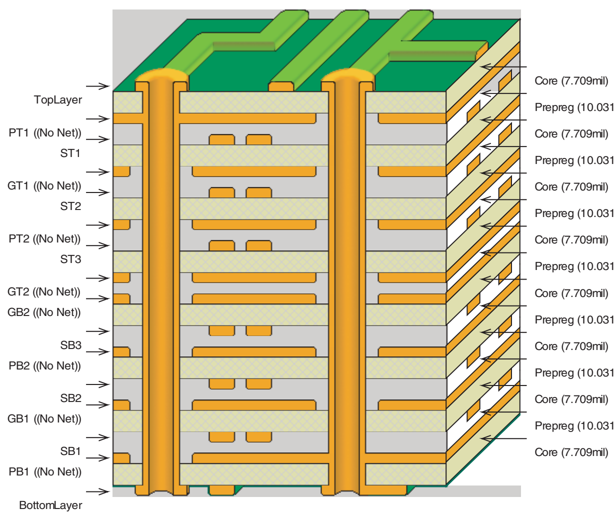


Figure 3: PCB Layer-Stack

The alternate signal, power, and ground plane from both sides have 40%, 70%, and 70% copper coverage, respectively, on each layer. Horizontal and vertical strips of controlled width and spacing determine the percentage of copper coverage. A concept of a daisy chain layout for PolarPAK can be followed from Figure 4.

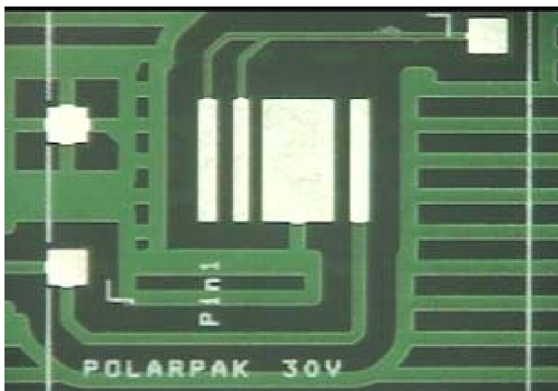


Figure 4: Daisy Chain Layout for PolarPAK

The connection from the PCB termination enters the right drain pin 4, where the first solder joint is formed between the PCB and right drain pin. An internal inverted cup structure connects two drain pins. In turn, the daisy chain connection continues to the second drain pin on the left side. The second solder joint of the daisy chain is formed between the left drain pin and the PCB. The daisy chain continues via a trace on the PCB to the gate - the second pin from the left - where the third solder joint is formed. A special modification on the part provides an internal connection between the gate and source pins. The fourth solder joint is formed at the source, a large metal slug at the third pin from left, and the PCB. A trace running out from the source connection completes the daisy chain. When monitoring the resistance of a daisy chain, all solder joints of one PolarPAK device are studied for thermal stress effects, including possible resulting solder joint failures. Furthermore, the three white square test pads shown in Figure 4 facilitate resistance measurement of each solder joint.

The recommended minimum pad layout shown in Figure 5 is used for the PCB layout. Refer to the Vishay Web site for up-to-date information.

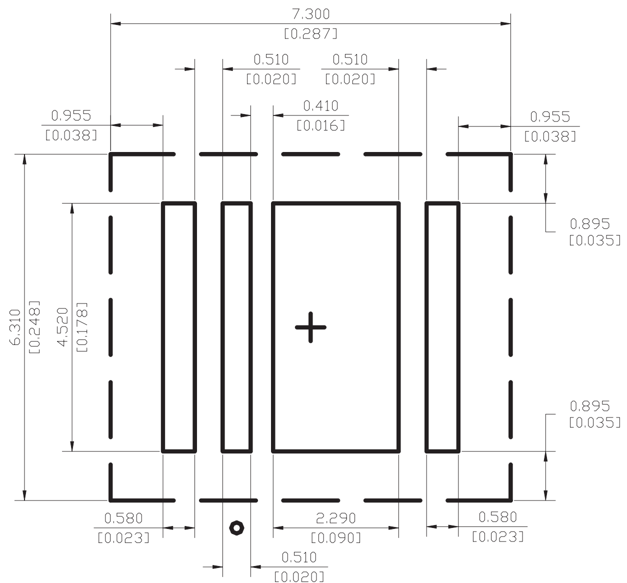


Figure 5: Recommended Minimum Pad Layout

The dimensions of the PCB are governed by the form factor required by the temperature cycling setup. Accordingly, a 16-pin edge connector termination is used to facilitate the connection setup.

One PCB can accommodate eight PolarPAK packages (see Figure 6). Appendix B covers PCB fabrication details.

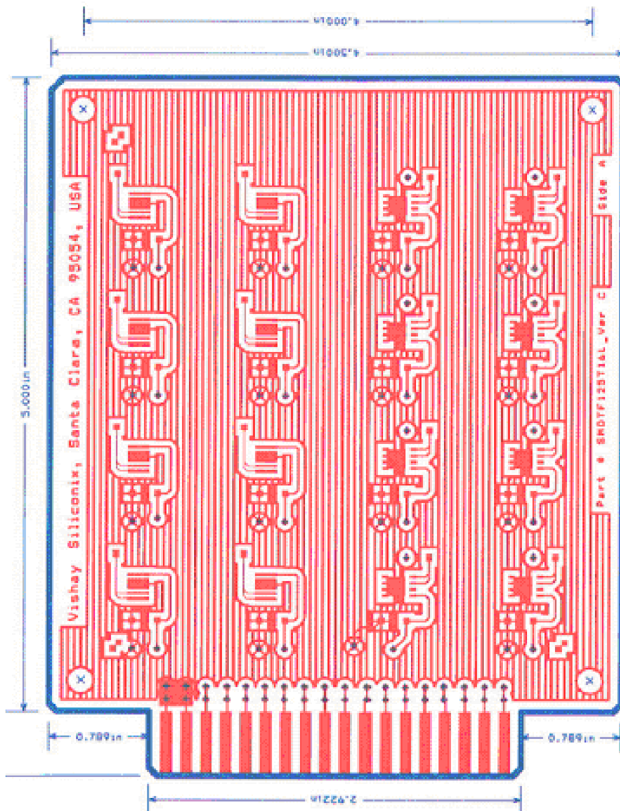


Figure: 6 PCB Dimensions

PCBA characteristics:

Surface finish: Immersion silver
Board thickness: 3.175 mm [0.125 in.]
Board size: 4.5 in. by 5 in.

Each PCB side is designed to accommodate two types of parts. PCB Part #SMDTF125T16L_Ver C accommodates PolarPAK and PowerPAK SO-8 single ext.

b) PCB assembly: The test sample build was determined by IPC-9701, which calls for 32 fresh and 10 reworked solder joint assemblies. Seven boards with seven parts on each board gives 49 assembled parts. Reworking two parts from six boards renders 12 reworked parts. Five boards from the reworked group and a seventh non-reworked board for temperature cycling were used to meet IPC-9701 criteria. The sixth reworked board was retained as a zero temperature cycle reference board.

Using the PCB assembly process developed and described in AppNote AN-xxx titled "Development of Lead-free soldering profile for PolarPAK"[2] seven PCBs were assembled with seven PolarPAK parts on each board. Part ID U16 was not assembled.

Assembly process parameters:

a. Stencil aperture opening: Increase of 10% -- the aperture increase from the original pad size was used

b. Aperture shape and size, stencil thickness, and aspect ratio are described in the following table:

Version	Aperture shape	Aperture opening		Stencil thickness (mil)	Aspect ratio	Area ratio	Component shape
		Width (mils)	Length (mils)				POLARPAK
CA	Rectangle	25.2	189.2	5	5.04	2.22	
CA	Rectangle	21.0	189.2	5	4.20	1.89	
CA	Rectangle	94.5	189.2	5	18.90	6.30	

- Aspect ratio (aperture opening / stencil thickness) = 2.5
- Minimum area ratio (LxW / 2(L+W)T) = 0.8

Solder pastes: The following solder paste was used:

- Lead-free solder paste SAC-387 (Tamura TLF-206-93G)

1. Stencil printing:

Machine: EKRA E5
Squeegee size / angle: 450 mm / 60°
Front/rear pressure: 40 Newtons
Print speed: 8-12 mm/s
Snap off: 0 mm
Separation speed: 0.5 mm/s
Stencil thickness: 5 mils
Stencil opening: See Table 1 below

Table 1

Version	Comp Type	Buildt Qty	Profile	Stencil Thickness	Aperture Design	
					Drain-Gate (mils)	Source
CA	PolarPAK	7	RSS	5 mils	21 x 189.2	94.5 x 189.2

2. Pick and place

Machine: Juki 2060E

Note: In each board, leave the first location empty (no load/part)

3. Reflow

Machine: BTU Pyramax 98

(seven heating zones and two cooling zones) - no nitrogen, air only

RSS profile shown in Figure 7 was used for the lead-free solder paste

For immediate reference, the reflow process and parameters used for lead-free solder are summarized below:

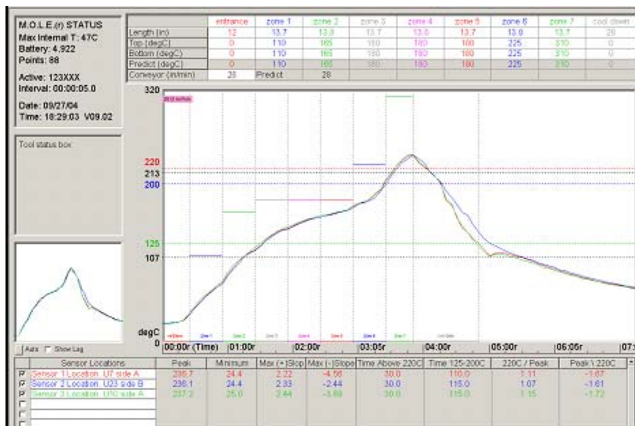


Figure 7: RSS Profile for Lead-Free
Peak Temperature: 237 °C
Time above 220 °C: 30 seconds
Soak time (120 °C to 200 °C): 115 seconds

Solder joint visual inspection criteria were derived from IPC-A-610D[4]; refer to Appendix D for relevant details. The visual inspection also included looking for any obvious solder joint defects such as a cold joint, solder bumps, bridges, or other flaws.

In addition, 2DX X-ray and 5DX X-ray processes were employed to inspect void levels on each solder joint. All images were compared by void level. During 2DX inspection the focus was on number and size of voids. 5DX measurements were sorted and selected based on the percentage of void areas. The first method, 2DX image review, was a qualitative comparison. The second method, 5DX parametric data, was a quantitative analysis. See Appendix A for best-case/worst-case void level X-ray images for PolarPAK. Using these criteria, good solder assemblies were achieved with void levels less than 25%.

c) Rework: Using the worst-case locations from the X-ray inspection results, six PCBs and two locations on each board were selected and marked "X" with indelegable black ink for rework. The originally soldered part was de-soldered and replaced with a new part.

Table 2: Rework Locations for Lead-Free Assemblies

Board #	Side	Comp Type	Rework Location
29	CA	PolarPAK	U10, U11
30	CA	PolarPAK	U11, U15
31	CA	PolarPAK	U12, U15
32	CA	PolarPAK	U11, U12
33	CA	PolarPAK	U13, U14
34	CA	PolarPAK	No Rework
35	CA	PolarPAK	U10, U12

Rework setup:
AirVac DRS24 - BGA rework machine
Special rework nozzle

Rework steps:

1. Remove components using a hot-air BGA rework machine
2. Clean up pads using a soldering iron
3. Solder bump pads using a soldering iron and solder wire SAC 305.
4. Apply no-clean gel flux on the pad
5. Place the component using the hot-air BGA rework machine
6. Reflow the component using the hot-air BGA rework machine per profiles shown below in Figure 8

Figure 8: Rework Reflow Profile
Rework Profile 1 - Part Removal, Lead-Free
Peak temperature: 236.7 °CTime above 217 °C: 82 seconds

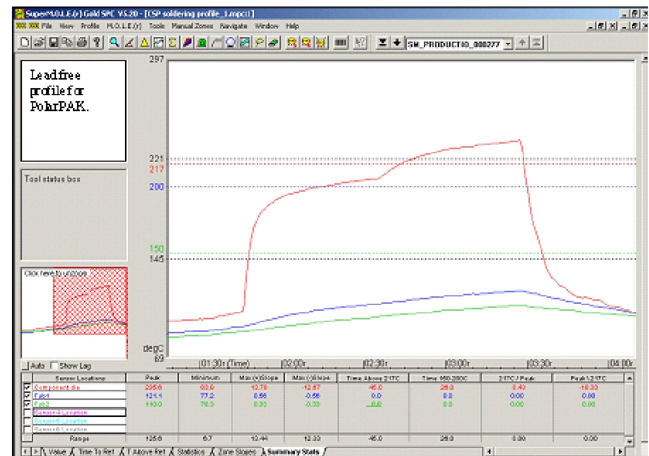


Figure: 10: Rework Reflow Profile
Rework Profile 2 - Part Assembly, Lead-Free
Peak temperature: 235.6 °CTime above 217 °C: 45 seconds

Figure 9 shows the arrangement of a thermocouple on a PCB during rework. The thermocouples are located on the rework part, close to the lead or foot of the adjacent part, and on the PCB surface close to the rework location to insure that the actual part and PCB temperature limits are never exceeded.

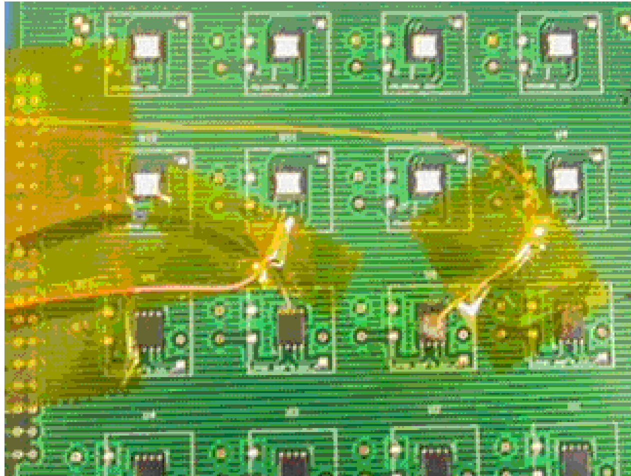


Figure 9: Arrangement of Thermocouple on PCB During Rework
Thermocouple attachment locations for rework
profile 1: U6 (reworked location, T/C on the package)
U7 (adjacent location, T/C on the solder joint)U11 (adjacent location, T/C on the solder joint)

Table 3: BGA Rework Machine Settings

Profile Event/Cycle	Profile 1	Profile 2
Preheat	Top: 200 °C Bottom: 400 °C Time: T/C @ 90 °C	Top: 200 °C Bottom: 400 °C Time: T/C @ 90 °C
Soak	Top: 300 °C, Flow: 50% Bottom: 350 °C Time: 60 seconds	Top: 300 °C, Flow: 50% Bottom: 350 °C Time: 90 seconds
Ramp	Top: 350 °C, Flow: 50%Bottom: 350 °CTime: 20 seconds	Top: 350 °C, Flow: 50% Bottom: 350 °C Time: 20 seconds
Reflow	Top: 350 °C, Flow: 50%Bottom: 350 °CTime: 30 seconds	Top: 350 °C, Flow: 55% Bottom: 350 °C Time: 30 seconds
Nozzle Height	0.125 in.	0.05 in.

Rework results:

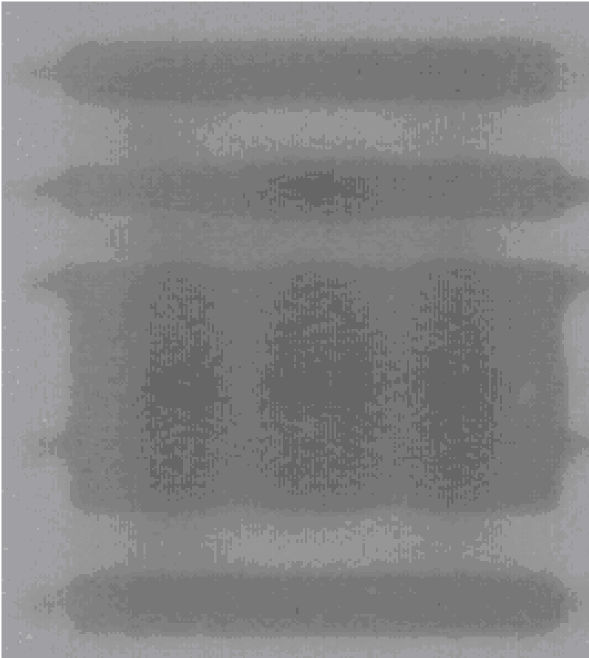


Figure 11: Smallest Void After Rework
Component Type: PolarPAK
Board#: 32
Location: U12

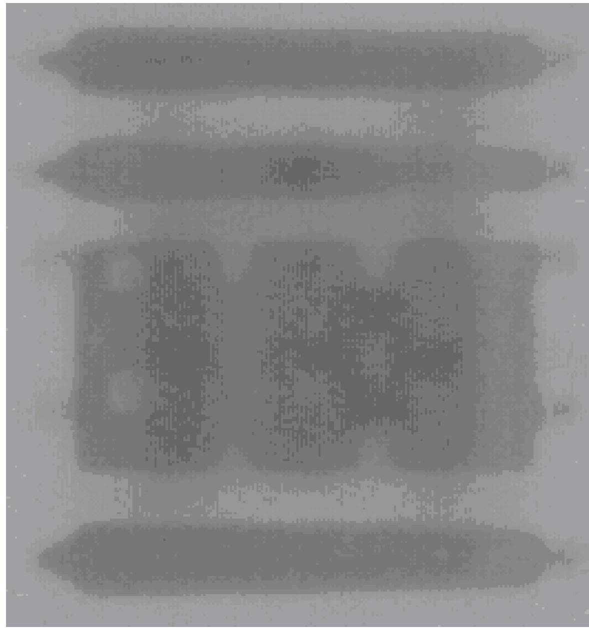


Figure 12: Largest void after rework
Component Type: PolarPAK
Board#: 33
Location: U13

Summary of complete assembly:

- Solder release is consistent
- The amount of voids for this package is in a range of 5% to 30%, which includes noise generated during the 5DX measurement due to the complexity of the package lead-frame
- No problem with rework

d) Thermal fatigue test:

This is the main phase of the DOE. Up to this point the work was focused on preparation. The thermal fatigue testing comprised of various steps:

(1) Test definition
(2) Test setup
(3) Temperature cycling chamber calibration
(4) Temperature cycling
(5) Test database
(6) Analysis result summary

(1) Test definition:

Appendix D is a brief summary of thermal fatigue by temperature cycling test definition guidelines derived from IPC-9701.

Basically, each solder joint is subjected to 3,000 temperature cycles as per the profile shown in Figure 13.

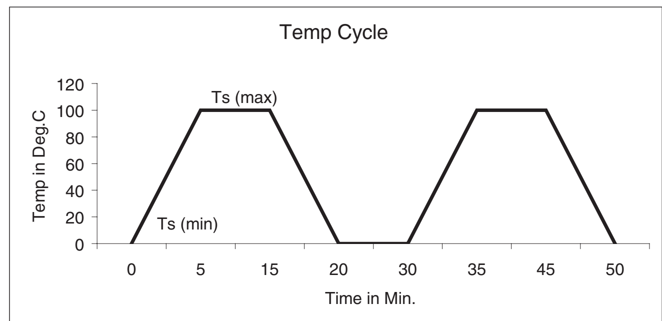


Figure 13: TC1 0 °C to 100 °C tolerance +/-5 °C

Time	Temp
0	0
5	100
15	100
20	0
30	0
35	100
45	100
50	0

If any solder joint failure occurs, it is detected by comparing the joint resistance and is recoded with respect to the cycle number in which it occurred.

(2) Test setup:

A programmable temperature cycling chamber was programmed for the temperature cycle shown in Figure 13. The test chamber had a pre-wired card-cage that could take multiple PCB assemblies conforming to the card-cage form-factor. Each daisy chain was connected to an analysis-tech event detector system. The latter device compared, at a preset interval of one cycle time during dwell-time, the resistance with preset value 1 kΩ, and reported/recorded an event any time the daisy chain resistance exceeded the preset value. Thus, even momentarily open circuits were caught and reported.

(3) Temperature cycling chamber calibration:

The temperature cycle chamber was calibrated for a thermal mass of test load by measuring the actual temperature profile on pertinent locations on the PCB assembly and component. Figure 14 shows the calibrated profile used during the actual testing.

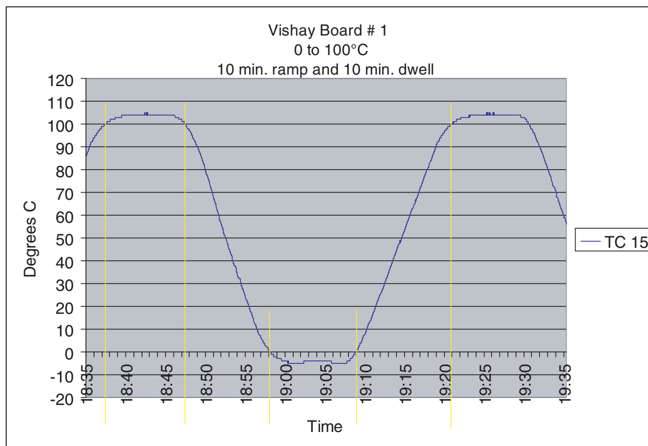


Figure 14: Calibration Profile

(4) Temperature cycling:

The very first and last steps of the temperature cycling test are measurements of daisy chain resistance. Appendix E is a tabulated record of each daisy chain resistance before and after the temperature cycling. The first resistance column is initial resistance and the second resistance column is the value after 3,000 cycles.

PCB assemblies were loaded in the temperature cycling chamber to begin the thermal fatigue test.

(5) Test database

The final test results are tabulated in the following table:

Table 4: 3,000-Cycle Test Data

Started 11/17/2004		Terminated 3/2/2005	
Board	**Package**	**Side ID**	**Fail**
29	PolarPAK	U9	
29	PolarPAK	U10	
29	PolarPAK	U11	
29	PolarPAK	U12	
29	PolarPAK	U13	
29	PolarPAK	U14	
29	PolarPAK	U15	
29	n/a	U16	N/A
31	PolarPAK	U9	
31	PolarPAK	U10	
31	PolarPAK	U11	
31	PolarPAK	U12	
31	PolarPAK	U13	
31	PolarPAK	U14	
31	PolarPAK	U15	
31	n/a	U16	N/A
32	PolarPAK	U9	
32	PolarPAK	U10	
32	PolarPAK	U11	
32	PolarPAK	U12	
32	PolarPAK	U13	
32	PolarPAK	U14	
32	PolarPAK	U15	
32	n/a	U16	N/A
33	PolarPAK	U9	
33	PolarPAK	U10	
33	PolarPAK	U11	
33	PolarPAK	U12	
33	PolarPAK	U13	
33	PolarPAK	U14	
33	PolarPAK	U15	
33	n/a	U16	N/A
34	PPAK SO8-EXT	U1	
34	PPAK SO8-EXT	U2	
34	PPAK SO8-EXT	U3	
34	PPAK SO8-EXT	U4	
34	PPAK SO8-EXT	U5	t0
34	PPAK SO8-EXT	U6	

Started 11/17/2004		Terminated 3/2/2005	
Board	**Package**	**Side ID**	**Fail**
34	PPAK SO8-EXT	U7	
34	n/a	U8	N/A
34	PolarPAK	U9	
34	PolarPAK	U10	
34	PolarPAK	U11	
34	PolarPAK	U12	
34	PolarPAK	U13	
34	PolarPAK	U14	
34	PolarPAK	U15	
34	n/a	U16	N/A
35	PolarPAK	U9	
35	PolarPAK	U10	
35	PolarPAK	U11	
35	PolarPAK	U12	
35	PolarPAK	U13	
35	PolarPAK	U14	
35	PolarPAK	U15	
35	n/a	U16	N/A

(6) Results summary

Table 5:

Package	First Fail	# Failed	% Failed
PolarPAK		0	0%

The above results show that the PolarPAK package passes the lead-free solder joint reliability test guidelines as per IPC-9701

REFERENCE:

[1] "Thermal fatigue analysis to study solder joint reliability for new-generation SMD parts introduced by Vishay Siliconix," by Serge Jaunay and Kandarp Pandya.

[2] IPC-9701 Standard for Solder Joint Reliability, an IPC publication.

[3] "Voiding: Occurrence and reliability issues with lead-free," by Martin Wickham, NPL.

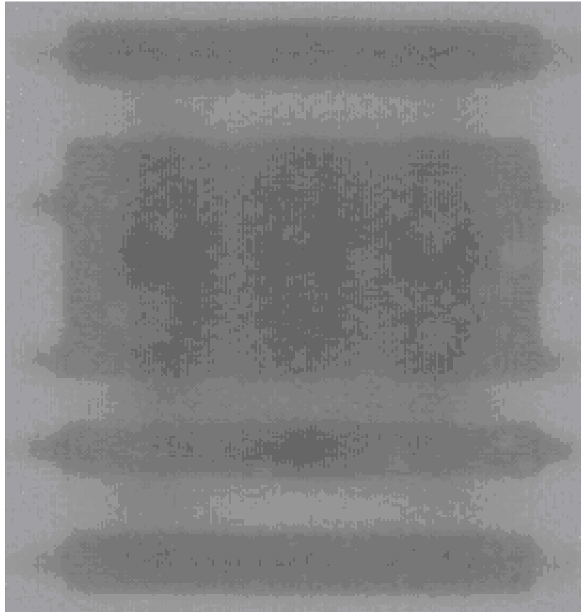
[4] IPC-A-610D Criteria for Solder Joint Quality Inspection.

Appendix A

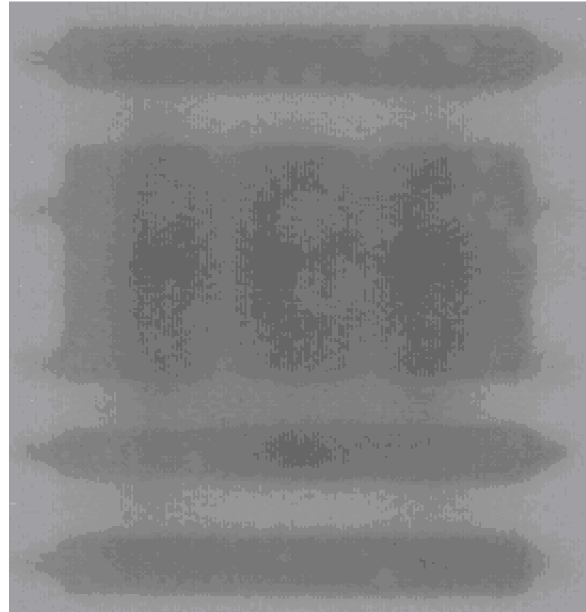
POLARPAK X-Ray Images

<u>After assembly (without rework)</u>

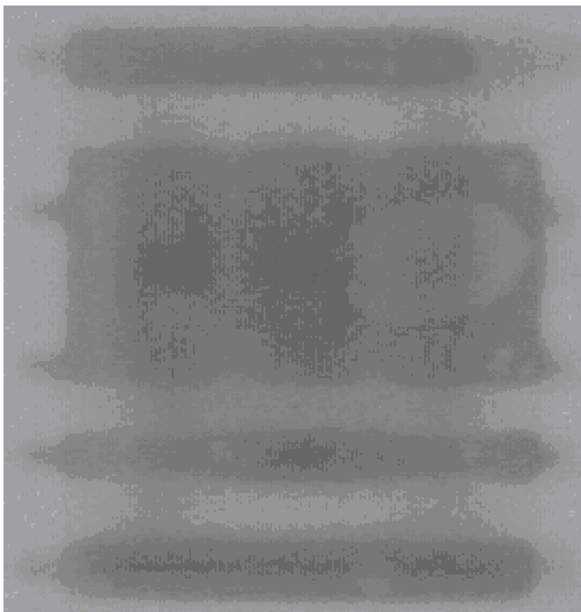
<u>Note:</u> The smallest voids are based on signal pins. All images are captured through 5DX. No void measurement is available because of too many false calls on this component type.



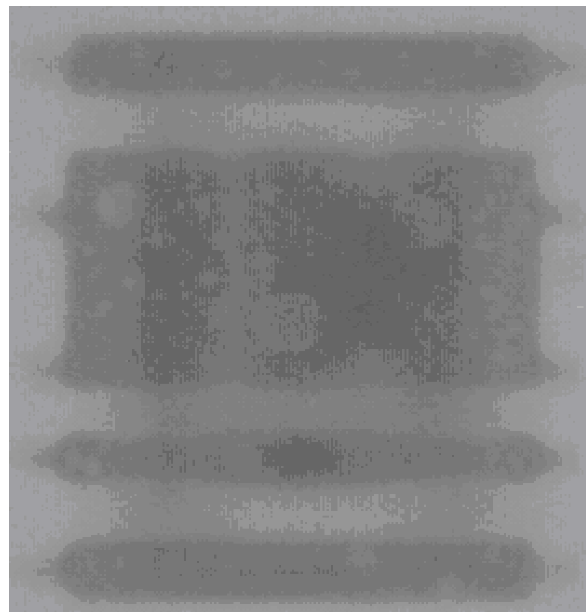
Smallest void
Board#: 29
Location: U14



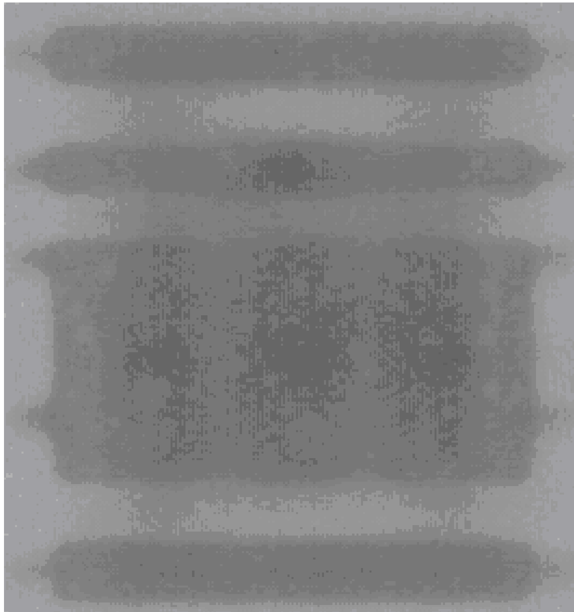
Smallest void
Board#: 30
Location: U11



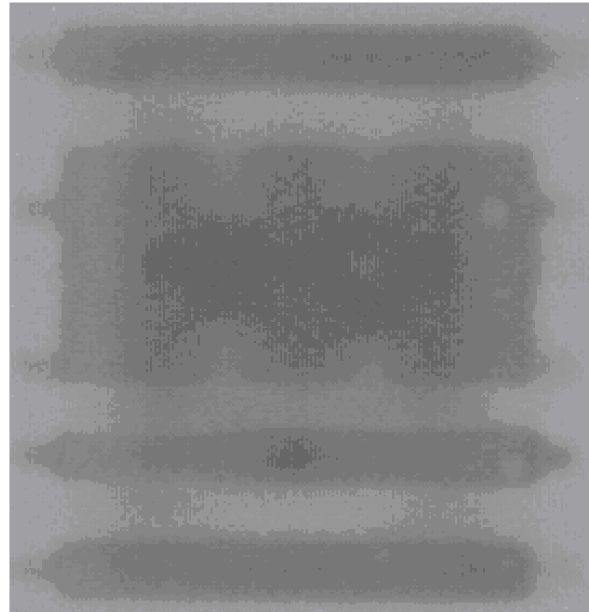
Largest void
Board#: 29
Location: U9



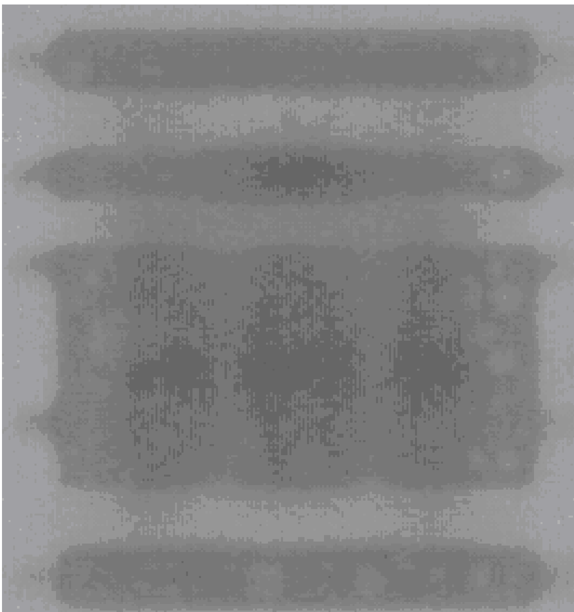
Largest void
Board#: 30
Location: U15



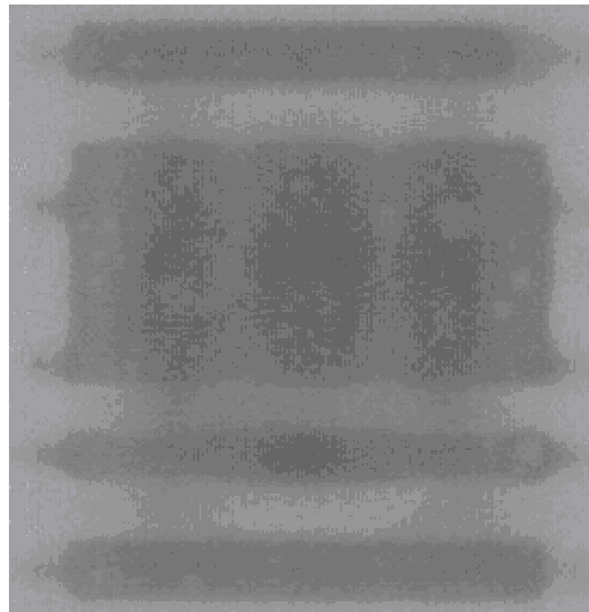
Smallest void
Board#: 31
Location: U11



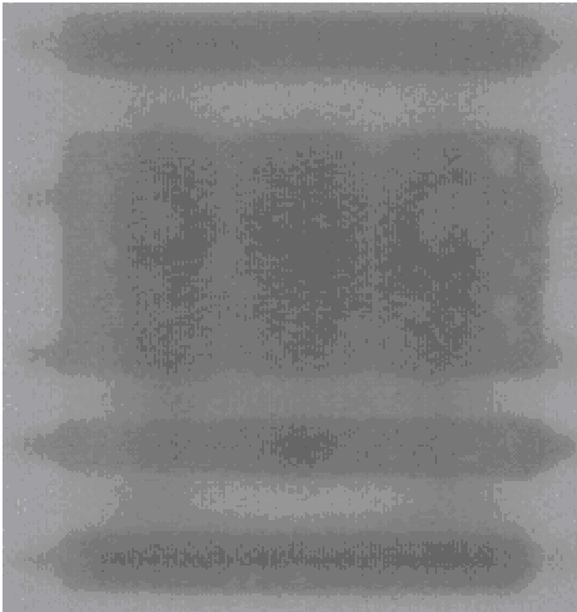
Smallest void
Board#: 32
Location: U11



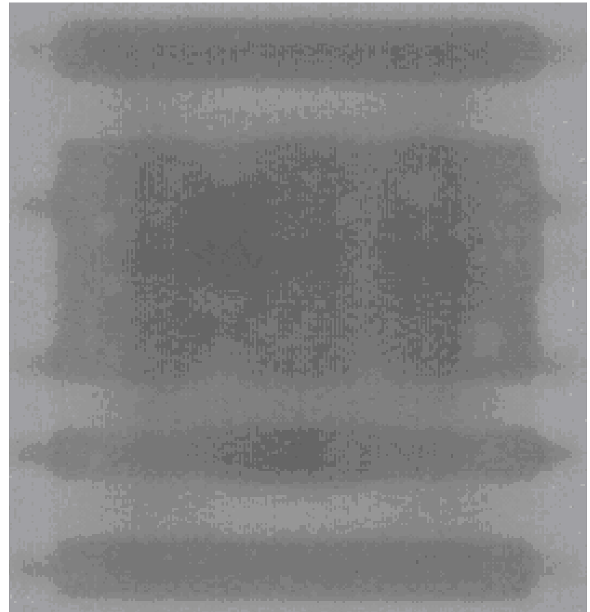
Largest void
Board#: 31
Location: U10



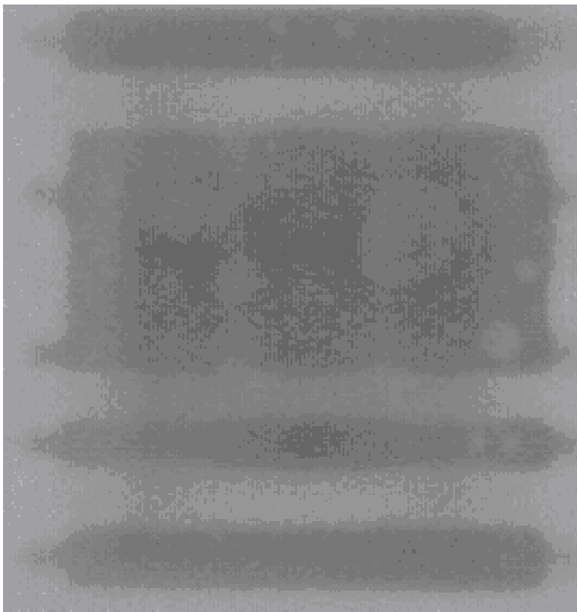
Largest void
Board#: 32
Location: U14



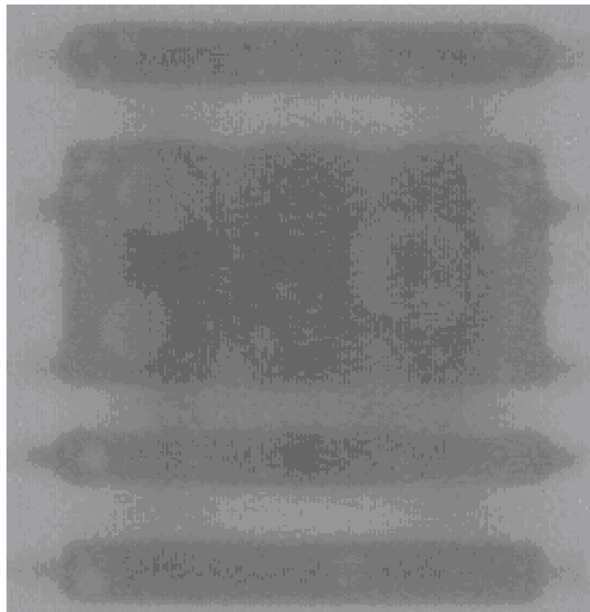
Smallest void
Board#: 33
Location: U12



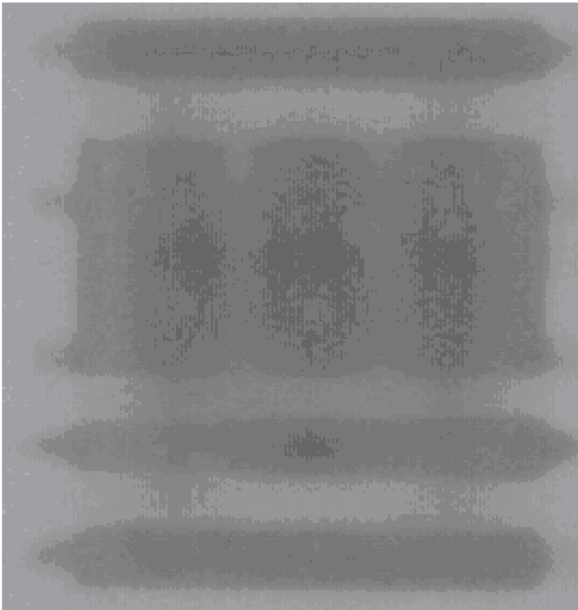
Smallest void
Board#: 34
Location: U13



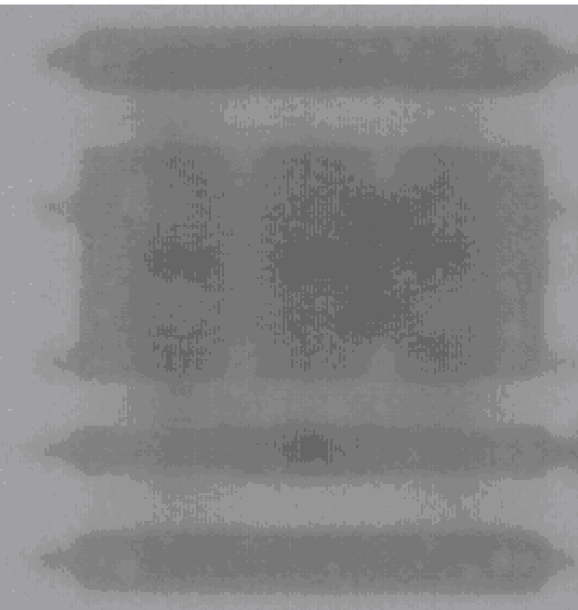
Largest void
Board#: 33
Location: U9



Largest void
Board#: 34
Location: U14



Smallest void
Board#: 35
Location: U12

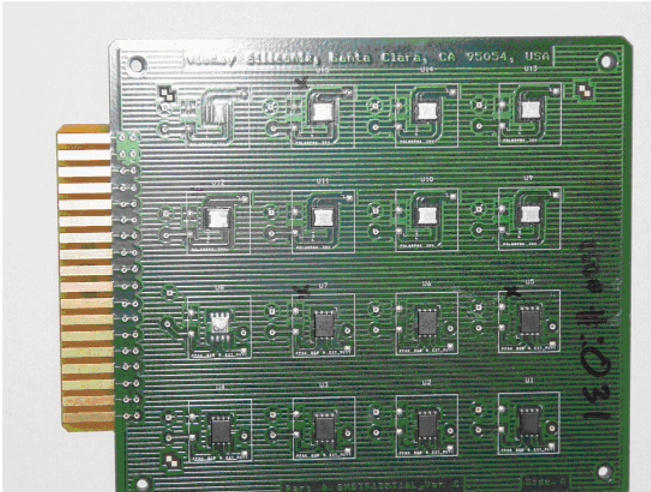


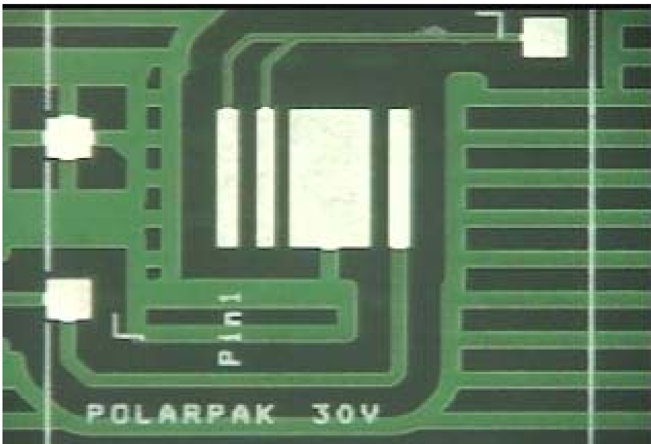
Largest void
Board#: 35
Location: U14

Appendix B

PCB Layout

SMD125T16L_Ver C_Side A





Appendix C

PCB Fabrication

Material: FR-4
Thickness: 3.175 mm [0.125 in.]
Number of copper layers: 16
Nominal outer layer (top/bottom) cu thickness: 35 µm [1378 µin.] 0.5 oz.
Nominal inner layer cu thickness: 12 µm [472 µin.] 0.5 oz.
Nominal FR4 insulation layer thickness: 231.8 µm [7,709 µin.]
Even internal layers 2, 4, 5, 7 from each side: Power and ground
Cu coverage on power/ground layers:70%
Cu coverage on Signal trace: 40%
Min. outer layer trace width: 150 µm [5906 µin.]
Test pads for each daisy chain to be provided
Minimum 15-mm [0.6-in.] clearance around each part for rework and if necessary the removal of the failed part without damage to the adjacent part/trace
Minimum via for large (drain) land pad:50%
Via size: Pitch: 1.0 mm [0.040 in.]
Diameter: 0.3 mm [0.012 in.]
Solder mask encroachment on the via pad for these via on the bottom side to prevent the solder from spreading on the bottom side.
Square test pad size: 1.5 mm [0.060 in.]
PTH Drill: 1.0 mm [0.040 in.]
Surface finish: (preferred)OSP (Organic Solderability Preservative)

Silkscreen or Cu etch to label all components, all test points, and location of pin is mandated.

Appendix D

Performance and Reliability of Solder Joints for Vishay Siliconix SMD Part Package -- PolarPAK

Scope of work for temperature cycling

Using IPC-9701 guidelines

Test sample size distribution:

Total number of test vehicles (PCBs): 6 (+1 reference board)
Total number of daisy chains: 42 (+7 on reference board)

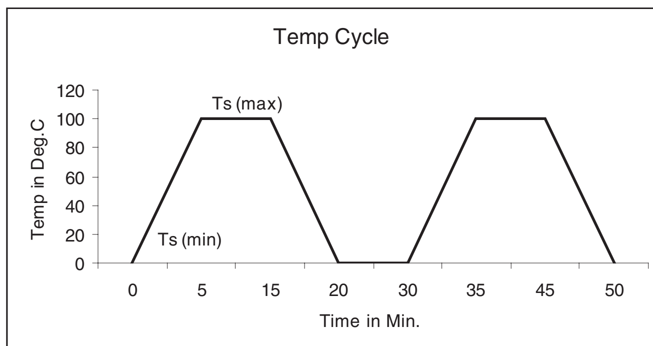
Variety of PCBs - lead-free assemblies:
PCB #SMD125T16L Ver_C Side A 6 (+1 reference board)

Number of PolarPAK parts on each PCB: 7
Number of PolarPAK daisy chains per PCB: 7

Number of parts reworked: 10 (+2 on reference board)
Number of parts reworked per PCB: 2 for 6 out of 7 test boards (including reference board)

Temperature cycle definition:

TC1 0 °C to 100 °C tolerance +/-5 °C



Time	Temp
0	0
5	100
15	100
20	0
30	0
35	100
45	100
50	0

Temperature ramp rate: 20 °C/minutes
High temperature dwell: 10 minutes
Low temperature dwell: 10 minutes

Test duration:
Whichever condition occurs first:

50% cumulative failure
or
Number of thermal cycles: NTC-D 3,000 cycles
In case of failure continue testing up to 6,000 cycles or 50% cumulative failures, whichever occurs first.

Test monitoring: Event detector or continuous monitoring of electrical resistance of each daisy chain

Temperature chamber characterization:

Component temperature to be monitored and recorded at each board location in the chamber during the initial setup. Characterization should be performed using a representative sample load, test board configuration, and fixtures.

Failure definition:

Event detector 1,000 W, 10 events (maximum), 1 µs duration (maximum), reports first verified as time-to-failure.
and/or
Data logger/voltmeter: 20% nominal resistance increase (maximum), five readings/scans (maximum)

Data documentation:

1. Detailed description of all experimental apparatus, including thermal chamber and data acquisition system
2. Temperature vs. time plots for both the board and chamber including the chamber setup characterization data
3. Resistance vs. time plot for data logger samples
4. Tabular data for the number of cycles to failure for all failures
5. Weibull analysis

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Appendix E

Continuity Test

Board#: 029 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.209	0.229	
U14	PolarPAK	0.317	0.336	
U13	PolarPAK	0.433	0.451	
U12	PolarPAK	0.072	0.088	
U11	PolarPAK	0.217	0.229	X' (Rework)
U10	PolarPAK	0.305	0.305	X' (Rework)
U9	PolarPAK	0.406	0.407	

Board#: 030 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.201	0.202	X' (Rework)
U14	PolarPAK	0.303	0.306	
U13	PolarPAK	0.425	0.417	
U12	PolarPAK	0.065	0.057	
U11	PolarPAK	0.213	0.205	X' (Rework)
U10	PolarPAK	0.297	0.317	
U9	PolarPAK	0.401	0.413	

Board#: 031 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.206	0.202	X' (Rework)
U14	PolarPAK	0.307	0.302	
U13	PolarPAK	0.425	0.422	
U12	PolarPAK	0.068	0.066	X' (Rework)
U11	PolarPAK	0.214	0.247	
U10	PolarPAK	0.296	0.303	
U9	PolarPAK	0.399	0.403	

Board#: 032 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.201	0.239	
U14	PolarPAK	0.305	0.344	
U13	PolarPAK	0.421	0.456	

Board#: 032 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U12	PolarPAK	0.061	0.092	X' (Rework)
U11	PolarPAK	0.207	0.233	X' (Rework)
U10	PolarPAK	0.291	0.316	
U9	PolarPAK	0.393	0.415	

Board#: 033 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.198	0.229	
U14	PolarPAK	0.304	0.336	X' (Rework)
U13	PolarPAK	0.415	0.443	X' (Rework)
U12	PolarPAK	0.059	0.084	
U11	PolarPAK	0.207	0.233	
U10	PolarPAK	0.293	0.301	
U9	PolarPAK	0.391	0.399	

Board#: 034 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.201	0.229	No
U14	PolarPAK	0.304	0.321	
U13	PolarPAK	0.415	0.438	
U12	PolarPAK	0.063	0.086	
U11	PolarPAK	0.209	0.228	
U10	PolarPAK	0.292	0.309	
U9	PolarPAK	0.394	0.410	

Board#: 035 (Lead-Free) Rev: C / Side: A				
Comp Ref	Package type	Res (Ohm)	Res (Ohm)	Note
U16	PolarPAK	Open	Open	No component
U15	PolarPAK	0.205	0.215	
U14	PolarPAK	0.312	0.311	
U13	PolarPAK	0.426	0.424	
U12	PolarPAK	0.066	0.053	X' (Rework)
U11	PolarPAK	0.215	0.214	
U10	PolarPAK	0.300	0.295	X' (Rework)
U9	PolarPAK	0.399	0.398	