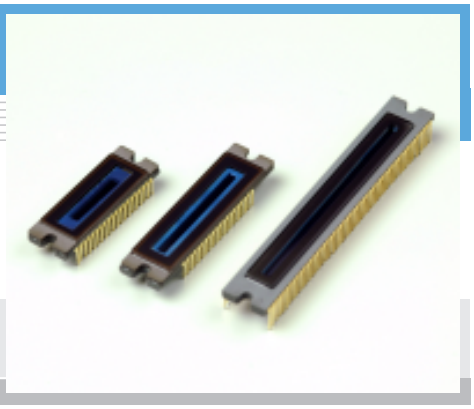
NEW

IMAGE SENSOR

Back-thinned TDI-CCD

S10200-02, S10201-04, S10202-08, S10202-16



Operating the back-thinned CCD in TDI mode delivers high sensitivity.

TDI-CCD captures clear and bright images even under low-light-level conditions. During TDI mode, the CCD captures an image of a moving object while transferring integrated signal charges synchronously with the object movement. This operation mode dramatically boosts sensitivity to high levels even when capturing fast moving objects. Our new TDI-CCD uses the back-thinned structure to achieve even higher quantum efficiency over a wide spectral range from UV to near IR region (200 to 1100 nm).

Features

- TDI mode gives high sensitivity
- High-speed, continuous image acquisition
- Back-thinned structure ensures high sensitivity from UV to near IR
- Multiple ports for high-speed line rate

Applications

- Sequential imaging of high-speed moving samples
- Inspection tasks on electronic parts production line
- Semiconductor inspection
- Flow cytometery

TDI (Time Delay Integration) mode

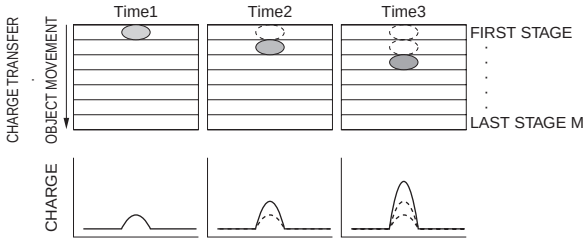
In FFT-CCD, signal charges in each line are vertically transferred during charge readout. TDI mode synchronizes this vertical transfer timing with the movement of the object, so that signal charges are integrated a number of times equal to the number of vertical stages of the CCD pixels.
In the TDI mode, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by the following equation:

$$v = f \times d$$

v: Object moving speed, Charge transfer speed, f: Vertical transfer frequency, d: Pixel size

In the right figure, when the first stage charges are transferred to the second stage, an additional charges are produced in the second stage by photoelectric conversion and accumulated. When this operation is continuously repeated until reaching the last stage M (the number of vertical stages), signal charges which are M times greater than the initial charges are accumulated. Since the signal charges on each line are output from the CCD horizontal shift register, a two-dimensional image can be continuously acquired. In this way the TDI mode achieves sensitivity which is M times higher than linear image sensors (S/N is improved $\sqrt{M}$ times). The TDI mode also improves sensitivity variations compared to frame mode operation.

● Schematic diagram showing integrated exposure by TDI mode



■ Selection guide

Type No.	Pixel size (μm)	Number of total pixels (H) × (V)	Number of active pixels (H) × (V)	Number of ports	Pixel rate (MHz/port)	Line rate (kHz)	Vertical transfer
S10200-02	12 × 12	1040 × 128	1024 × 128	2	30	50	Bidirectional
S10201-04		2080 × 128	2048 × 128	4			
S10202-08		4160 × 128	4096 × 128	8			
S10202-16		4224 × 128	4096 × 128	16		100	

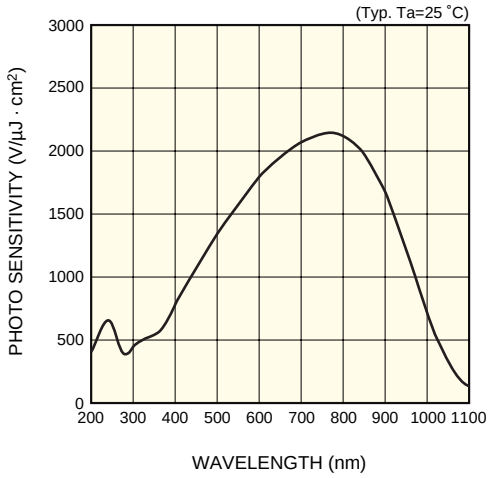
■ Specifications

Parameter	Specification
TDI stage	128
Anti-blooming	FW × 100 (Min.)
Vertical clock	3 phases
Horizontal clock	2 phases
Output circuit	Two-stage MOSFET source follower
Package	Ceramic DIP
Window	Quarts glass

PRELIMINARY DATA
Jan. 2007

SOLID STATE DIVISION

■ Spectral response (without window)



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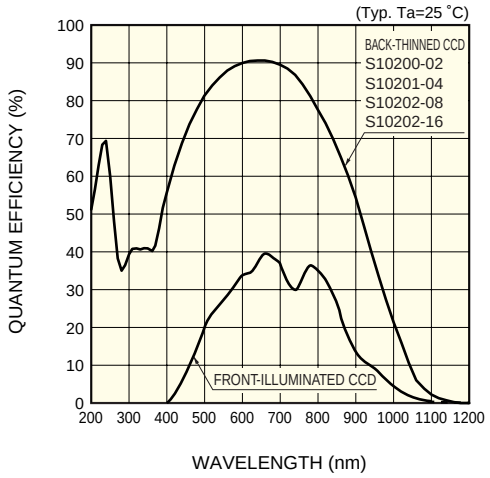

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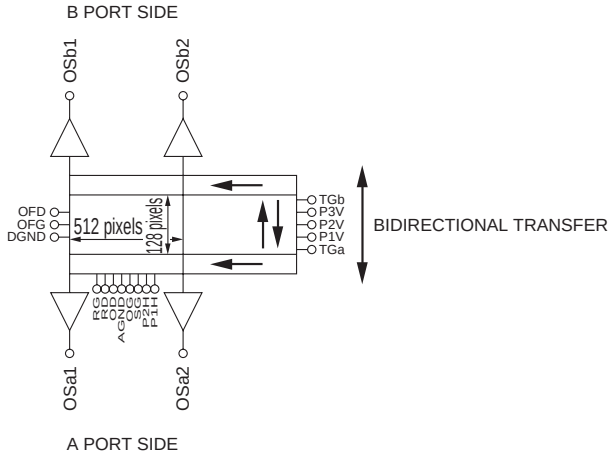
■ Sensor structure

S10200-02



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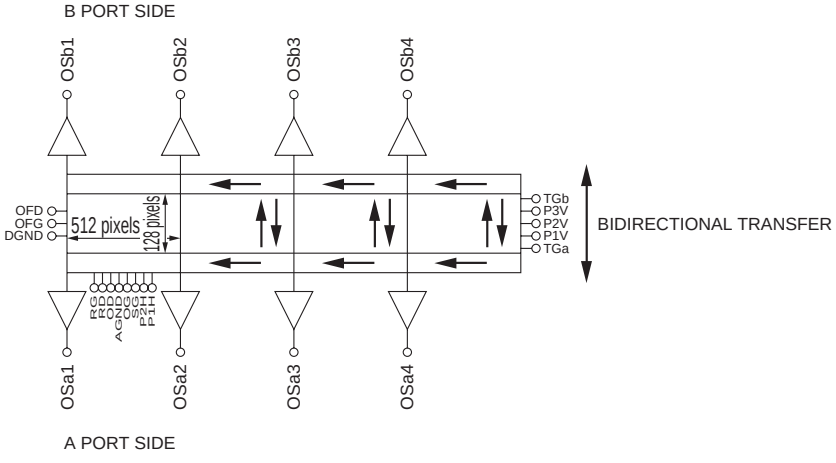
S10201-04



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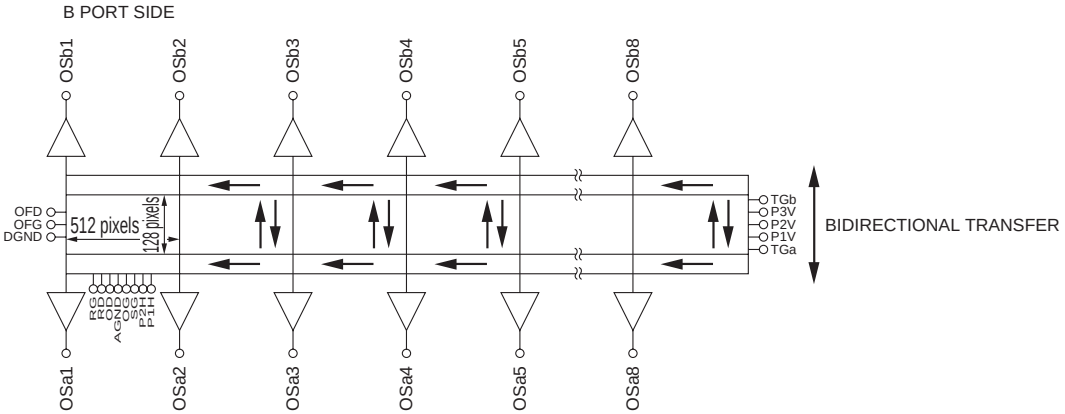
S10202-08



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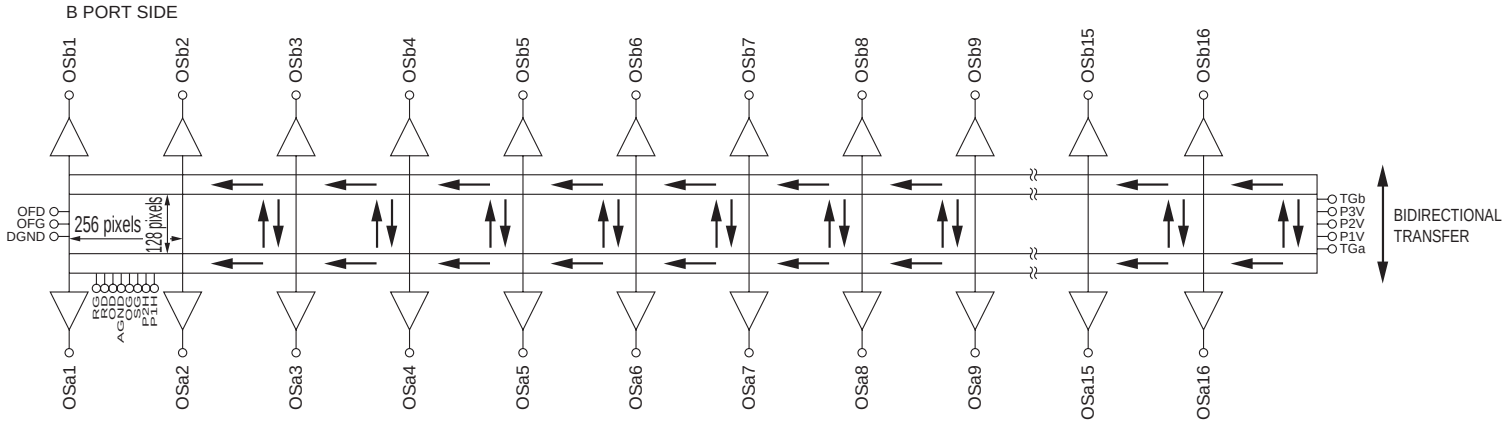
S10202-16



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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	60	°C
Storage temperature	Tstg	-50	-	70	°C
Output transistor drain voltage	V_{OD}	-0.5	-	25	V
Reset drain voltage	V_{RD}	-0.5	-	18	V
Overflow drain voltage	V_{OFD}	-0.5	-	18	V
Overflow gate voltage	V_{OFG}	-10	-	15	V
Summing gate voltage	V_{SG}	-10	-	15	V
Output gate voltage	V_{OG}	-10	-	15	V
Reset gate voltage	V_{RG}	-10	-	15	V
Transfer gate voltage	V_{TG}	-10	-	15	V
Vertical clock voltage	V_{P1V}, V_{P2V}, V_{P3V}	-10	-	15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	15	V

■ Operating conditions (TDI mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	12	15	18	V
Reset drain voltage		V_{RD}	11	12	13	V
Output gate voltage		V_{OG}	3	5	7	V
Substrate voltage		V_{DGND}, V_{AGND}	-	0	-	V
Overflow drain voltage		V_{OFD}	4	6	9	V
Overflow gate voltage		V_{OFG}	0	4	6	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}, V_{P3VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}, V_{P3VL}	-6	-5	-4	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-6	-5	-4	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SHL}	-6	-5	-4	
Reset gate voltage	High	V_{RGH}	7	8	9	V
	Low	V_{RGL}	-6	0	-	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-6	-5	-4	

■ Electrical and optical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	FW × Sv	-	V
Full well capacity *1	FW	100	120	140	ke^-
CCD node sensitivity	Sv	3	3.5	4	$\mu V/e^-$
Dark current *1, *2	DS	-	100	300	e^-/pixel
Readout noise *3	Nr	-	100	200	e^- rms
Dynamic range	DR	-	1200	-	-
Photo response non-uniformity *4	PRNU	-	±3	±10	%
Spectral response range	λ	-	200 to 1100	-	nm

*1: TDI mode
*2: Line rate 50 kHz, accumulated dark signal after 128-stage transfer
*3: Readout frequency 30 MHz
*4: Measured at one-half of the full well. In TDI mode.

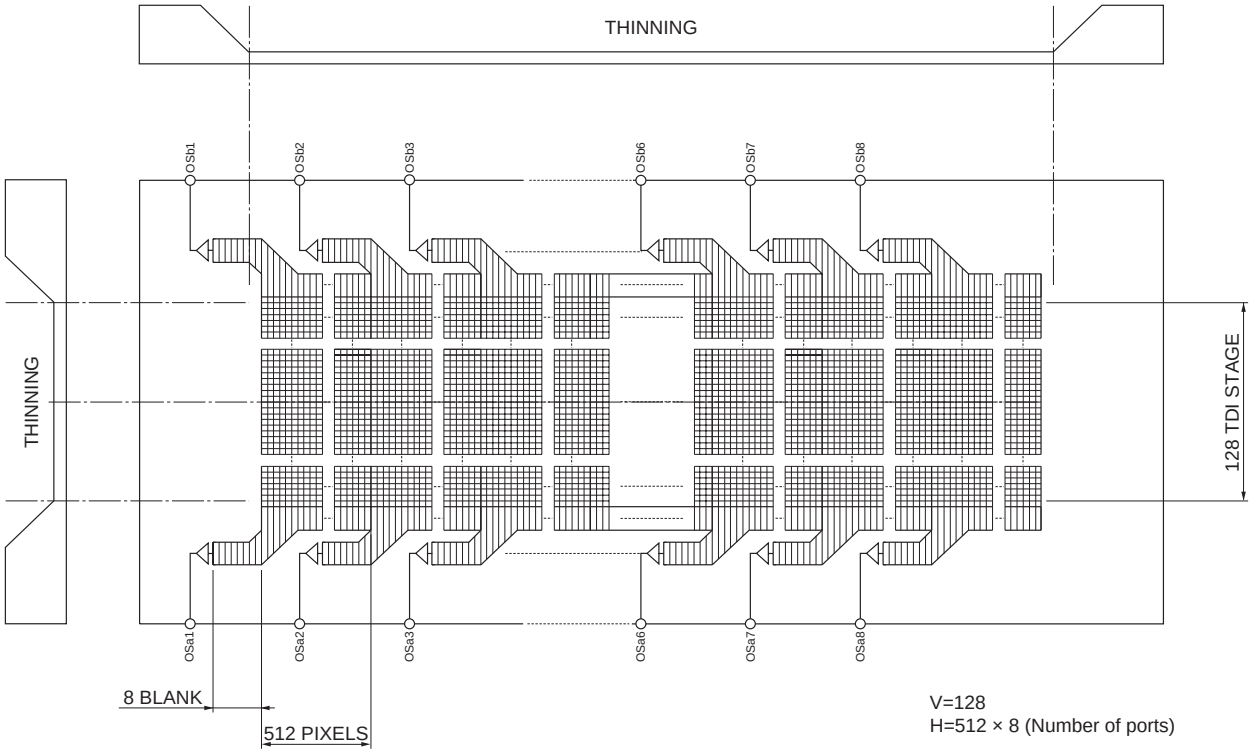
■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	30	40	MHz
Reset clock frequency		frg	-	30	40	MHz
Vertical shift register capacitance	S10200-02	C_{P1V}, C_{P2V}, C_{P3V}	-	250	-	pF
	S10201-04		-	400	-	
	S10202-08/-16		-	650	-	
Line rate	S10200-02	LR	-	50	-	kHz
	S10201-04		-	50	-	
	S10202-08		-	50	-	
	S10202-16		-	100	-	
Horizontal shift register capacitance	S10200-02	C_{P1H}, C_{P2H}	-	50	-	pF
	S10201-04		-	90	-	
	S10202-08/-16		-	90	-	
Transfer gate capacitance	S10200-02	C_{TG}	-	40	-	pF
	S10201-04		-	60	-	
	S10202-08/-16		-	100	-	
Summing gate capacitance	S10200-02	C_{SG}	-	20	-	pF
	S10201-04		-	40	-	
	S10202-08/-16		-	40	-	
Reset gate capacitance	S10200-02	C_{RG}	-	20	-	pF
	S10201-04		-	40	-	
	S10202-08/-16		-	40	-	
Charge transfer efficiency *5		CTE	0.99995	0.99999	-	-
Output level *6		Vout	-	6.5	-	V
Output impedance *7		Zo	-	300	-	Ω
Output MOSFET supply current/node		Ido	-	5	10	mA
Power consumption *6, *7		P	-	75	-	mW

*5: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*6: V_{OD}=15 V, Load resistance=2.2 kΩ
*7: Power consumption of the on-chip amplifier plus load resistance.

■ Device structure (Typical example: S10202-08)

Conceptual drawing of top view



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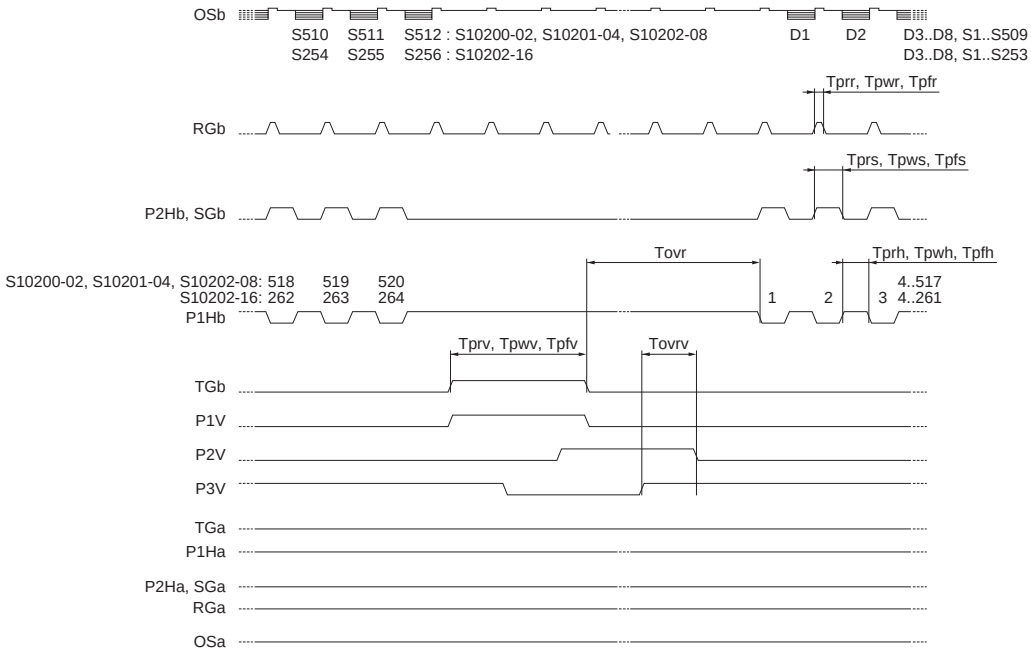
■ Timing chart

B port side readout



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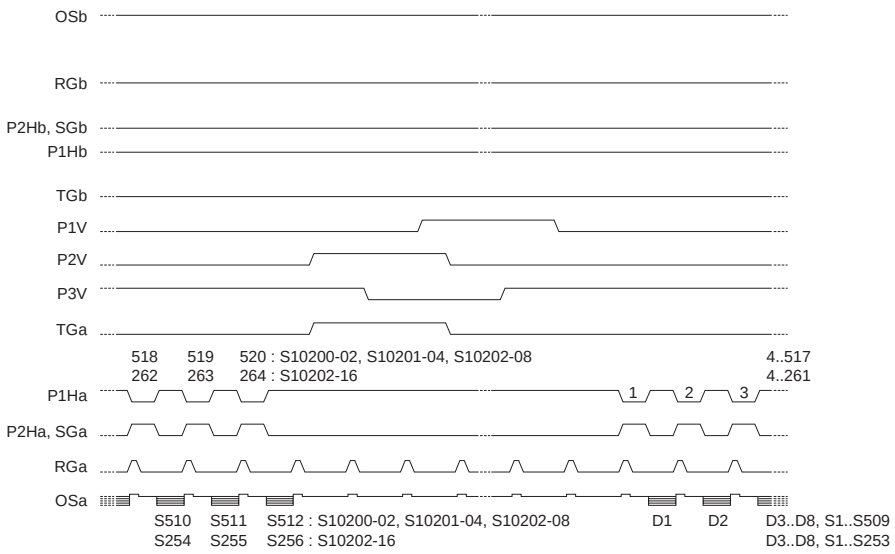
A port side readout



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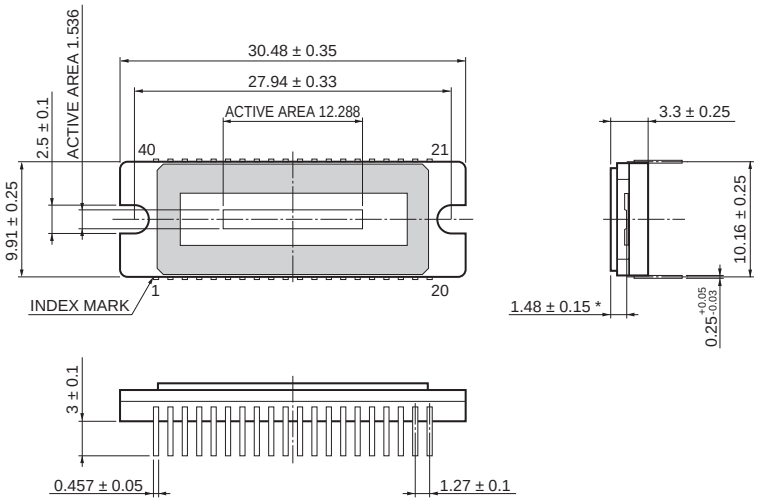
Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, 2V, 3V, TG	Pulse width	Tpwv	120	770	-	ns
	Rise and fall time	Tprv, Tpfv	2	10	-	ns
	Overlap time	Tovrv	30	300	-	ns
P1H, P2H	Pulse width *8	Tpwh	12.5	16.5	-	ns
	Rise and fall time *8	Tprh, Tpfh	3	6	-	ns
	Duty ratio *8	-	-	50	-	%
SG	Pulse width	Tpws	12.5	16.5	-	ns
	Rise and fall time	Tprs, Tpfs	2	4	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	Tpwr	5	6	-	ns
	Rise and fall time	Tprr, Tpfr	1	2	-	ns
TG - P1H	Overlap time	Tovr	30	1000	-	ns

*8: Symmetrical clock pulses should be overlapped at 50 % of maximum pulse amplitude.

■ Dimensional outlines (unit: mm)

S10200-02



* Distance between window surface and photosensitive surface

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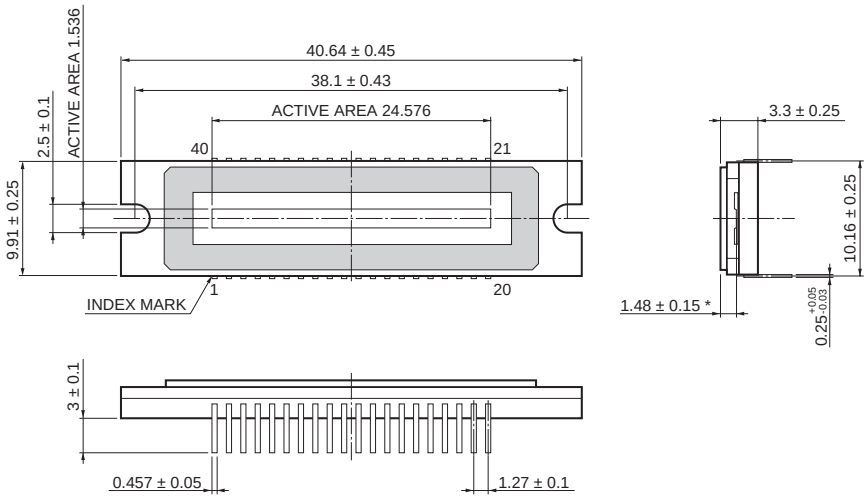
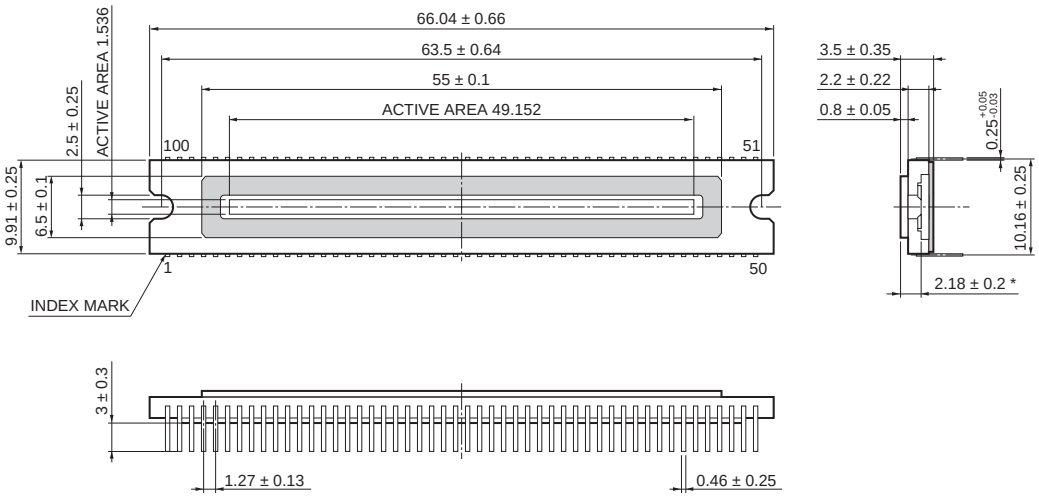
S10201-04



* Distance between window surface and photosensitive surface

KMPDA0219EA

S10202-08/-16



* Distance between window surface and photosensitive surface

KMPDA0220EA

■ Pin connections

S10200-02			S10201-04		
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	P2V	CCD vertical register clock-2	1	P2V	CCD vertical register clock-2
2	P3V	CCD vertical register clock-3	2	P3V	CCD vertical register clock-3
3	P1V	CCD vertical register clock-1	3	P1V	CCD vertical register clock-1
4	TGa	Transfer gate-a	4	TGa	Transfer gate-a
5	DGND	Digital GND	5	DGND	Digital GND
6	AGND	Analog GND	6	AGND	Analog GND
7	-		7	OSa1	Output transistor source-a1
8	OSa1	Output transistor source-a 1	8	OSa2	Output transistor source-a2
9	OSa2	Output transistor source-a 2	9	OSa3	Output transistor source-a3
10	-		10	OSa4	Output transistor source-a4
11	AGND	Analog GND	11	AGND	Analog GND
12	OD	Output drain	12	OD	Output drain
13	RD	Reset drain	13	RD	Reset drain
14	OG	Output gate	14	OG	Output gate
15	OFD	Overflow drain	15	OFD	Overflow drain
16	DGND	Digital GND	16	DGND	Digital GND
17	RGa	Reset gate-a	17	RGa	Reset gate-a
18	SGa	Summing gate-a	18	SGa	Summing gate-a
19	P1Ha	CCD horizontal register-a clock-1	19	P1Ha	CCD horizontal register-a clock-1
20	P2Ha	CCD horizontal register-a clock-2	20	P2Ha	CCD horizontal register-a clock-2
21	P2Hb	CCD horizontal register-b clock-2	21	P2Hb	CCD horizontal register-b clock-2
22	P1Hb	CCD horizontal register-b clock-1	22	P1Hb	CCD horizontal register-b clock-1
23	SGb	Summing gate-b	23	SGb	Summing gate-b
24	RGb	Reset gate-b	24	RGb	Reset gate-b
25	DGND	Digital GND	25	DGND	Digital GND
26	OFG	Overflow gate	26	OFG	Overflow gate
27	OG	Output gate	27	OG	Output gate
28	RD	Reset drain	28	RD	Reset drain
29	OD	Output drain	29	OD	Output drain
30	AGND	Analog GND	30	AGND	Analog GND
31	-		31	OSb4	Output transistor source-b4
32	OSb2	Output transistor source-b2	32	OSb3	Output transistor source-b3
33	OSb1	Output transistor source-b1	33	OSb2	Output transistor source-b2
34	-		34	OSb1	Output transistor source-b1
35	AGND	Analog GND	35	AGND	Analog GND
36	DGND	Digital GND	36	DGND	Digital GND
37	TGb	Transfer gate-b	37	TGb	Transfer gate-b
38	P1V	CCD vertical register clock-1	38	P1V	CCD vertical register clock-1
39	P3V	CCD vertical register clock-3	39	P3V	CCD vertical register clock-3
40	P2V	CCD vertical register clock-2	40	P2V	CCD vertical register clock-2

S10202-08					
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	P2V	CCD vertical register clock-2	51	P2V	CCD vertical register clock-2
2	P3V	CCD vertical register clock-3	52	P3V	CCD vertical register clock-3
3	P1V	CCD vertical register clock-1	53	P1V	CCD vertical register clock-1
4	TGa	Transfer gate-a	54	TGb	Transfer gate-b
5	DGND	Digital GND	55	SGb2	Summing gate-b 2
6	OFG	Overflow gate	56	RGb2	Reset gate-b 2
7	OFD	Overflow drain	57	DGND	Digital GND
8	RD	Reset drain	58	OFG	Overflow gate
9	OD	Output drain	59	OFD	Overflow drain
10	AGND	Analog GND	60	OG	Output gate
11	OSa1	Output transistor source-a1	61	RD	Reset drain
12	-		62	OD	Output drain
13	OSa2	Output transistor source-a2	63	AGND	Analog GND
14	-		64	-	
15	OSa3	Output transistor source-a3	65	OSb8	Output transistor source-b8
16	-		66	-	
17	OSa4	Output transistor source-a4	67	OSb7	Output transistor source-b7
18	-		68	-	
19	AGND	Analog GND	69	OSb6	Output transistor source-b6
20	OG	Output gate	70	-	
21	DGND	Digital GND	71	OSb5	Output transistor source-b5
22	RGa1	Reset gate-a 1	72	AGND	Analog GND
23	SGa1	Summing gate-a 1	73	DGND	Digital GND
24	P1Ha1	CCD horizontal register-a1 clock-1	74	P1Hb2	CCD horizontal register-b2 clock-1
25	P2Ha1	CCD horizontal register-a1 clock-2	75	P2Hb2	CCD horizontal register-b2 clock-2
26	P2Ha2	CCD horizontal register-a2 clock-2	76	P2Hb1	CCD horizontal register-b1 clock-2
27	P1Ha2	CCD horizontal register-a2 clock-1	77	P1Hb1	CCD horizontal register-b1 clock-1
28	DGND	Digital GND	78	SGb1	Summing gate-b 1
29	AGND	Analog GND	79	RGb1	Reset gate-b 1
30	OSa5	Output transistor source-a5	80	DGND	Digital GND
31	-		81	OG	Output gate
32	OSa6	Output transistor source-a6	82	AGND	Analog GND
33	-		83	-	
34	OSa7	Output transistor source-a7	84	OSb4	Output transistor source-b4
35	-		85	-	
36	OSa8	Output transistor source-a8	86	OSb3	Output transistor source-b3
37	-		87	-	
38	AGND	Analog GND	88	OSb2	Output transistor source-b2
39	OD	Output drain	89	-	
40	RD	Reset drain	90	OSb1	Output transistor source-b1
41	OG	Output gate	91	AGND	Analog GND
42	OFD	Overflow drain	92	OD	Output drain
43	OFG	Overflow gate	93	RD	Reset drain
44	DGND	Digital GND	94	OFD	Overflow drain
45	RGa2	Reset gate-a 2	95	OFG	Overflow gate
46	SGa2	Summing gate-a 2	96	DGND	Digital GND
47	TGa	Transfer gate-a	97	TGb	Transfer gate-b
48	P1V	CCD vertical register clock-1	98	P1V	CCD vertical register clock-1
49	P3V	CCD vertical register clock-3	99	P3V	CCD vertical register clock-3
50	P2V	CCD vertical register clock-2	100	P2V	CCD vertical register clock-2

S10202-16					
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	P2V	CCD vertical register clock-2	51	P2V	CCD vertical register clock-2
2	P3V	CCD vertical register clock-3	52	P3V	CCD vertical register clock-3
3	P1V	CCD vertical register clock-1	53	P1V	CCD vertical register clock-1
4	TGa	Transfer gate-a	54	TGb	Transfer gate-b
5	DGND	Digital GND	55	SGb2	Summing gate-b 2
6	OFG	Overflow gate	56	RGb2	Reset gate-b 2
7	OFD	Overflow drain	57	DGND	Digital GND
8	RD	Reset drain	58	OFG	Overflow gate
9	OD	Output drain	59	OFD	Overflow drain
10	AGND	Analog GND	60	OG	Output gate
11	OSa1	Output transistor source-a1	61	RD	Reset drain
12	OSa2	Output transistor source-a2	62	OD	Output drain
13	OSa3	Output transistor source-a3	63	AGND	Analog GND
14	OSa4	Output transistor source-a4	64	OSb16	Output transistor source-b16
15	OSa5	Output transistor source-a5	65	OSb15	Output transistor source-b15
16	OSa6	Output transistor source-a6	66	OSb14	Output transistor source-b14
17	OSa7	Output transistor source-a7	67	OSb13	Output transistor source-b13
18	OSa8	Output transistor source-a8	68	OSb12	Output transistor source-b12
19	AGND	Analog GND	69	OSb11	Output transistor source-b11
20	OG	Output gate	70	OSb10	Output transistor source-b10
21	DGND	Digital GND	71	OSb9	Output transistor source-b9
22	RGa1	Reset gate-a 1	72	AGND	Analog GND
23	SGa1	Summing gate-a 1	73	DGND	Digital GND
24	P1Ha1	CCD horizontal register-a1 clock-1	74	P1Hb2	CCD horizontal register-b2 clock-1
25	P2Ha1	CCD horizontal register-a1 clock-2	75	P2Hb2	CCD horizontal register-b2 clock-2
26	P2Ha2	CCD horizontal register-a2 clock-2	76	P2Hb1	CCD horizontal register-b1 clock-2
27	P1Ha2	CCD horizontal register-a2 clock-1	77	P1Hb1	CCD horizontal register-b1 clock-1
28	DGND	Digital GND	78	SGb1	Summing gate-b 1
29	AGND	Analog GND	79	RGb1	Reset gate-b 1
30	OSa9	Output transistor source-a9	80	DGND	Digital GND
31	OSa10	Output transistor source-a10	81	OG	Output gate
32	OSa11	Output transistor source-a11	82	AGND	Analog GND
33	OSa12	Output transistor source-a12	83	OSb8	Output transistor source-b8
34	OSa13	Output transistor source-a13	84	OSb7	Output transistor source-b7
35	OSa14	Output transistor source-a14	85	OSb6	Output transistor source-b6
36	OSa15	Output transistor source-a15	86	OSb5	Output transistor source-b5
37	OSa16	Output transistor source-a16	87	OSb4	Output transistor source-b4
38	AGND	Analog GND	88	OSb3	Output transistor source-b3
39	OD	Output drain	89	OSb2	Output transistor source-b2
40	RD	Reset drain	90	OSb1	Output transistor source-b1
41	OG	Output gate	91	AGND	Analog GND
42	OFD	Overflow drain	92	OD	Output drain
43	OFG	Overflow gate	93	RD	Reset drain
44	DGND	Digital GND	94	OFD	Overflow drain
45	RGa2	Reset gate-a 2	95	OFG	Overflow gate
46	SGa2	Summing gate-a 2	96	DGND	Digital GND
47	TGa	Transfer gate-a	97	TGb	Transfer gate-b
48	P1V	CCD vertical register clock-1	98	P1V	CCD vertical register clock-1
49	P3V	CCD vertical register clock-3	99	P3V	CCD vertical register clock-3
50	P2V	CCD vertical register clock-2	100	P2V	CCD vertical register clock-2

■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk, etc. that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

TDI camera C10000 series

The TDI camera C10000 series is useful in a wide range of imaging applications that require both high speed and high sensitivity, including in-line monitoring and inspection.

■ Specifications

Parameter	C10000-301	C10000-401
Pixel number	1024 (H) × 128 (V)	2048 (H) × 128 (V)
Device structure	Back-thinned type	
Pixel size	12 µm (H) × 12 µm (V)	
Effective area	12.29 mm (H) × 1.536 mm (V)	24.58 mm (H) × 1.536 mm (V)
TDI transfer direction	Bi direction	
Readout mode	TDI readout mode or Frame readout mode *9	
TDI output channel	2 ports (512 × 2)	4 ports (512 × 4)
Anti-blooming	Lateral overflow drain (× 100)	
TDI pixel clock rate	30 MHz	
TDI line rate	0.45 kHz to 50 kHz	
Full-well capacity (Typ.)	100000 electrons	
Readout noise (Typ.)	130 electrons rms	
Dynamic range (Typ.)	770 : 1	
A/D converter	12-bit / 8-bit *10	
Image processing	Real-time shading correction with internal DSP	
Lens mount	C-mount	F-mount
Interface	Base configuration	
Camera output clock	60 MHz	
Camera output channel	1 port (1024 × 1)	2 ports (1024 × 2)
TDI line rate control	Internal setting by serial command *11 External trigger	
Analog enhancement gain	0 dB to 14 dB	
Power / Power consumption	DC +12 V / 20 V · A	
Camera control	Serial control in Camera link	

*9: Frame readout mode is useful for easy focusing, but it is not suitable for measurement.
Please consult with our sales office for details.
*10: Selectable by serial command.
*11: Internal TDI line rate can be set in 33 ns steps.

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Cat. No. KMPD1098E02
Apr. 2007 DN