

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74AC125P, TC74AC125F, TC74AC125FN, TC74AC125FT TC74AC126P, TC74AC126F, TC74AC126FN

TC74AC125P/F/FN/FT Quad Bus Buffer

TC74AC126P/F/FN Quad Bus Buffer

The TC74AC125/126 are advanced high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

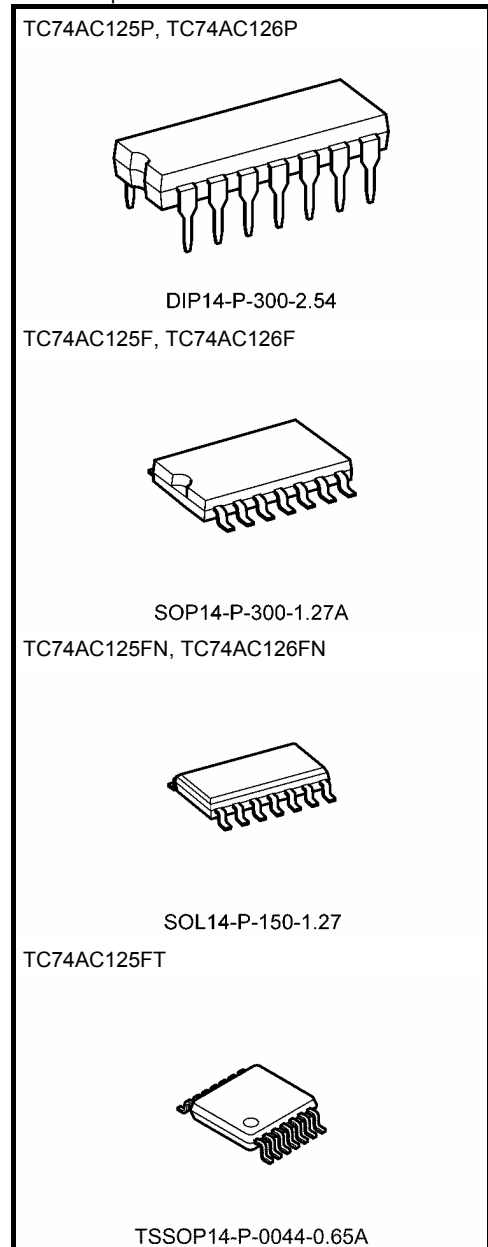
The TC74AC125 requires the 3-state control input  $\bar{G}$  to be set high to place the output into the high impedance state, whereas the TC74AC126 requires the control input to be set low to place the output into high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $t_{pd} = 4.0 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 8 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA}$  (min)  
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC}(\text{opr}) = 2 \text{ to } 5.5 \text{ V}$
- Pin and function compatible with 74F125/126

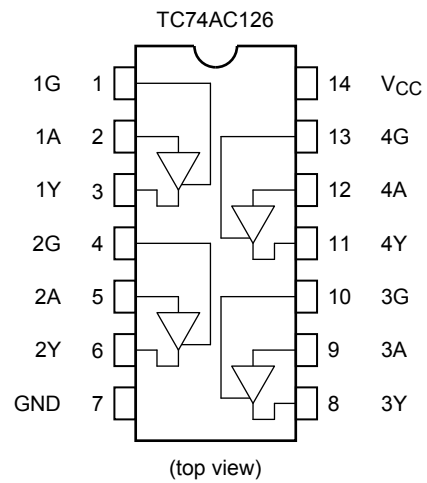
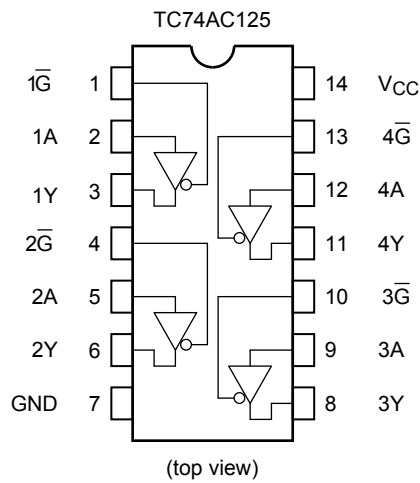
Note: xxxFN (JEDEC SOP) is not available in Japan.



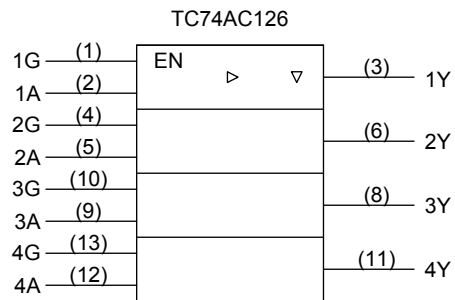
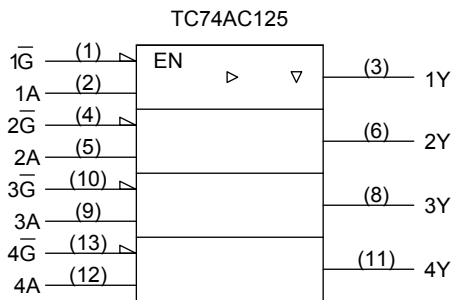
#### Weight

DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

## Pin Assignment



## IEC Logic Symbol



## Truth Table

**TC74AC125**

Inputs		Output
$\bar{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care

Z: High impedance

**TC74AC126**

Inputs		Output
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't care

Z: High impedance

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied up to 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dV	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-level output voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—				
I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—				
Low-level output voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 12 mA	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44				
I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65				
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

## AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \text{ } \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Propagation delay time	t <sub>pLH</sub>	—	3.3 ± 0.3	—	6.4	10.5	1.0	12.0	ns
	t <sub>pHL</sub>	—	5.0 ± 0.5	—	4.7	7.0	1.0	8.0	
Output enable time	t <sub>pZL</sub>	—	3.3 ± 0.3	—	7.1	12.3	1.0	14.0	ns
	t <sub>pZH</sub>	—	5.0 ± 0.5	—	5.0	7.9	1.0	9.0	
Output disable time	t <sub>pLZ</sub>	—	3.3 ± 0.3	—	5.1	8.8	1.0	10.0	ns
	t <sub>pHZ</sub>	—	5.0 ± 0.5	—	4.6	6.6	1.0	7.5	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Output capacitance	C <sub>OUT</sub>	—	—	10	—	—	—	pF	
Power dissipation capacitance	C <sub>PD</sub>	(Note)	—	24	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

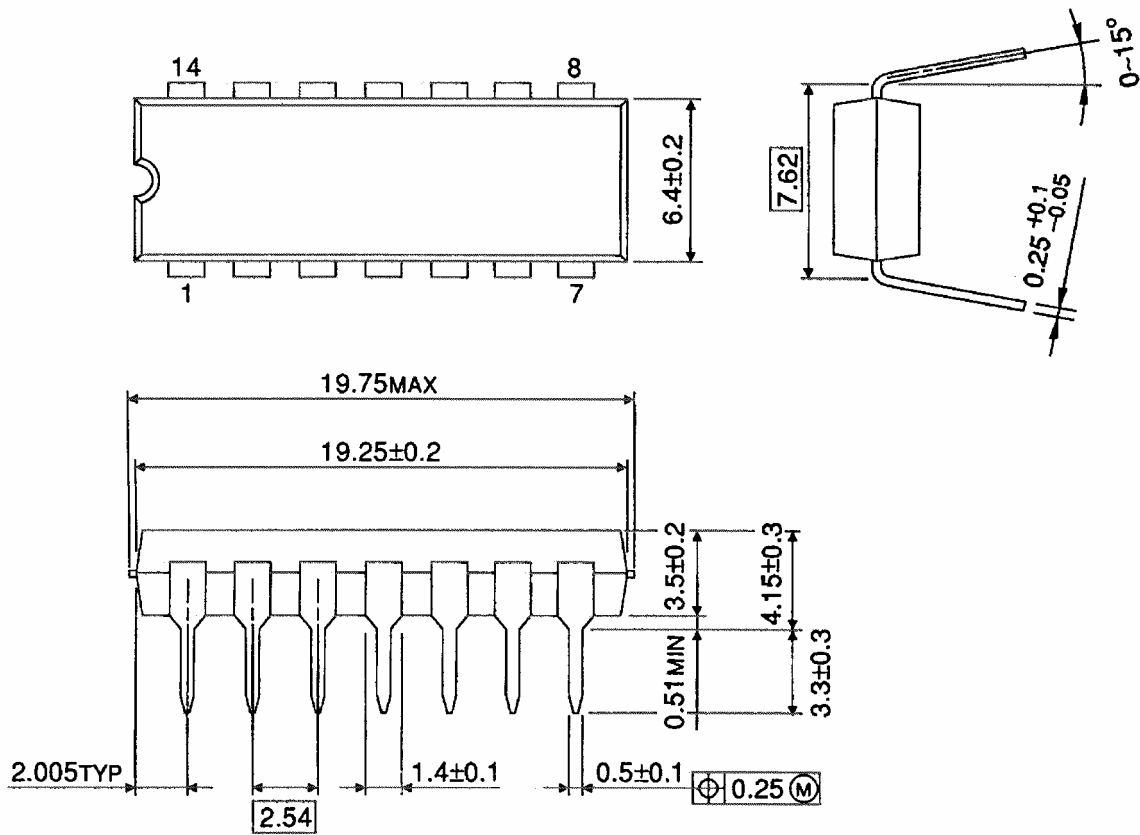
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

## Package Dimensions

DIP14-P-300-2.54

Unit : mm

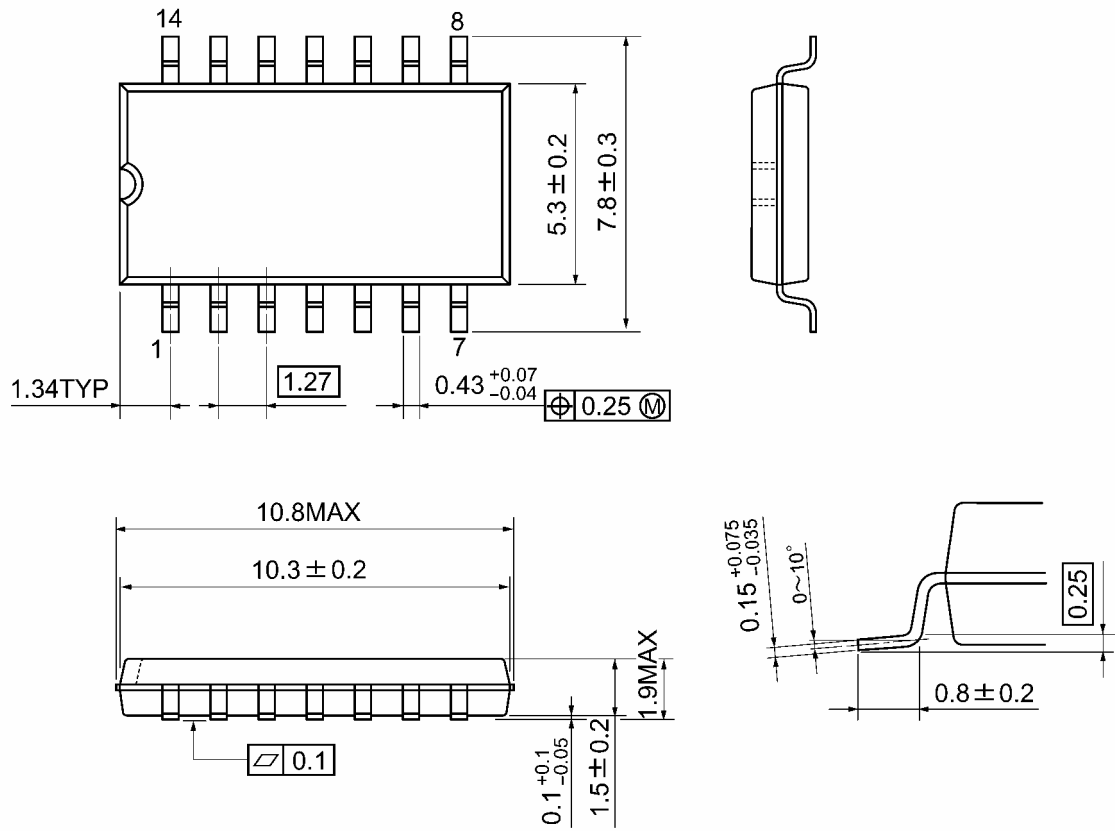


Weight: 0.96 g (typ.)

**Package Dimensions**

SOP14-P-300-1.27A

Unit: mm

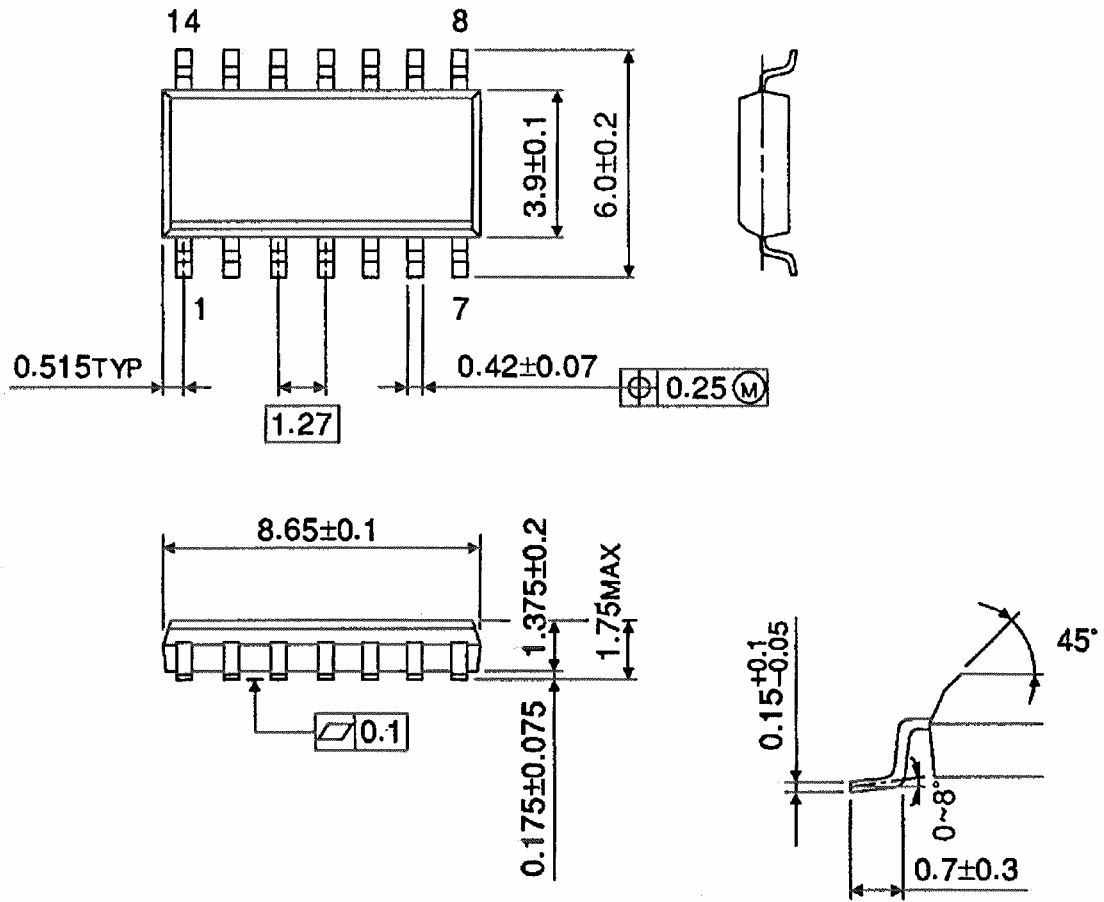


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

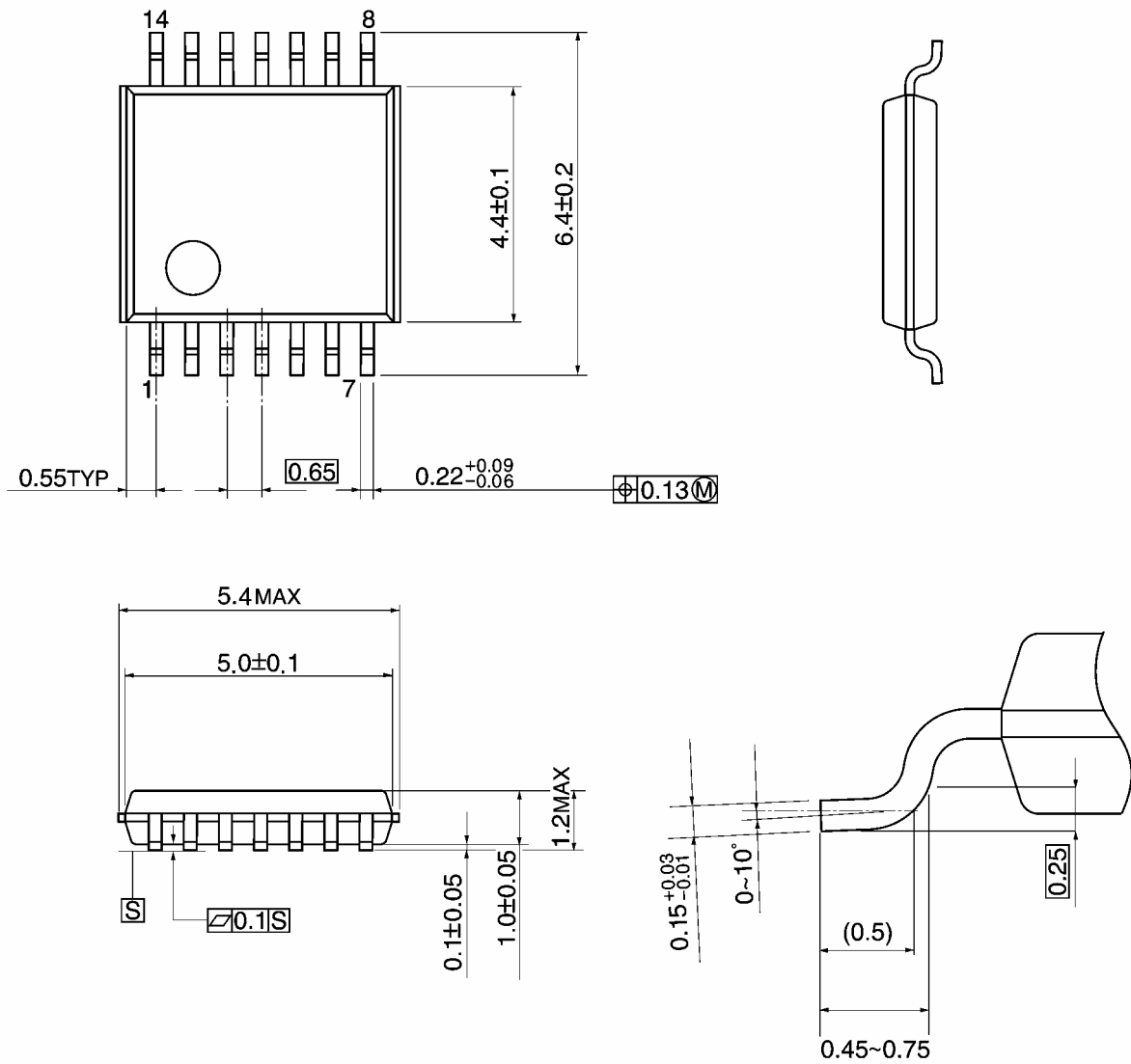
Weight: 0.12 g (typ.)



**Package Dimensions**

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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20070701-EN GENERAL

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