19-1013; Rev 0; 11/07

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

General Description

The MAX16050 monitors up to 5 voltages and sequences up to 4 voltages, while the MAX16051 monitors up to 6 voltages and sequences up to 5 voltages. These devices provide an adjustable delay as each supply is turned on and they monitor each power-supply voltage. When all of the voltages reach their final values and the reset delay timer expires, a power-on-reset (POR) output deasserts allowing the microcontroller (µC) to operate. If any voltage falls below its threshold, the reset output asserts and all voltage supplies are turned off. The MAX16050/MAX16051 can be daisy-chained to control a higher number of voltages in a system.

During a power-down event, the MAX16050/MAX16051 can reverse sequence the outputs. In this situation, each voltage is turned off sequentially until it reaches a 250mV level, at which point, the next supply is turned off. The MAX16050/MAX16051 also provide internal pulldown circuitry that turns on during power-down, to help discharge large output capacitors.

The MAX16050/MAX16051 feature a charge-pump supply output that can be used as a pullup voltage for driving external n-channel MOSFETs and an overvoltage output that indicates when any of the monitored voltages exceeds its overvoltage threshold. The MAX16050 also provides three sequence control inputs for changing the sequence order, while the MAX16051 has a fixed sequence order.

The MAX16050/MAX16051 are available in a 28-pin (4mm x 4mm) thin QFN package and are fully specified over the -40°C to +85°C extended operating temperature range.

Applications

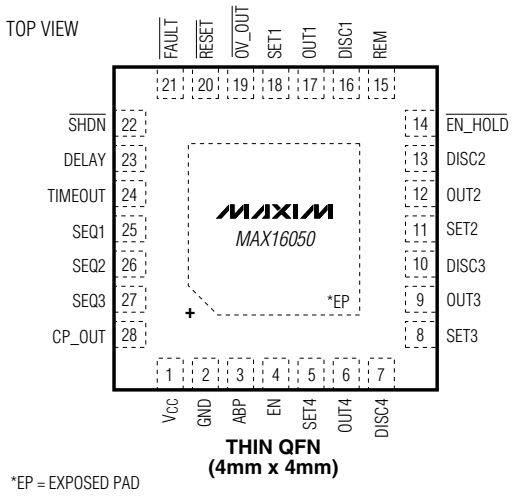
Servers
Workstations
Networking Systems
Telecom Equipment
Storage Systems

Typical Operating Circuit appears at end of data sheet.

Features

- **Monitor Up to 6 Voltages/Sequence Up to 5 Voltages**
- **Pin-Selectable Sequencing Order (MAX16050 Only)**
- **Reverse-Sequencing Capability on Shutdown**
- **Overvoltage Monitoring with Independent Output**
- **±1.5% Threshold Accuracy**
- **2.7V to 13.2V Operating Voltage Range**
- **Charge Pump to Fully Enhance External n-Channel FETs**
- **Capacitor-Adjustable Sequencing Delay**
- **Fixed or Capacitor-Adjustable Reset Timeout**
- **Internal 85mA Pulldowns for Discharging Capacitive Loads Quickly**
- **Daisy-Chaining Capability to Communicate Across Multiple Devices**
- **Small 4mm x 4mm, 28-Pin TQFN Package**

Pin Configurations



Pin Configurations continued at end of data sheet.

Ordering Information

PART	MONITORED VOLTAGES	VOLTAGES SEQUENCED	PIN-PACKAGE	PACKAGE CODE
MAX16050ETI+	5	4	28 TQFN-EP*	T2844-1
MAX16051ETI+	6	5	28 TQFN-EP*	T2844-1

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes lead-free package.

**EP = Exposed pad.*

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} .....-0.3V to +30V
REM, OUT_, DISC_.....-0.3V to +30V
$\overline{RESET}$, $\overline{SHDN}$, SET_, $\overline{FAULT}$, $\overline{EN\_HOLD}$, EN, DELAY, $\overline{OV\_OUT}$, ABP, TIMEOUT, SEQ_.....-0.3V to +6V
CP_OUT.....-0.3V to (V_{CC} + 6V)
$\overline{RESET}$ Current 50mA
DISC_ Current.....180mA
Input/Output Current (all other pins).....20mA

Continuous Power Dissipation (T_A = +70°C)
28-Pin (4mm x 4mm) Thin QFN (derate 28.6mW/°C above +70°C) 2285mW*
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**As per JEDEC51 Standard (Multilayer Board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 13.2V, V_{EN} = V_{ABP}, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	V_{CC}	Voltage on V_{CC} to ensure the device is fully operational	2.7		13.2	V
Operating Voltage	V_{CCR}	$V_{DISC\_}$ = $V_{OUT\_}$ = $V_{\overline{RESET}}$ = low, voltage on V_{CC} rising		1.8		V
Regulated Supply Voltage	V_{ABP}	I_{ABP} = 1mA (external sourcing current from ABP)	2.45		2.90	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage on ABP, ABP rising	2.1	2.3		V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	ABP falling		100		mV
Supply Current	I_{CC}	V_{CC} = 3.3V, all OUT_ = high, no load		0.7	1.1	mA
MONITORED ANALOG INPUTS						
SET_ Threshold	V_{TH}	SET_ falling	0.492	0.5	0.508	V
SET_ Threshold Hysteresis	V_{TH_HYS}	SET_ rising		0.5		%V_{TH}
SET1–SET4 Input Current	I_{SET}	$V_{SET\_}$ = 0.5V	-100		+100	nA
SET5 Input Current	I_{SET5}	V_{SET5} = 0.5V (MAX16051 only)	-30		+30	µA
SET_ Threshold Tempco	$\Delta V_{TH/\_TC}$			30		ppm/°C
Overvoltage Threshold	V_{TH_OV}	SET_ falling	0.541	0.55	0.558	V
Overvoltage Threshold Hysteresis		SET_ rising		0.5		%V_{TH_OV}
EN Threshold	V_{TH_EN}	EN_ falling	0.492	0.5	0.508	V
EN Threshold Hysteresis	V_{EN_HYS}	EN_ rising		0.5		%V_{TH_EN}
EN Input Current	I_{EN}	V_{EN} = 0.5V	-100		+100	nA
SEQUENCING, CAPACITOR DISCHARGE, AND SEQUENCE TIMING OUTPUTS						
OUT_ Output Low Voltage	V_{OL_OUT}	V_{CC} = 3.3V, I_{SINK} = 3.2mA			0.3	V
		V_{CC} = 1.8V, I_{SINK} = 100µA			0.3	
OUT_ Leakage Current	I_{LKG_OUT}	$V_{OUT\_}$ = 12V, OUT_ asserted			1	µA
DISC_ Output Pulldown Current	I_{OL_DISC}	Pulldown current during fault condition or power-down mode, $V_{DISC\_}$ = 1V		85		mA
DISC_ Output Leakage Current	I_{LKG_DISC}	$V_{DISC\_}$ = 3.3V, not in power-down mode			1	µA
DISC_ Power Low Threshold	V_{TH_PL}	DISC_ falling	200	250	300	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 13.2V, V_{EN} = V_{ABP}, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DELAY, TIMEOUT Output Source Current	I_{DT}	V_{DELAY} = $V_{TIMEOUT}$ = 0V	1.7	2.5	3.0	µA
DELAY, TIMEOUT Threshold Voltage	V_{TH_DT}		1.218	1.250	1.281	V
DIGITAL INPUTS/OUTPUTS						
$\overline{SHDN}$, $\overline{FAULT}$, $\overline{EN\_HOLD}$ Input-Logic Low Voltage	V_{IL}				0.4	V
$\overline{SHDN}$, $\overline{FAULT}$, $\overline{EN\_HOLD}$ Input-Logic High Voltage	V_{IH}		2			V
$\overline{EN\_HOLD}$ Input Current	I_I				1	µA
$\overline{EN\_HOLD}$ to OUT Delay	t_{EN_OUT}			3		µs
$\overline{FAULT}$, $\overline{SHDN}$ to ABP Pullup Resistance	R_P		60	100	160	kΩ
$\overline{SHDN}$ to OUT_ Delay	t_{OUT}			12		µs
$\overline{RESET}$ Output Low Voltage	V_{OL}	V_{CC} = 3.3V, I_{SINK} = 3.2mA			0.3	V
		V_{CC} = 1.8V, I_{SINK} = 100µA			0.3	
REM, $\overline{FAULT}$ Output Low Voltage	V_{OL_RF}	V_{CC} = 3.3V, I_{SINK} = 3.2mA			0.3	V
$\overline{FAULT}$ Pulse Width	t_{FAULT_PW}		1.9			µs
SET_ to $\overline{FAULT}$ Delay Time	t_{SET_FAULT}	SET_ falling below respective threshold		2.5		µs
SEQ1–SEQ3 Logic-High Level	V_{IH_SEQ}	MAX16050 only	V_{ABP} - 0.35			V
SEQ1–SEQ3 Logic High-Impedance (No Connect) Level	V_{IX_SEQ}	MAX16050 only	0.92		1.45	V
SEQ1–SEQ3 Logic-Low Level	V_{IL_SEQ}	MAX16050 only			0.33	V
SEQ1–SEQ3 High-Impedance State Tolerance Current	I_{IX}	MAX16050 (Note 3)	-6		+6	µA
RESET CIRCUIT						
$\overline{RESET}$, REM, $\overline{OV\_OUT}$ Output Leakage	I_{LKG}	$V_{\overline{RESET}}$ = V_{REM} = $V_{\overline{OV\_OUT}}$ = 5V			1	µA
$\overline{RESET}$ Timeout Period	t_{RP}	TIMEOUT = ABP	50	128	300	ms
OUT_, $\overline{FAULT}$, $\overline{SHDN}$ to $\overline{RESET}$ Delay	t_{RST}	TIMEOUT = unconnected		3		µs
CHARGE-PUMP OUTPUT						
CP_OUT Voltage	V_{CP_OUT}	I_{CP_OUT} = 0.5µA	V_{CC} + 4.6	V_{CC} + 5	V_{CC} + 5.8	V
CP_OUT Source Current	I_{CP_OUT}	V_{CP_OUT} = V_{CC} + 2V	17	25	30	µA

Note 1: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 2: When the voltage is below the V_{UVLO} and above V_{CCR}, OUT_ and $\overline{RESET}$ are asserted low.

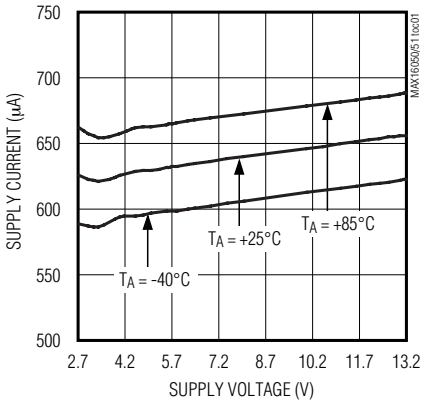
Note 3: SEQ1–SEQ3 are inputs with three logic levels: high, low, and high-impedance.

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

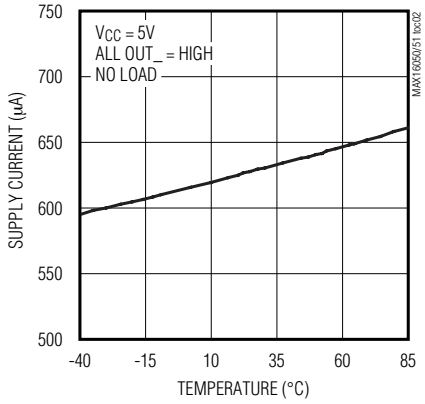
Typical Operating Characteristics

(V_{CC} = 5V; V_{EN} = V_{ABP}, T_A = +25°C, unless otherwise noted.)

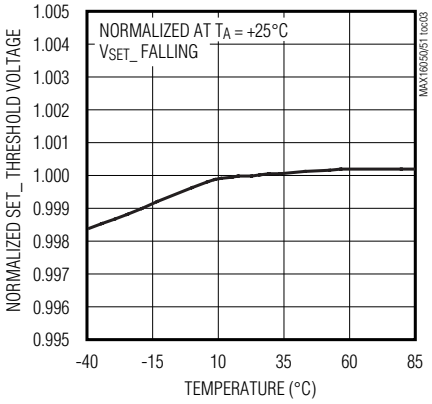
SUPPLY CURRENT vs. SUPPLY VOLTAGE



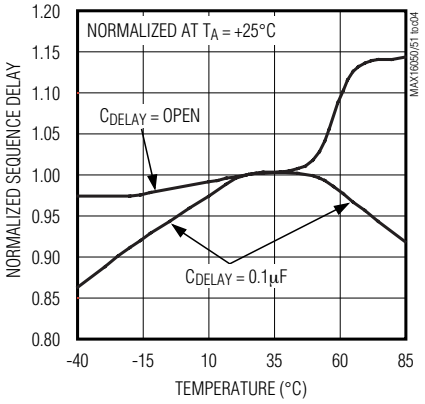
SUPPLY CURRENT vs. TEMPERATURE



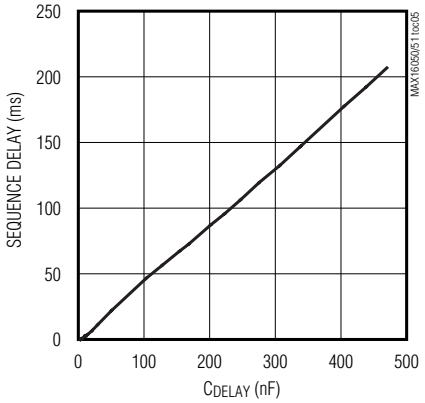
NORMALIZED SET_ THRESHOLD VOLTAGE vs. TEMPERATURE



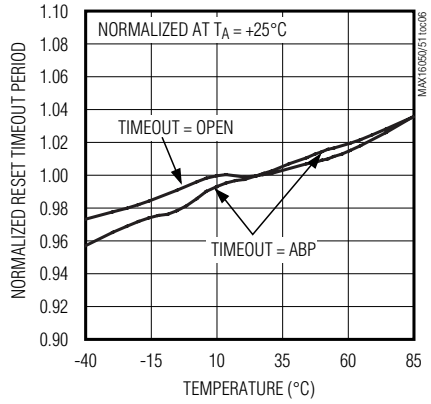
NORMALIZED SEQUENCE DELAY vs. TEMPERATURE



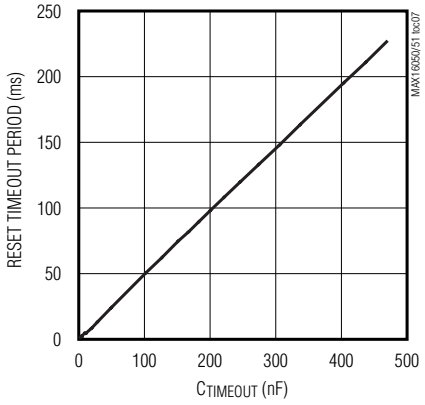
SEQUENCE DELAY vs. C_{DELAY}



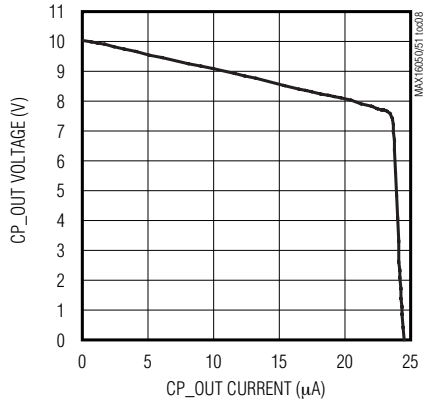
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



RESET TIMEOUT PERIOD vs. $C_{TIMEOUT}$



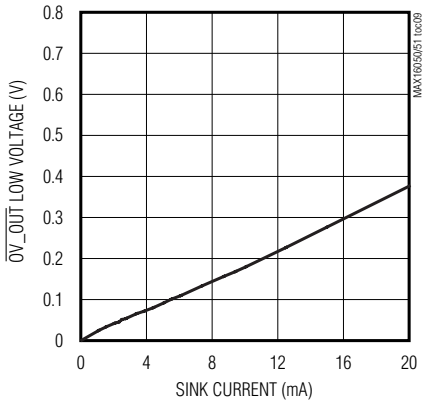
CP_OUT VOLTAGE vs. CP_OUT CURRENT



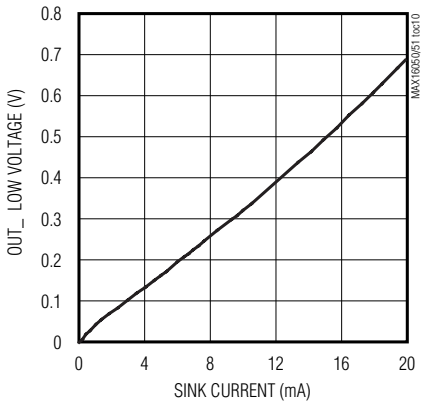
Typical Operating Characteristics (continued)

(V_{CC} = 5V; V_{EN} = V_{ABP}, T_A = +25°C, unless otherwise noted.)

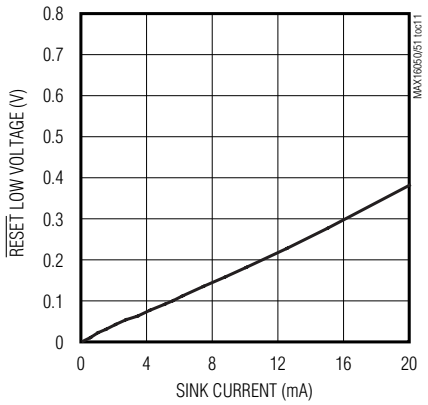
$\overline{OV\_OUT}$ LOW VOLTAGE vs. SINK CURRENT



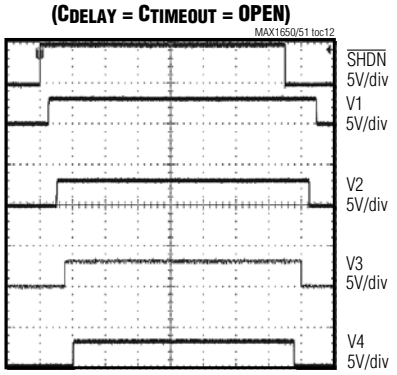
OUT_ LOW VOLTAGE vs. SINK CURRENT



$\overline{RESET}$ LOW VOLTAGE vs. SINK CURRENT

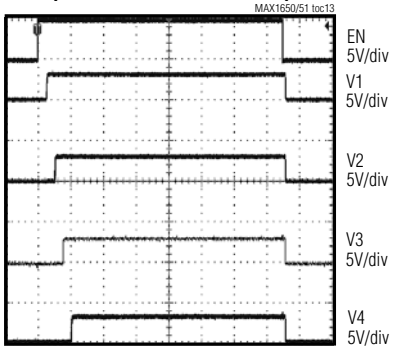


REVERSE SEQUENCE POWER-DOWN USING $\overline{SHDN}$ (C_{DELAY} = $C_{TIMEOUT}$ = OPEN)



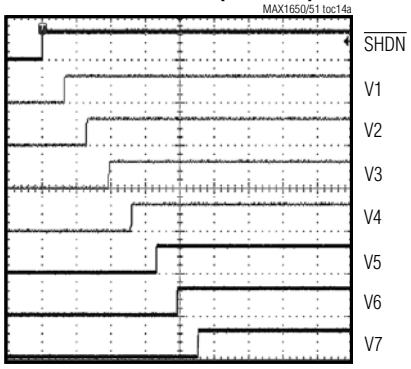
40µs/div

SIMULTANEOUS POWER-DOWN USING EN (C_{DELAY} = $C_{TIMEOUT}$ = OPEN)



40µs/div

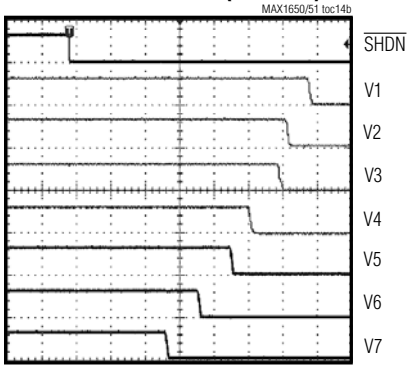
DAISY-CHAINING TWO DEVICES WITH $\overline{SHDN}$ RISING (FIGURE 7)



100µs/div

C_{DELAY} (U1) = C_{DELAY} (U2) = 100pF
$\overline{SHDN}$ = 5V/div
V1–V7 = 5V/div

DAISY-CHAINING TWO DEVICES WITH $\overline{SHDN}$ FALLING (FIGURE 7)



10µs/div

C_{DELAY} (U1) = C_{DELAY} (U2) = 100pF
$\overline{SHDN}$ = 5V/div
V1–V7 = 5V/div

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

Pin Description

PIN		NAME	FUNCTION
MAX16050	MAX16051		
1	1	V_{CC}	Device Power-Supply Input. Connect to 2.7V to 13.2V. Bypass V_{CC} to GND with a 0.1µF capacitor.
2	2	GND	Ground
3	3	ABP	Internal Supply Bypass Input. Connect a 1µF capacitor from ABP to GND. ABP is an internally generated voltage and must not be used to supply more than 1mA to external circuitry.
4	4	EN	Analog Enable Input. Connect a resistive divider at EN to monitor a voltage. The EN threshold is 0.5V.
5	5	SET4	Set Monitored Threshold 4 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET4 threshold is 0.5V.
6	6	OUT4	Open-Drain Output 4. When the voltage at SET3* is above 0.5V, OUT4 goes high impedance. OUT4 requires an external pullup resistor and can be pulled up to 13.2V.
7	7	DISC4	Discharge Pulldown Input 4. During normal operation, DISC4 is high impedance. During a fault condition or power-down, DISC4 provides an 85mA sink current.
8	8	SET3	Set Monitored Threshold 3 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET3 threshold is 0.5V.
9	9	OUT3	Open-Drain Output 3. When the voltage at SET2* is above 0.5V, OUT3 goes high impedance. OUT3 requires an external pullup resistor and can be pulled up to 13.2V.
10	10	DISC3	Discharge Pulldown Input 3. During normal operation, DISC3 is high impedance. During a fault condition or power-down, DISC3 provides an 85mA sink current.
11	11	SET2	Set Monitored Threshold 2 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET2 threshold is 0.5V.
12	12	OUT2	Open-Drain Output 2. When the voltage at SET1* is above 0.5V, OUT2 goes high impedance. OUT2 requires an external pullup resistor and can be pulled up to 13.2V.
13	13	DISC2	Discharge Pulldown Input 2. During normal operation, DISC2 is high impedance. During a fault condition or power-down, DISC2 provides an 85mA sink current.
14	14	$\overline{EN\_HOLD}$	Enable Hold Input. When $\overline{EN\_HOLD}$ is low, the device does not start the reverse-sequencing process regardless of the status of the $\overline{SHDN}$ input. Reverse sequencing is allowed when this input is pulled high. Connect to ABP if unused.
15	15	REM	Open-Drain Bus Removal Output. REM goes high impedance when all DISC_ inputs are below the DISC_ power low threshold (V_{TH_PL}). REM goes low when any DISC_ input goes above V_{TH_PL}. REM requires an external pullup resistor and can be pulled up to 13.2V.
16	16	DISC1	Discharge Pulldown Input 1. During normal operation, DISC1 is high impedance. During a fault condition or power-down, DISC1 provides an 85mA sink current.
17	17	OUT1	Open-Drain Output 1. When the voltage at EN* is above 0.5V, OUT1 goes high impedance. OUT1 requires an external pullup resistor and can be pulled up to 13.2V.

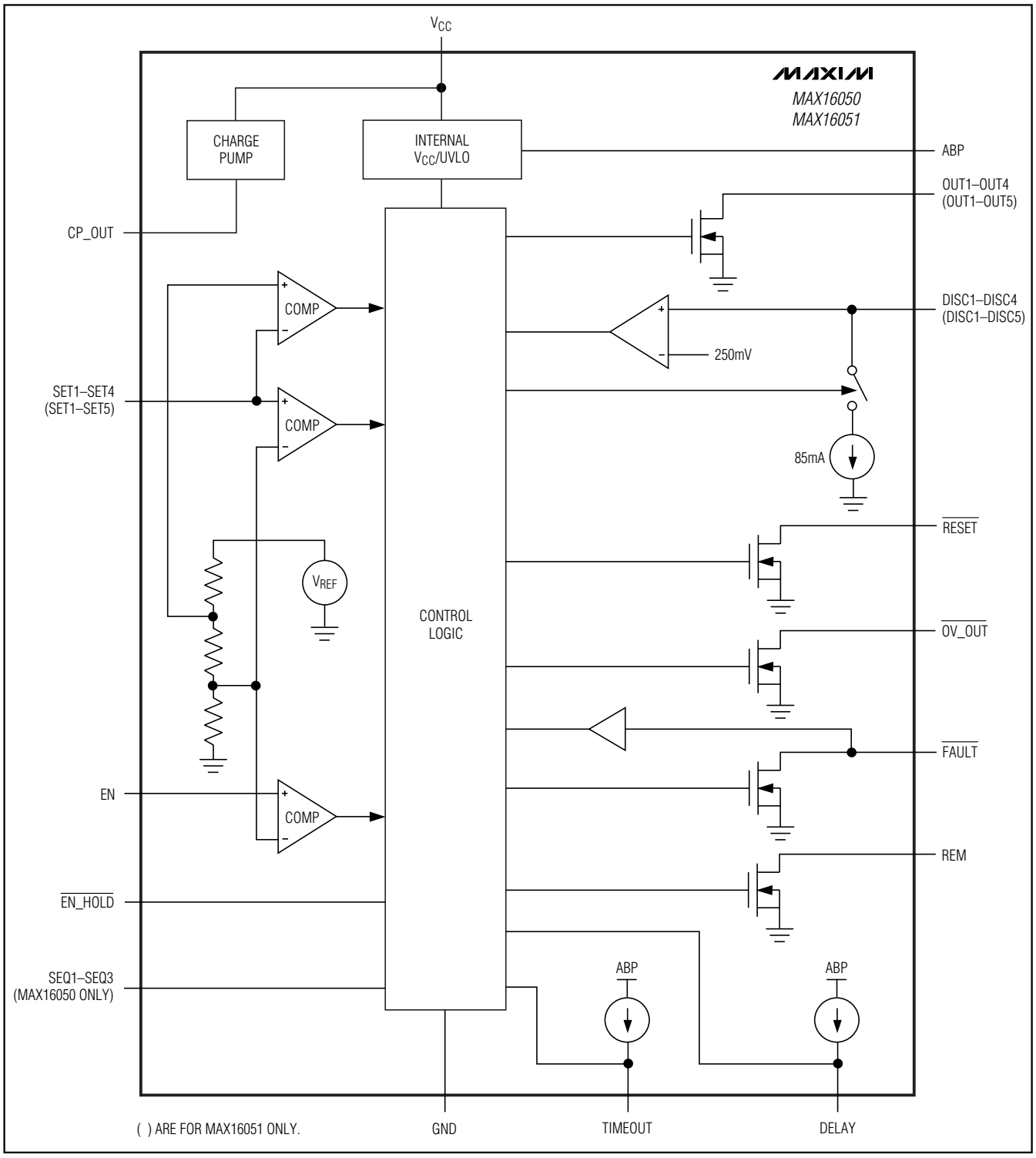
**This applies to the MAX16051. For the MAX16050, see Table 1 for the output sequence order.*

Pin Description (continued)

PIN		NAME	FUNCTION
MAX16050	MAX16051		
18	18	SET1	Set Monitored Threshold 1 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET1 threshold is 0.5V.
19	19	$\overline{OV\_OUT}$	Open-Drain Overvoltage Output. When any of the SET_ voltages exceed their 0.55V overvoltage threshold, $\overline{OV\_OUT}$ goes low. When all of the SET_ voltages are below their overvoltage threshold, $\overline{OV\_OUT}$ goes high impedance after a short propagation delay.
20	20	$\overline{RESET}$	Open-Drain Reset Output. When any of the monitored voltages (including EN) falls below its threshold, $\overline{SHDN}$ is pulled low, or $\overline{FAULT}$ is pulled low, $\overline{RESET}$ asserts and stays asserted for at least the minimum reset timeout period after all of these conditions are removed. The reset timeout is 128ms (typ) when TIMEOUT is connected to ABP or can be adjusted by connecting a capacitor from TIMEOUT to GND.
21	21	$\overline{FAULT}$	$\overline{FAULT}$ Synchronization Input/Output. While EN = $\overline{SHDN}$ = high, $\overline{FAULT}$ is pulled low when any of the SET_ voltages falls below their respective threshold. Pull $\overline{FAULT}$ low manually to assert a simultaneous power-down. $\overline{FAULT}$ is internally pulled up to ABP by a 100kΩ resistor.
22	22	$\overline{SHDN}$	Active-Low Shutdown Input. When $\overline{SHDN}$ is pulled low, the device will reverse sequence for power-down operation. $\overline{SHDN}$ is internally pulled up to ABP by a 100kΩ resistor.
23	23	DELAY	Adjustable Sequence Delay Timing Input. Connect a capacitor from DELAY to GND to set the sequence delay between each OUT_. Leave DELAY unconnected for a 10µs (typ) delay.
24	24	TIMEOUT	Adjustable Reset Timeout Input. Connect a capacitor from TIMEOUT to GND to set the reset timeout period. Connect TIMEOUT to ABP for the fixed timeout of 128ms (typ). Leave TIMEOUT unconnected for a 10µs (typ) delay.
25	—	SEQ1	Sequence Order Select Inputs. SEQ1, SEQ2, and SEQ3 allow the order of sequencing for each supply to be programmable (Table 1).
26	—	SEQ2	
27	—	SEQ3	
28	28	CP_OUT	Charge-Pump Output. An internal charge pump boosts CP_OUT to (V_{CC} + 5V) to provide a pullup voltage that can be used to drive external n-channel MOSFETs. CP_OUT sources up to 25µA.
—	25	DISC5	Discharge Pulldown Input 5. During normal operation, DISC5 is high impedance. During a fault condition or power-down, DISC5 provides an 85mA sink current.
—	26	OUT5	Open-Drain Output 5. When the voltage at SET4 is above 0.5V, OUT5 goes high impedance. OUT5 requires an external pullup resistor and can be pulled up to 13.2V.
—	27	SET5	External Set Monitored Threshold 5. Monitor a voltage by setting the threshold with an external resistive divider. The SET5 threshold is 0.5V.
—	—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the GND plane for improved heat dissipation. Do not use EP as the only ground connection.

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

Functional Diagram



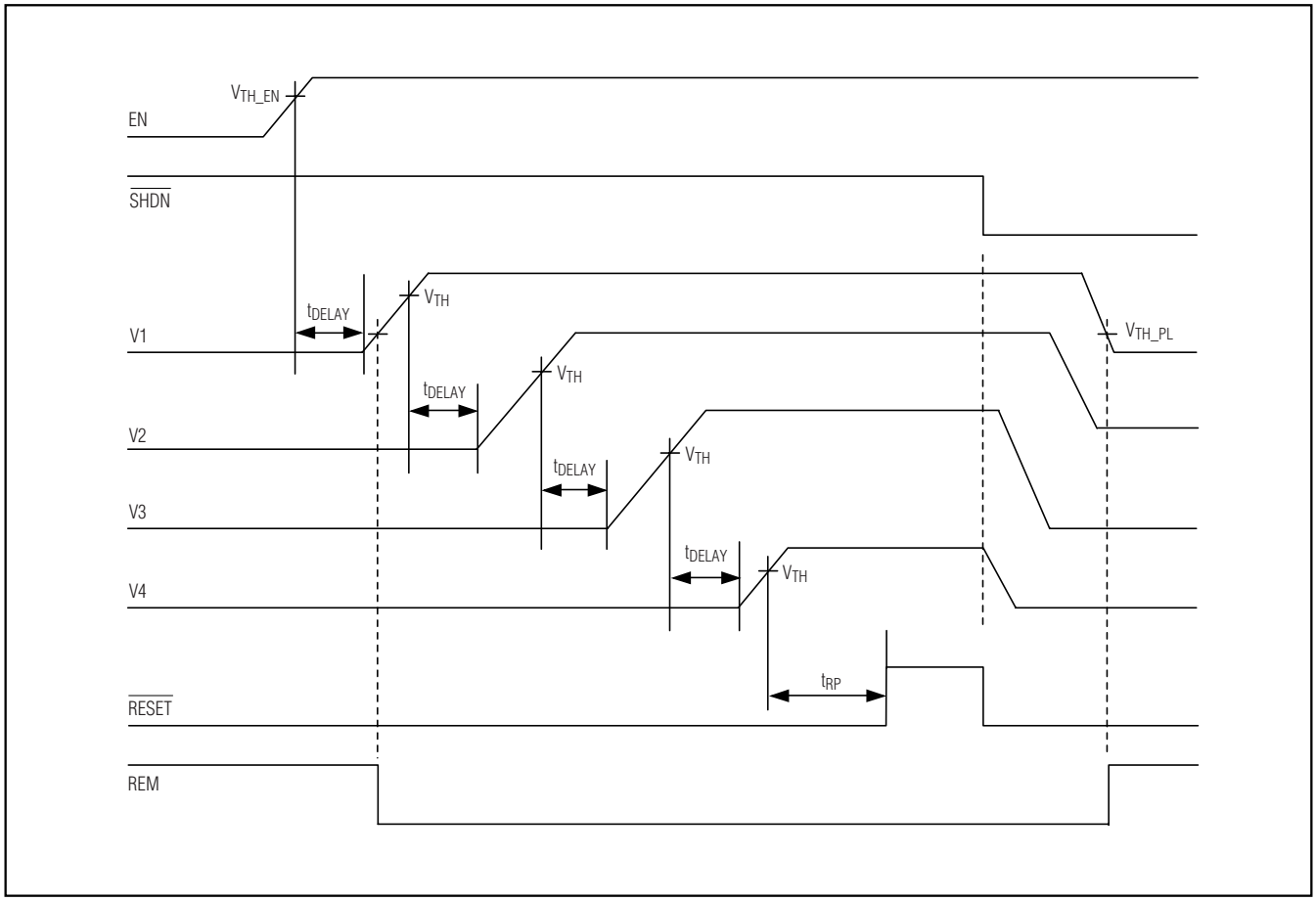


Figure 1. Sequencing Timing Diagram with Reverse Order Power-Down Using $\overline{SHDN}$

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

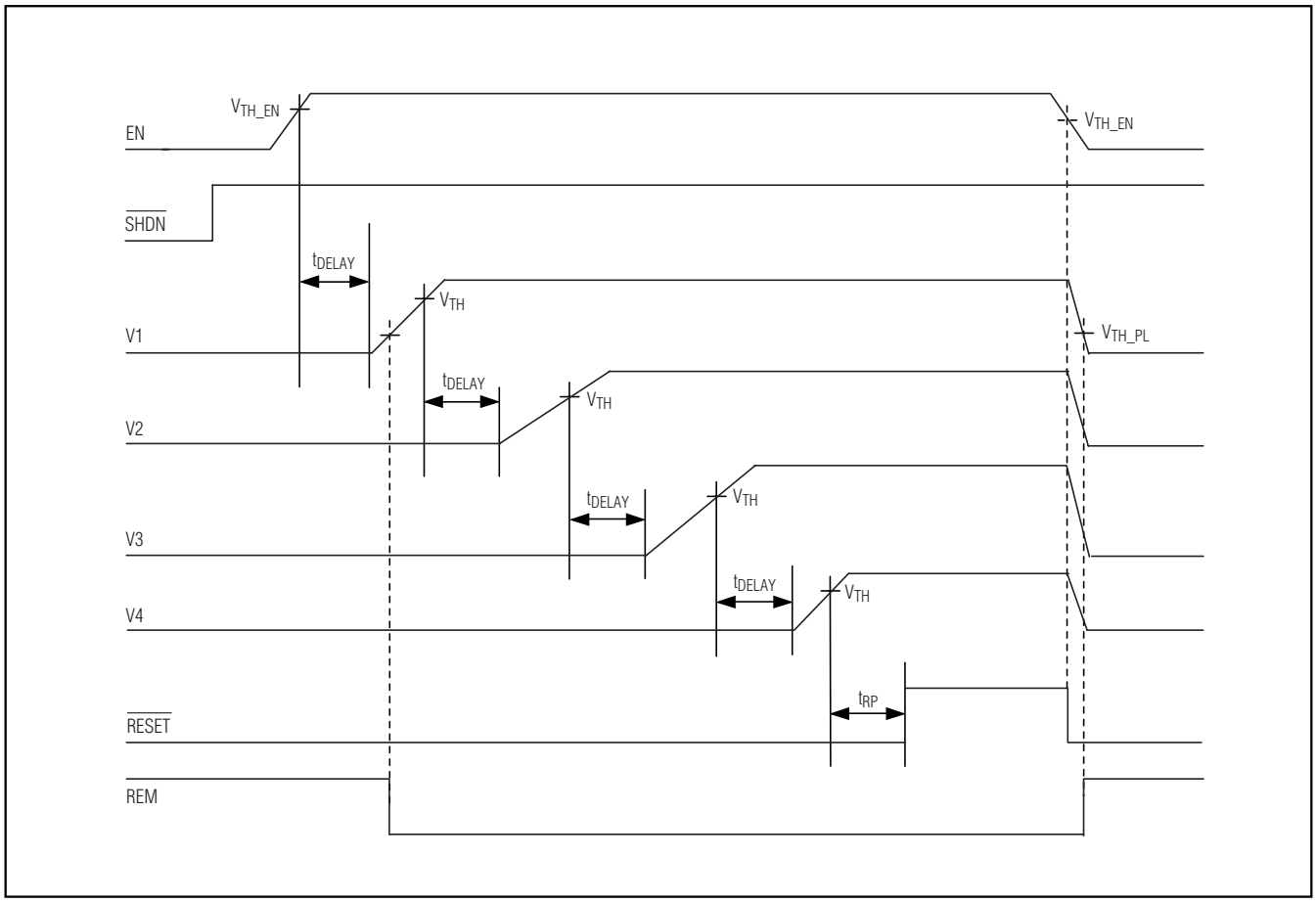


Figure 2. Sequencing Timing Diagram with Simultaneous Order Power-Down Using EN

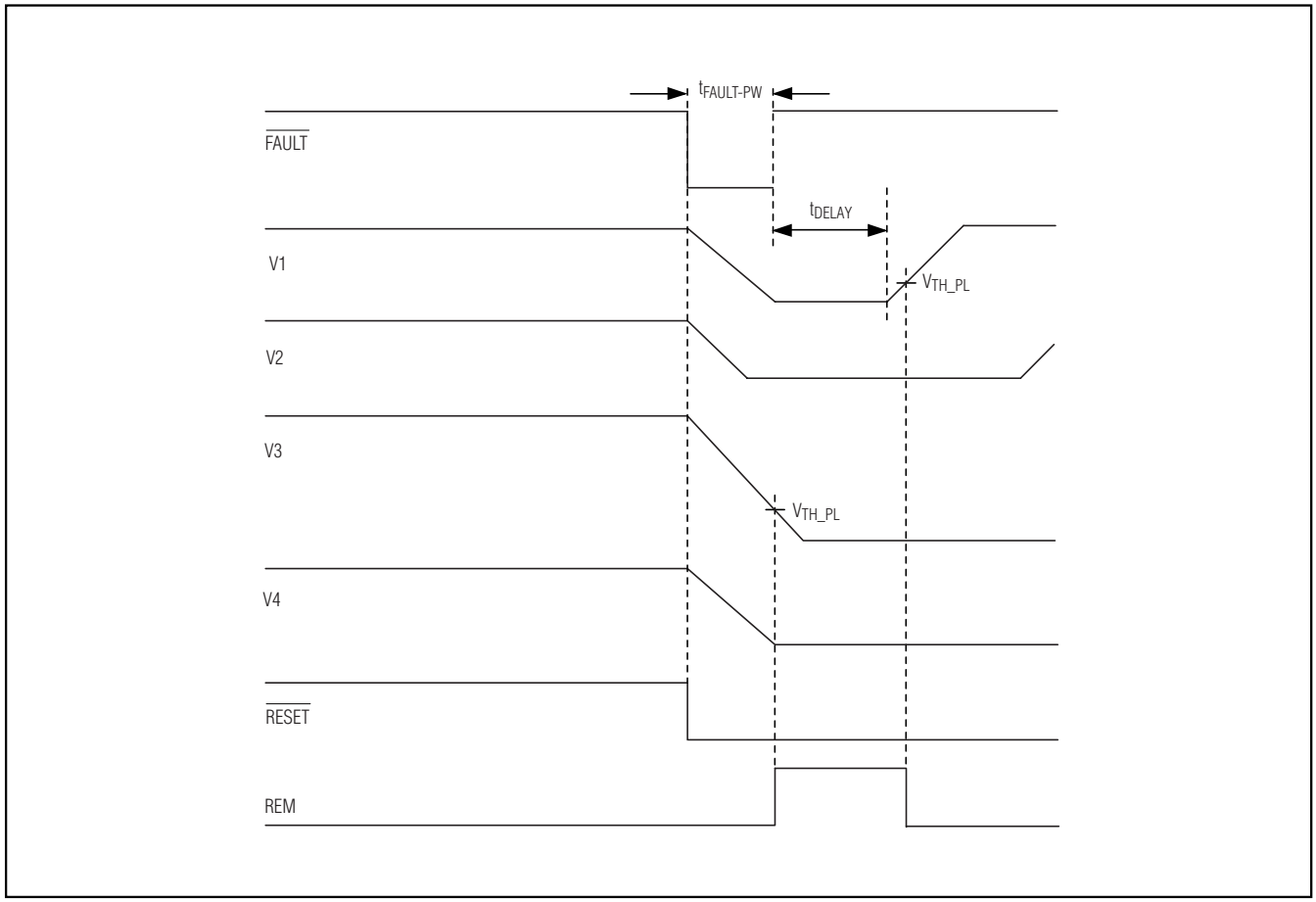


Figure 3. Sequencing Timing Diagram During a System Fault

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

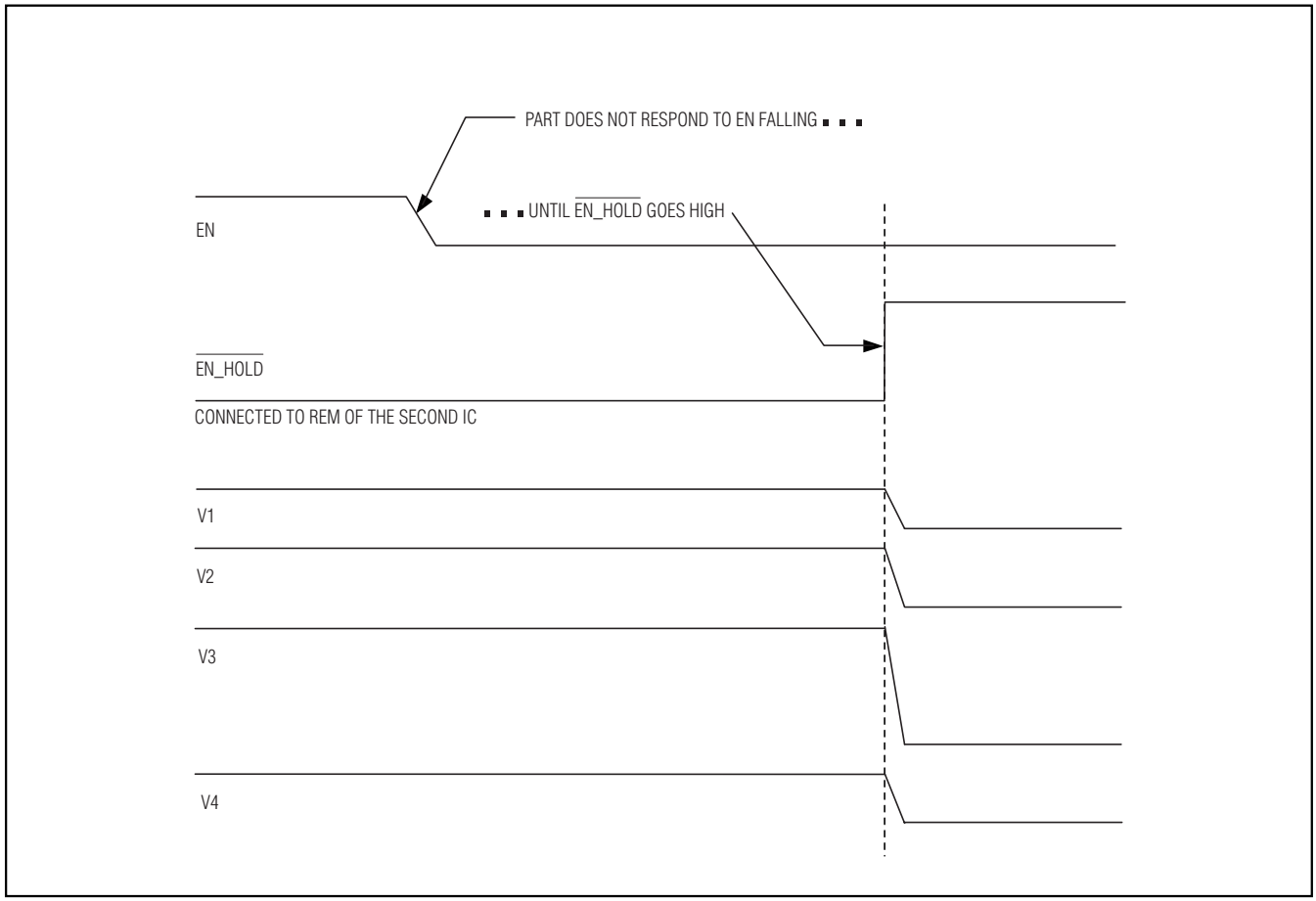


Figure 4. Power-Down Characteristics when REM of the Second IC is Connected to $\overline{\text{EN\_HOLD}}$ *of the First IC*

Detailed Description

The MAX16050 monitors up to 5 voltages (Figure 5) with the ability to sequence up to 4 voltages, while the MAX16051 monitors up to 6 voltages with the ability to sequence up to 5 voltages. These devices control system power-up and power-down in a particular sequence order. The MAX16050/MAX16051 turn off all supplies and assert a reset to the processor when any of the voltages falls below its respective threshold. The MAX16050/MAX16051 offer an 85mA pulldown feature that helps discharge the output capacitance of DC-DC converters to ensure timely power-down. In addition, the MAX16050/MAX16051 also reverse sequence, monitoring each power-supply output voltage present at the associated DISC_ input and ensuring that the voltage falls below 250mV before turning off the next supply.

The MAX16050 provides three sequence logic inputs, which select the sequence order from 24 possible combinations (Table 1). In the default mode (SEQ1 = SEQ2 = SEQ3 = High Impedance), the power-up sequence is OUT1→OUT2→OUT3→OUT4. The MAX16051 features an additional channel and the sequence order is fixed at OUT1→OUT2→OUT3→OUT4→OUT5. For complex systems with a large number of power supplies, the MAX16050/MAX16051 can be used in a daisy-chain configuration. Reverse sequencing in the daisy-chained configuration is still possible.

The MAX16050/MAX16051 keep all OUT_ low (all of the supplies in the off-state) until four conditions are met.

1) The voltage at ABP exceeds the undervoltage lockout threshold.
2) The voltage at the analog enable input (EN) is above its threshold.
3) The shutdown input, $\overline{SHDN}$, is not asserted.
4) All DISC_ voltages must be below 250mV.

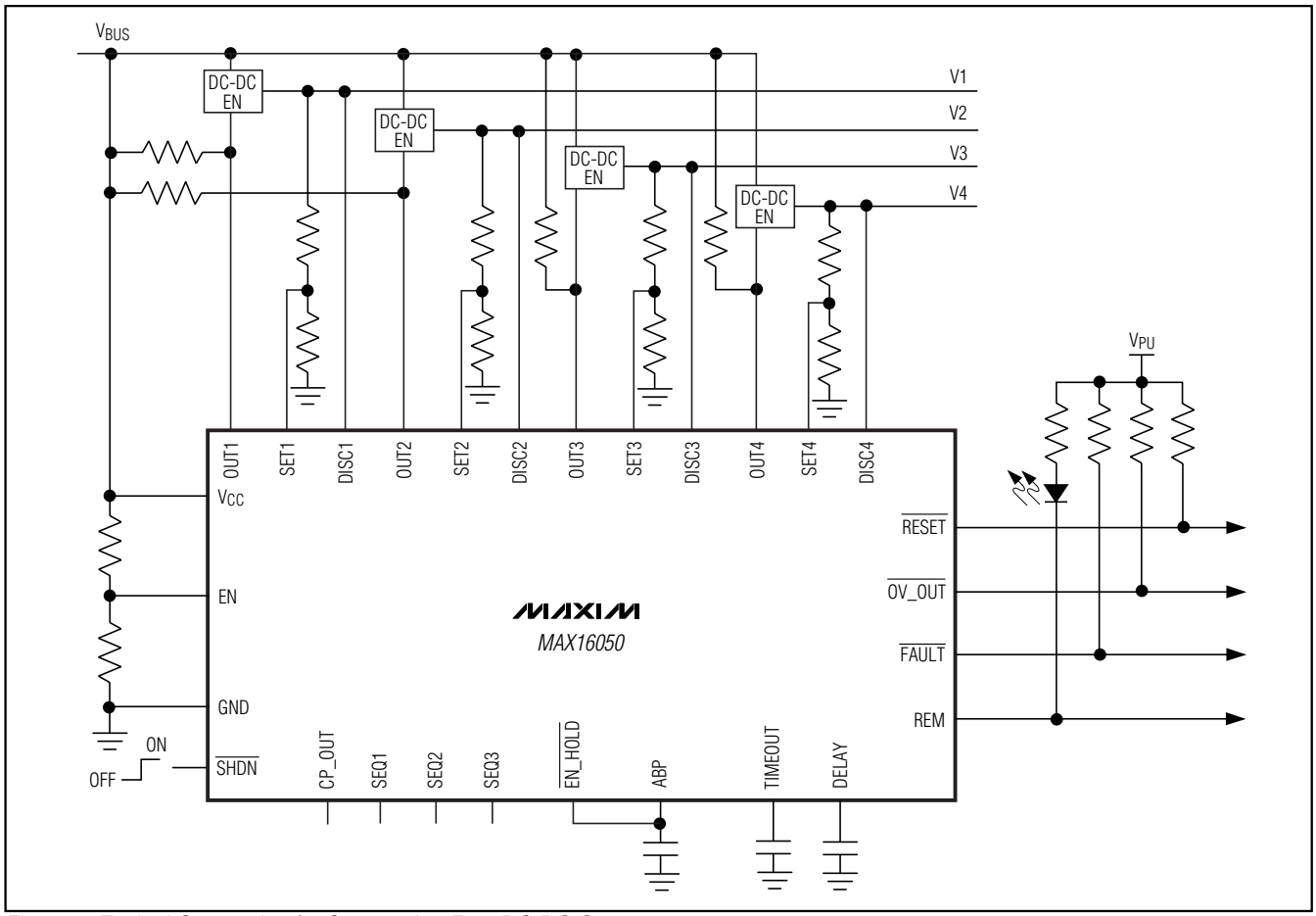


Figure 5. Typical Connection for Sequencing Four DC-DC Converters

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

When all of these conditions are met, the device starts the power-sequencing process by turning on OUT1–OUT_ in the sequence order. The sequence delay between each OUT_ is the time required for the power-supply voltage to exceed the undervoltage threshold plus the additional time delay set by the external delay capacitor; if no capacitor is connected to the sequence delay timing input (DELAY), only a short propagation delay (10µs) occurs. As each voltage meets its respective threshold, the next OUT_ in the sequence goes high impedance (open-drain output), allowing the next power supply to turn on, which is then monitored by the next input stage. When all of the voltages exceed their respective thresholds, the reset output ($\overline{RESET}$) deasserts after a reset timeout period to allow the system controller to start operating.

After sequencing is complete, if any SET_ input drops below its threshold, a fault is detected. All power supplies are simultaneously turned off by the OUT_ outputs asserting low, the $\overline{RESET}$ output asserting, the DISC_ current pulldown turning on, and the $\overline{FAULT}$ output pulling low for at least 1.9µs. The MAX16050/MAX16051 will then be ready to power on again. Sequencing begins as soon as the four startup conditions are met.

Sequencing

The MAX16050 features three three-state sequence logic inputs that select one of the 24 possible sequence orders (Table 1). These inputs allow the sequence order to be changed even after the board layout is finalized. The MAX16051 offers five channels and the device powers up in a fixed order from OUT1 to OUT5.

Table 1. MAX16050 Sequencing Table Logic

SEQ1	SEQ2	SEQ3	SEQUENCE ORDER			
			FIRST SUPPLY	SECOND SUPPLY	THIRD SUPPY	FOURTH SUPPLY
High-Z	High-Z	High-Z	OUT1	OUT2	OUT3	OUT4
High-Z	High-Z	Low	OUT1	OUT2	OUT4	OUT3
High-Z	High-Z	High	OUT1	OUT3	OUT2	OUT4
High-Z	Low	High-Z	OUT1	OUT3	OUT4	OUT2
High-Z	Low	Low	OUT1	OUT4	OUT2	OUT3
High-Z	Low	High	OUT1	OUT4	OUT3	OUT2
High-Z	High	High-Z	OUT2	OUT1	OUT3	OUT4
High-Z	High	Low	OUT2	OUT1	OUT4	OUT3
High-Z	High	High	OUT2	OUT3	OUT1	OUT4
Low	High-Z	High-Z	OUT2	OUT3	OUT4	OUT1
Low	High-Z	Low	OUT2	OUT4	OUT1	OUT3
Low	High-Z	High	OUT2	OUT4	OUT3	OUT1
Low	Low	High-Z	OUT3	OUT1	OUT2	OUT4
Low	Low	Low	OUT3	OUT1	OUT4	OUT2
Low	Low	High	OUT3	OUT2	OUT1	OUT4
Low	High	High-Z	OUT3	OUT2	OUT4	OUT1
Low	High	Low	OUT3	OUT4	OUT1	OUT2
Low	High	High	OUT3	OUT4	OUT2	OUT1
High	High-Z	High-Z	OUT4	OUT1	OUT2	OUT3
High	High-Z	Low	OUT4	OUT1	OUT3	OUT2
High	High-Z	High	OUT4	OUT2	OUT1	OUT3
High	Low	High-Z	OUT4	OUT2	OUT3	OUT1
High	Low	Low	OUT4	OUT3	OUT1	OUT2
High	Low	High	OUT4	OUT3	OUT2	OUT1

Charge-Pump Output (CP_OUT)

The MAX16050/MAX16051 feature an on-chip charge pump that drives its output voltage to 5V above V_{CC}, and it can be used as a pullup voltage to drive one or more external n-channel MOSFETs (see the *Typical Operating Circuit*). The charge-pump output can be modeled as a 25µA current source with a compliance voltage of (V_{CC} + 5V); the slew rate can be controlled by connecting a capacitor from the gate of the MOSFET to ground. When using CP_OUT to provide the pullup voltage for multiple MOSFETs, ensure that the voltage is enough to enhance a MOSFET despite the load of the other pullup resistors (which may be connected to outputs that are deasserted low).

Disabling Channels

If any channel is not used, connect the associated SET_ input to another SET_ input that is previous to the disabled channel in the sequence order. Connect DISC_ of the disabled channel to GND or leave it unconnected. The channel exclusion feature adds more flexibility to the device in a variety of different applications.

$\overline{SHDN}$ and EN Inputs

The shutdown input ($\overline{SHDN}$) initiates a reverse sequencing event. When $\overline{SHDN}$ is brought low, the device will sequentially power down in reverse order. During this period, all DISC_ inputs are monitored to make sure the voltage of each supply falls below 250mV before allowing the next supply to shut down. The next OUT_ goes low as soon as the previous DISC_ input drops below 250mV without any capacitor-adjusted delay. This continues until all supplies are turned off. $\overline{SHDN}$ is internally pulled up to ABP.

When EN falls below its threshold, the device performs a simultaneous power-down and does not reverse sequence. When either $\overline{SHDN}$ or EN initializes the power-down event, the reset output ($\overline{RESET}$) immediately asserts. At the end of the power-down event, when all DISC_ voltages are below 250mV, the bus removal output (REM) goes high impedance.

Reset Output ($\overline{RESET}$)

The MAX16050/MAX16051 include a reset output. $\overline{RESET}$ is an open-drain output and requires an external pullup resistor.

When any of the monitored voltages falls below its threshold, $\overline{SHDN}$ is pulled low, EN falls below its threshold, or $\overline{FAULT}$ is pulled low, $\overline{RESET}$ asserts and stays asserted for at least the minimum reset timeout period after all of these conditions are removed. Connect a capacitor from TIMEOUT to GND to adjust the reset timeout period. Connect TIMEOUT to ABP for the fixed timeout of 128ms (typ). Leave TIMEOUT unconnected for a 10µs (typ) timeout period.

$\overline{FAULT}$ Input/Output

The $\overline{FAULT}$ input/output asserts to signal a fault if any of the SET_ monitored voltages falls below its threshold while EN = $\overline{SHDN}$ = high. $\overline{FAULT}$ is internally pulled up to ABP by a 100kΩ resistor. $\overline{FAULT}$ also can be used as an input. Pull $\overline{FAULT}$ low to simultaneously shut down the OUT_ outputs .

For multichip solutions, all of the $\overline{FAULT}$ input/outputs can be connected together. In case of a fault condition, all outputs on every device are turned off and the internal pulldown circuitry is activated simultaneously.

Overvoltage Fault Output ($\overline{OV\_OUT}$)

The MAX16050/MAX16051 include an overvoltage fault output. $\overline{OV\_OUT}$ is an open-drain output and requires an external pullup resistor. When any of the SET_ voltages exceed their 0.55V overvoltage threshold, $\overline{OV\_OUT}$ goes low. When all of the SET_ voltages are below their overvoltage threshold, $\overline{OV\_OUT}$ goes high impedance after a short propagation delay.

Discharge Inputs (DISC_)

The discharge inputs (DISC_) discharge power-supply capacitors during a power-down or fault event and monitor power-supply output voltages during reverse sequencing. When an OUT_ output goes low, the associated DISC_ activates an 85mA pulldown current to discharge any output capacitors. This helps the power-supply output drop below the 250mV level so the next power supply can be turned off. During normal operation, DISC_ is high impedance and will not load the circuit.

Bus Removal Output (REM)

The MAX16050/MAX16051 include an open-drain bus removal output (REM) that indicates when it is safe to disconnect the input power after a controlled power-down operation. REM monitors DISC_ voltages and goes low when any DISC_ input voltage goes above the DISC_ power low threshold (V_{TH_PL}). REM goes high when all DISC_ inputs are below the DISC_ power low threshold (V_{TH_PL}). For a visual signal of when it is unsafe to remove a powered board from the bus, connect an LED to REM.

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

Enable Hold Input ($\overline{EN\_HOLD}$)

When $\overline{EN\_HOLD}$ is low, a high-to-low transition on $\overline{SHDN}$ or on EN is ignored. $\overline{EN\_HOLD}$ must be high for $\overline{SHDN}$ or EN to disable the device. This feature is used when multiple MAX16050/MAX16051s are daisy-chained (see Figure 7). Connect $\overline{EN\_HOLD}$ to ABP if not used.

Delay Time Input (DELAY)

Connect a capacitor (C_{DELAY}) between DELAY and GND to adjust the sequencing delay period (t_{DELAY}) that occurs between sequenced channels. Use the following formula to estimate the delay:

$$t_{DELAY} = 10\mu s + (500k\Omega \times C_{DELAY})$$

where t_{DELAY} is in seconds and C_{DELAY} is in Farads. Leave DELAY unconnected for the default 10µs (typ) delay.

Reset Timeout Input (TIMEOUT)

Connect a capacitor ($C_{TIMEOUT}$) from TIMEOUT to GND to set the reset timeout period. After all SET_ inputs exceed their thresholds (V_{TH}), $\overline{RESET}$ remains low for the programmed timeout period, t_{RP}, before deasserting (see Figure 1). Use the following formula to estimate the reset timeout period:

$$t_{RP} = 10\mu s + (500k\Omega \times C_{TIMEOUT})$$

where t_{RP} is in seconds and $C_{TIMEOUT}$ is in Farads. Leave TIMEOUT unconnected for the default 10µs (typ) timeout delay or connect TIMEOUT to ABP to enable a fixed 128ms (typ) timeout.

Applications Information

Resistor Value Selection

The MAX16050/MAX16051 feature four and five SET_ inputs, respectively, and the threshold voltage (V_{TH}) at each SET_ input is 0.5V (typ). To monitor a voltage V_{1TH}, connect a resistive divider network to the circuit as shown in Figure 6, and use the following equation to calculate the monitored threshold voltage:

$$V_{1TH} = V_{TH} \times \left(1 + \frac{R1}{R2}\right)$$

Balance accuracy and power dissipation when choosing the external resistors. The input to the voltage monitor is a high-impedance input with a small 100nA leakage current. This leakage current contributes to the overall error of the threshold voltage, and this error is proportional to the value of the resistors used to set the threshold. Small-valued resistors reduce the error but increase the power consumption. Use the following equation to estimate the value of the resistors based on the amount of acceptable error:

$$R_1 = \frac{e_A \times V_{1TH}}{I_{SET}}$$

where e_A is the fraction of the maximum acceptable absolute resistive divider error attributable to the input leakage current (use 0.01 for ±1%), V_{1TH} is the power-good threshold for the power supply being monitored, and I_{SET} is the worst-case SET_ input leakage current (see the *Electrical Characteristics* table). Calculate R2 as follows:

$$R_2 = \frac{V_{TH} \times R_1}{V_{1TH} - V_{TH}}$$

Pullup Resistor Values

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{CC} = 3.3V and the pullup voltage is 5V, keep the sink current less than 3.2mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 1.6kΩ. For a 13.2V pullup, the resistor should be larger than 4.1kΩ.

Extra care must be taken when using CP_OUT as the pullup voltage. If multiple pullup resistors are connected to CP_OUT and one or more of the connected OUT_ outputs are asserted, the current drawn can drop the CP_OUT voltage enough to prevent an enabled MOSFET from turning on completely.

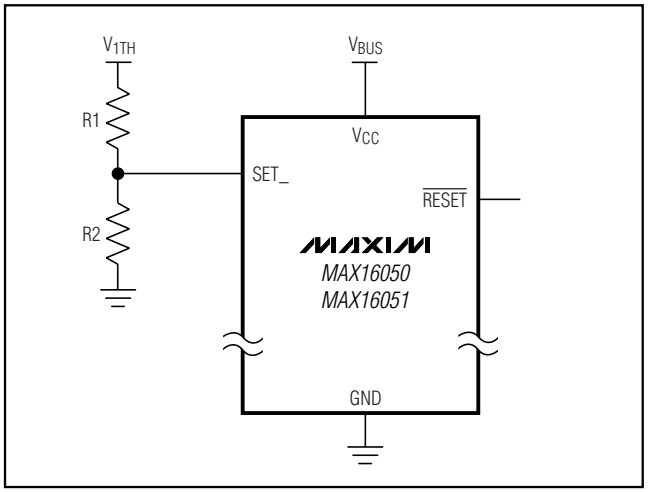


Figure 6. Setting the SET_ Input

Daisy-Chaining the MAX16050/MAX16051

The MAX16050/MAX16051 can be daisy-chained to sequence and monitor a large number of voltages (Figure 7). When a fault occurs on any of the monitored inputs, $\overline{FAULT}$ goes low, signaling a fast power-down. Connect all $\overline{FAULT}$ pins of the MAX16050/MAX16051 together to ensure that all power supplies are turned off during a fault.

In Figure 7, $\overline{SHDN}$ is pulled low to initiate the power-down sequence. When all of the supply voltages monitored by U2 are off, the bus removal output (REM) goes high, thereby allowing U1 to start sequencing down. REM normally is at a logic-low state when all voltages are good. Connect U2's REM to U1's $\overline{EN\_HOLD}$ to force U1 to stay on even if EN and $\overline{SHDN}$ are pulled low. This enable-and-hold circuitry allows the system to power down correctly.

MOSFET Selection

The external pass MOSFET connects in series with the sequenced power-supply source. Since the load current and the MOSFET drain-to-source impedance (R_{DSON}) determine the voltage drop, the on-characteristics of the MOSFET affect the load supply accuracy. For highest supply accuracy and lowest voltage drop, select a MOSFET with an appropriate drain-to-source on-resistance with a gate-to-source bias of 4.5V to 6.0V (see Table 2).

Layout and Bypassing

For better noise immunity, bypass V_{CC} to GND with a 0.1µF capacitor installed as close to the device as possible. Bypass ABP to GND with a 1µF capacitor installed as close to the device as possible; ABP is an internally generated voltage and must not be used to supply more than 1mA to external circuitry. Connect the exposed pad (EP) to the ground plane for improved heat dissipation. Do not use EP as the only ground connection for the device.

Table 2. Recommended MOSFETs

MANUFACTURER	PART	V_{DS} (V)	V_{GSth} (V)	R_{DSON} AT V_{GS} = 4.5V (mΩ)	I_{MAX} AT 50mV VOLTAGE DROP (A)	Qg (nC) (TYP)	FOOTPRINT
Fairchild	FDC633N	30	0.67	42	1.19	11	Super SOT™-6
	FDP8030L FDB8030L	30	1.5	4.5	11.11	120	TO-220 TO-263AB
	FDD6672A	30	1.2	9.5	5.26	33	TO-252
	FDS8876	30	2.5 (max)	17	2.94	15	SO-8
Vishay	Si7136DP	20	3	4.5	11.11	24.5	SO-8
	Si4872DY	30	1	10	5	27	SO-8
	SUD50N02-09P	20	3	17	2.94	10.5	TO-252
	Si1488DH	20	0.95	49	1.02	6	SOT-363 SC70-6
International Rectifier	IRL3716	20	3	4.8	10.4	53	TO220AB D^2PAK TO-262
	IRL3402	20	0.7	10	5	78 (max)	TO-220AB
	IRL3715Z	20	2.1	15.5	3.22	7	TO220AB D^2PAK TO-262
	IRLML2502	20	1.2	45	1.11	8	SOT23-3 Micro3™

Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

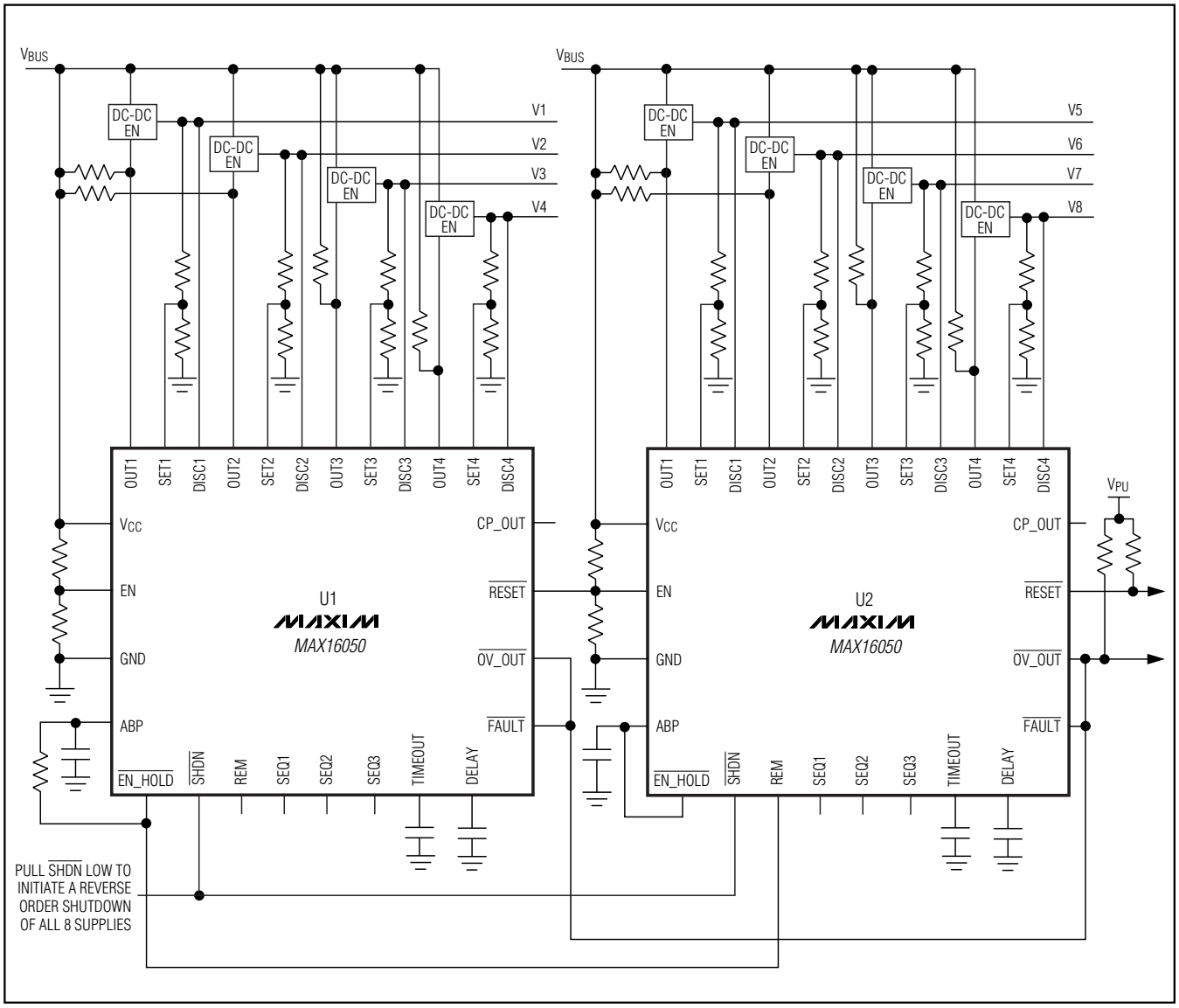
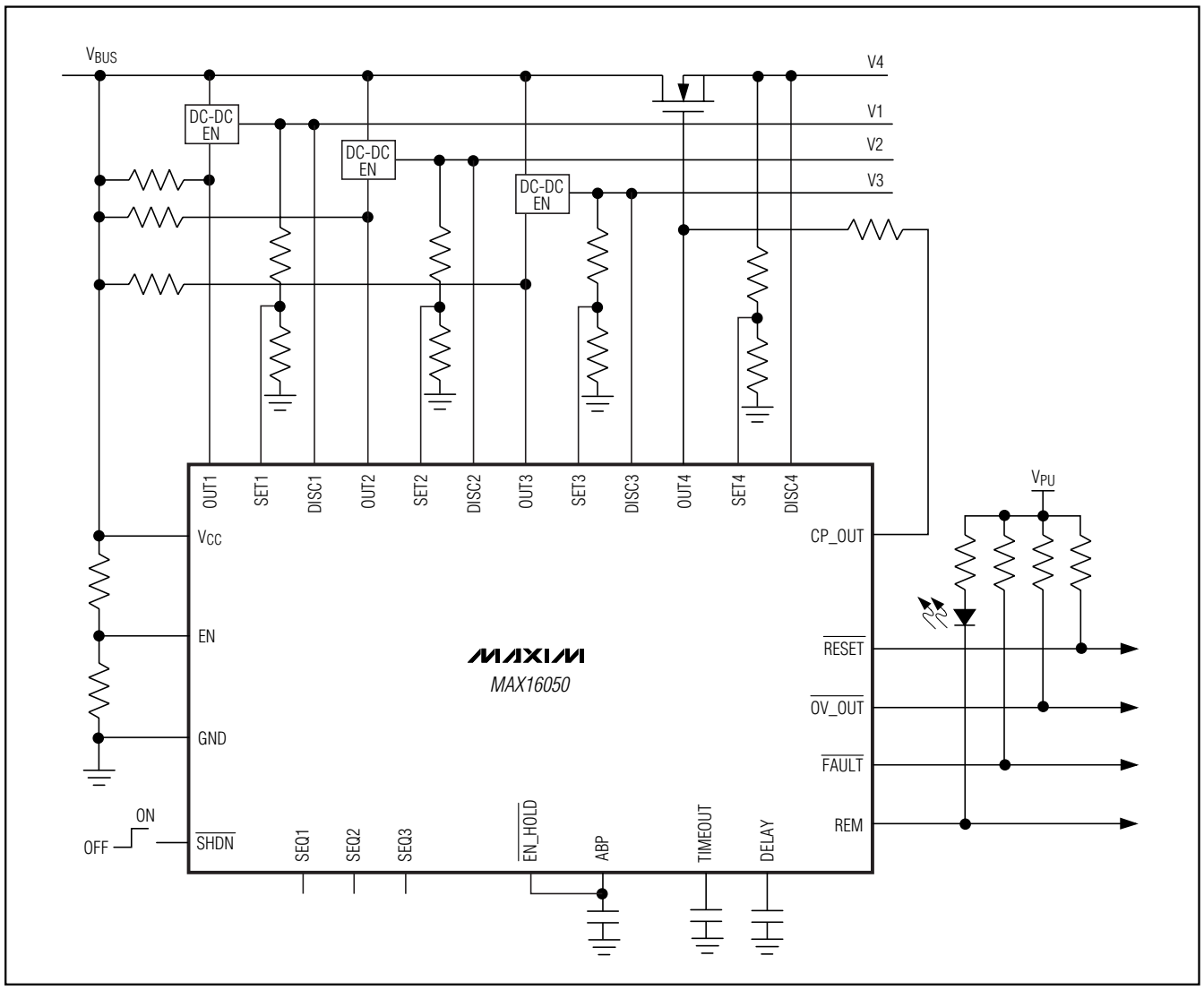


Figure 7. Daisy-Chaining Two Devices to Sequence Up to 8 Voltages

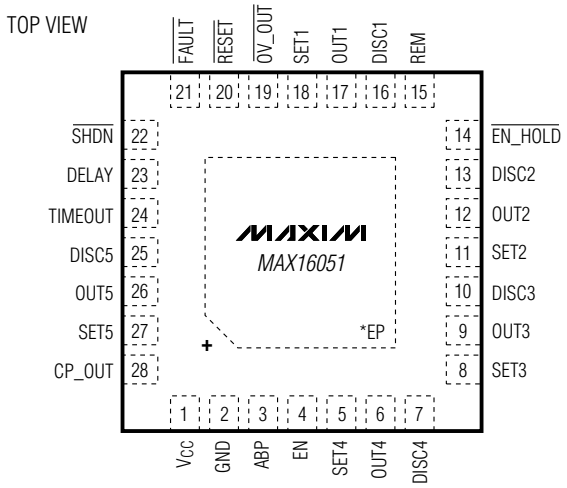
Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

Typical Operating Circuit



Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

Pin Configurations (continued)



THIN QFN (4mm x 4mm)

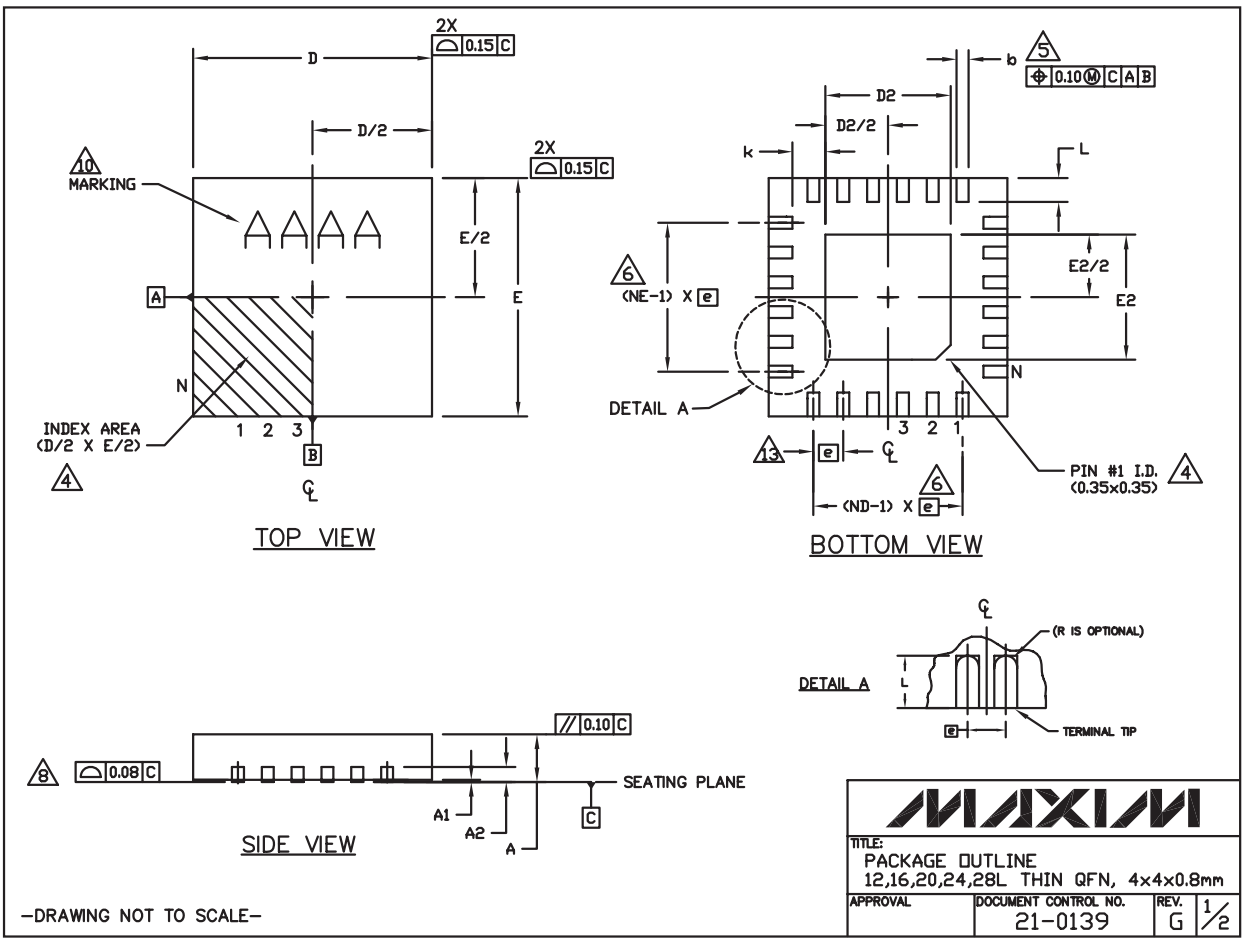
*EP = EXPOSED PAD

Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	G	2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.