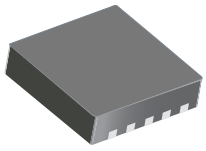
Dual Output Boost Regulator Using Single Inductor

Features and Benefits

- Two independently controlled channels for dual display
- Output voltage up to 23 V
- 2.7 to 9 V input
- Output disconnect allows less than 1 µA supply current during shutdown
- Single-pin dimming control for WLED
- 1.2 MHz switching frequency
- 1.5 A switch current limit
- OVP, Pulse-by-Pulse OCP, OTP, and Soft Start

Package: 10 pin MLP/DFN (suffix EJ) with exposed thermal pad



Approximate Scale 1:1

Description

The A8481 is a step-up dc-to-dc converter in a thermally-enhanced MLP package. A constant 1.2 MHz switching frequency, with current-mode control scheme, provides stable low-noise operation at high load conditions.

The A8481 is a dual output OLED + WLED driver. This device is suitable for driving OLED bias supply as well as WLEDs for backlight. For OLED it is capable of delivering 80 mA at 18 V, and can drive five WLEDs at 20 mA.

Independent output control and output disconnect make this IC ideally suited for battery operated, dual display portable applications. The IC disconnects input from the output path during shutdown, allowing shutdown currents less than 1 µA.

The A8481 is available in a 10-pin 3 mm × 3 mm MLP package that has a nominal height of only 0.75 mm.

Applications include:

- Dual-panel cellular phone with OLED and WLED backlight
- Personal Digital Assistant (PDA)
- Camcorder, personal stereo, MP3 player, camera

Typical Applications

Additional applications on page 11

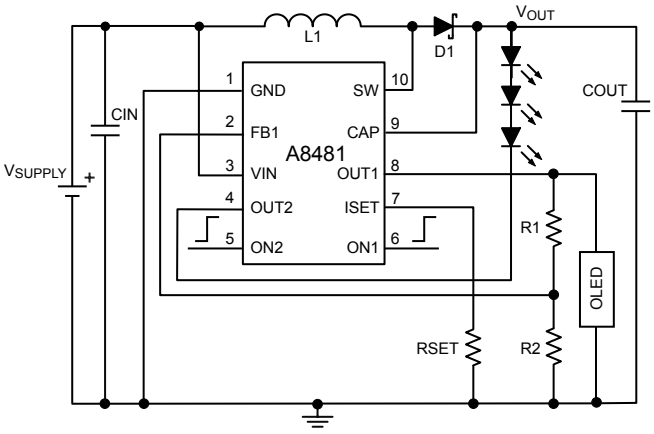


Figure 1a. Typical application circuit for A8481 driving OLED and three WLEDs

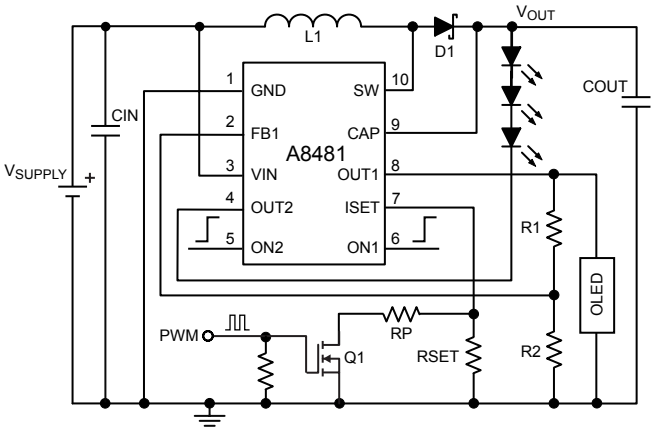
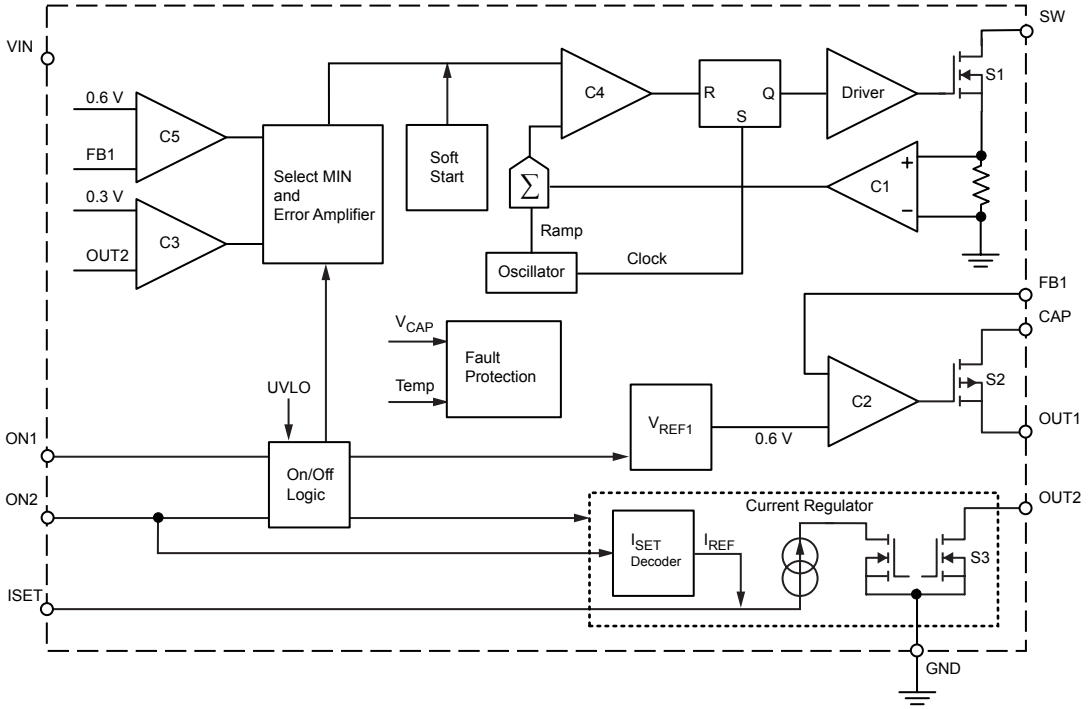


Figure 1b. OUT2 current dimming with PWM on ISET pin, with parallel resistor

Functional Block Diagram



Absolute Maximum Ratings

Input or Output Voltage
- SW, CAP, OUT1, OUT2 pins ..... **–0.3 to 26 V**
- VIN pin, V_{IN} ..... **–0.3 to 9.5 V**
- All other pins, V_x ..... **–0.3 to V_{IN} + 0.3 V (7 V max.)**

Operating Ambient Temperature, T_A ..... **–40°C to 85°C**

Maximum Junction Temperature, T_J(max) ..... **150°C**

Storage Temperature, T_S ..... **–55°C to 150°C**

Package Thermal Characteristics

$R_{\theta JA}$ = 45 °C/W, on a 4-layer board. Additional information is available on the Allegro Web site.

Pb

Ordering Information

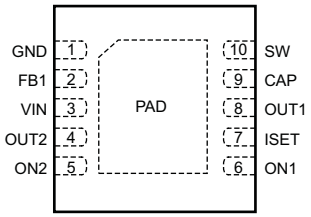
Use the following complete part numbers when ordering:

Part Number	Packing[a]	Description
A8481EEJTR-T[b]	7-in. reel, 1500 pieces/reel	EJ package, MLP/DFN(SON) leadless surface mount with exposed thermal pad

[a]Contact Allegro for additional packing options.

[b]Lead (Pb) free, with leadframe plating 100% matte tin.

Pin-out Diagram



(Top View)

Number	Name	Description
1	GND	Power ground and signal ground reference; connect directly to the ground plane.
2	FB1	This is the feedback pin for controlling voltage on the OUT1 pin. The nominal reference voltage on this pin is 600 mV. In order to minimize noise, connect the feedback resistor network close to this pin.
3	VIN	This is the power input supply connection to the circuit. A bypass capacitor tying this pin to GND must be connected close to this pin.
4	OUT2	This is the current sink pin for the WLED supply. The load current through this pin can be controlled through the ISET pin or the ON2 pin.
5	ON2	This is the enable pin for OUT2. This pin is also used for the serial input interface to control the OUT2 current.
6	ON1	This is the enable pin for OUT1.
7	ISET	This pin is used to set load current through the OUT2 pin.
8	OUT1	This is the voltage-controlled pin for the OLED drive. An internal switch disconnects the OLED during shutdown.
9	CAP	This is the connection to the output capacitor for the boost regulator output.
10	SW	This is the connection between the internal boost switch and the external inductor. Because rapid changes of current occur at this pin, the board traces connected to this pin should be minimized and the inductor and diode should be connected as close to this pin as possible.
–	Pad	Exposed thermal pad. Connect to GND plane for enhanced thermal performance.

Operation State Control Truth Table

Pin		State Description
ON1	ON2	
0	0	IC shutdown. Total input current from VIN is < 1 µA.
0	1	OUT2 on, OUT1 off. Boost stage is controlled to regulate OUT2 current with switch S2 off.
1	0	OUT1 on, OUT2 off. Boost stage is controlled to regulate OUT1 voltage and to turn switch S3 off.
1	1	OUT2 and OUT1 on. Boost stage is controlled such that voltage on the CAP pin is sufficient to bias OUT1 and OUT2.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, VIN = ON1 = ON2 = 3.0 V, R_{SET} = 30 kΩ (unless noted otherwise)

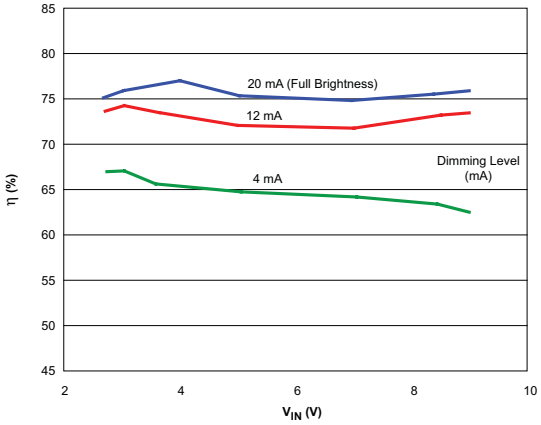
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		2.7	–	9	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	2.25	2.45	2.60	V
Feedback Reference Voltage	V_{FB}		584	610	636	mV
Feedback Voltage Line Regulation		2.7 V ≤ V_{IN} ≤ 9 V	–	0.1	–	%/V
Feedback Input Current	I_{FB}		–	45	100	nA
Switch Current Limit	I_{SWLim}		–	1.5	–	A
Switch Frequency	f_{SW}		1	1.2	1.4	MHz
Switch Maximum Duty Cycle*	DC		85	90	–	%
Switch S1 On Resistance	$R_{DS1(on)}$	I_{SW} = 0.5 A	–	225	–	mΩ
Switch Leakage Current	I_{LSW}	V_{SW} = 5 V	–	–	1	µA
Quiescent Input Current	$I_{IN(Q)}$	ON1 = ON2 = 0 V	–	–	1	µA
ON1, ON2 Logic Input Levels						
Input Threshold Low	V_{IL}		–	–	0.4	V
Input Threshold High	V_{IH}		1.5	–	–	V
Input Leakage	I_L		–	65	–	µA
Overvoltage Protection						
Output Overvoltage Rising Limit	V_{OVPR}		–	24.5	25.5	V
I_{SET} to I_{OUT2} Current Gain	A_{SET}	I_{SET} = 10 µA	890	1000	1110	A/A
ISET Pin Voltage	V_{SET}		–	0.6	–	V
ISET Current Range	I_{SET}		1	–	20	µA
ON2 Serial Pulse Timing						
ON2 Pulse Low Time	t_{LO}		0.5	–	20	µs
ON2 Pulse High Time	t_{HI}		0.5	–	–	µs
Initial ON2 Pulse High Time	t_{HII}	First ON2 pulse after shutdown	1	–	–	ms
Shut Down Delay	t_{SHDN}	Falling edge on ON2	–	1	2	ms
Thermal Shutdown Threshold	T_{SHDN}		–	160	–	(°)
Thermal Shutdown Hysteresis	$T_{SHDNhys}$		–	10	–	(°)
Soft-Start Period	t_{SS}	V_{OUT} = 10 V	–	2	–	ms

*Guaranteed by design.

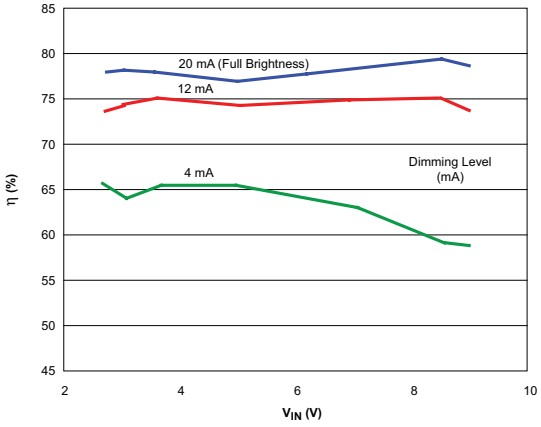
Performance Characteristics

Tests performed using application circuit shown in figure 1(a)
L1 = 4.7 µH, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, V_{IN} = 3 V (unless otherwise noted)

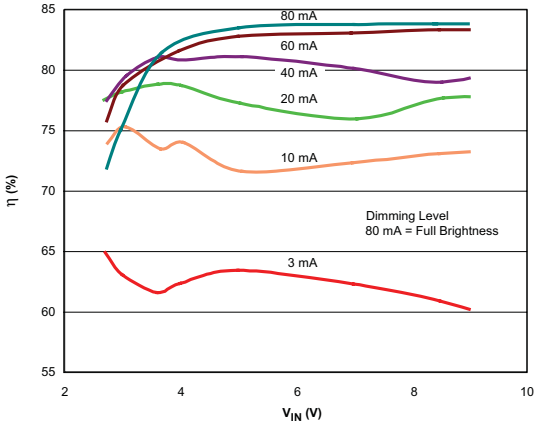
Efficiency with OUT1 off, OUT2 on, 5 WLEDs
Over range of dimming levels, LED voltage drop at 20 mA = 16.3 V



Efficiency with OUT2 on, OUT1 off, 3 WLEDs
Over range of dimming levels, LED voltage drop at 20 mA = 9 V



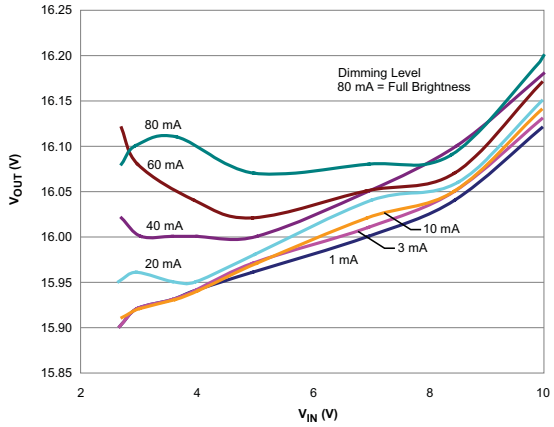
Efficiency with OUT1 on, OUT2 off
V_{OUT1} = 16 V



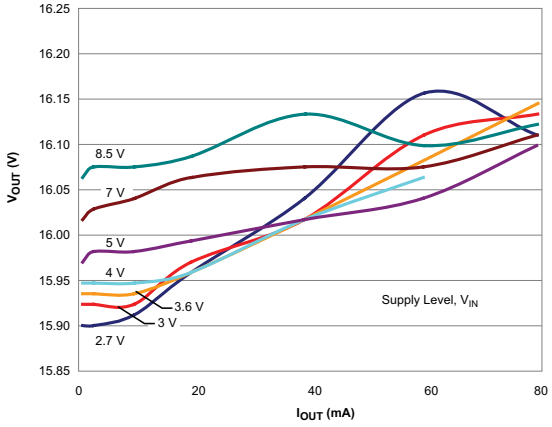
Performance Characteristics

Tests performed using application circuit shown in figure 1(a)
L1 = 4.7 µH, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, V_{IN} = 3 V (unless otherwise noted)

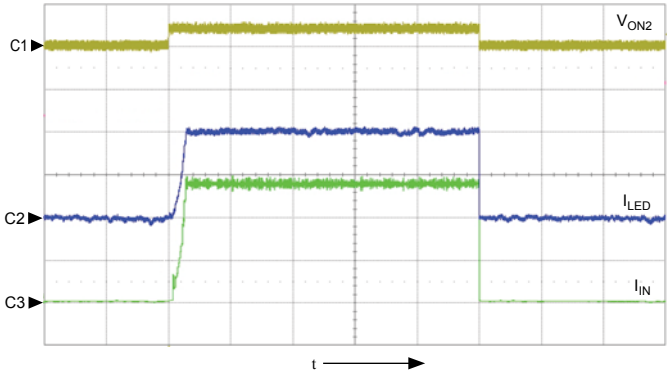
OLED Line Regulation
V_{OUT1} = 16 V



OLED Load Regulation
V_{OUT1} = 16 V

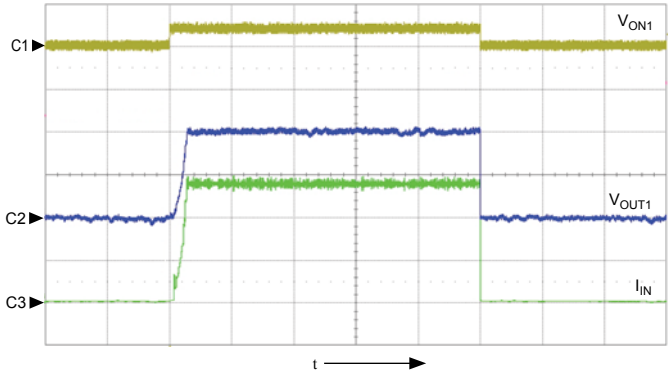


WLED Startup, 5 LEDs, 20 mA



Symbol	Parameter	Units/Division
C1	V_{ON2}	5 V
C2	I_{LED}	10.0 mA
C3	I_{IN}	50 mA
t	time	5 ms

OLED Startup, 18 V, 80 mA



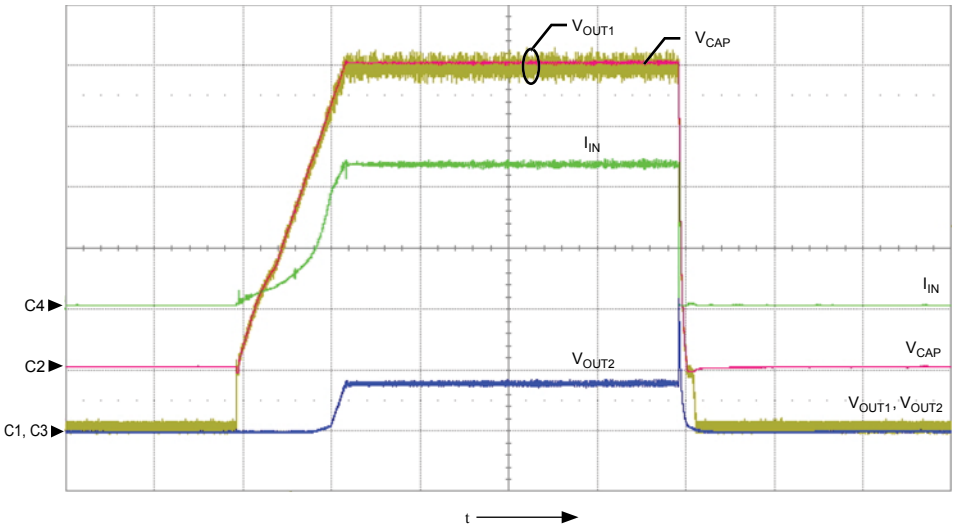
Symbol	Parameter	Units/Division
C1	V_{ON1}	5 V
C2	V_{OUT1}	5 V
C3	I_{IN}	500 mA
t	time	5 ms

Performance Characteristics

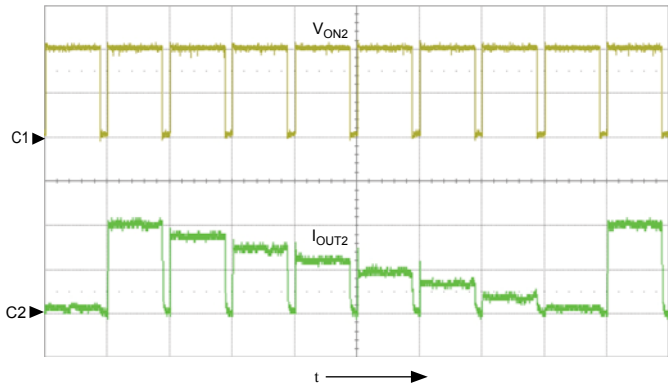
Tests performed using application circuit shown in figure 1(a)
L1 = 4.7 µH, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, V_{IN} = 3 V (unless otherwise noted)

OLED (18 V, 80 mA) and WLED (5 LEDs, 20 mA)
Simultaneous startup and shutdown

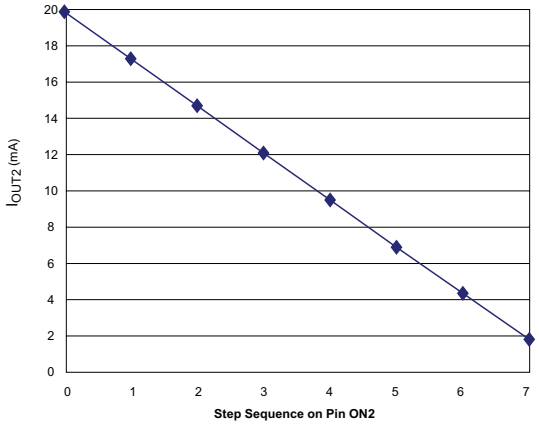
Symbol	Parameter	Units/Division
C1	V_{OUT1}	3 V
C2	V_{CAP}	3 V
C3	V_{OUT2}	3 V
C4	I_{IN}	200 mA
t	time	5 ms



Serial Dimming Using ON2



Symbol	Parameter	Units/Division
C1	V_{ON2}	1 V
C2	I_{OUT2}	10 mA
t	time	5 ms



Functional Description

The A8481 is a dual output converter with two-stage architecture. The first stage is a boost stage, which boosts input battery voltage to a sufficient level to drive an OLED or a set of series-connected WLEDs. This stage uses 1.2 MHz constant frequency, current mode control. Typical application circuits are shown in figures 1 and 4.

The constant voltage drive for OLED is provided through the OUT1 pin. The internal switch S2, connected between the CAP and OUT1 pins, acts as either a switch or as a linear regulator when OUT1 is on. Switch S2 disconnects the OLED when OUT1 is disabled.

For driving OLEDs, output voltage is sensed by the FB1 pin through a voltage divider network. Output voltage (V) is set as:

$$V_{OUT1} = 0.6 \times \frac{R_1 + R_2}{R_2} \quad (1)$$

The OUT2 pin provides a constant-current sink for a set of series-connected WLEDs. It is capable of sinking 20 mA current. Switch S3 is the current regulator. Current through S3 can be adjusted by controlling resistor connected to the ISET pin. It can also be programmed through the ON2 pin.

The IC provides protections against output overvoltage on the CAP pin, overload, and over temperature. Also, it has an input undervoltage lockout to avoid malfunction and battery drain.

At light loads, instantaneous inductor current drops to zero. This is known as discontinuous mode operation and will result in some low frequency ripple. In discontinuous mode, the voltage at the SW pin will ring, due to the resonant LC circuit formed by the inductor and the switch and diode capacitance. This ringing is low frequency and is not harmful. It can be damped with a resistor across the inductor, but this will reduce efficiency and is not recommended.

Start-up Sequence

When either or both outputs, OUT1 and OUT2, are enabled and V_{IN} is greater than V_{IN}(min), the boost stage is ramped-up with soft start. If only OUT1 is enabled, it controls the boost stage soft start. OUT2 controls soft start if only OUT2 is enabled.

When only one output is enabled, the corresponding output switch, S2 or S3, completely turns on. If ON1 and ON2 are both enabled at start-up, the boost stage is controlled by the channel that requires greater voltage than the other channel. Both outputs turn on simultaneously. When both enable signals are low, the A8481 enters shutdown mode.

During normal operation, if both outputs are enabled and one output is out of regulation, that output will control the boost loop. The corresponding output switch will completely turn on and the other output switch will linearly regulate. For example:

- Case A. If the current through the OUT2 pin falls below 95% of the set value (I_{SET} multiplied by internal gain), the boost stage will be controlled by OUT2, such that current through OUT2 is same as the set value. OUT1 will be regulated through S2 working as an LDO linear regulator.
- Case B. If the voltage across the FB pin falls below 95% of the set value, the boost stage will be controlled by OUT1. The current through OUT2 will be controlled through S3 working as current sink.

WLED Dimming Control

In the A8481, WLED brightness can be controlled by the following variety of methods:

- External resistance on the ISET pin

Dimming level can be set by controlling the resistance between the ISET pin and ground. The resistance between the ISET pin and ground can be dynamically controlled by switching a parallel resistor, R_P, as shown in figure 1b.

- Serial programming through the ON2 pin

The OUT2 pin current can be adjusted by clocking the ON2 pin to 8 different levels, ranging from 8% to 100% of the level determined by R_{SET}. An internal digital circuit decodes the clock signal and sets the current of the OUT2 pin. Figure 2 illustrates the timing definition of the clock at the ON2 pin. The 8 levels of serial dimming are shown in the following table.

Pulse Count	I_{OUT2}	Pulse Count	I_{OUT2}
0	100%	4	47%
1	87%	5	34%
2	74%	6	21%
3	61%	7	8%
		8	100%

The default setting is 100%, which is the OUT2 level when no clock pulse has been applied. The OUT2 current level is decreased in steps as each pulse is applied. After the minimum level is reached, the counter rolls over to 100% again.

Dimming with serial programming is disabled during startup, for the initialization period, t_{HII}. When ON2 is pulled low for time longer than t_{SHDN}, the counter resets.

When changing from one specific dimming level to another, the user may not want to have to store the latest dimming level. A simpler method is to program a memory reset and apply the required number of pulses, from 100% to the target dimming level. The total "LED off" time during shutdown, reenable, and dimming level programming can be kept sufficiently short, such that no delay is discernable to the human eye.

- PWM Control through the ON2 pin

The average current for the LEDs can be determined by controlling the duty cycle of the LED current using external PWM on ON2 pin. When the ON2 pin is high, current at the 100% level flows through the LEDs. When ON2 is low, the LED current is less than 1 µA.

PWM can be applied only after the t_{HII} period. The duty cycle and frequency range will be limited due to t_{SHDN}. Typically, PWM control through the range of 0 to 80% can be achieved at 100 Hz PWM frequency.

- PWM Control through the ISET pin

The average current for the LEDs can be controlled with external PWM on the ISET pin, as shown in figure 4a.

PWM dimming accuracy is shown in figure 3. The PWM source used had a high level of 3 V and low level of 0 V. Also, R_{SET}=30 kΩ and R_P=100 Ω.

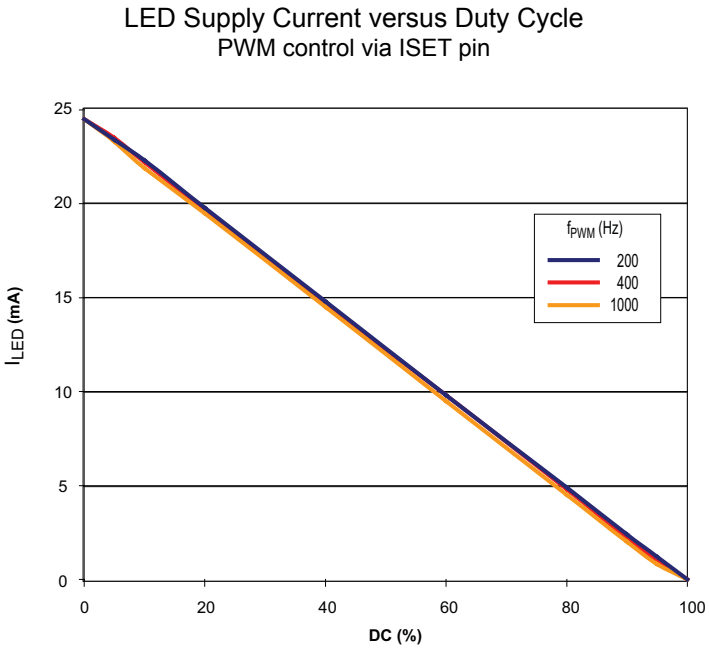


Figure 3. Accuracy of External PWM on ISET

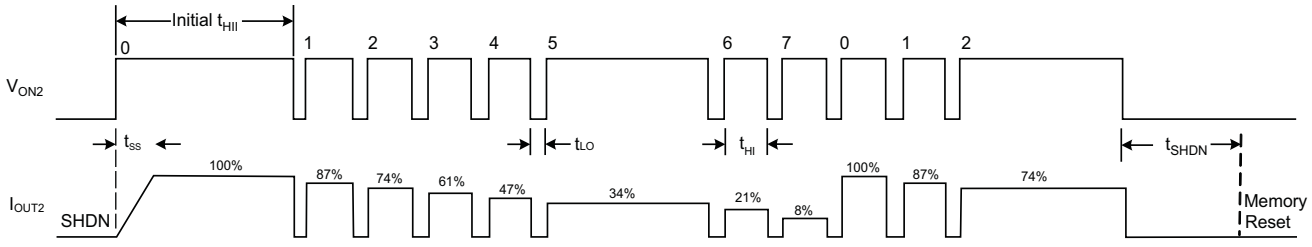


Figure 2. ON2 Clock Timing Definition

Applications Information

Component Selection

The component values shown in the application circuits (figures 1 and 4) will be sufficient for most applications. To reduce the output ripple, the output inductor may be increased in value, but in most cases this will result in excessive board area and cost.

Inductor Selection

The inductor is the most important component in the power supply design because it affects the steady-state performance, transient response, and loop stability. The inductance value, dc resistance, and the saturation current should be considered when choosing the inductor. The dc current of the inductor can be calculated by:

$$I_{L\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (2)$$

and the inductance value can be calculated by:

$$L_{min} = \frac{V_{imin}}{\Delta_i \times \eta} \times \left(1 - \frac{V_{imin}}{V_{OUT}}\right) \times \frac{1}{f} \quad (3)$$

where Δi = (20% to 40%) × I_{L_DC} is the peak-to-peak ripple current.

Smaller inductance values force the converter into discontinuous mode, which will reduce the maximum output current. Larger inductance values reduce the gain and phase margin, which will result in instability of the loop.

The inductor should have low winding resistance, typically < 0.2 Ω and low 1.2 MHz core loss for better efficiency.

The inductor should have a saturation current higher than 1.5 A, in order to provide 20 V at the OUTx pins, and 100 mA at 2.7 V_{IN}. For high temperature operation, a suitable derating factor should be considered. Several inductor manufacturers, including: Coilcraft, Murata, Panasonic, Sumida, Taiyo Yuden, and TDK, have and are developing suitable small-size inductors.

Diode Selection

The diode should have a low forward voltage to reduce conduction losses and a low capacitance to reduce switching losses. Schottky diodes can provide both of these features, if carefully selected. The forward voltage drop is a natural advantage for Schottky diodes and decreases as the current rating increases. However, as the current rating increases, the diode capacitance also increases, so the optimum selection is usually the lowest current rating above the circuit maximum.

The diode RMS current rating should be:

$$I_{DIODE(RMS)} = I_{OUT} = I_{IN}\sqrt{1-D} \quad . \quad (4)$$

Diode PIV should be higher than the output voltage on the CAP pin.

Capacitor Selection

The input capacitor selection is based on the input voltage ripple. It can be calculated as:

$$C_{IN}(min) = \frac{\Delta i}{8 \times f \times V_{IN(ripple)}} \quad (5)$$

where $V_{IN(ripple)}$ is the input ripple.
The output capacitor selection is based on the output ripple requirement. It can be calculated by:

$$C_{OUT} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{1}{f} \times \frac{I_{OUT}}{V_{ripple(pp)}} \quad (6)$$

where V_{ripple} is the peak-to-peak output ripple.

In addition, the ESR-related output ripple can be calculated by:

$$V_{ripple(ESR)} = I_{OUT} \times ESR \quad . \quad (7)$$

If a ceramic capacitor is selected, the ESR-related ripple can be neglected, due to the low ESR. If a tantalum electrolytic capacitor is selected, this portion of ripple voltage has to be considered.

During load transient response, a larger output capacitance always helps to supply or absorb additional current, which results in lower overshoot and undershoot voltage.

Because the capacitor values are low, ceramic capacitors are the best choice for this application. To reduce performance variation over temperature, low drift types such as X7R and X5R should be used. Recommended specifications are shown in the table below. Suitable capacitors are available from TDK, Taiyo Yuden, Murata, Kemet, and AVX.

The output capacitor is placed on the CAP pin only. An additional capacitor can be added on the OUT1 pin, but it is not needed for proper operation and it cannot replace the capacitor on the CAP pin.

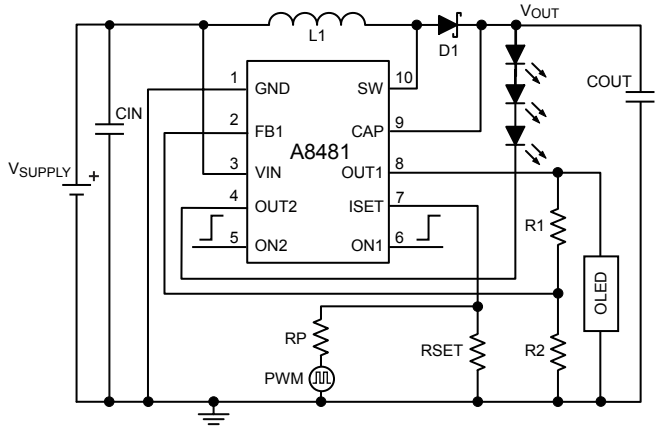


Figure 4a. OUT2 current dimming with PWM on ISET pin

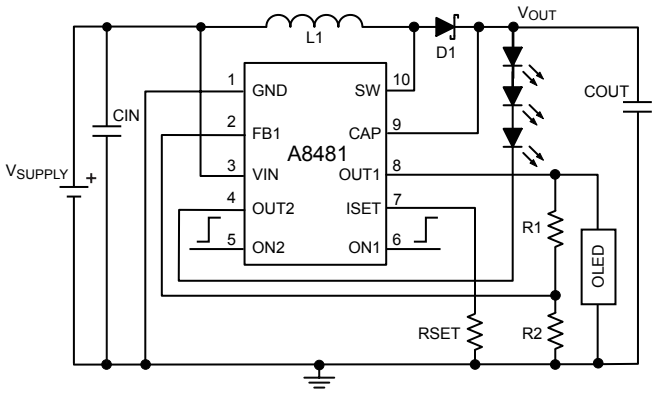
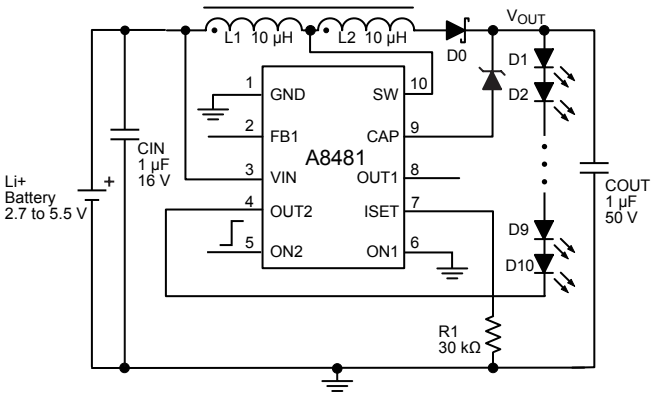


Figure 4b. Three WLED and OLED driver



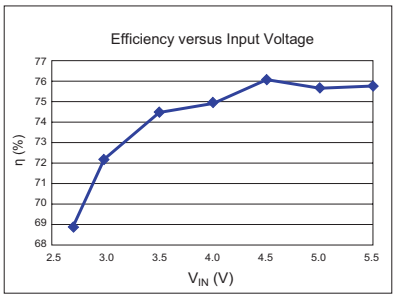


Figure 4c. Ten WLED driver

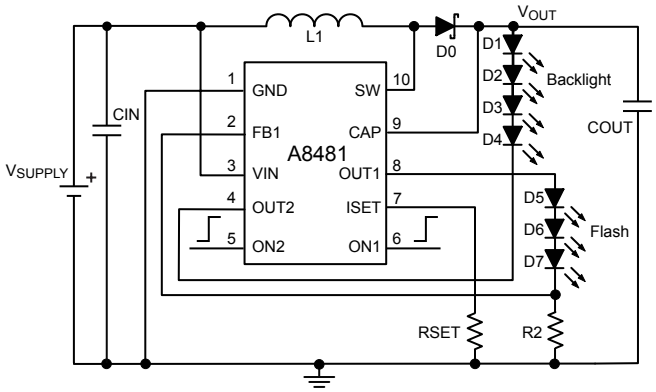


Figure 4d. Four WLED backlight and three 100 mA WLED flash driver

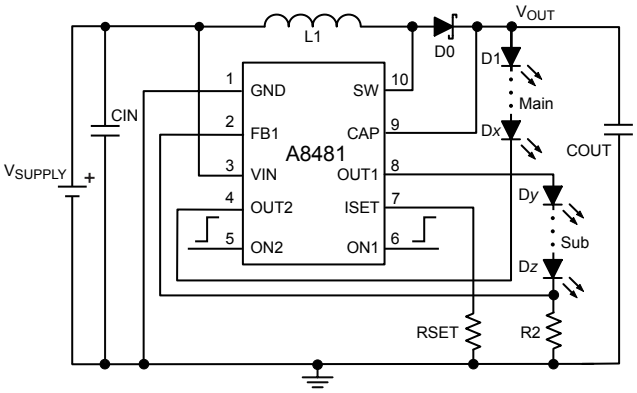
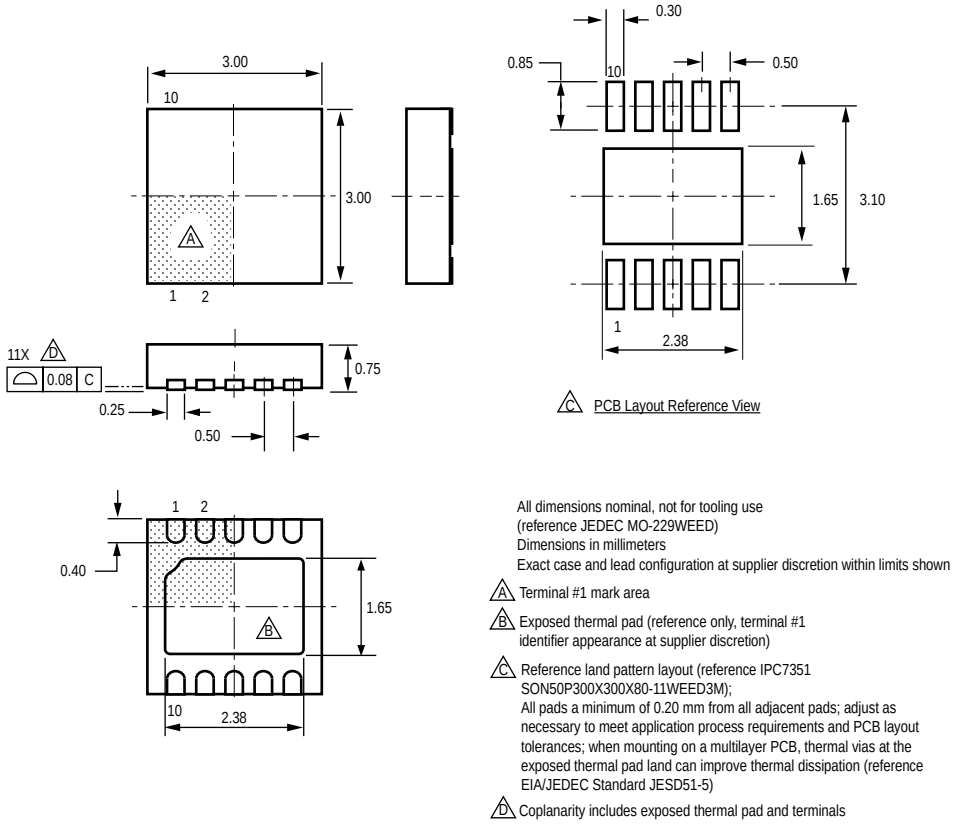


Figure 4e. WLED Main and WLED sub driver

Package EJ, 10-Pin MLP/DFN



All dimensions nominal, not for tooling use
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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