Data Sheet | February 11, 2008 | FN6154.4

## *39µA Micropower Single and Dual Precision Rail-to-Rail Input-Output (RRIO) Low Input Bias Current Op Amps*

The ISL28156 and ISL28256 are micropower precision operational amplifiers optimized for single supply operation at 5V and can operated down to 2.4V.

These devices feature an Input Range Enhancement Circuit (IREC), which enables them to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.5V above a 5.0V supply (0.25 for a 2.5V supply) and to within 10mV from ground. The output operation is rail-to-rail.

The 1/f corner of the voltage noise spectrum is at 1kHz. This results in low frequency noise performance, which can only be found on devices with an order of magnitude higher than the supply current.

ISL28156 and ISL28256 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

## *Ordering Information*

| PART NUMBER (Note) | PART MARKING | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|
| ISL28156FHZ-T7* | GABV | 6 Ld SOT-23 | MDP0038 |
| ISL28156FBZ | 28156 FBZ | 8 Ld SOIC | MDP0027 |
| ISL28156FBZ-T7* | 28156 FBZ | 8 Ld SOIC | MDP0027 |
| *Coming Soon* ISL28256FBZ | 28256 FBZ | 8 Ld SOIC | MDP0027 |
| *Coming Soon* ISL28256FBZ-T7* | 28256 FBZ | 8 Ld SOIC | MDP0027 |
| *Coming Soon* ISL28256FUZ | 8256Z | 8 Ld MSOP | MDP0043 |
| *Coming Soon* ISL28256FUZ-T7* | 8256Z | 8 Ld MSOP | MDP0043 |

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## *Features*

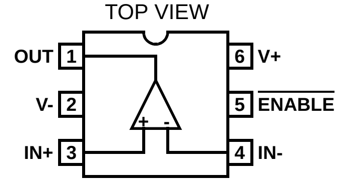
- 39µA typical supply current
- 5nA max input bias current
- 250kHz gain bandwidth product ($A_V = 1$)
- 2.4V to 5.5V single supply voltage range
- Rail-to-rail input and output
- Enable pin (ISL28156 only)
- Pb-free (RoHS compliant)

## *Applications*

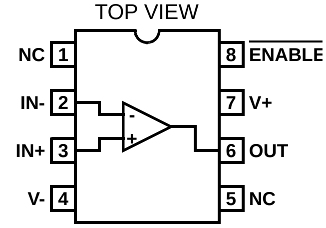
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

## *Pinouts*

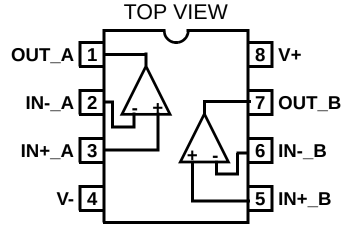
**ISL28156**
**(6 LD SOT-23)**
TOP VIEW



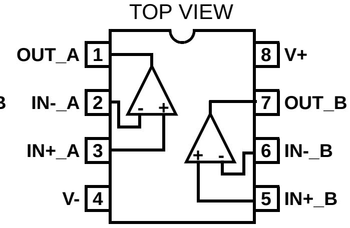

**ISL28156**
**(8 LD SOIC)**
TOP VIEW




**ISL28256**
**(8 LD SOIC)**
TOP VIEW




**ISL28256**
**(8 LD MSOP)**
TOP VIEW



## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage . . . . . . . . . . 5.5V
Supply Turn On Voltage Slew Rate . . . . . . . . . . 1V/µs
Differential Input Current . . . . . . . . . . 5mA
Differential Input Voltage . . . . . . . . . . 0.5V
Input Voltage . . . . . . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
  Human Body Model . . . . . . . . . . 3kV
  Machine Model . . . . . . . . . . 300V

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) |
|---|---|
| 6 Ld SOT-23 Package | 230 |
| 6 Ld SO Package | 110 |
| 8 Ld MSOP Package | 115 |

Output Short-Circuit Duration . . . . . . . . . . Indefinite
Ambient Operating Temperature Range . . . . . . . . . -40°C to +125°C
Storage Temperature Range . . . . . . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . . . . . . +125°C
Pb-free reflow profile . . . . . . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

$V_+$ = 5V, $V_-$ = 0V,$V_{CM}$ = 2.5V, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 1) | TYP | MAX (Note 1) | UNIT |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | 8 Ld SOIC | -120<br>**-200** | -7 | 120<br>**250** | µV |
| | | 6 Ld SOT-23 | -400<br>**-450** | -7 | 400<br>**450** | µV |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Input Offset Drive vs Temperature | | | 1.5 | | µV/°C |
| $I_{OS}$ | Input Offset Current | | -1.5<br>**-5** | 0.34 | 1.2<br>**2.5** | nA |
| $I_B$ | Input Bias Current | | -2<br>**-3.5** | 1.14 | 5<br>**5** | nA |
| $E_N$ | Input Noise Voltage Density | $F_O$ = 1kHz | | 46 | | nV/√Hz |
| $I_N$ | Input Noise Current Density | $F_O$ = 1kHz | | 0.14 | | pA/√Hz |
| CMIR | Input Common-Mode Voltage Range | | 0 | | 5 | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = 0V to 5V | 80<br>**75** | 110 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.4V to 5V | 90<br>**75** | 104 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 0.5V to 4.5V, $R_L$ = 100kΩ | 200<br>**175** | 412 | | V/mV |
| | | $V_O$ = 0.5V to 4.5V, $R_L$ = 1kΩ | 35<br>**30** | 70 | | V/mV |
| $V_{OUT}$ | Maximum Output Voltage Swing | Output low, $R_L$ = 100kΩ | | 3 | 6<br>**8** | mV |
| | | Output low, $R_L$ = 1kΩ | | 130 | 150<br>**200** | mV |
| | | Output high, $R_L$ = 100kΩ | 4.992<br>**4.99** | 4.985 | | V |
| | | Output high, $R_L$ = 1kΩ | 4.85<br>**4.8** | 4.88 | | V |
| SR | Slew Rate | | | 0.05 | | V/µs |
| GBW | Gain Bandwidth Product | $A_V$ = 1 | | 250 | | kHz |
| $I_{S,ON}$ | Supply Current, Enabled | | 29<br>**18** | 39 | 47<br>**56** | µA |

## Electrical Specifications

$V_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 1) | TYP | MAX (Note 1) | UNIT |
|---|---|---|---|---|---|---|
| $I_{S,OFF}$ | Supply Current, Disabled | | | 10 | 14<br>**16** | µA |
| $I_O$+ | Short-Circuit Output Current | $R_L$ = 10Ω | 28<br>**23** | 31 | | mA |
| $I_O$- | Short-Circuit Output Current | $R_L$ = 10Ω | 24<br>**18** | 26 | | mA |
| $V_{SUPPLY}$ | Supply Operating Range | Guaranteed by PSRR test | 2.4 | | 5 | V |
| $V_{ENH}$ | Enable Pin High Level | | **2** | | | V |
| $V_{ENL}$ | Enable Pin Low Level | | | | **0.8** | V |
| $I_{ENH}$ | Enable Pin Input Current | $V_{EN}$ = 5V | 0.7 | 1 | 1.2<br>**1.2** | µA |
| $I_{ENL}$ | Enable Pin Input Current | $V_{EN}$ = 0V | 10 | 16 | 25<br>**30** | nA |
| $t_{EN}$ | Enable to Output On-state Delay Time (ISL28156) | $V_{OUT}$ = 1V (enable state); $V_{\overline{EN}}$ = High to Low | | 10.8 | | µs |
| $t_{\overline{EN}}$ | Enable to Output Off-state Delay Time (ISL28156) | $V_{OUT}$ = 0V (disabled state) $V_{\overline{EN}}$ = Low to High | | 0.1 | | µs |

NOTE:

1. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

## *Typical Performance Curves*

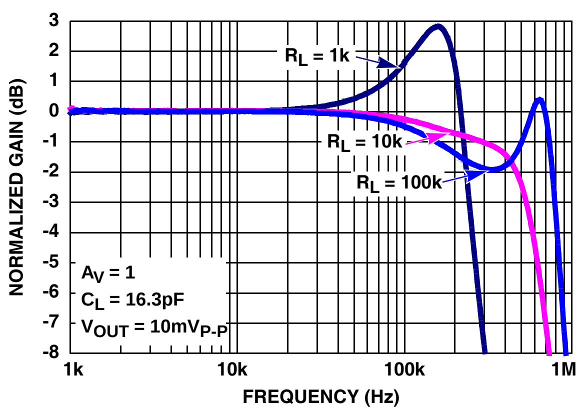



FIGURE 1. GAIN vs FREQUENCY vs RL

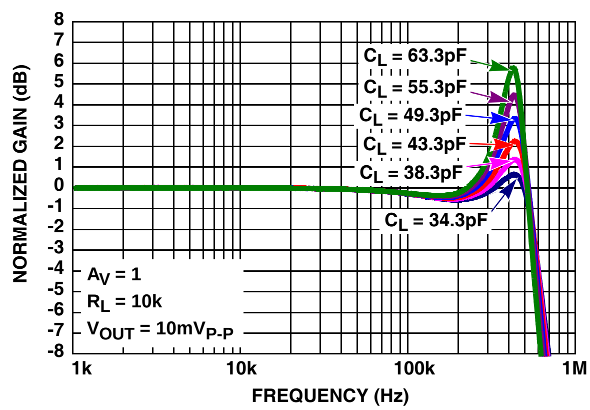



FIGURE 2. GAIN vs FREQUENCY vs $C_L$

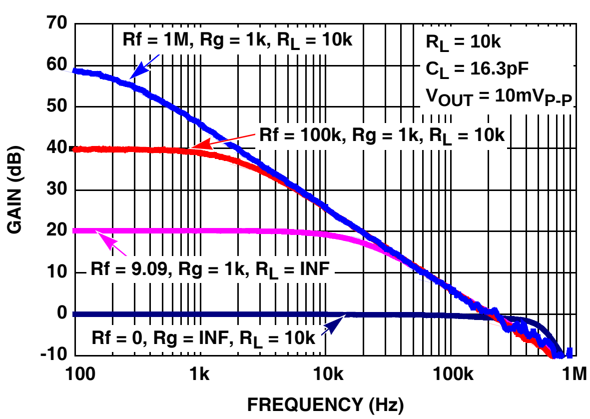



FIGURE 3. CLOSED LOOP GAIN vs FREQUENCY

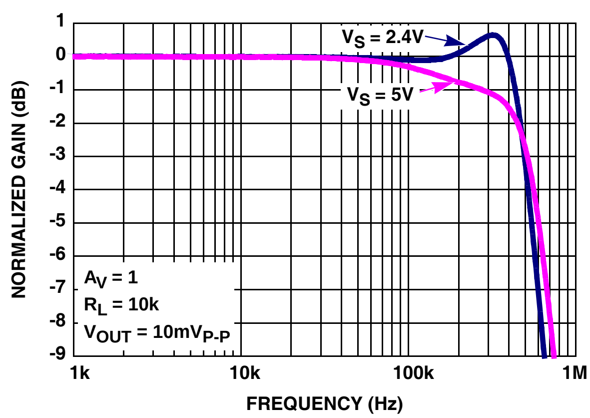



FIGURE 4. GAIN vs FREQUENCY vs $V_S$

## *Typical Performance Curves* (Continued)

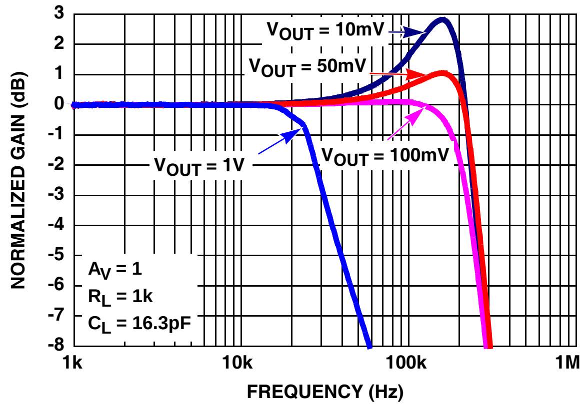



FIGURE 5. GAIN vs FREQUENCY vs $V_{OUT}$

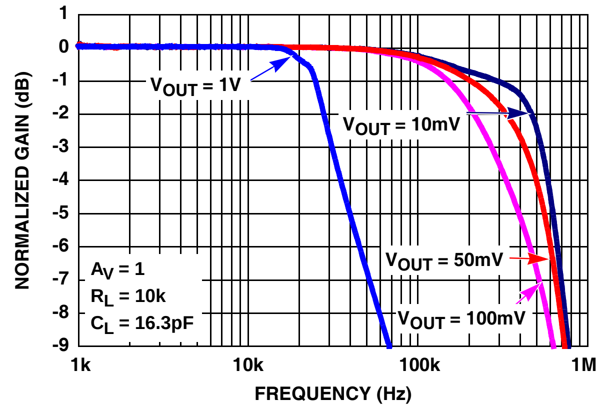



FIGURE 6. GAIN vs FREQUENCY vs $V_{OUT}$

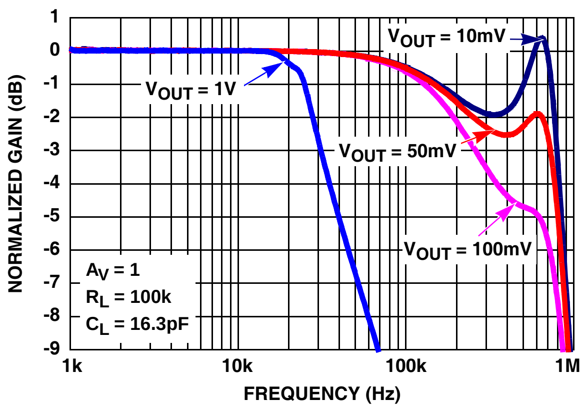



FIGURE 7. GAIN vs FREQUENCY vs $V_{OUT}$

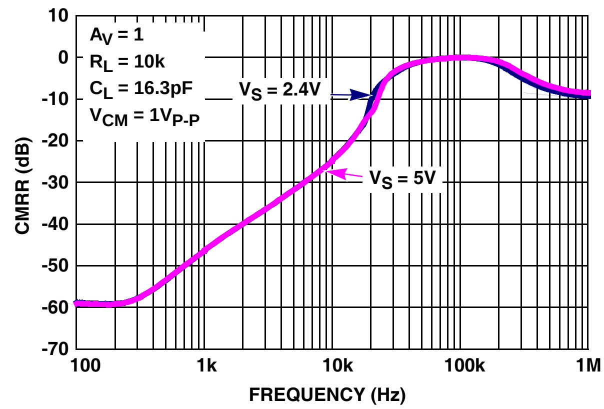



FIGURE 8. CMRR vs FREQUENCY

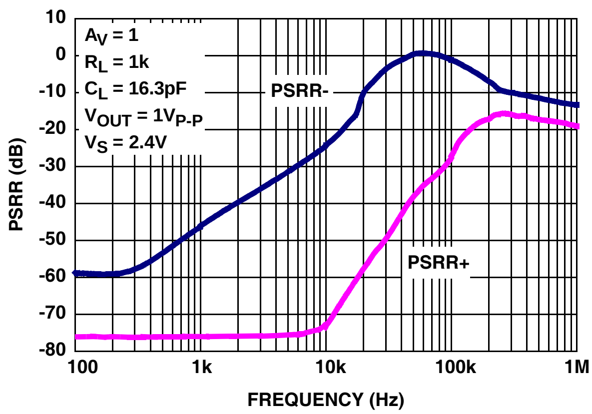



FIGURE 9. PSRR vs FREQUENCY, $V_S$ = 2.4V

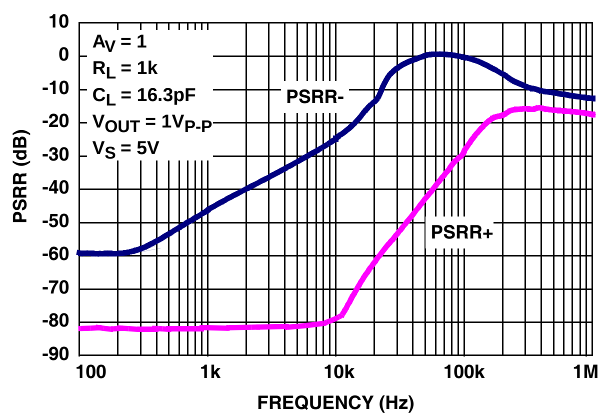



FIGURE 10. PSRR vs FREQUENCY, $V_S$ = 5V

## *Typical Performance Curves* (Continued)

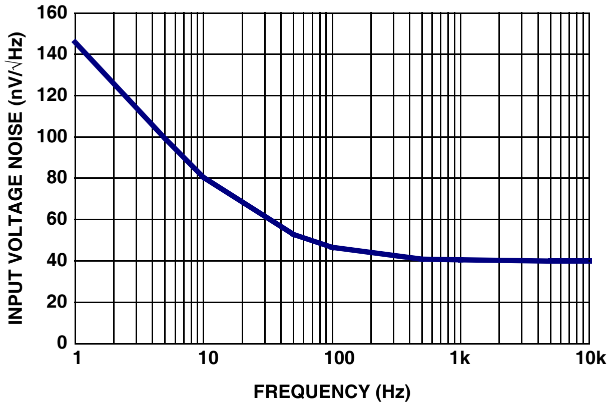



FIGURE 11. INPUT VOLTAGE NOISE vs FREQUENCY

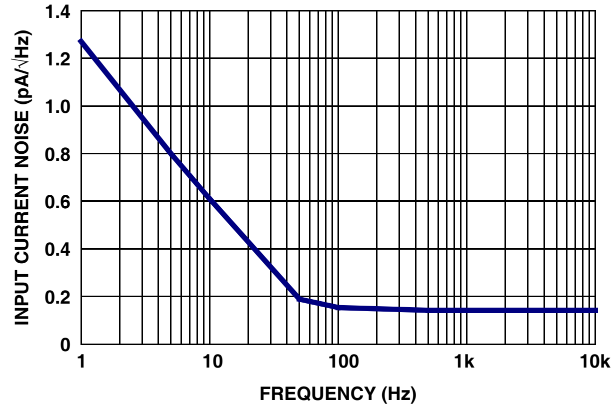



FIGURE 12. INPUT CURRENT NOISE vs FREQUENCY

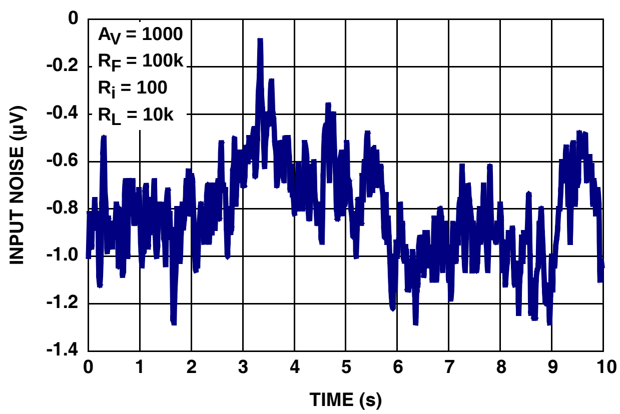



FIGURE 13. 1Hz TO 10Hz INPUT NOISE

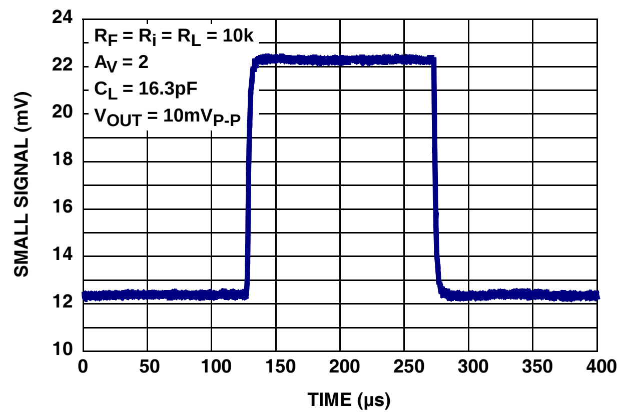



FIGURE 14. SMALL SIGNAL STEP RESPONSE

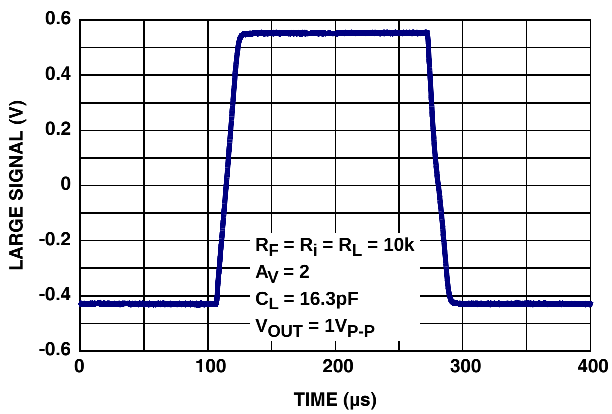



FIGURE 15. LARGE SIGNAL STEP RESPONSE

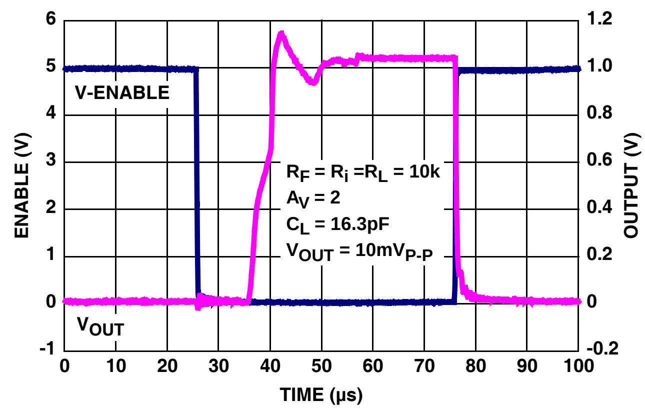



FIGURE 16. ENABLE TO OUTPUT DELAY

## *Typical Performance Curves* (Continued)

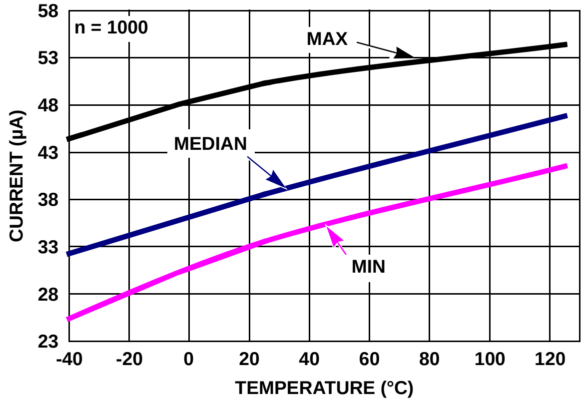



FIGURE 17. SUPPLY CURRENT ENABLED vs TEMPERATURE $V_S$ = ±2.5V

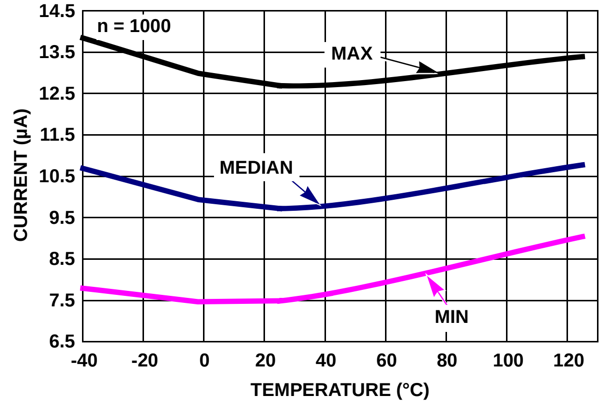



FIGURE 18. SUPPLY CURRENT DISABLED vs TEMPERATURE $V_S$ = ±2.5V

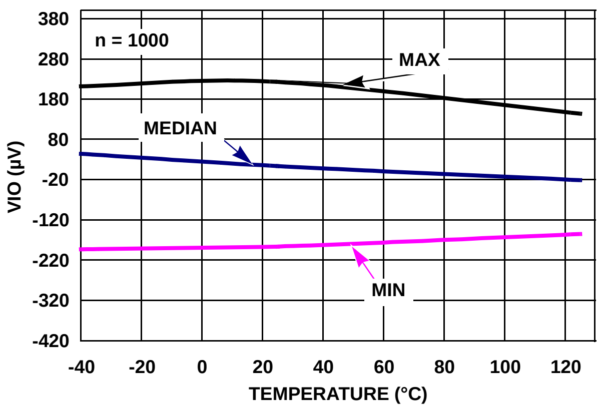



FIGURE 19. VIO SO8 PACKAGE vs TEMPERATURE $V_S$ = ±2.5V

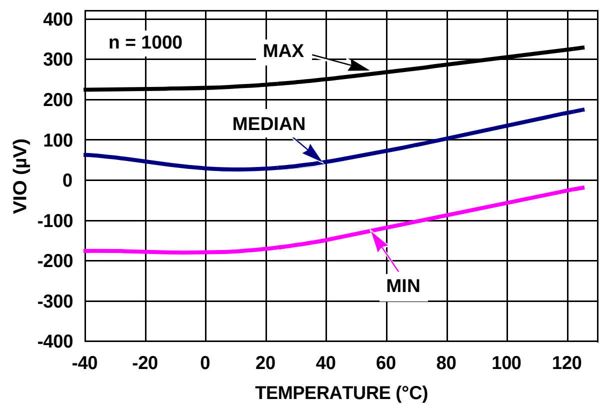



FIGURE 20. VIO SO8 PACKAGE vs TEMPERATURE $V_S$ = ±1.2V

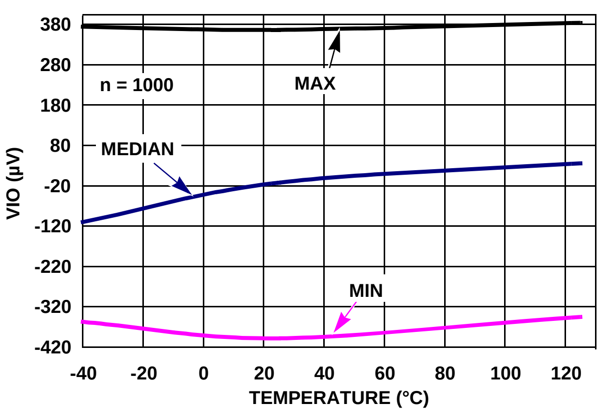



FIGURE 21. VIO SOT-23 PACKAGE vs TEMPERATURE $V_S$ = ±2.5V

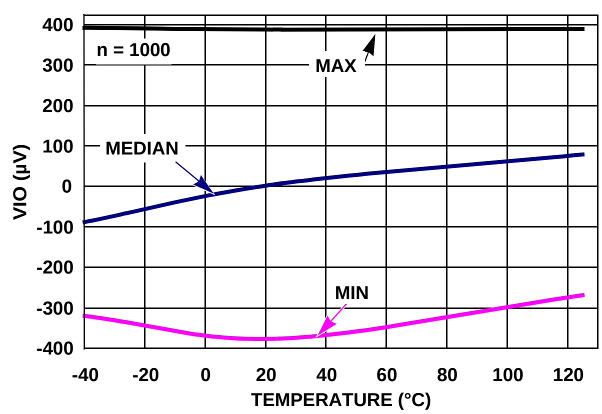



FIGURE 22. VIO SOT-23 PACKAGE vs TEMPERATURE $V_S$ = ±1.2V

## *Typical Performance Curves* (Continued)

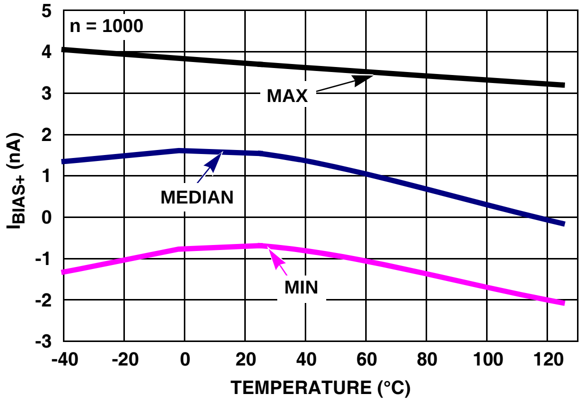



FIGURE 23. $I_{BIAS+}$ vs TEMPERATURE $V_S$ = ±2.5V

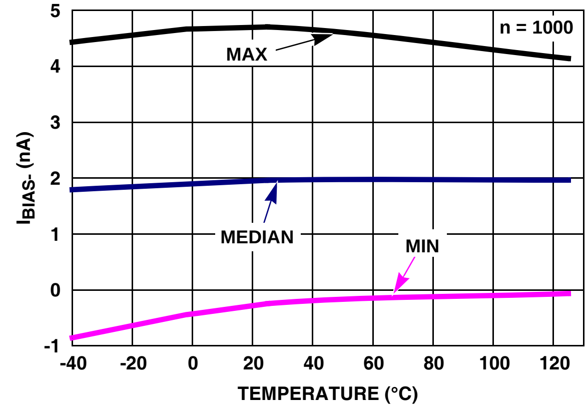



FIGURE 24. $I_{BIAS-}$ vs TEMPERATURE $V_S$ = ±2.5V

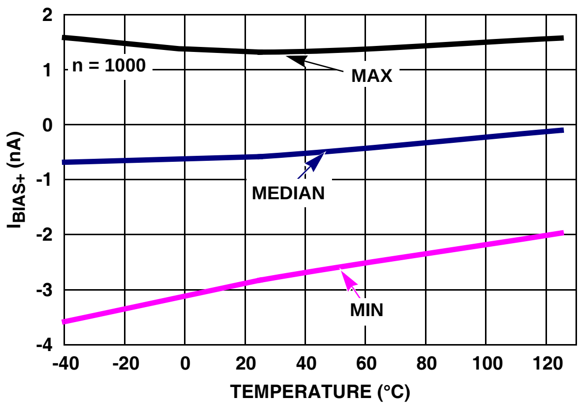



FIGURE 25. $I_{BIAS+}$ vs TEMPERATURE $V_S$ = ±1.5V

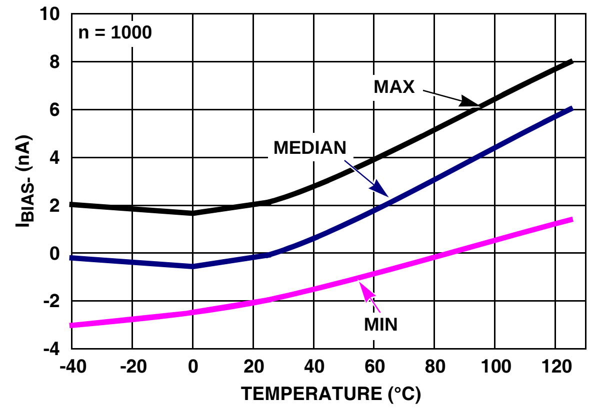



FIGURE 26. $I_{BIAS-}$ vs TEMPERATURE $V_S$ = ±1.2V

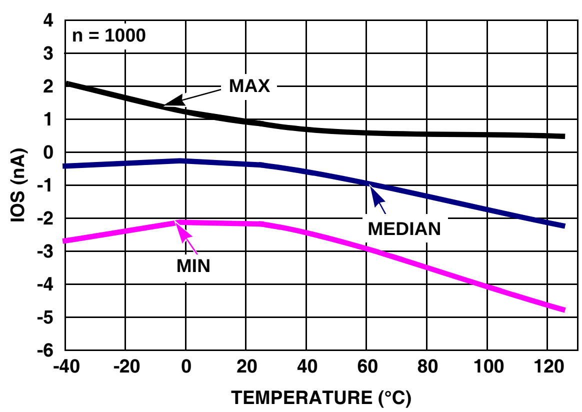



FIGURE 27. IOS vs TEMPERATURE $V_S$ = ±2.5V

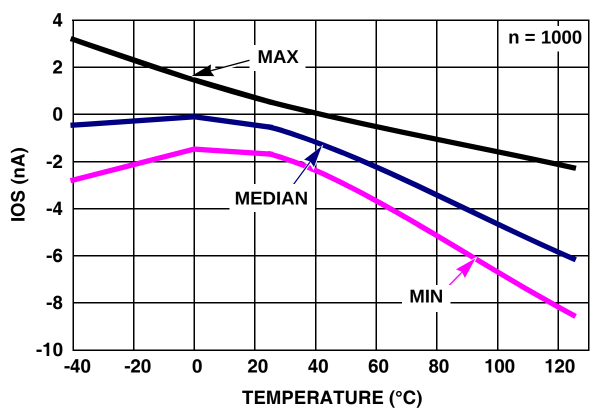



FIGURE 28. IOS vs TEMPERATURE $V_S$ = ±1.5V

## *Typical Performance Curves* (Continued)

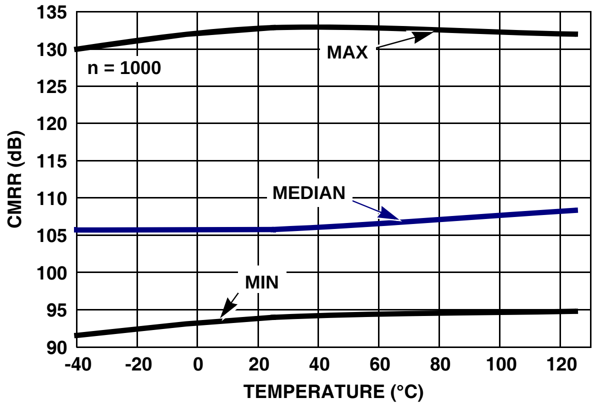



FIGURE 29. CMRR vs TEMPERATURE V+ = ±2.5V, ±1.5V

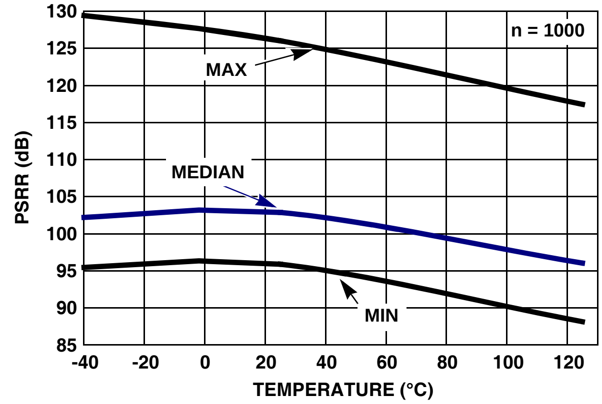



FIGURE 30. PSRR vs TEMPERATURE ±1.2V to ±2.5V

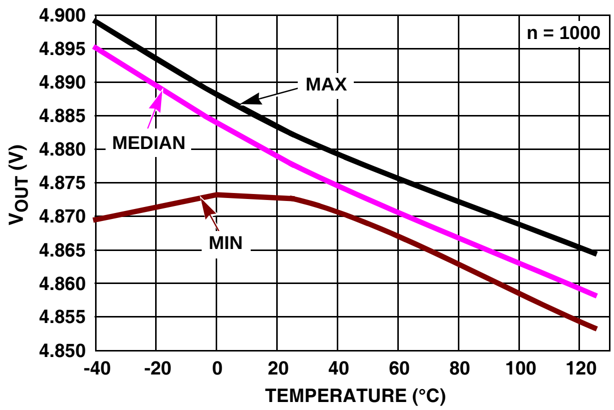



FIGURE 31. $V_{OUT}$ HIGH vs TEMPERATURE $V_S$ = ±2.5V, $R_L$ = 1k

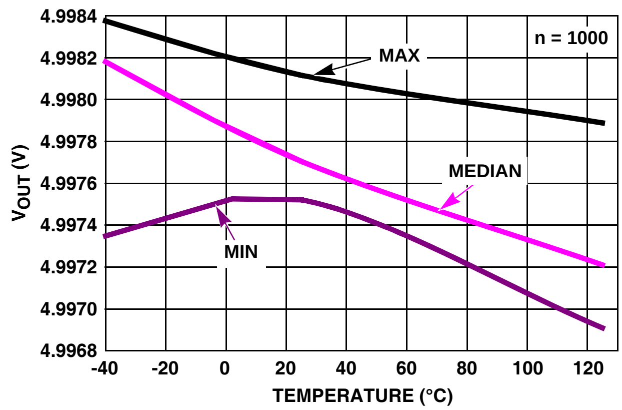



FIGURE 32. $V_{OUT}$ HIGH $V_S$ = ±2.5V, $R_L$ = 100k

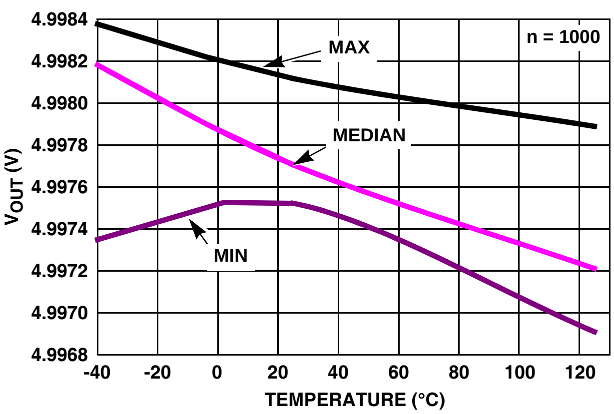



FIGURE 33. $V_{OUT}$ LOW $V_S$ = ±2.5V, $R_L$ = 1k

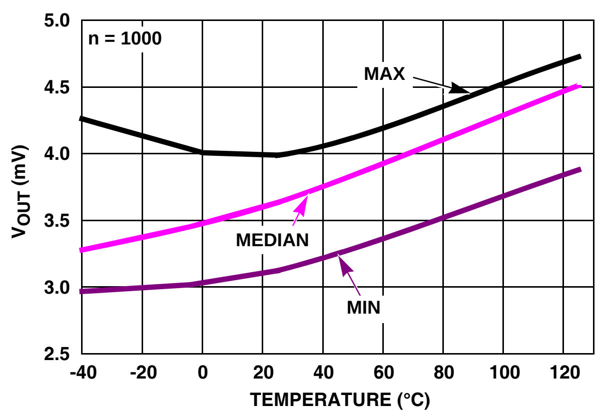
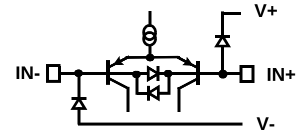
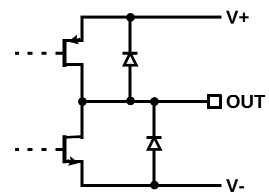
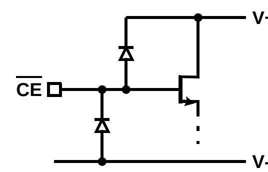



FIGURE 34. $V_{OUT}$ LOW $V_S$ = ±2.5V, $R_L$ = 100k

## Pin Descriptions

| ISL28156 (6 Ld SOT-23) | ISL28156 (8 Ld SOIC) | ISL28256 (8 Ld MSOP) | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|---|---|
| | 1, 5 | | NC | Not connected | |
| 4 | 2 | 2 (A)<br>6 (B) | IN-<br>IN-_A<br>IN-_B | Inverting input | <br>Circuit 1 |
| 3 | 3 | 3 (A)<br>5 (B) | IN+<br>IN+_A<br>IN+_B | Non-inverting input | (See Circuit 1) |
| 2 | 4 | 4 | V- | Negative supply | |
| 1 | 6 | 1 (A)<br>7 (B) | OUT<br>OUT_A<br>OUT_B | Output | <br>Circuit 2 |
| 6 | 7 | 8 | V+ | Positive supply | |
| 5 | 8 | | $\overline{ENABLE}$ | Chip enable | <br>Circuit 3 |

## Applications Information

### Introduction

The ISL28156 is a single BiMOS rail-to-rail input, output (RRIO) operational amplifier with an enable feature. The ISL28256 is a dual version without the enable feature. Both devices are designed to operate from single supply (2.4V to 5.0V) or dual supplies (±1.2V to ±2.5V) while drawing only 39µA of supply current per amplifier. This combination of low power and precision performance makes this device suitable for a variety of low power applications including battery powered systems.

### Rail-to-Rail Input/Output

These devices feature bi-polar inputs, which have an input common mode range that extends up to 0.5V beyond the V+ rail, and to within 10mV of the V- rail. The CMOS outputs typically swing to within about 4mV of the supply rails with a 100kΩ load. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction.

### Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA (Figure 35).

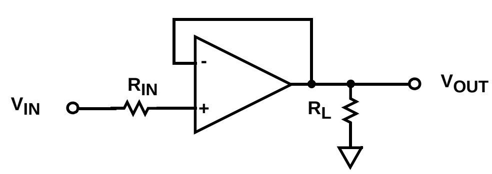



**FIGURE 35. INPUT CURRENT LIMITING**

### Enable/Disable Feature

The ISL28156 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10µA. By disabling the part, multiple ISL28156 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$

pin. The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together.

### Using Only One Channel

The ISL28256 is a dual op amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 36).

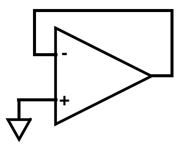



**FIGURE 36. PREVENTING OSCILLATIONS IN UNUSED CHANNELS**

### Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

### Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)

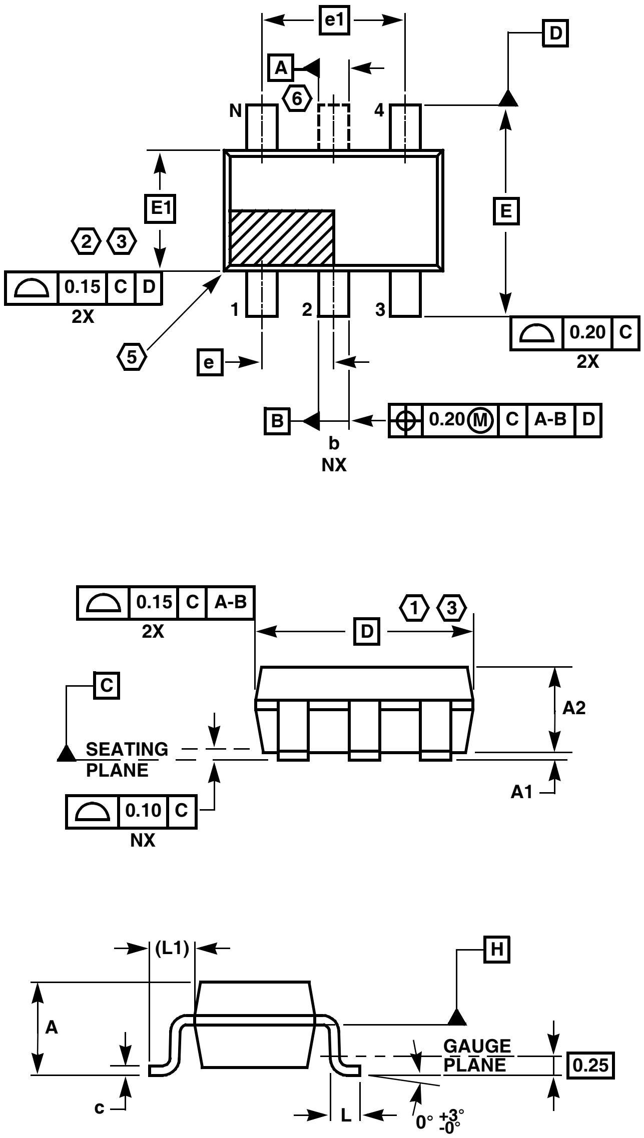
$PD_{MAX}$ for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = 2{*}V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- $T_{MAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package
- $PD_{MAX}$ = Maximum power dissipation of 1 amplifier
- $V_S$ = Supply voltage
- $I_{MAX}$ = Maximum supply current of 1 amplifier
- $V_{OUTMAX}$ = Maximum output voltage swing of the application
- $R_L$ = Load resistance

## SOT-23 Package Family




## MDP0038

**SOT-23 PACKAGE FAMILY**

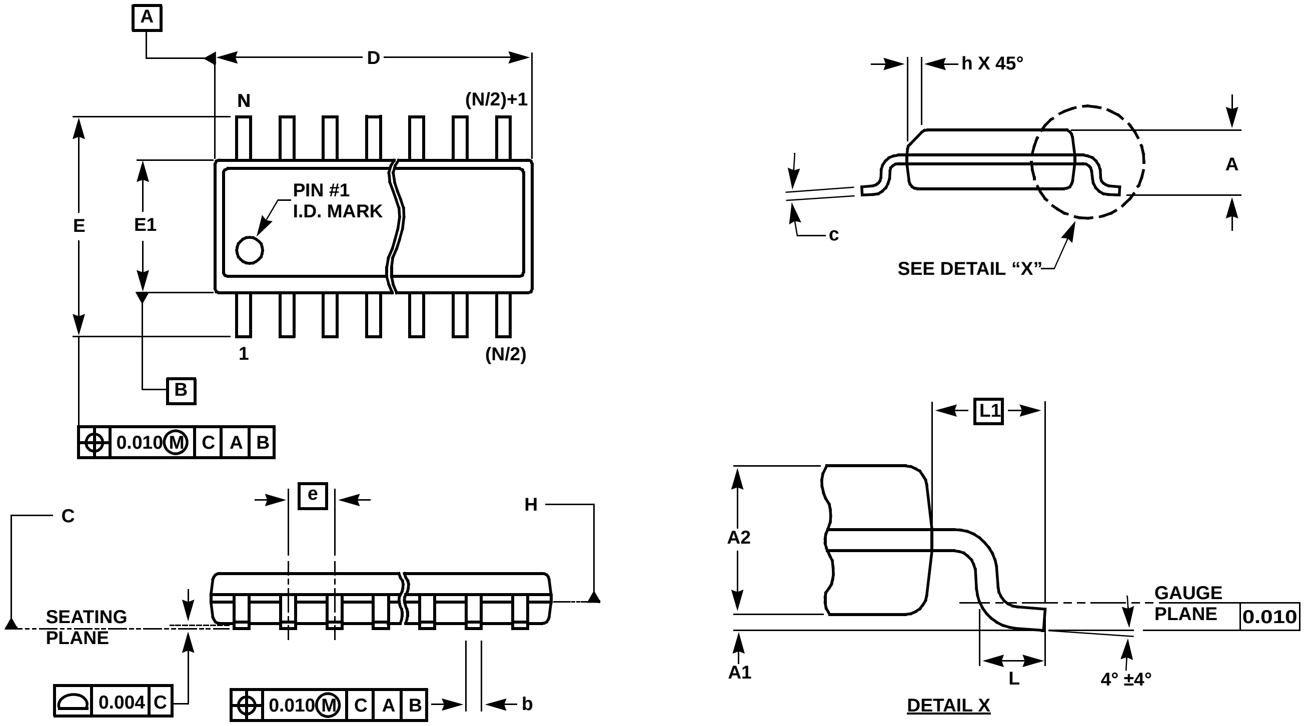
| SYMBOL | MILLIMETERS | | TOLERANCE |
|---|---|---|---|
| | SOT23-5 | SOT23-6 | |
| A | 1.45 | 1.45 | MAX |
| A1 | 0.10 | 0.10 | ±0.05 |
| A2 | 1.14 | 1.14 | ±0.15 |
| b | 0.40 | 0.40 | ±0.05 |
| c | 0.14 | 0.14 | ±0.06 |
| D | 2.90 | 2.90 | Basic |
| E | 2.80 | 2.80 | Basic |
| E1 | 1.60 | 1.60 | Basic |
| e | 0.95 | 0.95 | Basic |
| e1 | 1.90 | 1.90 | Basic |
| L | 0.45 | 0.45 | ±0.10 |
| L1 | 0.60 | 0.60 | Reference |
| N | 5 | 6 | Reference |

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

## Small Outline Package Family (SO)




## MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

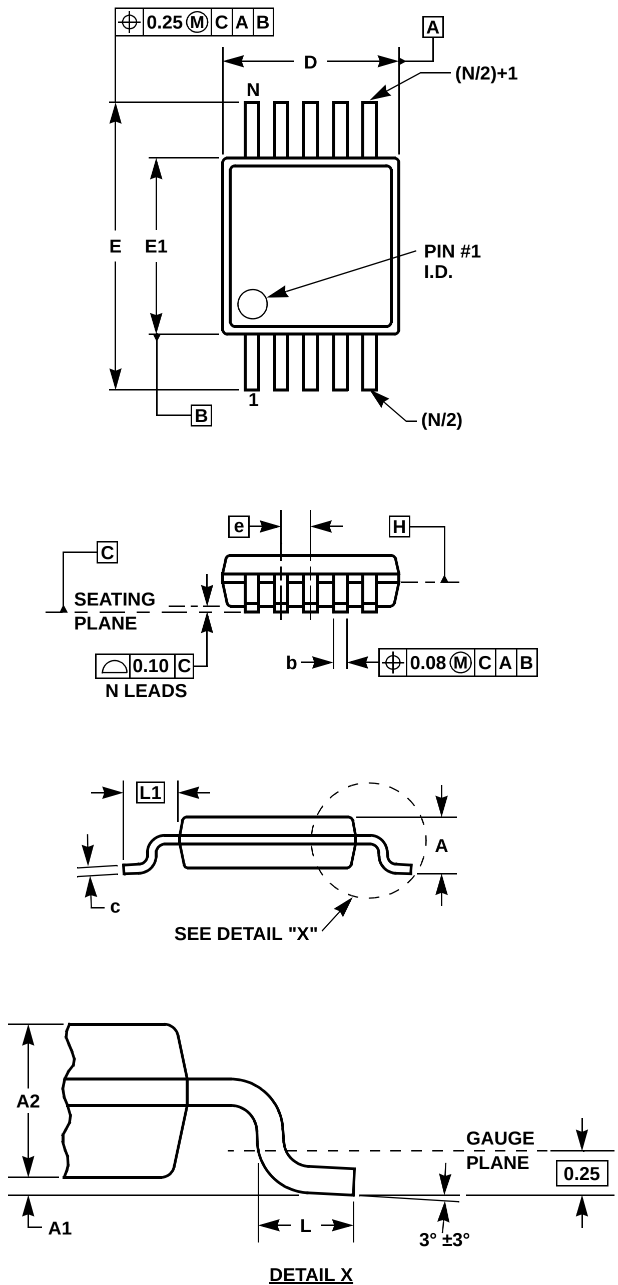
| SYMBOL | INCHES | | | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | SO-8 | SO-14 | SO16 (0.150”) | SO16 (0.300”) (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994

## Mini SO Package Family (MSOP)




### MDP0043

**MINI SO PACKAGE FAMILY**

| SYMBOL | MILLIMETERS | | TOLERANCE | NOTES |
|---|---|---|---|---|
| | MSOP8 | MSOP10 | | |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | ±0.05 | - |
| A2 | 0.86 | 0.86 | ±0.09 | - |
| b | 0.33 | 0.23 | +0.07/-0.08 | - |
| c | 0.18 | 0.18 | ±0.05 | - |
| D | 3.00 | 3.00 | ±0.10 | 1, 3 |
| E | 4.90 | 4.90 | ±0.15 | - |
| E1 | 3.00 | 3.00 | ±0.10 | 2, 3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | ±0.15 | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.