V_{DRM}	= 5600	V
V_{DSM}	= 6500	V
$I_{T(AV)M}$	= 1370	A
$I_{T(RMS)}$	= 2160	A
I_{TSM}	= 21.9×10^3	A
$V_{(T0)}$	= 1.18	V
r_T	= 0.632	mΩ

Phase Control Thyristor

5STP 12K6500

Doc. No. 5SYA1069-01 May 04

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate**

Blocking

Maximum rated values [1)]

Symbol	Conditions	5STP 12K6500	5STP 12K6200	5STP 12K5800
V_{DSM}, V_{RSM}	f = 5 Hz, t_p = 10 ms	6500 V	6200 V	5800 V
V_{DRM}, V_{RRM}	f = 50 Hz, t_p = 10 ms	5600 V	5300 V	4900 V
dV/dt_{crit}	Exp. to 3750 V, T_{vj} = 125°C	2000 V/µs		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DSM}	V_{DSM}, T_{vj} = 125°C			600	mA
Reverse leakage current	I_{RSM}	V_{RSM}, T_{vj} = 125°C			600	mA

V_{DRM}/ V_{RRM} are equal to V_{DSM}/ V_{RSM} values up to T_{vj} = 110°C

Mechanical data

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		45	50	60	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				1.15	kg
Housing thickness	H	F_M = 50 kN, T_a = 25 °C				mm
Surface creepage distance	D_S		45			mm
Air strike distance	D_a		24			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, T_c = 70°C			1370	A
RMS on-state current	$I_{T(RMS)}$				2160	A
Peak non-repetitive surge current	I_{TSM}	tp = 10 ms, T_{vj} = 125 °C, $V_D = V_R$ = 0 V			21.9×10^3	A
Limiting load integral	I^2t				2.4×10^6	A^2s
Peak non-repetitive surge current	I_{TSM}	tp = 8.3 ms, T_{vj} = 125 °C, $V_D = V_R$ = 0 V			23.35×10^3	A
Limiting load integral	I^2t				2.26×10^6	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 1500 A, T_{vj} = 125 °C			2.12	V
Threshold voltage	$V_{(T0)}$	I_T = 800 A - 2000 A, T_{vj}= 125 °C			1.18	V
Slope resistance	r_T				0.632	mΩ
Holding current	I_H	T_{vj} = 25 °C			125	mA
		T_{vj} = 125 °C			75	mA
Latching current	I_L	T_{vj} = 25 °C			600	mA
		T_{vj} = 125 °C			200	mA

Switching

Maximum rated values [1)]

Parameter	Symbol	Conditions		min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	T_{vj} = 125 °C, I_{TRM} = 1300 A,	Cont. f = 50 Hz			250	A/µs
Critical rate of rise of on-state current	di/dt_{crit}	$V_D \leq$ 3750 V, I_{FG} = 2 A, t_r = 0.5 µs	Cont. f = 1Hz			1000	A/µs
Circuit-commutated turn-off time	t_q	T_{vj} = 125°C, I_{TRM} = 800 A, V_R = 200 V, di_T/dt = -1 A/µs, $V_D \leq 0.67 \cdot V_{DRM}$, dv_D/dt = 20V/µs		800			µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_{rr}	T_{vj} = 125°C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1 A/µs	1600		2600	µAs
Gate turn-on delay time	t_{gd}	$V_D = 0.4 \cdot V_{RM}$, I_{FG} = 2 A, t_r = 0.5 µs, T_{vj} = 25 °C			3	µs

Triggering

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 9			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate-trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 125 °C	0.3			V
Gate non-trigger current	I_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 125°C	10			mA

Thermal

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				125	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 45...60 kN			11	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 45...60 kN			22	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 45...60 kN			22	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 45...60 kN			2	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 45...60 kN			4	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_{th\,i}(1 - e^{-t/t_i})$$

i	1	2	3	4
$R_{th\,i}$(K/kW)	7.347	2.414	0.797	0.447
τ_i(s)	0.9879	0.0995	0.0157	0.0040

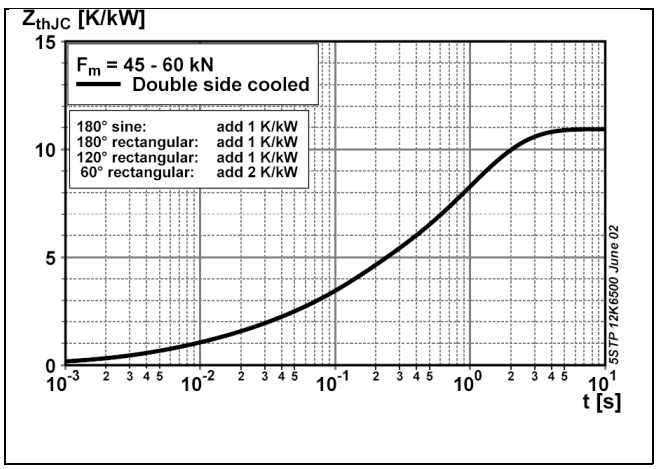

Fig. 1 Transient thermal impedance junction-to case.

Max. on-state characteristic model:

$$V_{T25} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 200 – 14000 A

A_{25}	B_{25}	C_{25}	D_{25}
12.00×10^{-6}	300.10×10^{-6}	237.6×10^{-3}	-5.56×10^{-3}

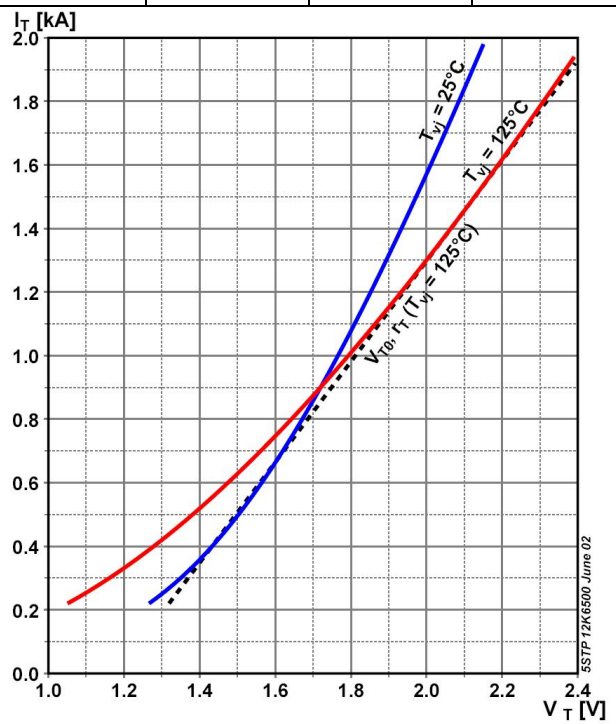

Fig. 2 Max. on-state voltage characteristics

Max. on-state characteristic model:

$$V_{T125} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 200 – 14000 A

A_{125}	B_{125}	C_{125}	D_{125}
197.70×10^{-6}	295.90×10^{-6}	131.10×10^{-3}	18.70×10^{-3}

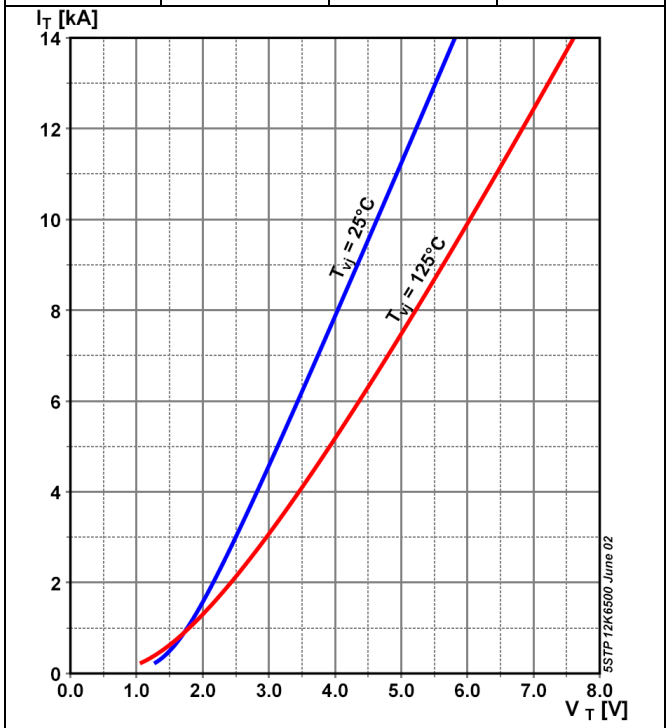

Fig. 3 Max. on-state voltage characteristics

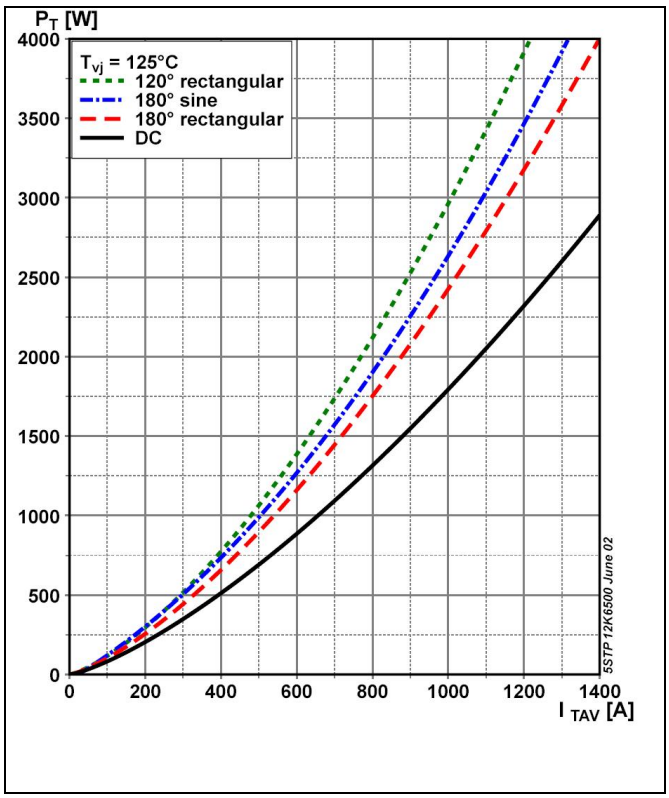

Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

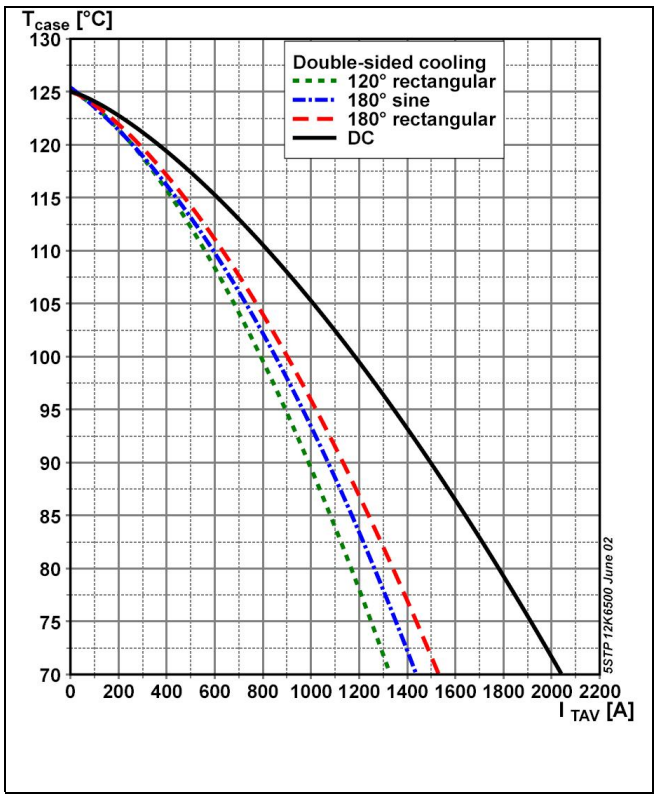

Fig. 5 Max. permissible case temperature vs. mean on-state current.

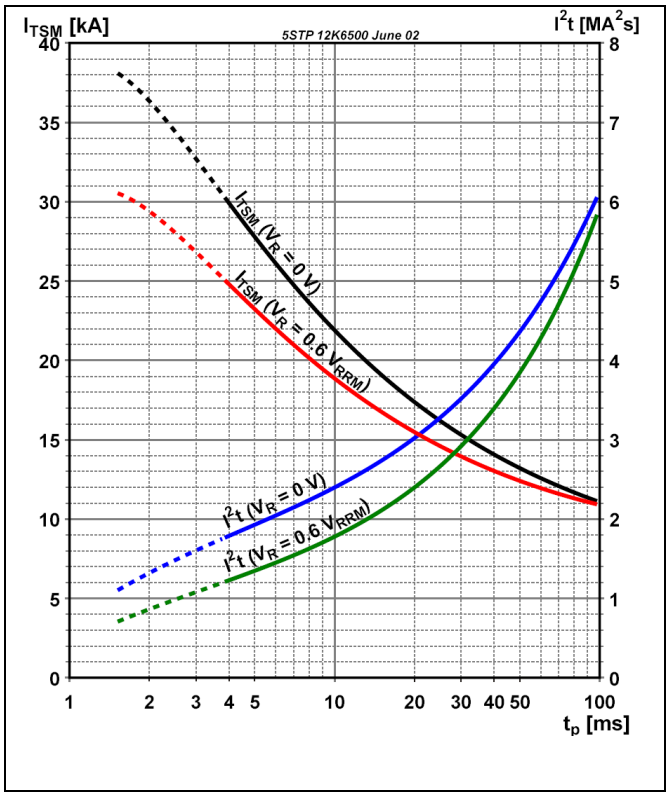

Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

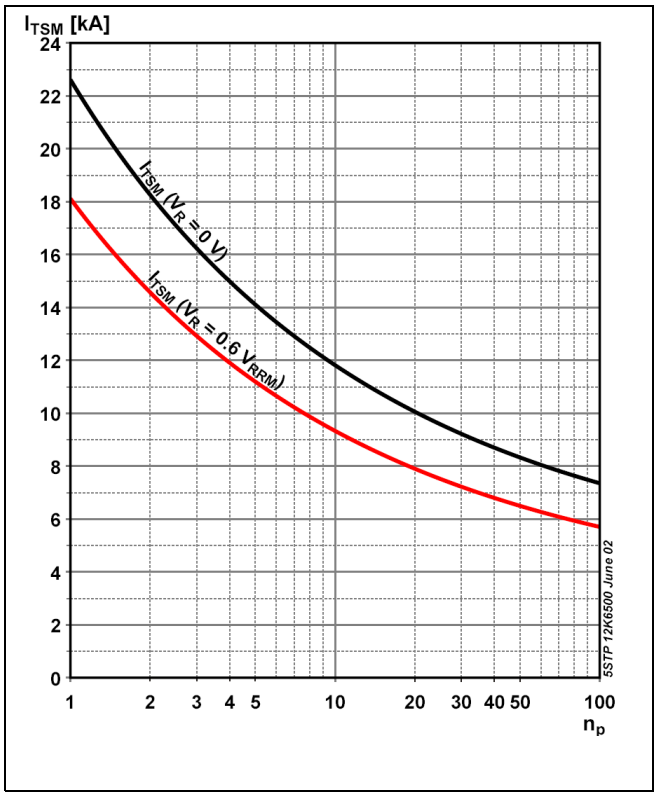

Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

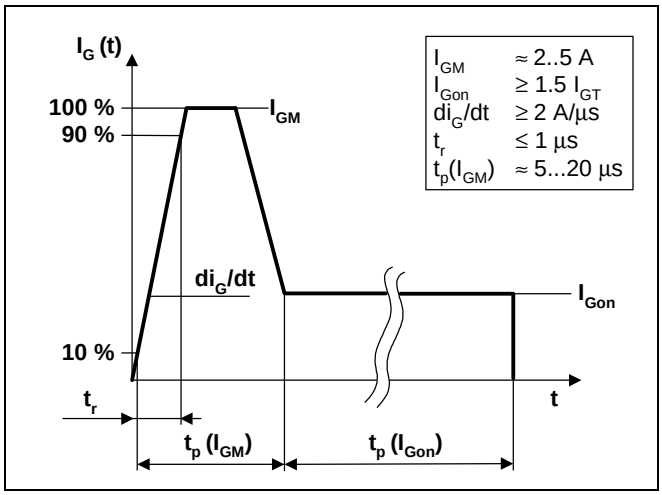

Fig. 8 Recommended gate current waveform.

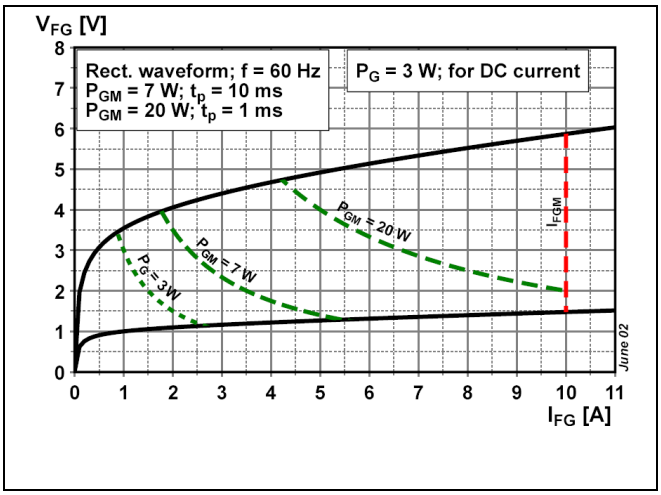

Fig. 9 Max. peak gate power loss.

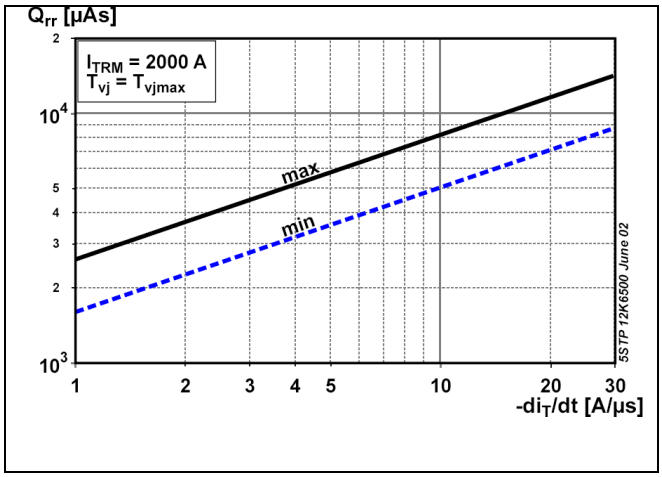

Fig. 10 Recovery charge vs. decay rate of on-state current.

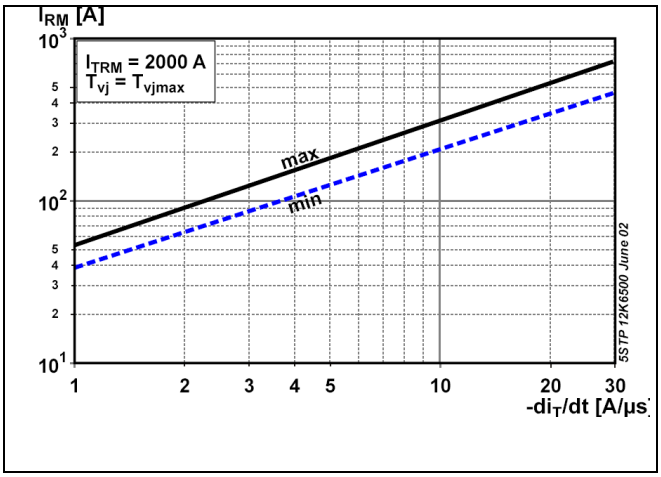

Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

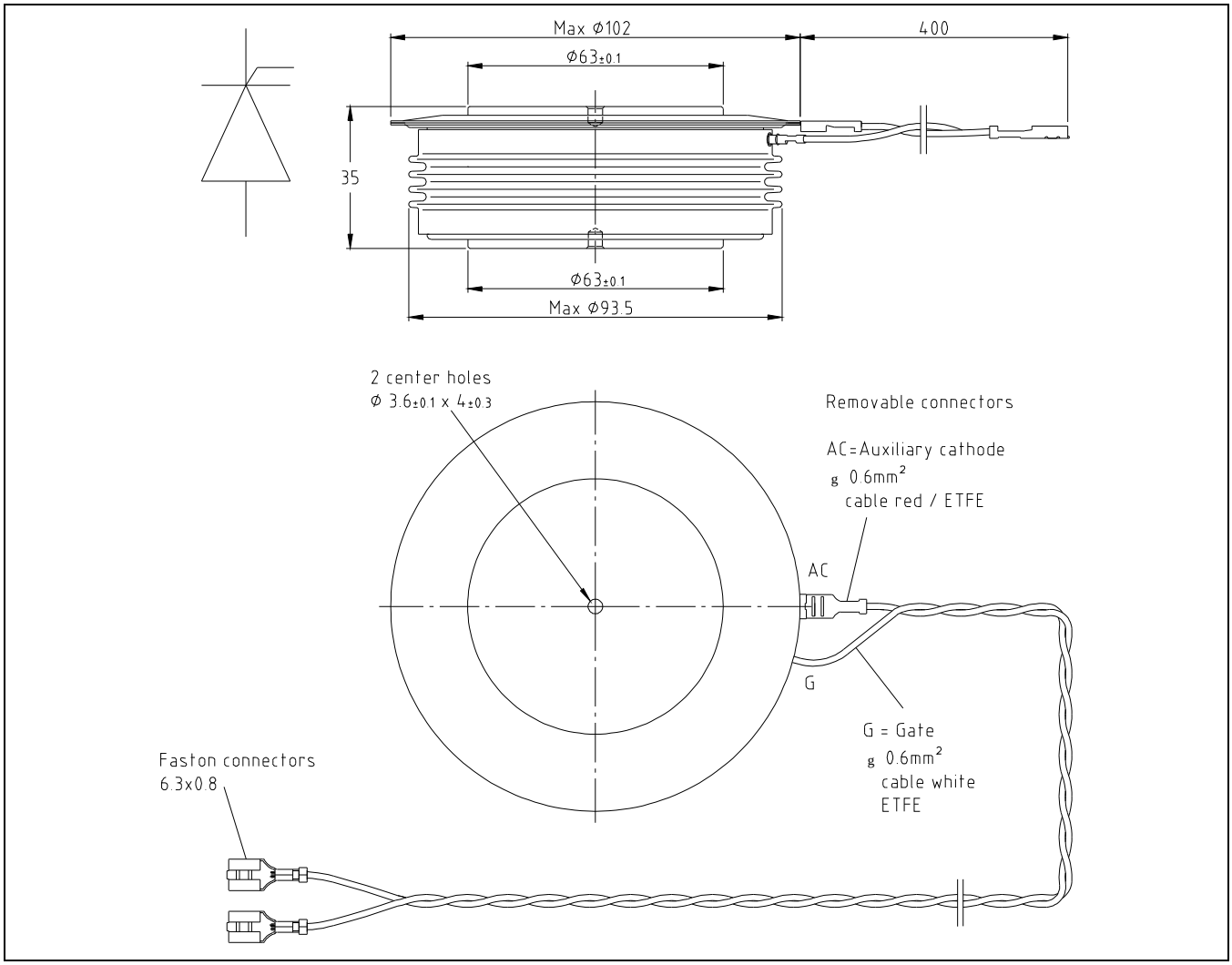

Fig. 12 Device Outline Drawing.

Related application notes:

Doc. Nr	Titel
5SYA2020	Design of RC-Snubber for Phase Control Applications
5SYA2034	Gate-drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors

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