

# LPV7215

## Micropower, CMOS Input, RRIO, 1.8V, Push-Pull Output Comparator

### General Description

The LPV7215 is an ultra low-power comparator with a typical power supply current of 580 nA. It has the best-in-class power supply current versus propagation delay performance available among National's low-power comparators. The propagation delay is as low as 4.5 microseconds with 100 mV overdrive at 1.8V supply.

Designed to operate over a wide range of supply voltages, from 1.8V to 5.5V, with guaranteed operation at 1.8V, 2.7V and 5.0V, the LPV7215 is ideal for use in a variety of battery-powered applications. With rail-to-rail common mode voltage range, the LPV7215 is well suited for single-supply operation.

Featuring a push-pull output stage, the LPV7215 allows for operation with absolute minimum power consumption when driving any capacitive or resistive load.

Available in a choice of space-saving packages, the LPV7215 is ideal for use in handheld electronics and mobile phone applications. The LPV7215 is manufactured with National's advanced VIP50 process.

### Features

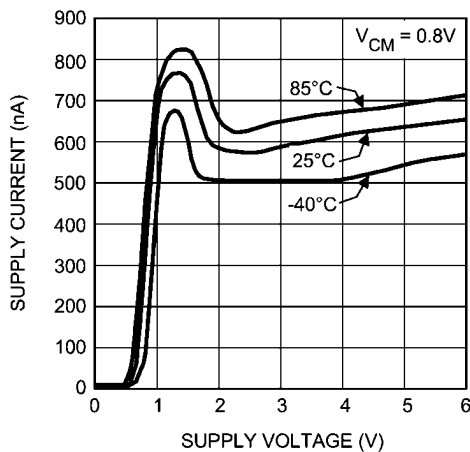
(For  $V^+ = 1.8V$ , typical unless otherwise noted)

- Ultra low power consumption 580 nA
- Wide supply voltage range 1.8V to 5.5V
- Propagation delay 4.5  $\mu s$
- Push-Pull output current drive @ 5V 19 mA
- Temperature range  $-40^{\circ}C$  to  $85^{\circ}C$
- Rail-to-Rail input
- Tiny 5-Pin SOT23 and SC70 packages

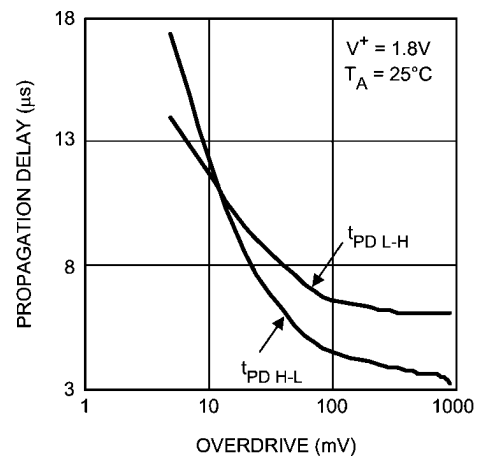
### Applications

- RC timers
- Window detectors
- IR receiver
- Multivibrators
- Alarm and monitoring circuits

### Typical Application



Supply Current vs. Supply Voltage 20123605



Propagation Delay vs. Overdrive 20123602

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

### ESD Tolerance (Note 2)

Human Body Model	2000V
Machine Model	200V
V <sub>IN</sub> Differential	±2.5V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	6V
Voltage at Input/Output pins	V <sup>+</sup> +0.3V, V <sup>-</sup> -0.3V
Storage Temperature Range	-65°C to +150°C
Junction Temperature (Note 3)	+150°C

### Soldering Information

Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

## Operating Ratings (Note 1)

Temperature Range (Note 3)	-40°C to 85°C
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	1.8V to 5.5V
Package Thermal Resistance (θ <sub>JA</sub> (Note 3))	
5-Pin SC70	456°C/W
5-Pin SOT23	234°C/W

## 1.8V Electrical Characteristics (Note 8)

Unless otherwise specified, all limits are guaranteed for T<sub>A</sub> = 25°C, V<sup>+</sup> = 1.8V, V<sup>-</sup> = 0V, and V<sub>CM</sub> = V<sup>+</sup>/2, V<sub>O</sub> = V<sup>-</sup>. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units	
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 0.3V		580	750 <b>825</b>	nA	
		V <sub>CM</sub> = 1.5V		790	980 <b>1050</b>		
V <sub>OS</sub>	Input Offset Voltage	SC70 Package	V <sub>CM</sub> = 0V		±0.3	±2.8 <b>±3.5</b>	mV
			V <sub>CM</sub> = 1.8V		±0.4	±2.2 <b>±2.9</b>	
		SOT23 Package	V <sub>CM</sub> = 0V			±3.2 <b>±3.9</b>	
			V <sub>CM</sub> = 1.8V			±2.5 <b>±3.2</b>	
TCV <sub>OS</sub>	Input Offset Average Drift	(Note 7)		±1		µV/C	
I <sub>B</sub>	Input Bias Current (Note 6)	V <sub>CM</sub> = 1.6V		-40		fA	
I <sub>OS</sub>	Input Offset Current			10		fA	
CMRR	Common Mode Rejection Ratio	V <sub>CM</sub> Stepped from 0V to 0.7V	66 <b>65</b>	88		dB	
		V <sub>CM</sub> Stepped from 1.2V to 1.8V	68 <b>65</b>	87			
		V <sub>CM</sub> Stepped from 0V to 1.8V	56 <b>55</b>	77			
PSRR	Power Supply Rejection Ratio	V <sup>+</sup> = 1.8V to 5.5V, V <sub>CM</sub> = 0V	66 <b>63</b>	82		dB	
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 55 dB	<b>-0.1</b>		<b>1.9</b>	V	
A <sub>V</sub>	Voltage Gain			120		dB	
V <sub>O</sub>	Output Swing High	I <sub>O</sub> = 500 µA	1.63 <b>1.60</b>	1.69		V	
		I <sub>O</sub> = 1 mA	1.46 <b>1.40</b>	1.60			
	Output Swing Low	I <sub>O</sub> = -500 µA			88	180 <b>210</b>	mV
		I <sub>O</sub> = -1 mA			180	310 <b>370</b>	

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
$I_{OUT}$	Output Current	Source $V_O = V+/2$	1.75 <b>1.5</b>	2.26		mA
		Sink $V_O = V+/2$	2.35 <b>1.75</b>	3.1		
	Propagation Delay (High to Low)	Overdrive = 10 mV		13		$\mu$ s
		Overdrive = 100 mV		4.5 <b>6.5</b> <b>8</b>		
	Propagation Delay (Low to High)	Overdrive = 10 mV		12.5		$\mu$ s
		Overdrive = 100 mV		6.6 <b>9</b> <b>10.5</b>		
$t_{rise}$	Rise Time	Overdrive = 10 mV $C_L = 30$ pF, $R_L = 1$ M $\Omega$		80		ns
		Overdrive = 100 mV $C_L = 30$ pF, $R_L = 1$ M $\Omega$		75		
$t_{fall}$	Fall Time	Overdrive = 10 mV $C_L = 30$ pF, $R_L = 1$ M $\Omega$		70		ns
		Overdrive = 100 mV $C_L = 30$ pF, $R_L = 1$ M $\Omega$		65		

## 2.7V Electrical Characteristics (Note 8)

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ , and  $V_{CM} = V+/2$ ,  $V_O = V^-$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units	
$I_S$	Supply Current	$V_{CM} = 0.3\text{V}$		605	780 <b>860</b>	nA	
		$V_{CM} = 2.4\text{V}$		815	1010 <b>1090</b>		
$V_{OS}$	Input Offset Voltage	SC70 Package	$V_{CM} = 0\text{V}$		$\pm 0.3$	$\pm 2.8$ <b><math>\pm 3.5</math></b>	mV
			$V_{CM} = 2.7\text{V}$		$\pm 0.3$	$\pm 2.2$ <b><math>\pm 2.9</math></b>	
		SOT23 Package	$V_{CM} = 0\text{V}$			$\pm 3.2$ <b><math>\pm 3.9</math></b>	
			$V_{CM} = 2.7\text{V}$			$\pm 2.5$ <b><math>\pm 3.2</math></b>	
$TCV_{OS}$	Input Offset Average Drift	(Note 7)		$\pm 1$		$\mu\text{V}/\text{C}$	
$I_B$	Input Bias Current (Note 6)	$V_{CM} = 1.8\text{V}$		-40		fA	
$I_{OS}$	Input Offset Current			20		fA	
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from 0V to 1.6V	72 <b>69</b>	90		dB	
		$V_{CM}$ Stepped from 2.1V to 2.7V	71 <b>66</b>	94			
		$V_{CM}$ Stepped from 0V to 2.7V	59 <b>58</b>	80			
PSRR	Power Supply Rejection Ratio	$V^+ = 1.8\text{V}$ to 5.5V, $V_{CM} = 0\text{V}$	66 <b>63</b>	82		dB	
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 55$ dB	<b>-0.1</b>		<b>2.8</b>	V	
$A_V$	Voltage Gain			120		dB	

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V <sub>O</sub>	Output Swing High	I <sub>O</sub> = 500 μA	2.57 <b>2.55</b>	2.62		V
		I <sub>O</sub> = 1 mA	2.47 <b>2.43</b>	2.53		
	Output Swing Low	I <sub>O</sub> = -500 μA		60	130 <b>160</b>	mV
		I <sub>O</sub> = -1 mA		120	250 <b>300</b>	
I <sub>OUT</sub>	Output Current	Source V <sub>O</sub> = V <sup>+</sup> /2	4.5 <b>3.8</b>	5.7		mA
		Sink V <sub>O</sub> = V <sup>+</sup> /2	5.6 <b>4</b>	7.5		
	Propagation Delay (High to Low)	Overdrive = 10 mV		14.5		μs
		Overdrive = 100 mV		5.8	8.5 <b>9.5</b>	
	Propagation Delay (Low to High)	Overdrive = 10 mV		15		
		Overdrive = 100 mV		7.5	10 <b>11</b>	
t <sub>rise</sub>	Rise Time	Overdrive = 10 mV C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1 MΩ		90		ns
		Overdrive = 100 mV C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1 MΩ		85		
t <sub>fall</sub>	Fall Time	Overdrive = 10 mV C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1 MΩ		85		ns
		Overdrive = 100 mV C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1 MΩ		75		

### 5V Electrical Characteristics (Note 8)

Unless otherwise specified, all limits are guaranteed for T<sub>A</sub> = 25°C, V<sup>+</sup> = 5V, V<sup>-</sup> = 0V, and V<sub>CM</sub> = V<sup>+</sup>/2, V<sub>O</sub> = V<sup>-</sup>. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units	
I <sub>S</sub>	Supply Current	V <sub>CM</sub> = 0.3V		612	790 <b>970</b>	nA	
		V <sub>CM</sub> = 4.7V		825	1030 <b>1230</b>		
V <sub>OS</sub>	Input Offset Voltage	SC70 Package	V <sub>CM</sub> = 0V		±0.3	±3 <b>±3.7</b>	mV
			V <sub>CM</sub> = 5V			±2.3 <b>±3.0</b>	
		SOT23 Package	V <sub>CM</sub> = 0V			±3.4 <b>±4.1</b>	
			V <sub>CM</sub> = 5V			±2.6 <b>±3.3</b>	
TCV <sub>OS</sub>	Input Offset Average Drift	(Note 7)		±1		μV/C	
I <sub>B</sub>	Input Bias Current (Note 6)	V <sub>CM</sub> = 4.5V		-400		fA	
I <sub>OS</sub>	Input Offset Current			20		fA	

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from 0V to 3.9V	72 <b>69</b>	98		dB
		$V_{CM}$ Stepped from 4.4V to 5V	73 <b>70</b>	92		
		$V_{CM}$ Stepped from 0V to 5V	64 <b>63</b>	82		
PSRR	Power Supply Rejection Ratio	$V^+ = 1.8V$ to 5.5V, $V_{CM} = 0V$	66 <b>63</b>	82		dB
CMVR	Input Common-Mode Voltage Range	CMRR $\geq$ 55 dB	<b>-0.1</b>		<b>5.1</b>	V
$A_V$	Voltage Gain			120		dB
$V_O$	Output Swing High	$I_O = 500 \mu A$	4.9 <b>4.88</b>	4.94		V
		$I_O = 1 \text{ mA}$	4.82 <b>4.79</b>	4.89		
	Output Swing Low	$I_O = -500 \mu A$			43 <b>110</b>	mV
		$I_O = -1 \text{ mA}$			88 <b>170</b> <b>200</b>	
$I_{OUT}$	Output Current	Source $V_O = V^+/2$	13.0 <b>9.0</b>	17		mA
		Sink $V_O = V^+/2$	14.5 <b>10.5</b>	19		
	Propagation Delay (High to Low)	Overdrive = 10 mV		18		$\mu s$
		Overdrive = 100 mV		7.7	13.5 <b>15</b>	
	Propagation Delay (Low to High)	Overdrive = 10 mV		30		$\mu s$
		Overdrive = 100 mV		12	15 <b>17.5</b>	
$t_{rise}$	Rise Time	Overdrive = 10 mV $C_L = 30 \text{ pF}$ , $R_L = 1 \text{ M}\Omega$		100		ns
		Overdrive = 100 mV $C_L = 30 \text{ pF}$ , $R_L = 1 \text{ M}\Omega$		100		
$t_{fall}$	Fall Time	Overdrive = 10 mV $C_L = 30 \text{ pF}$ , $R_L = 1 \text{ M}\Omega$		115		ns
		Overdrive = 100 mV $C_L = 30 \text{ pF}$ , $R_L = 1 \text{ M}\Omega$		95		
		$C_L = 30 \text{ pF}$ , $R_L = 1 \text{ M}\Omega$				

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

**Note 2:** Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

**Note 3:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC board.

**Note 4:** Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

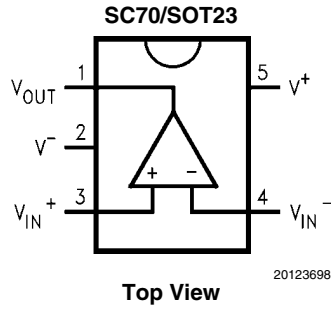
**Note 5:** Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

**Note 6:** Positive current corresponds to current flowing into the device.

**Note 7:** Offset voltage average drift determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

**Note 8:** Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

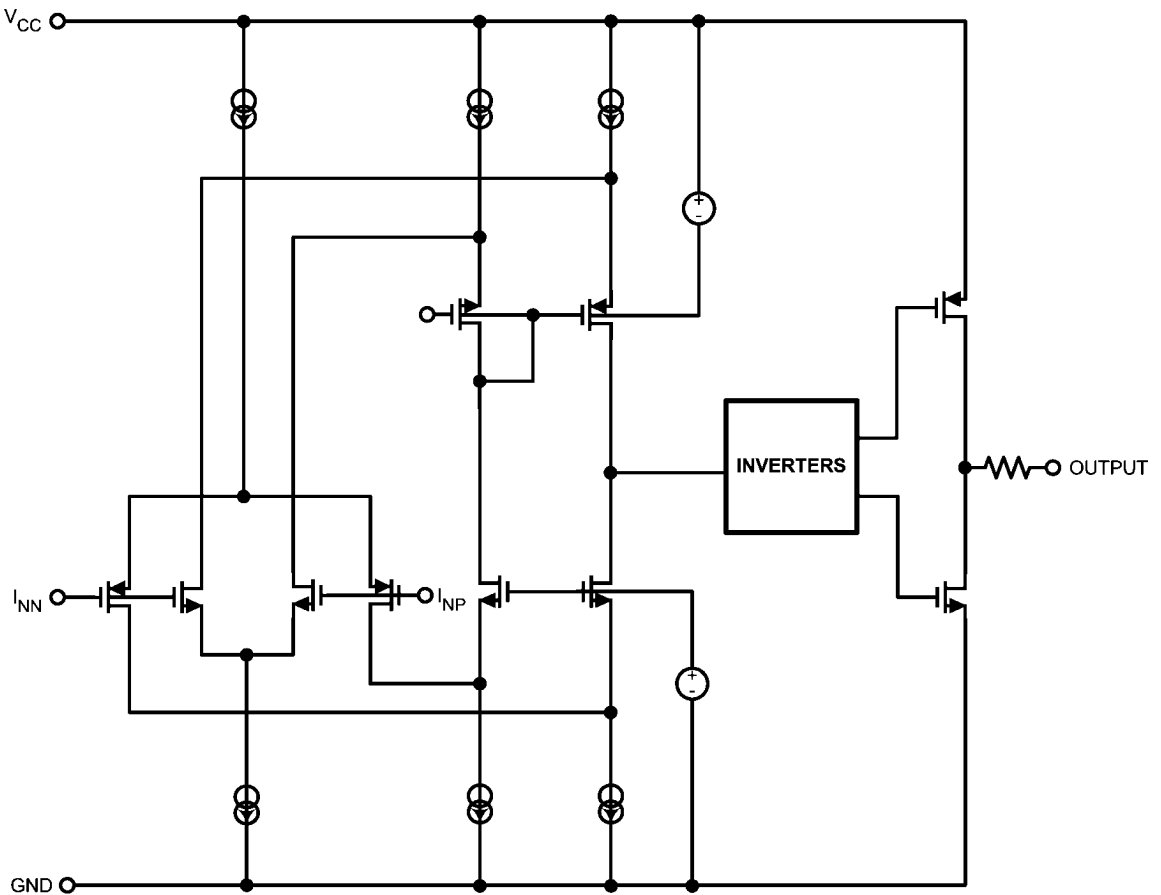
### Connection Diagram



### Ordering Information

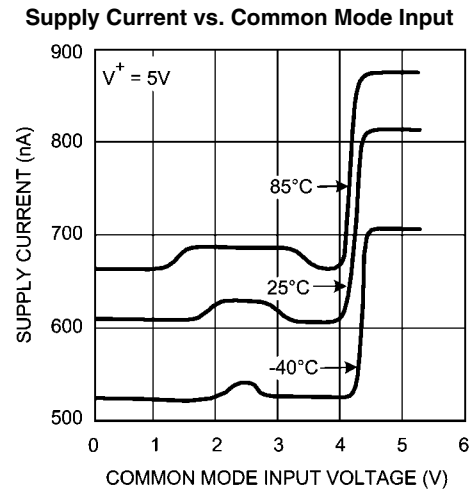
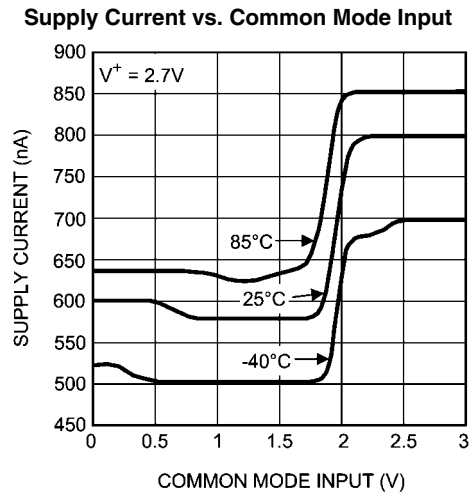
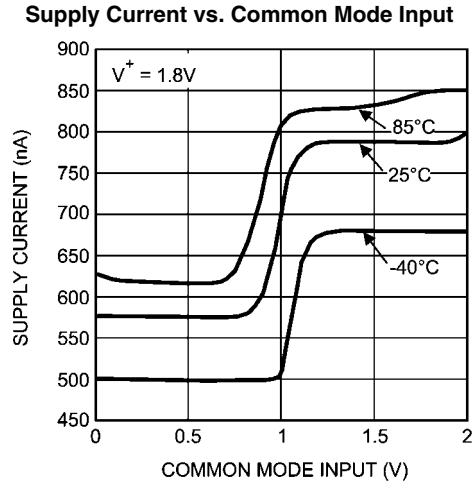
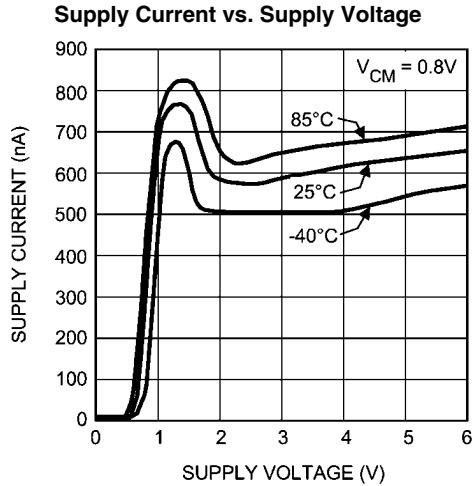
Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LPV7215MF	C30A	1k Units Tape and Reel	MF05A
	LPV7215MFX		3k Units Tape and Reel	
5-Pin SC70	LPV7215MG	C37	1k Units Tape and Reel	MAA05A
	LPV7215MGX		3k Units Tape and Reel	

### Simplified Schematic Diagram

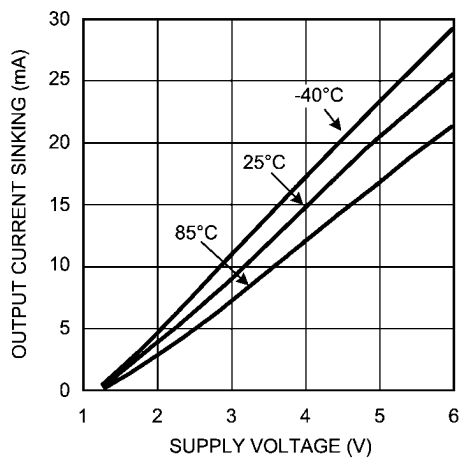


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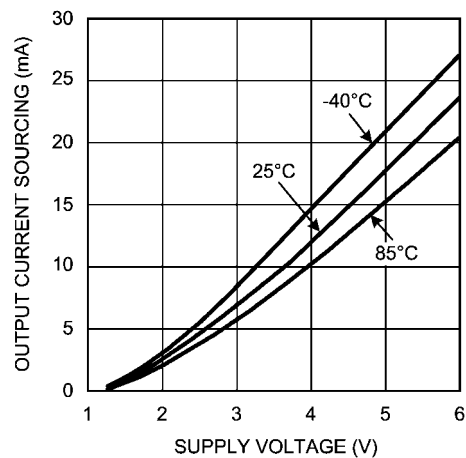
**Typical Performance Characteristics** At  $T_J = 25^\circ\text{C}$  unless otherwise specified.

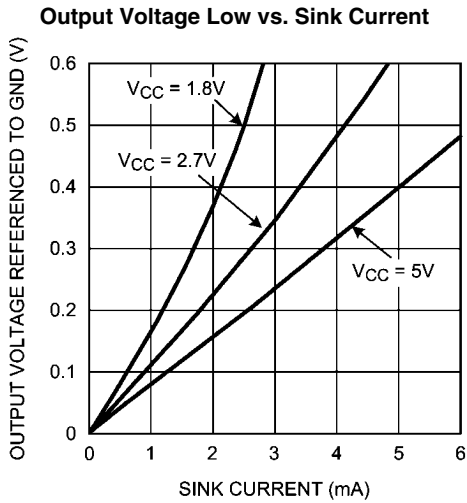


**Short Circuit Sinking Current vs. Supply Voltage**

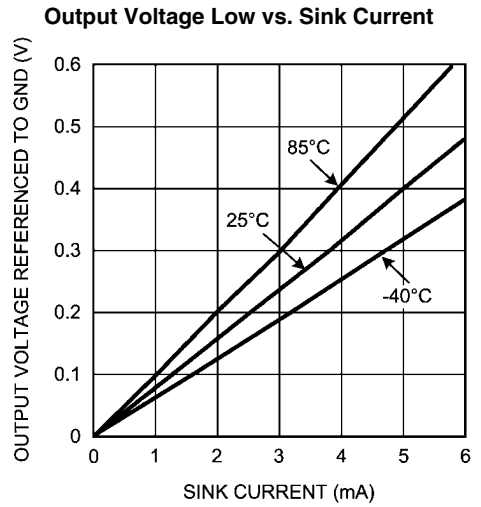


**Short Circuit Sourcing Current vs. Supply Voltage**

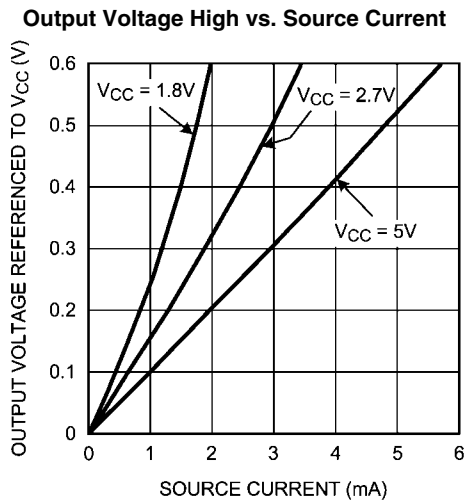




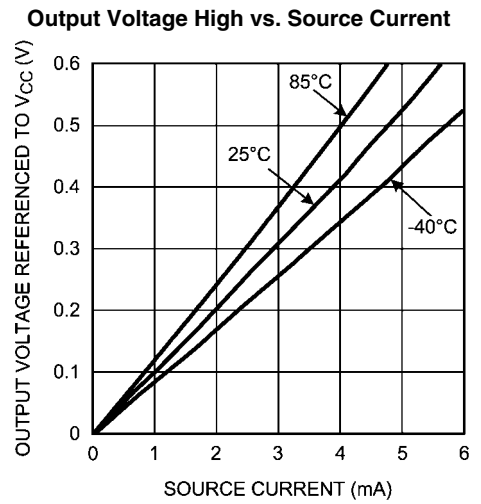
20123650



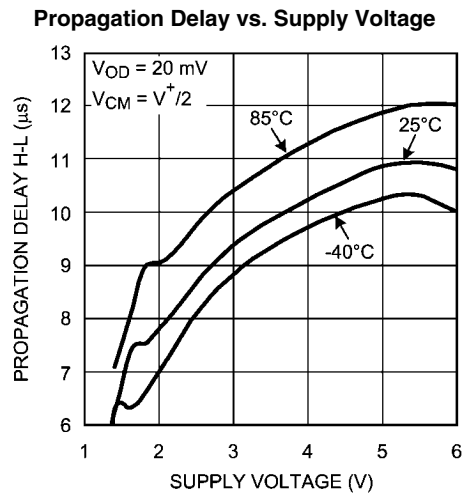
20123651



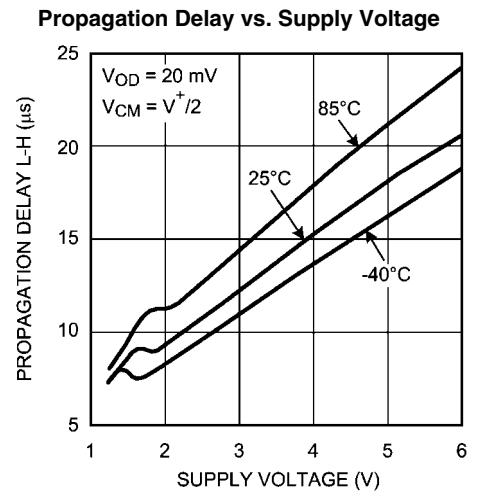
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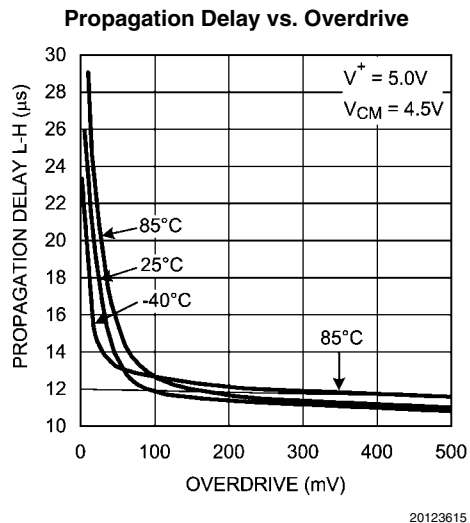
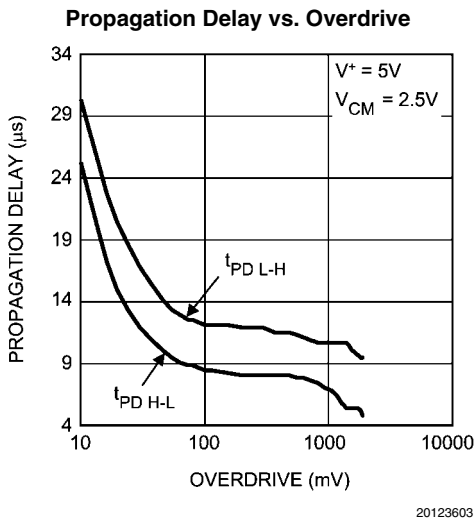
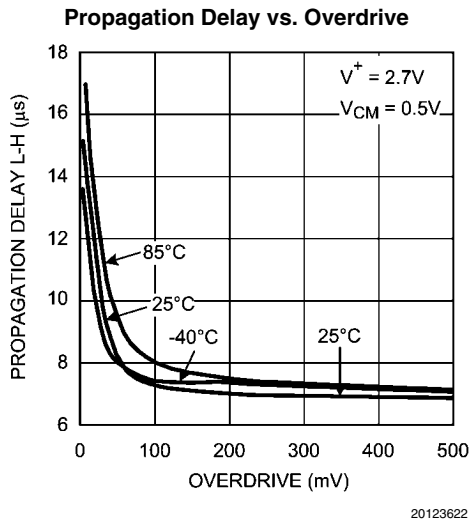
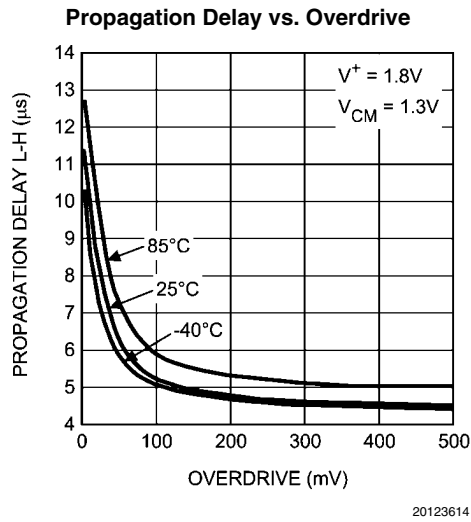
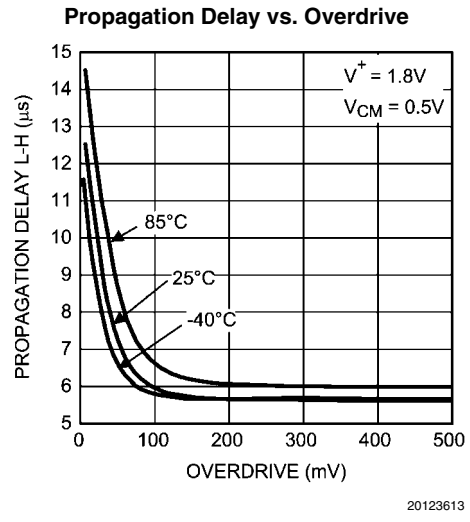
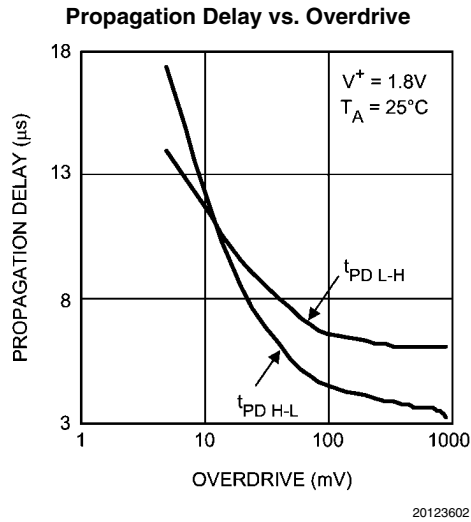


20123611

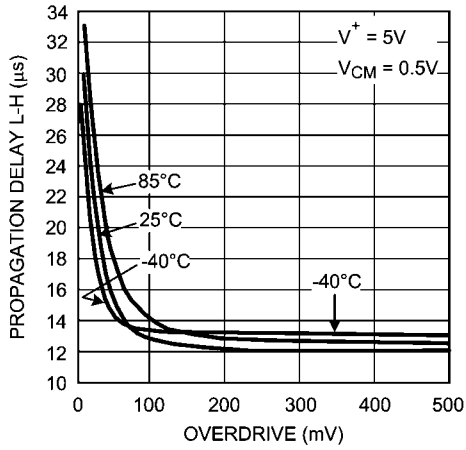


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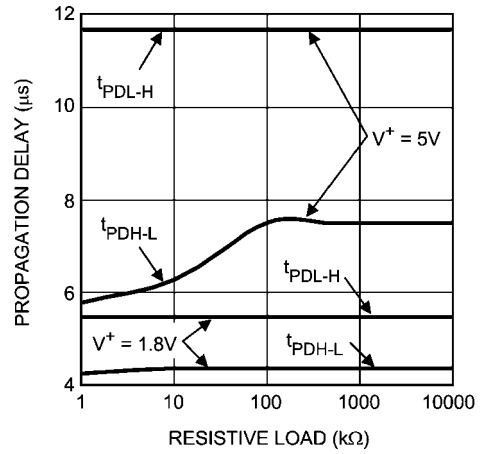


Propagation Delay vs. Overdrive



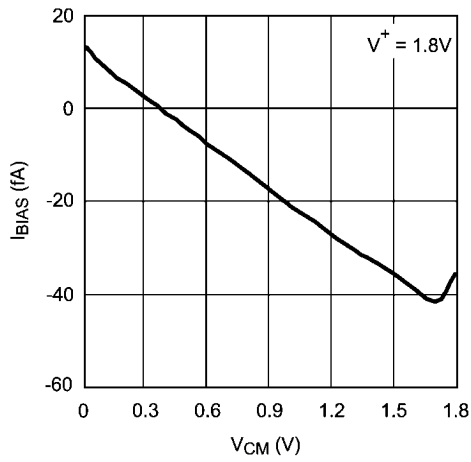
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Propagation Delay vs. Resistive Load



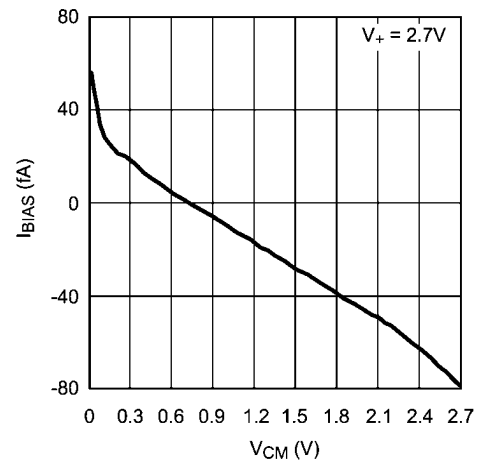
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I<sub>BIAS</sub> vs. V<sub>CM</sub>



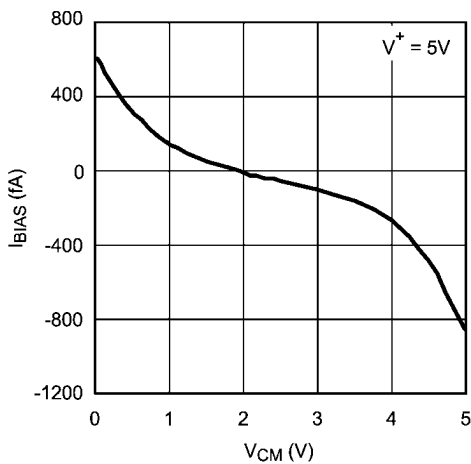
20123620

I<sub>BIAS</sub> vs. V<sub>CM</sub>



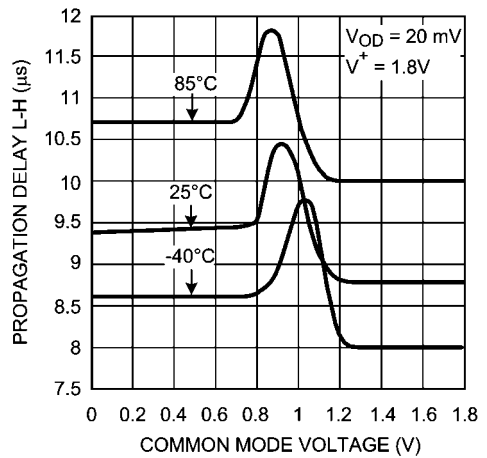
20123618

I<sub>BIAS</sub> vs. V<sub>CM</sub>



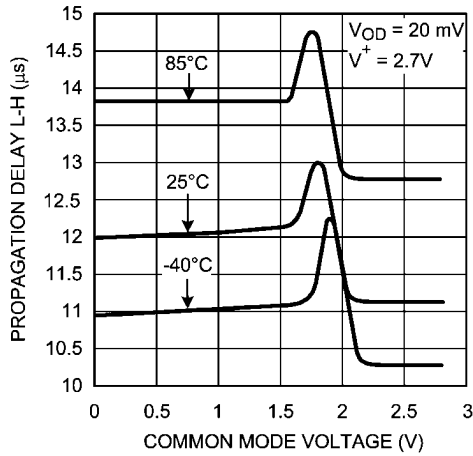
20123619

Propagation Delay vs. Common Mode Input



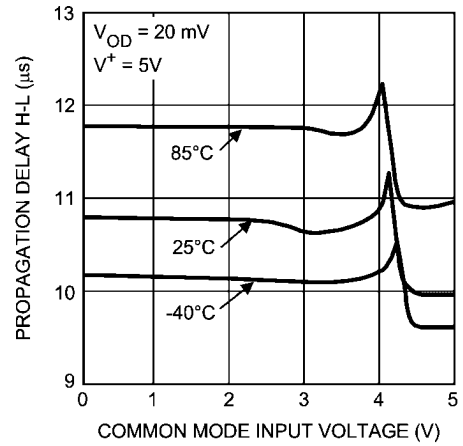
20123624

Propagation Delay vs. Common Mode Input



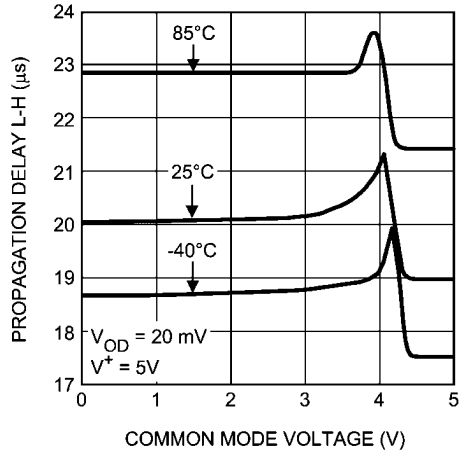
20123625

Propagation Delay vs. Common Mode Input



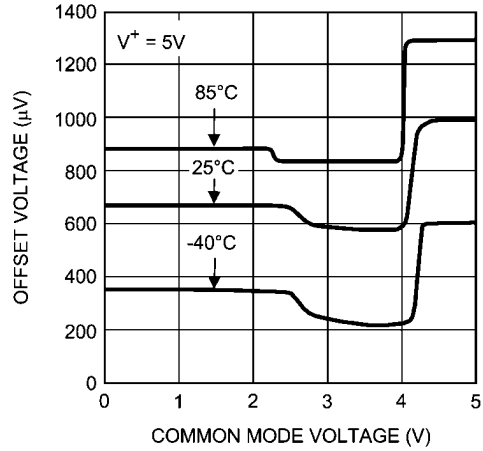
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Propagation Delay vs. Common Mode Input



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Offset Voltage vs. Common Mode Input



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## Application Information

Low supply current and fast propagation delay distinguish the LPV7215 from other low power comparators.

### INPUT STAGE

The LPV7215 has rail-to-rail input common mode voltage range. It can operate at any differential input voltage within this limit as long as the differential voltage is greater than zero. A differential input of zero volts may result in oscillation.

The differential input stage of the comparator is a pair of PMOS and NMOS transistors, therefore, no current flows into the device. The input bias current measured is the leakage current in the MOS transistors and input protection diodes. This low bias current allows the comparator to interface with a variety of circuitry and devices with minimal concern about matching the input resistances.

The input to the comparator is protected from excessive voltage by internal ESD diodes connected to both supply rails. This protects the circuit from both ESD events, as well as signals that significantly exceed the supply voltages. When this occurs the ESD protection diodes will become forward biased and will draw current into these structures, resulting in no input current to the terminals of the comparator. Until this occurs, there is essentially no input current to the diodes. As a result, placing a large resistor in series with an input that may be exposed to large voltages, will limit the input current but have no other noticeable effect.

### OUTPUT STAGE

The LPV7215 has a MOS push-pull rail-to-rail output stage. The push-pull transistor configuration of the output keeps the total system power consumption to a minimum. The only current consumed by the LPV7215 is the less than 1  $\mu\text{A}$  supply current and the current going directly into the load. No power is wasted through the pull-up resistor when the output is low. The output stage is specifically designed with deadtime between the time when one transistor is turned off and the other is turned on (break-before-make) in order to minimize shoot through currents. The internal logic controls the break-before-make timing of the output transistors. The break-before-make timing of the output transistors. The break-before-make delay varies with temperature and power condition.

### OUTPUT CURRENT

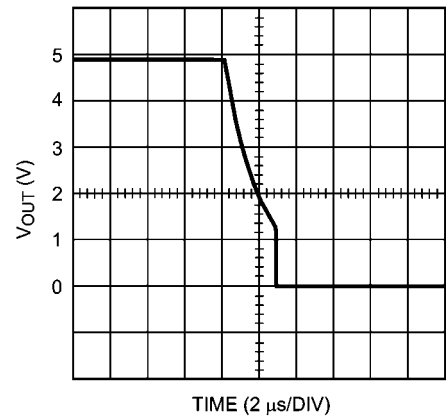
Even though the LPV7215 uses less than 1  $\mu\text{A}$  supply current, the outputs are able to drive very large currents. The LPV7215 can source up to 17 mA and can sink up to 19 mA, when operated at 5V supply. This large current handling capability allows driving heavy loads directly.

### RESPONSE TIME

Depending upon the amount of overdrive, the propagation delay will be typically 6 to 30  $\mu\text{s}$ . The curves showing propagation delay vs. overdrive in the "Typical Characteristics" section shows the delay time when the input is preset with 100 mV across the inputs and then is driven the other way by 10 mV to 500 mV.

The output signal can show a step during switching depending on the load. A fast RC time constant due to both small capacitive and resistive loads will show a significant step in the output signal. A slow RC time constant due to either a large resistive or capacitive load will have a clipped corner on the output signal. The step is observed more prominently during a falling transition from high to low.

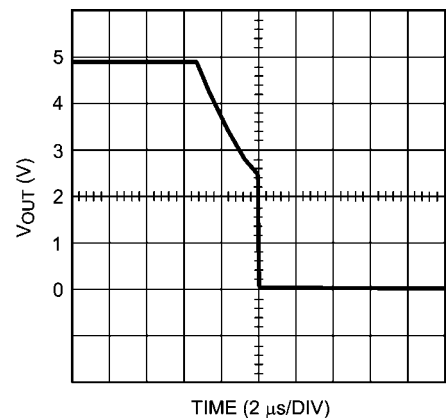
The plot in *Figure 1* shows the output for single 5V supply with a 100 k $\Omega$  resistor. The step is at 1.3V.



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**FIGURE 1. Output Signal without Capacitive Load**

The plot in *Figure 2* shows the output signal when a 20 pF capacitor is added as a load. The step is at about 2.5V.



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**FIGURE 2. Output Signal with 20 pF Load**

**CAPACITIVE AND RESISTIVE LOADS**

The propagation delay is not affected by capacitive loads at the output of the LPV7215. However, resistive loads slightly affect the propagation delay on the falling edge by a reduction of almost 2 μs depending on the load resistance value.

**NOISE**

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is that the output may oscillate between high and low when the differential input is near zero. The exceptionally high gain of this comparator, 120 dB, eliminates this problem. Less than 1 μV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See section on adding hysteresis.)

**LAYOUT/BYPASS CAPACITORS**

Proper grounding and the use of a ground plane will help to ensure the specified performance of the LPV7215. Minimizing trace lengths, reducing unwanted parasitic capacitance and using surface-mount components will also help.

Comparators are very sensitive to input noise. To minimize supply noise, power supplies should be capacitively decoupled by a 0.01 μF ceramic capacitor in parallel with a 10 μF electrolytic capacitor.

**HYSTERESIS**

In order to improve propagation delay when low overdrive is needed hysteresis can be added.

**INVERTING COMPARATOR WITH HYSTERESIS**

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V+ of the comparator as shown in Figure 3. When VIN at the inverting input is less than VA, the voltage at the non-inverting input of the comparator (VIN < VA), the output voltage is high (for simplicity assume VO switches as high as V+). The three network resistors can be represented as R1//R3 in series with R2.

The lower input trip voltage VA1 is defined as

$$V_{A1} = V_{CC}R_2 / ((R_1//R_3) + R_2)$$

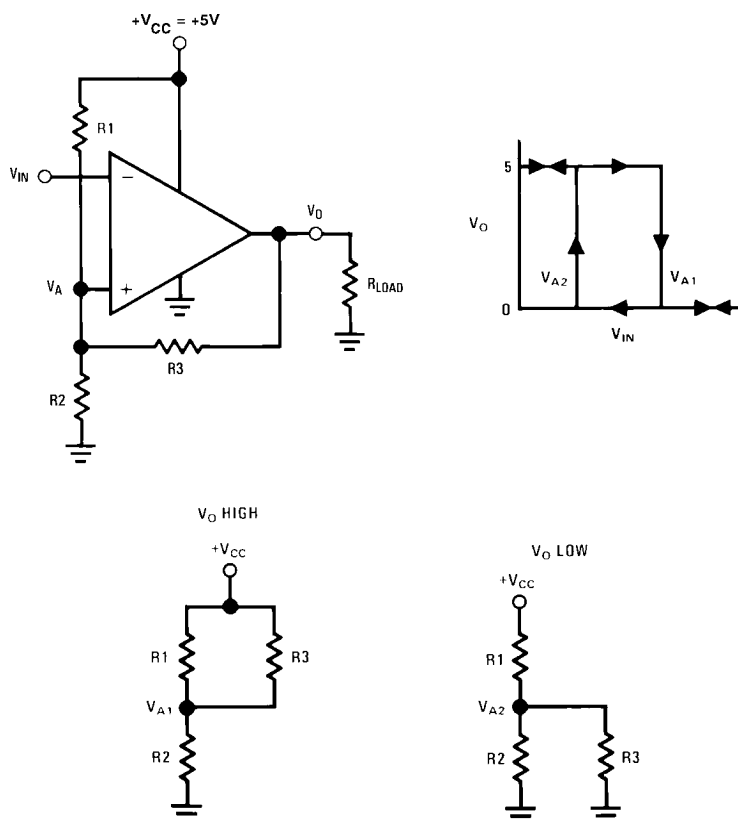
When VIN is greater than VA, the output voltage is low or very close to ground. In this case the three network resistors can be presented as R2//R3 in series with R1.

The upper trip voltage VA2 is defined as

$$V_{A2} = V_{CC} (R_2//R_3) / ((R_1 + (R_2//R_3))$$

The total hysteresis provided by the network is defined as  $\Delta V_A = V_{A1} - V_{A2}$

$$\Delta V_A = \frac{+V_{CC}R_1R_2}{R_1R_2 + R_1R_3 + R_2R_3}$$



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**FIGURE 3. Inverting Comparator with Hysteresis**

**NON-INVERTING COMPARATOR WITH HYSTERESIS**

A non-inverting comparator with hysteresis requires a two-resistor network, and a voltage reference ( $V_{REF}$ ) at the inverting input. When  $V_{IN}$  is low, the output is also low. For the output to switch from low to high,  $V_{IN}$  must rise up to  $V_{IN1}$  where  $V_{IN1}$  is calculated by.

$$V_{IN1} = \frac{V_{REF} (R_1 + R_2)}{R_2}$$

As soon as  $V_O$  switches to  $V_{CC}$ ,  $V_A$  will step to a value greater than  $V_{REF}$ , which is given by

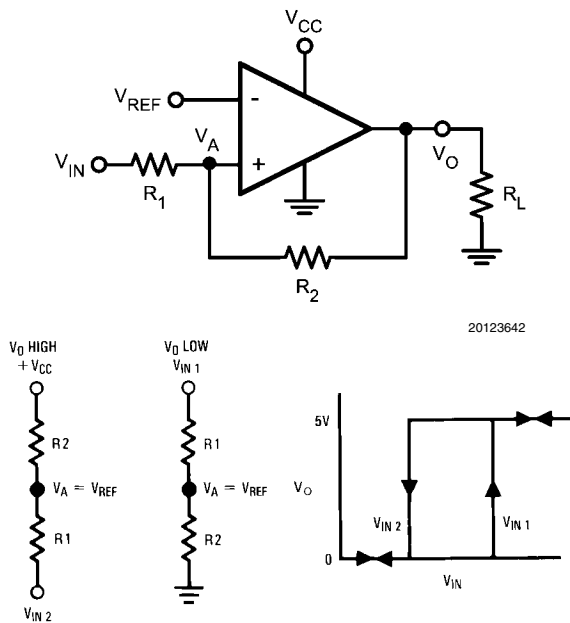
$$V_A = V_{IN} + \frac{(V_{CC}-V_{IN1}) R_1}{R_1 + R_2}$$

To make the comparator switch back to its low state,  $V_{IN}$  must equal  $V_{REF}$  before  $V_A$  will again equal  $V_{REF}$ .  $V_{IN2}$  can be calculated by

$$V_{IN2} = \frac{V_{REF} (R_1 + R_2) - V_{CC} R_1}{R_2}$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ .

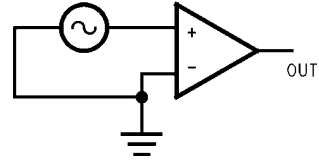
$$\Delta V_{IN} = V_{CC} R_1 / R_2$$



**FIGURE 4. Non-Inverting Comparator with Hysteresis**

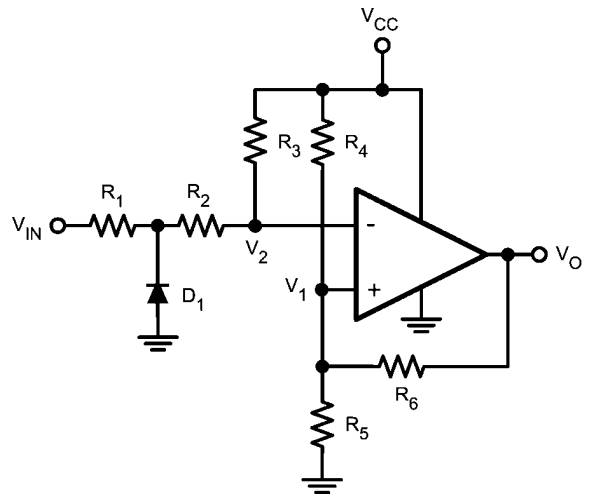
**ZERO CROSSING DETECTOR**

In a zero crossing detector circuit, the inverting input is connected to ground and the non-inverting input is connected to a 100 mV<sub>PP</sub> AC signal. As the signal at the non-inverting input crosses 0V, the comparator's output changes state.



**FIGURE 5. Zero Crossing Detector**

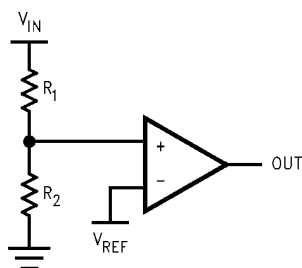
To improve switching times and to center the input threshold to ground a small amount of positive feedback is added to the circuit. The voltage divider,  $R_4$  and  $R_5$ , establishes a reference voltage,  $V_1$ , at the positive input. By making the series resistance,  $R_1$  plus  $R_2$  equal to  $R_5$ , the switching condition,  $V_1 = V_2$ , will be satisfied when  $V_{IN} = 0$ . The positive feedback resistor,  $R_6$ , is made very large with respect to  $R_5$  ( $R_6 = 2000 R_5$ ). The resultant hysteresis established by this network is very small ( $\Delta V_1 < 10$  mV) but it is sufficient to insure rapid output voltage transitions. Diode  $D_1$  is used to insure that the inverting input terminal of the comparator never goes below approximately  $-100$  mV. As the input terminal goes negative,  $D_1$  will forward bias, clamping the node between  $R_1$  and  $R_2$  to approximately  $-700$  mV. This sets up a voltage divider with  $R_2$  and  $R_3$  preventing  $V_2$  from going below ground. The maximum negative input overdrive is limited by the current handling ability of  $D_1$ .



**FIGURE 6. Zero Crossing Detector with Positive Feedback**

**THRESHOLD DETECTOR**

Instead of tying the inverting input to 0V, the inverting input can be tied to a reference voltage. As the input on the non-inverting input passes the  $V_{REF}$  threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

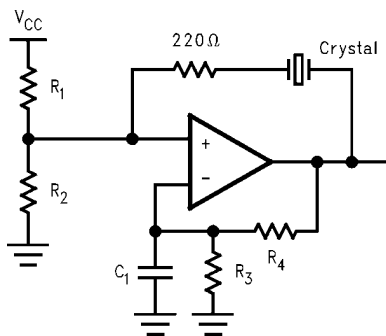


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**FIGURE 7. Threshold Detector**

**CRYSTAL OSCILLATOR**

A simple crystal oscillator using the LPV7215 is shown in *Figure 8*. Resistors  $R_1$  and  $R_2$  set the bias point at the comparator's non-inverting input. Resistors  $R_3$  and  $R_4$  and capacitor  $C_1$  set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.

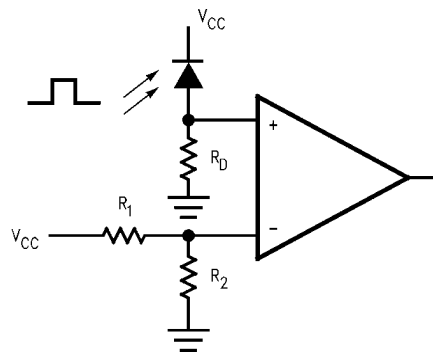


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**FIGURE 8. Crystal Oscillator**

**IR RECEIVER**

The LPV7215 can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across  $R_D$ . When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions.

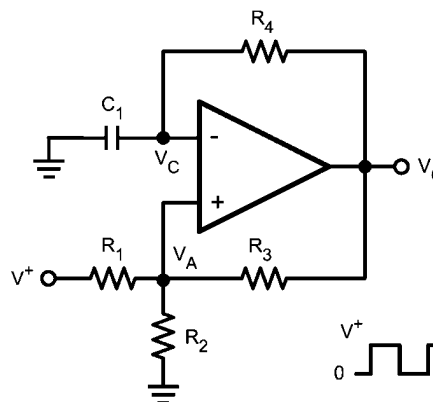


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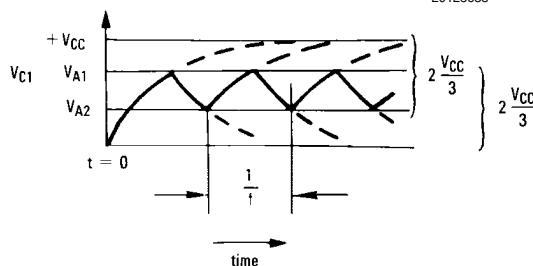
**FIGURE 9. IR Receiver**

**SQUARE WAVE GENERATOR**

A typical application for a comparator is as a square wave oscillator. The circuit in *Figure 10* generates a square wave whose period is set by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ . The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.



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**FIGURE 10. Square Wave Oscillator**

Consider the output of *Figure 10* to be high to analyze the circuit. That implies that the inverted input ( $V_C$ ) is lower than the non-inverting input ( $V_A$ ). This causes the  $C_1$  to be charged through  $R_4$ , and the voltage  $V_C$  increases until it is equal to the non-inverting input. The value of  $V_A$  at this point is

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3}$$

If  $R_1 = R_2 = R_3$  then  $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of  $V_A$  at this point is

$$V_{A2} = \frac{V_{CC} (R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)}$$

If  $R_1 = R_2 = R_3$  then  $V_{A2} = V_{CC}/3$

The capacitor  $C_1$  now discharges through  $R_4$ , and the voltage  $V_C$  decreases until it is equal to  $V_{A2}$ , at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge  $C_1$  from  $2V_{CC}/3$  to  $V_{CC}/3$ , which is given by  $R_4 C_1 \cdot \ln 2$ . Hence the formula for the frequency is:

$$F = 1 / (2 \cdot R_4 \cdot C_1 \cdot \ln 2)$$

**WINDOW DETECTOR**

A window detector monitors the input signal to determine if it falls between two voltage levels.

The comparator outputs A and B are high only when

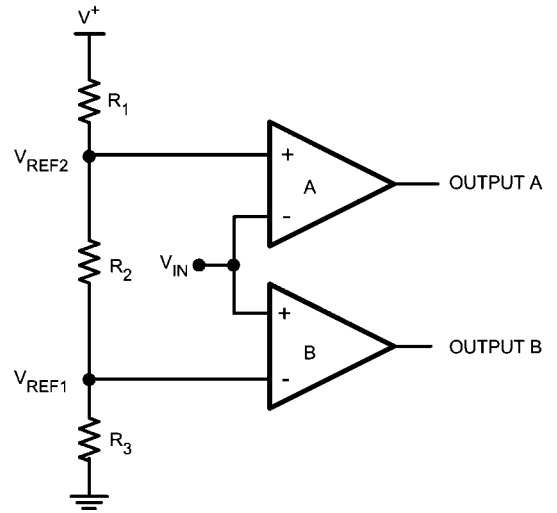
$V_{REF1} < V_{IN} < V_{REF2}$  "or within the window."

where these are defined as

$$V_{REF1} = R_3 / (R_1 + R_2 + R_3) \cdot V^+$$

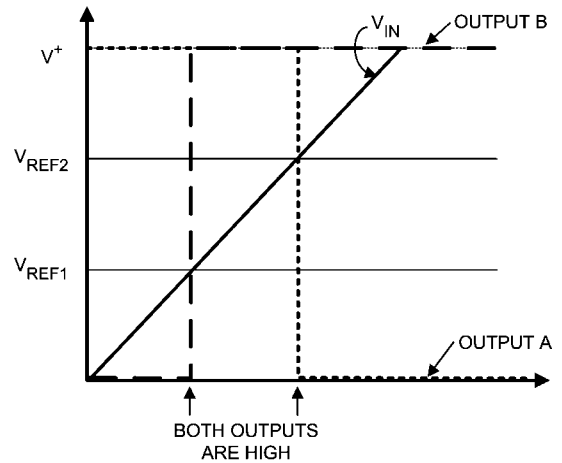
$$V_{REF2} = (R_2 + R_3) / (R_1 + R_2 + R_3) \cdot V^+$$

Others names for window detectors are: threshold detector, level detectors, and amplitude trigger or detector.



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**FIGURE 11. Window Detector**

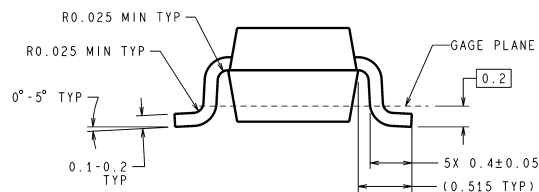
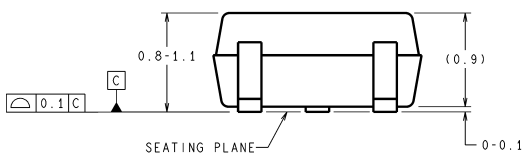
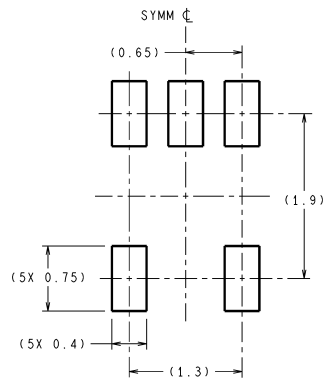
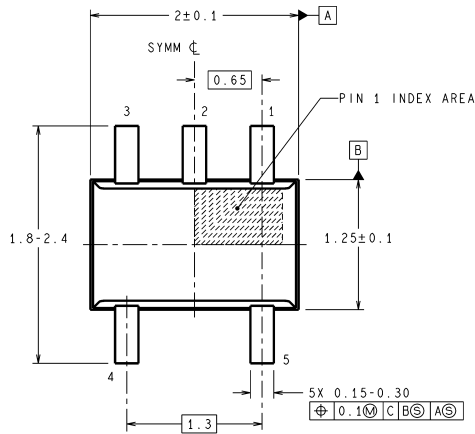


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**FIGURE 12. Window Detector Output Signal**



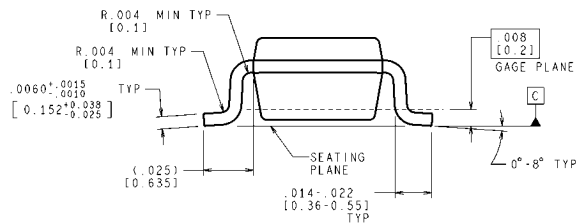
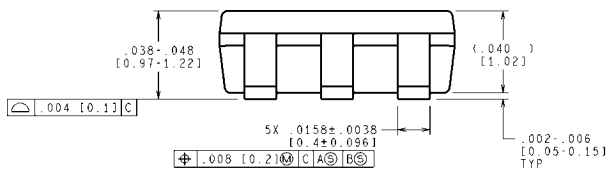
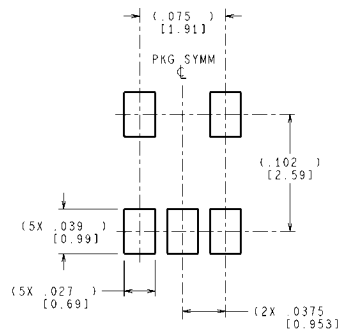
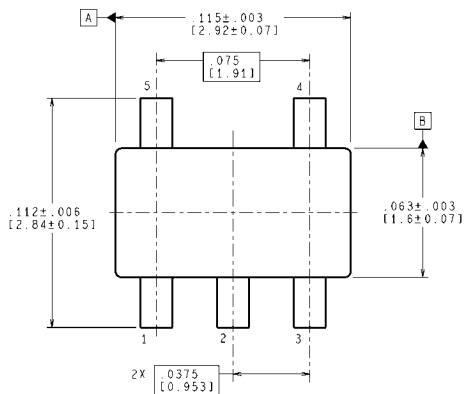
**Physical Dimensions** inches (millimeters) unless otherwise noted



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MAA05A (Rev D)

**5-Pin SC70  
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Ethernet	<a href="http://www.national.com/ethernet">www.national.com/ethernet</a>	Packaging	<a href="http://www.national.com/packaging">www.national.com/packaging</a>
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