FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13723-6E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90390 Series

MB90394HA/F394H/F394HA/ MB90V390H/V390HA/V390HB

■ DESCRIPTION

The MB90390-series with up to five FULL-CAN* interfaces and Flash ROM is especially designed for automotive and industrial applications. Its main feature are up to five on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35 µm CMOS technology, Fujitsu now offers on-chip Flash-ROM program memory up to 512 Kbytes. An internal voltage booster removes the necessity for a second programming voltage.

An on board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features 6 Stepper Motor Controllers with slew rate controlled high current outputs.

Furthermore it features an 8-channel Output Compare Unit and a 6-channel Input Capture Unit with two separate 16-bit free running timers. Up to 4 UARTs constitute additional functionality for communication purposes.

* : Controller Area Network (CAN) - License of Robert Bosch GmbH

Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 42 ns instruction execution time)
- New 0.35 µm CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- Up to five FULL-CAN interfaces; conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 8 external interrupts)
- EI^{2}OS - Automatic transfer function indep.of CPU; 16 channels of intelligent I/O Services
- 18-bit Time-base counter
- Watchdog Timer
- 2 full duplex UARTs; support 10.4 Kbps (USA standard)
- Up to 2 full duplex UARTs (LIN/SCI)
- Serial I/O : 1 channel for synchronous data transfer
- Optional I^{2}C* with 400 Kbps
- A/D Converter : 15 channels analog inputs (Resolution 10 bits or 8 bits)
- 16-bit reload timer × 2 channels
- ICU (Input capture) 16-bit × 6 channels (2 input pins are shared with OCU outputs)
- OCU (Output capture) 16-bit × 8 channels (2 output pins are shared with ICU input pins)
- 16-bit free running timer × 2 channels (FRT0 : ICU 0/1, OCU 0/1/2/3, FRT1 : ICU 2/3/4/5, OCU 4/5/6/7)
- 8/16-bit Programmable Pulse Generator 6 channels × 16-bit/12 channels × 8-bit
- Stepping Motor Controller 6 channels with slew rate controlled high current outputs
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
- Program Patch Function
- Fast Interrupt processing
- Low Power Consumption mode
  Sleep mode
  Timebase timer mode
  Stop mode
  CPU intermittent mode
- Sound Generator
- Real Time Watch Timer
- Built-In Clock Modulation circuit
- Programmable input levels (Automotive Hysteresis / CMOS Hysteresis, initial level is Automotive Hysteresis)
- Package : 120-pin plastic LQFP

* : Purchase of Fujitsu I^{2}C components conveys a license under the Philips I^{2}C Patent Rights to use, these components in an I^{2}C system provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.

■ PRODUCT LINEUP

Parameter \ Part Number	MB90394HA	MB90F394H MB90F394HA	MB90V390H	MB90V390HA/ MB90V390HB
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)			
ROM	ROM memory 384 Kbytes	Boot-block Flash memory 384 Kbytes Hard-wired reset vector, points to address $FFA000_H$	External	
RAM	10 Kbytes		16 Kbytes	30 Kbytes
Emulator-specific power supply*1	—		Yes	
Technology	0.35 µm CMOS with on-chip voltage regulator for internal power supply	0.35 µm CMOS with on-chip voltage regulator for internal power supply + Flash memory with On-chip charge pump for programming voltage	0.35 µm CMOS with on-chip voltage regulator for internal power supply	
Operating voltage range	3.5 V to 5.5 V (4.0 V to 5.5 V: during Flash programming and erasing, 4.5 V to 5.5 V: if A/D Converter is used)		5 V ± 10%	
Temperature range	−40 °C to +85 °C		—	
Package	LQFP-120		PGA-299	
UART (2 channels)	Full duplex double buffer Supports asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 24 MHz			
UART (LIN/SCI)	1 channel			2 channels
I^2C (400 Kbps)	1 channel	—	1 channel	
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 24 MHz			
A/D Converter	15 input channels 10-bit or 8-bit resolution Conversion time : Min 4.9 µs include sample time (per one channel, depends on machine clock frequency)			
16-bit Reload Timer (2 channels)	Operation clock frequency : $fsys/2^1$, $fsys/2^3$, $fsys/2^5$ (fsys = System clock frequency) Supports External Event Count function			

(Continued)

Part Number / Parameter	MB90394HA	MB90F394H MB90F394HA	MB90V390H	MB90V390HA/ MB90V390HB
Watch Timer	Directly operates with the oscillation clock Read/Write accessible Second/Minute/Hour registers Signals interrupts			
16-bit I/O Timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = System clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 2/3/4/5, OCU 4/5/6/7			
16-bit Output Compare (8 channels)	Signals an interrupt when a match with 16-bit I/O Timer Eight 16-bit compare registers. A pair of compare registers can be used to generate an output signal. OCU 6/7 outputs are shared with ICU 3/5 inputs			
16-bit Input Capture (6 channels)	Rising edge, falling edge or rising & falling edge sensitive Six 16-bit Capture registers Signals an interrupt upon external event ICU 3/5 inputs are shared with OCU 6/7 outputs			
8/16-bit Programmable Pulse Generator (6 channels)	Supports 8-bit and 16-bit operation modes Twelve 8-bit reload counters Twelve 8-bit reload registers for L pulse width Twelve 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 102.4 µs at fosc = 5 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)			
CAN Interface (up to 5 channels)	2 channels		5 channels	
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full-bit compare/Full-bit mask/Two partial bit masks Supports up to 1 Mbps MB90F394H, MB90V390H, MB90V390HA : Do not use CAN message buffer RAM and clock modulator at the same time.			
Stepping Motor Controller (6 channels)	Four high current outputs with controlled slew rate for each channel Synchronized two 8-bit PWM's for each channel			
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive			
Sound Generator	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM frequency : 62.5 kHz, 31.2 kHz, 15.6 kHz, 7.8 kHz at System clock = 16 MHz Tone frequency : PWM frequency/2/ (reload value + 1)			

(Continued)

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Parameter \ Part Number	MB90394HA	MB90F394H MB90F394HA	MB90V390H	MB90V390HA/ MB90V390HB
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal Port-wise programmable as CMOS Hysteresis or automotive Hysteresis inputs (default)			
Clock Modulator	Spread spectrum clock modulator for reducing electromagnetic emissions. Frequency and Phase Modulation modes. MB90F394H : Do not use frequency modulation. MB90F394H, MB90V390H, MB90V390HA : Do not use CAN message buffer RAM and clock modulator at the same time.			
Flash Memory	—	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years*3 Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage	—	

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

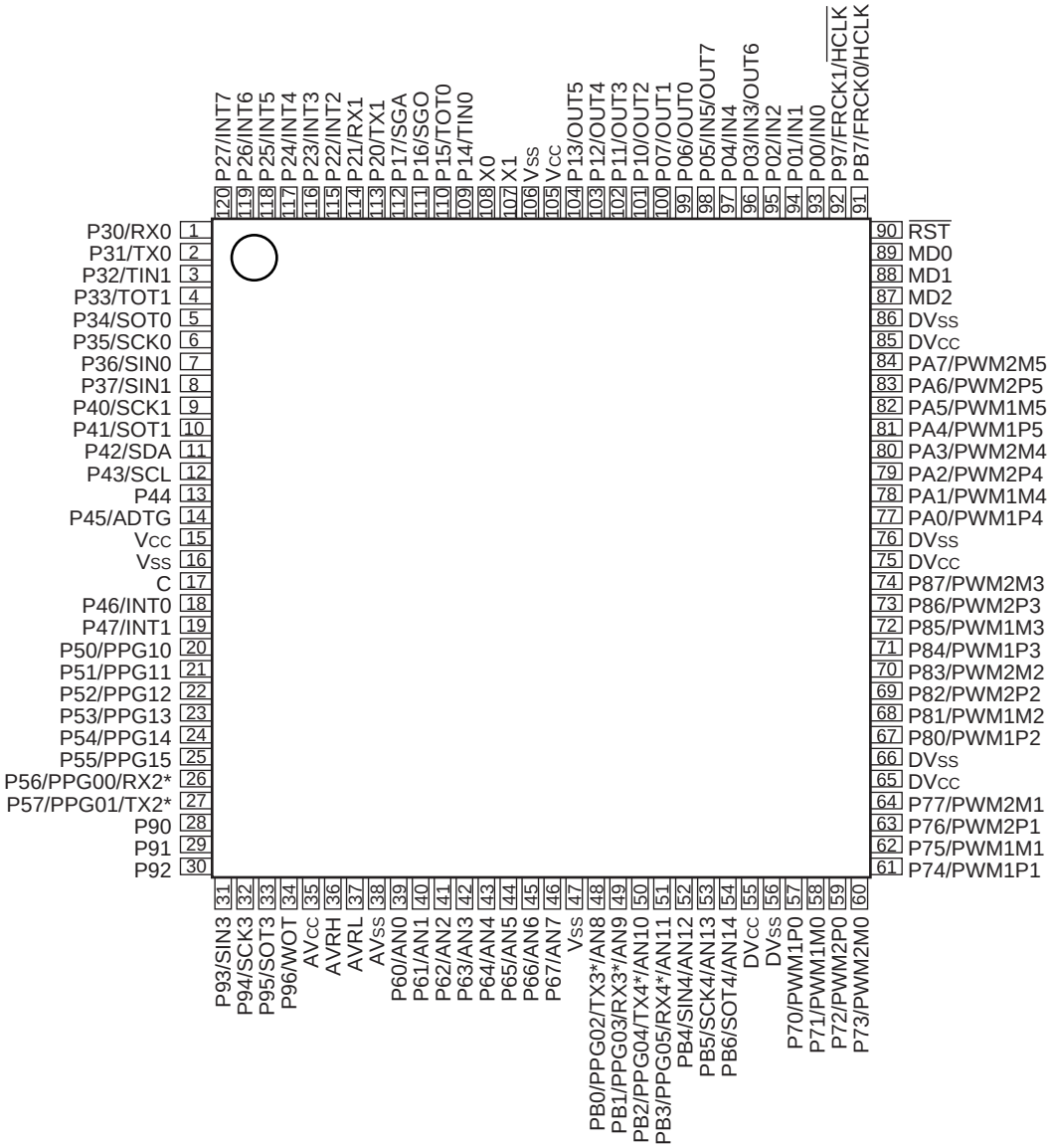
*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

*3 : This value comes from the technology qualification (using Arrehenius equation to translate high temperature measurements into normalized value at +85 °C)

■ PIN ASSIGNMENTS

• MB90V390H

(TOP VIEW)

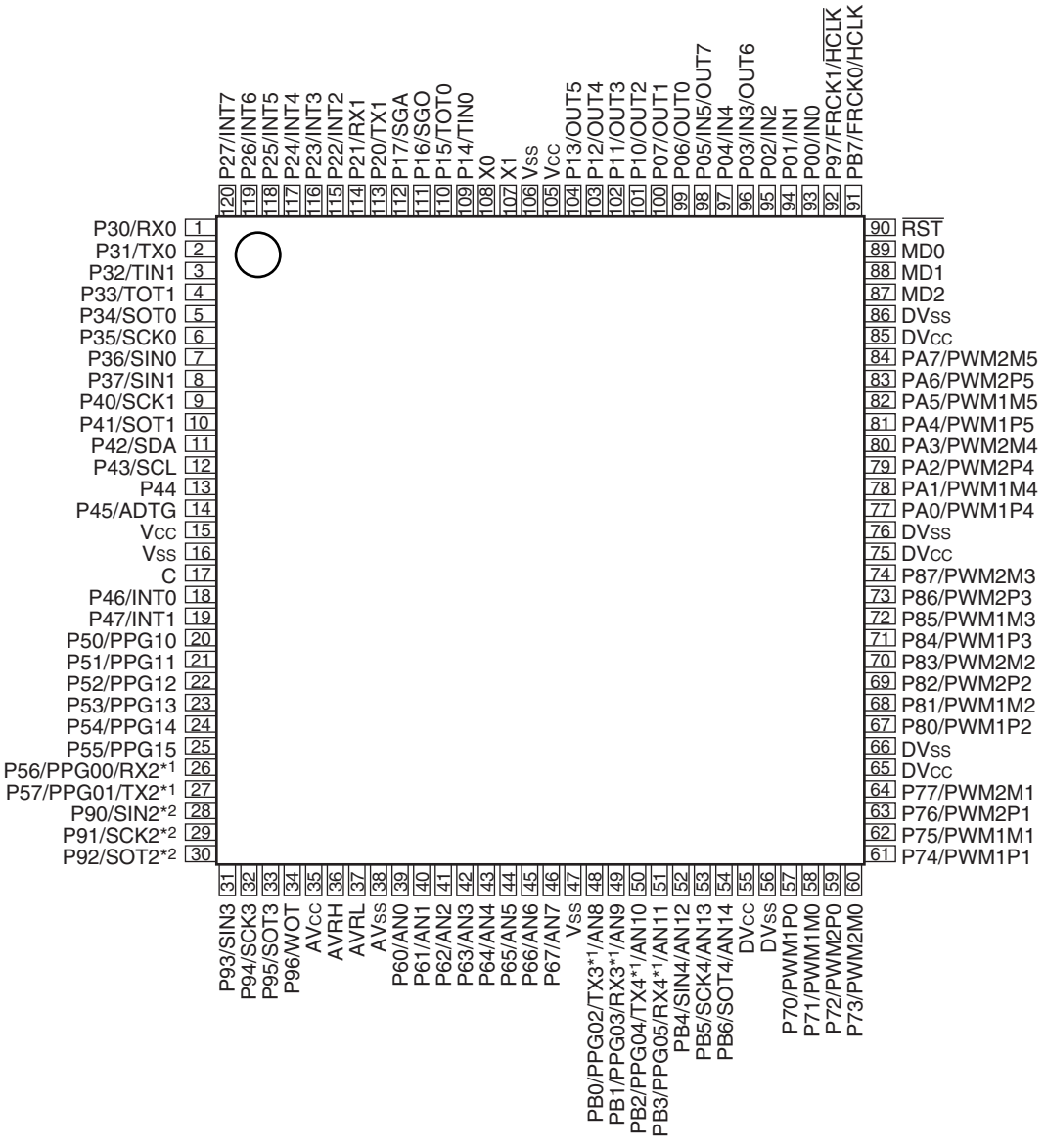


(FPT-120P-M21)

* : MB90V390H/HA/HB only

- MB90V390HA/MB90V390HB

(TOP VIEW)

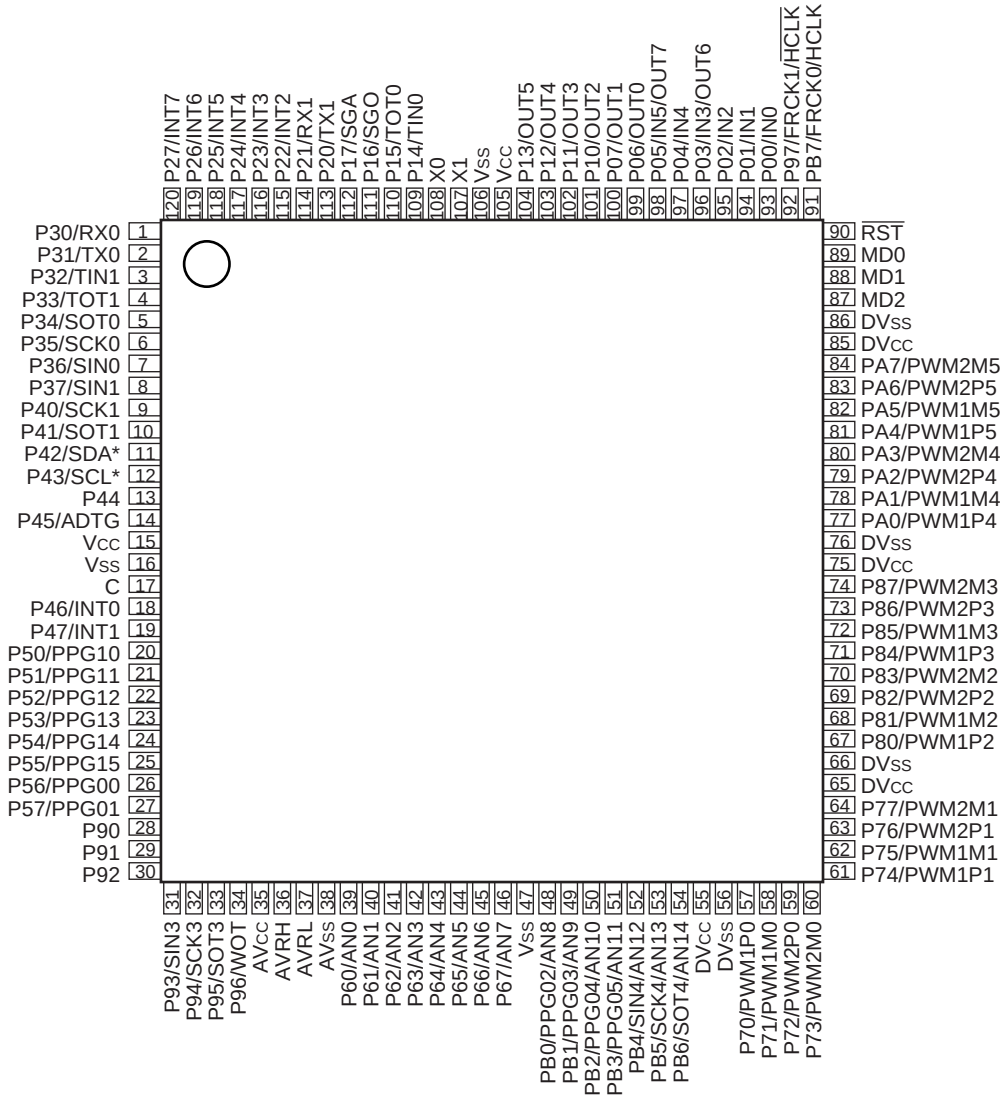


(FPT-120P-M21)

*1 : MB90V390H/HA/HB only
*2 : MB90V390HA/HB only

- MB90394HA/MB90F394H/MB90F394HA

(TOP VIEW)



(FPT-120P-M21)

* : These pins are not available in MB90F394H/MB90F394HA.

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type*	Function
107	X1	A	Oscillation output
108	X0		Oscillation input
90	$\overline{\text{RST}}$	B	Reset input
93 to 95	P00 to P02	D	General purpose I/O
	IN0 to IN2		Inputs for the Input Captures 0 to 2
96	P03	D	General purpose I/O
	IN3		Input for the Input Capture 3
	OUT6		Output for the Output Compare 6
97	P04	D	General purpose I/O
	IN4		Input for the Input Capture 4
98	P05	D	General purpose I/O
	IN5		Input for the Input Capture 5
	OUT7		Output for the Output Compare 7
99 to 104	P06, P07, P10 to P13	D	General purpose I/O
	OUT0 to OUT5		Outputs for the Output Compares 0 to 5
109	P14	D	General purpose I/O
	TIN0		TIN0 input for the 16-bit Reload Timer 0
110	P15	D	General purpose I/O
	TOT0		TOT0 output for the 16-bit Reload Timer 0
111	P16	D	General purpose I/O
	SGO		SGO output for the Sound Generator
112	P17	D	General purpose I/O
	SGA		SGA output for the Sound Generator
113	P20	D	General purpose I/O
	TX1		TX output for CAN Interface 1
114	P21	D	General purpose I/O
	RX1		RX input for CAN Interface 1
115 to 120	P22 to P27	D	General purpose I/O
	INT2 to INT7		External interrupt inputs for INT2 to INT7
1	P30	D	General purpose I/O
	RX0		RX input for CAN Interface 0
2	P31	D	General purpose I/O
	TX0		TX output for CAN Interface 0

(Continued)

Pin no.	Pin name	Circuit type*	Function
3	P32	D	General purpose I/O
	TIN1		TIN1 input for the 16-bit Reload Timer 1
4	P33	D	General purpose I/O
	TOT1		TOT1 output for the 16-bit Reload Timer 1
5	P34	D	General purpose I/O
	SOT0		SOT output for UART 0
6	P35	D	General purpose I/O
	SCK0		SCK I/O for UART 0
7	P36	D	General purpose I/O
	SIN0		SIN input for UART 0
8	P37	D	General purpose I/O
	SIN1		SIN input for UART 1
9	P40	D	General purpose I/O
	SCK1		SCK I/O for UART 1
10	P41	D	General purpose I/O
	SOT1		SOT output for UART 1
11	P42	D	General purpose I/O
	SDA		Serial data for I^2C interface (except MB90F394H(A))
12	P43	D	General purpose I/O
	SCL		Serial clock for I^2C interface (except MB90F394H(A))
13	P44	D	General purpose I/O
14	P45	D	General purpose I/O
	ADTG		External trigger input of the A/D Converter
18, 19	P46, P47	D	General purpose I/O
	INT0, INT1		External interrupt inputs for INT0 to INT1
20 to 25	P50 to P55	D	General purpose I/O
	PPG10 to PPG15		Outputs for the Programmable Pulse Generators 10 to 15
26	P56	D	General purpose I/O
	PPG00		Output for the Programmable Pulse Generator 0
	RX2		RX input for CAN Interface 2 (only MB90V390H/HA/HB)
27	P57	D	General purpose I/O
	PPG01		Output for the Programmable Pulse Generator 1
	TX2		TX output for CAN Interface 2 (only MB90V390H/HA/HB)
28	P90	D	General purpose I/O
	SIN2		SIN input for UART 2 (only MB90V390HA/HB)

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Pin no.	Pin name	Circuit type*	Function
29	P91	D	General purpose I/O
	SCK2		SCK input/output for UART 2 (only MB90V390HA/HB)
30	P92	D	General purpose I/O
	SOT2		SOT output for UART 2 (only MB90V390HA/HB)
31	P93	D	General purpose I/O
	SIN3		SIN input for UART 3 (LIN/SCI)
32	P94	D	General purpose I/O
	SCK3		SCK input/output for UART 3 (LIN/SCI)
33	P95	D	General purpose I/O
	SOT3		SOT output for UART 3 (LIN/SCI)
34	P96	D	General purpose I/O
	WOT		WOT output for the Watch Timer
39 to 46	P60 to P67	E	General purpose I/O
	AN0 to AN7		Inputs for the A/D Converter
48	PB0	E	General purpose I/O
	PPG02		Output for the Programmable Pulse Generator 2
	TX3		TX output for CAN Interface 3 (only MB90V390H/HA/HB)
	AN8		Input for the A/D Converter
49	PB1	E	General purpose I/O
	PPG03		Output for the Programmable Pulse Generator 3
	RX3		RX input for CAN Interface 3 (only MB90V390H/HA/HB)
	AN9		Input for the A/D Converter
50	PB2	E	General purpose I/O
	PPG04		Output for the Programmable Pulse Generator 4
	TX4		TX output for CAN Interface 4 (only MB90V390H/HA/HB)
	AN10		Input for the A/D Converter
51	PB3	E	General purpose I/O
	PPG05		Output for the Programmable Pulse Generator 5
	RX4		RX input for CAN Interface 4 (only MB90V390H/HA/HB)
	AN11		Input for the A/D Converter
52	PB4	E	General purpose I/O
	SIN4		SIN input for the Serial I/O
	AN12		Input for the A/D Converter

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Pin no.	Pin name	Circuit type*	Function
53	PB5	E	General purpose I/O
	SCK4		SCK input/output for the Serial I/O
	AN13		Input for the A/D Converter
54	PB6	E	General purpose I/O
	SOT4		SOT output for the Serial I/O
	AN14		Input for the A/D Converter
57 to 60	P70 to P73	F	General purpose I/O
	PWM1P0 PWM1M0 PWM2P0 PWM2M0		Output for Stepping Motor Controller channel 0
61 to 64	P74 to P77	F	General purpose I/O
	PWM1P1 PWM1M1 PWM2P1 PWM2M1		Output for Stepping Motor Controller channel 1
67 to 70	P80 to P83	F	General purpose I/O
	PWM1P2 PWM1M2 PWM2P2 PWM2M2		Output for Stepping Motor Controller channel 2
71 to 74	P84 to P87	F	General purpose I/O
	PWM1P3 PWM1M3 PWM2P3 PWM2M3		Output for Stepping Motor Controller channel 3
77 to 80	PA0 to PA3	F	General purpose I/O
	PWM1P4 PWM1M4 PWM2P4 PWM2M4		Output for Stepping Motor Controller channel 4
81 to 84	PA4 to PA7	F	General purpose I/O
	PWM1P5 PWM1M5 PWM2P5 PWM2M5		Output for Stepping Motor Controller channel 5
91	PB7	D	General purpose I/O
	FRCK0		FRCK0 input for the 16-bit I/O Timer 0
	HCLK		Oscillation Clock output

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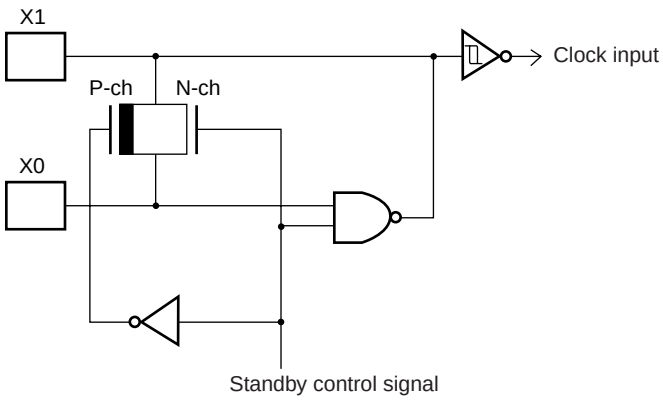
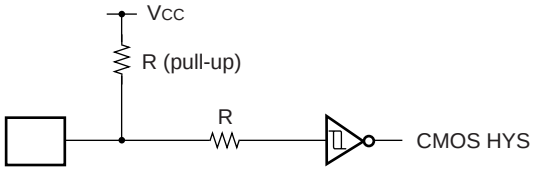
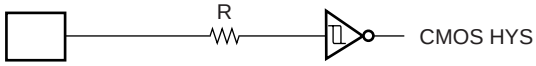
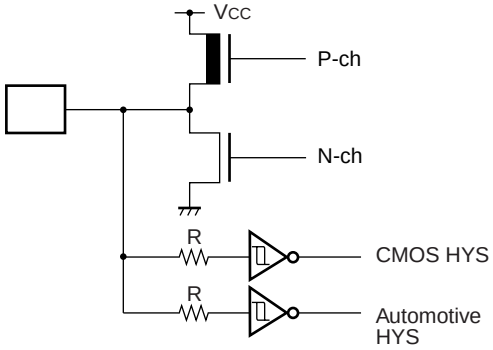
Pin no.	Pin name	Circuit type*	Function
92	P97	D	General purpose I/O
	FRCK1		FRCK1 input for the 16-bit I/O Timer 1
	$\overline{\text{HCLK}}$		Inverted Oscillation Clock output
55 65 75 85	DVcc	—	Dedicated power supply pins for the high current output buffers (Pin No. 57 to 84)
56 66 76 86	DVss	—	Dedicated ground pins for the high current output buffers (Pin No. 57 to 84)
35	AV_{CC}	—	Dedicated power supply pin (5 V) for the A/D converter
36	AVRH	—	Dedicated pos. reference voltage pin for the A/D converter
37	AVRL	—	Dedicated neg. reference voltage pin for the A/D converter
38	AVss	—	Dedicated power supply pin (0 V) for the A/D converter
88, 89	MD1, MD0	C	These are input pins used to designate the operating mode. They should be connected directly to V_{CC} or V_{SS}.
87	MD2	G	This is an input pin used to designate the operating mode. It should be connected directly to V_{CC} or V_{SS}.
15 105	Vcc	—	These are power supply (5 V) input pins
16 47 106	Vss	—	These are power supply (0 V) input pins
17	C	—	This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 µF (MB90394HA/ MB90F394H(A)/MB90V390H)/0.22 µF (MB90V390HA/HB) ceramic capacitor.

* : Refer to “■ I/O CIRCUIT TYPE” for I/O circuit type.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation feedback resistor : 1 MΩ approx.
B		• CMOS Hysteresis input with pull-up Resistor : 50 kΩ approx.
C		• EVA/ROM device : CMOS Hysteresis input • Flash device : CMOS input.
D		• CMOS output • CMOS Hysteresis input • Automotive Hysteresis input Note : The input characteristic may be different for different pins/devices. Refer to V_{IHS} in "■ ELECTRICAL CHARACTERISTICS 3.DC Characteristics"

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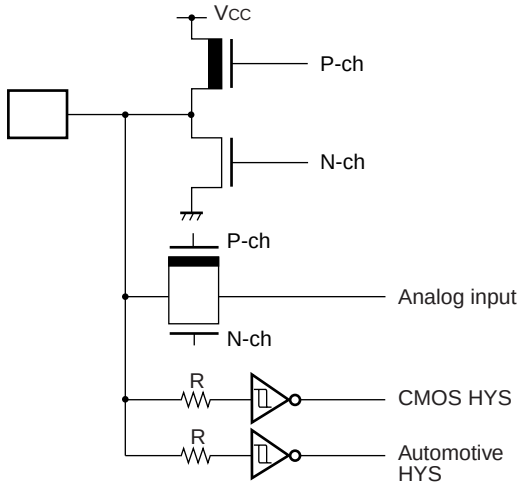
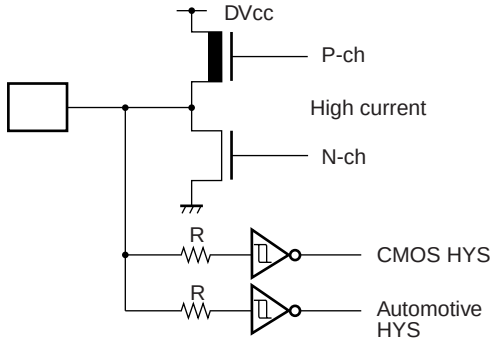
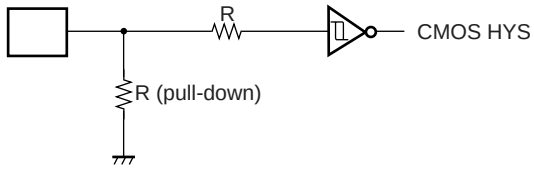
Type	Circuit	Remarks
E		• CMOS output • CMOS Hysteresis input • Automotive Hysteresis input • Analog input Note : The input characteristic may be different for different pins/devices. Refer to V_{IHS} in "■ ELECTRICAL CHARACTERISTICS 3.DC Characteristics"
F		• CMOS high current output • CMOS Hysteresis input • Automotive Hysteresis input
G		• EVA/ROM device : CMOS Hysteresis input with pull-down Resistor : 50 kΩ approx. • Flash device : CMOS input without pull-down.

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter if A/D Converter is unused.
- Notes on Energization
- Caution on Operations during PLL Clock Mode

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

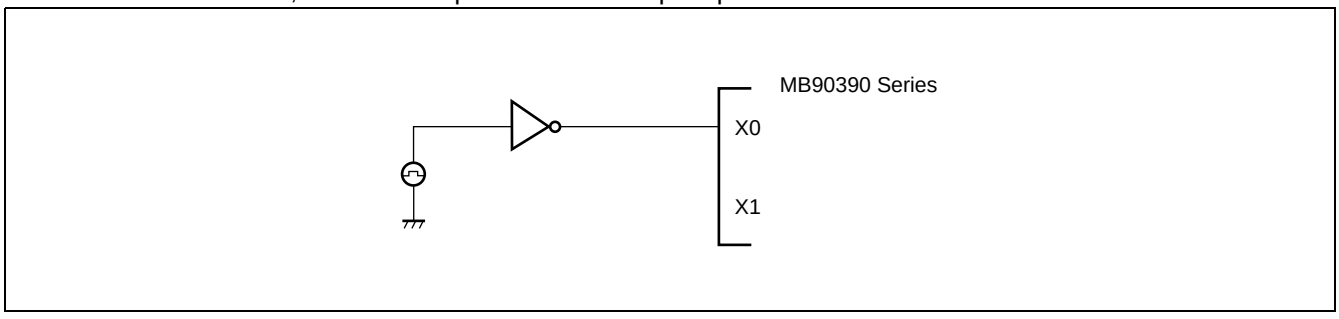
3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

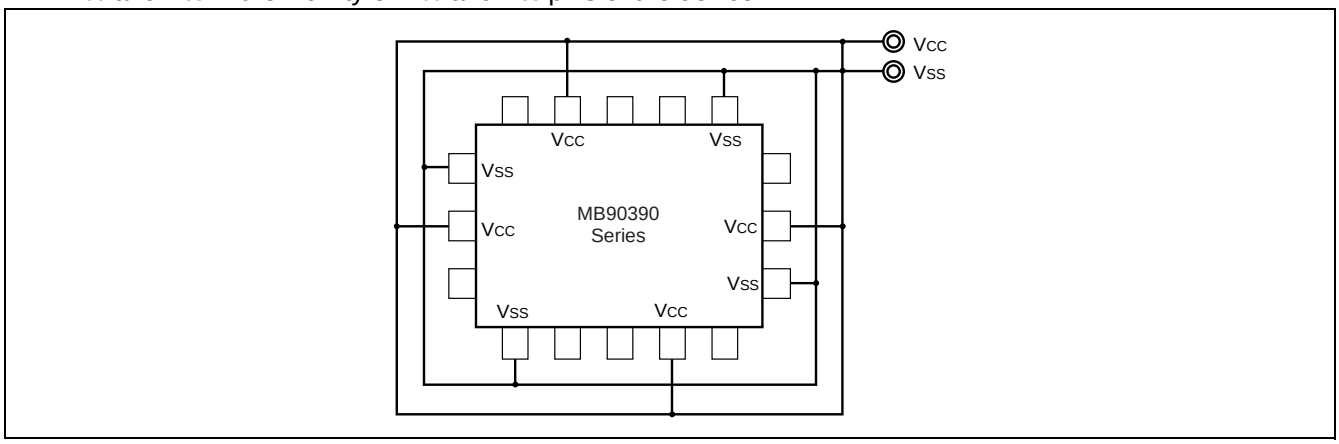
4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



5. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device.



6. Pull-up/down resistors

The MB90390 Series does not support internal pull-up/down resistors. Use external components where needed.

7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

9. Connection of Unused Pins of A/D Converter if A/D Converter is unused

Connect unused pins of A/D converter to AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Energization

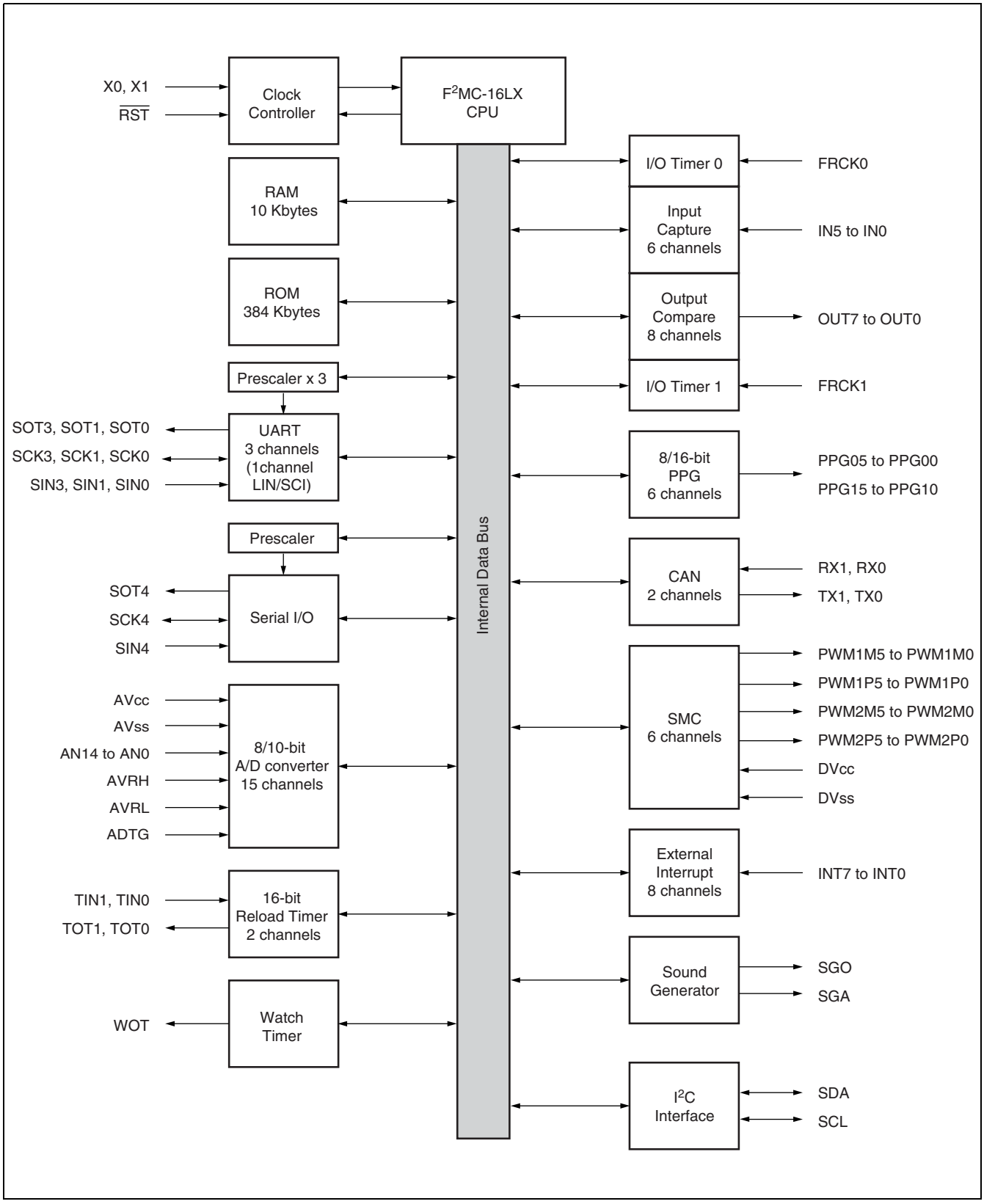
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more µs (0.2 V to 2.7 V) .

11. Notes on During Operation of PLL Clock Mode

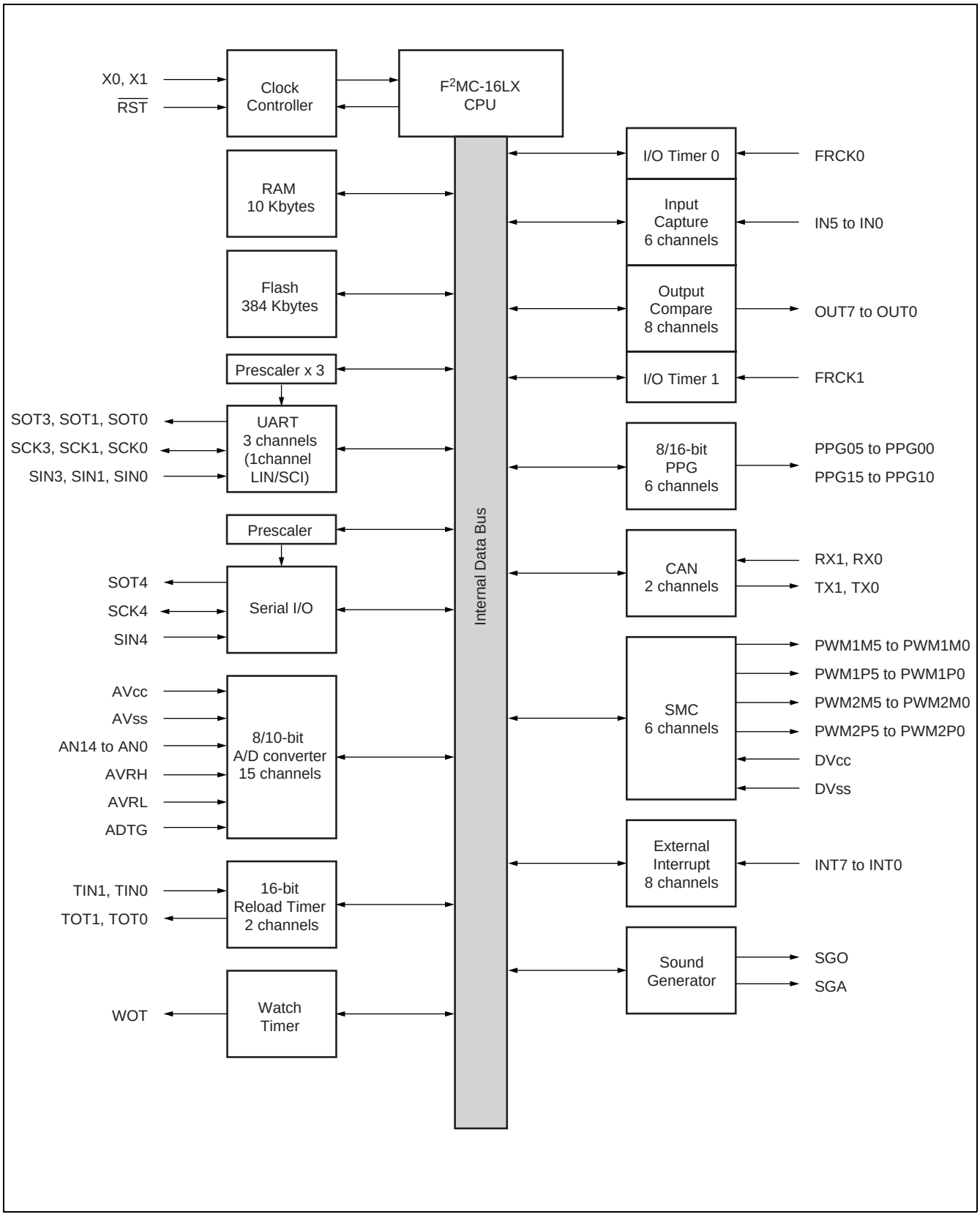
On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

■ BLOCK DIAGRAMS

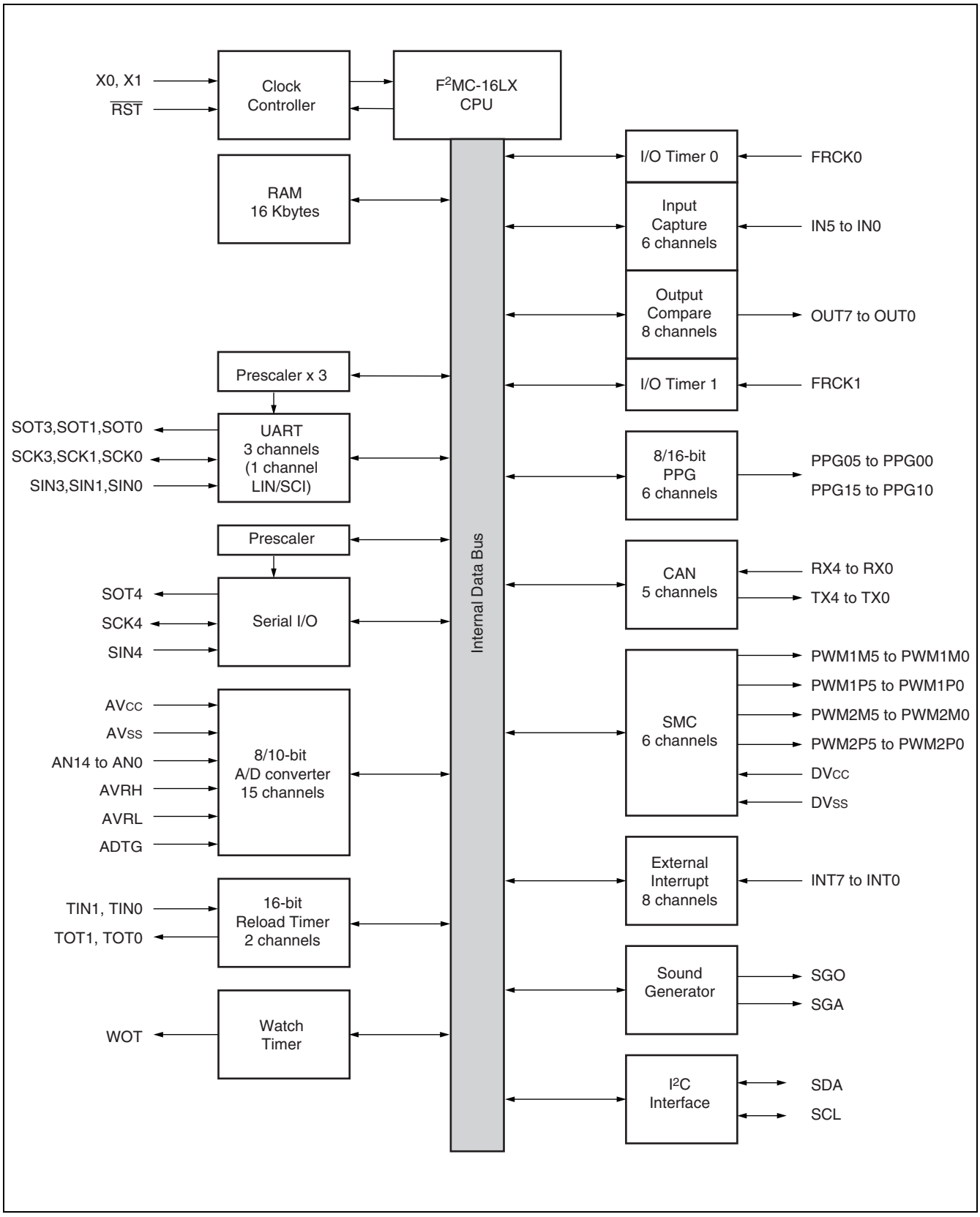
- **MB90394HA**



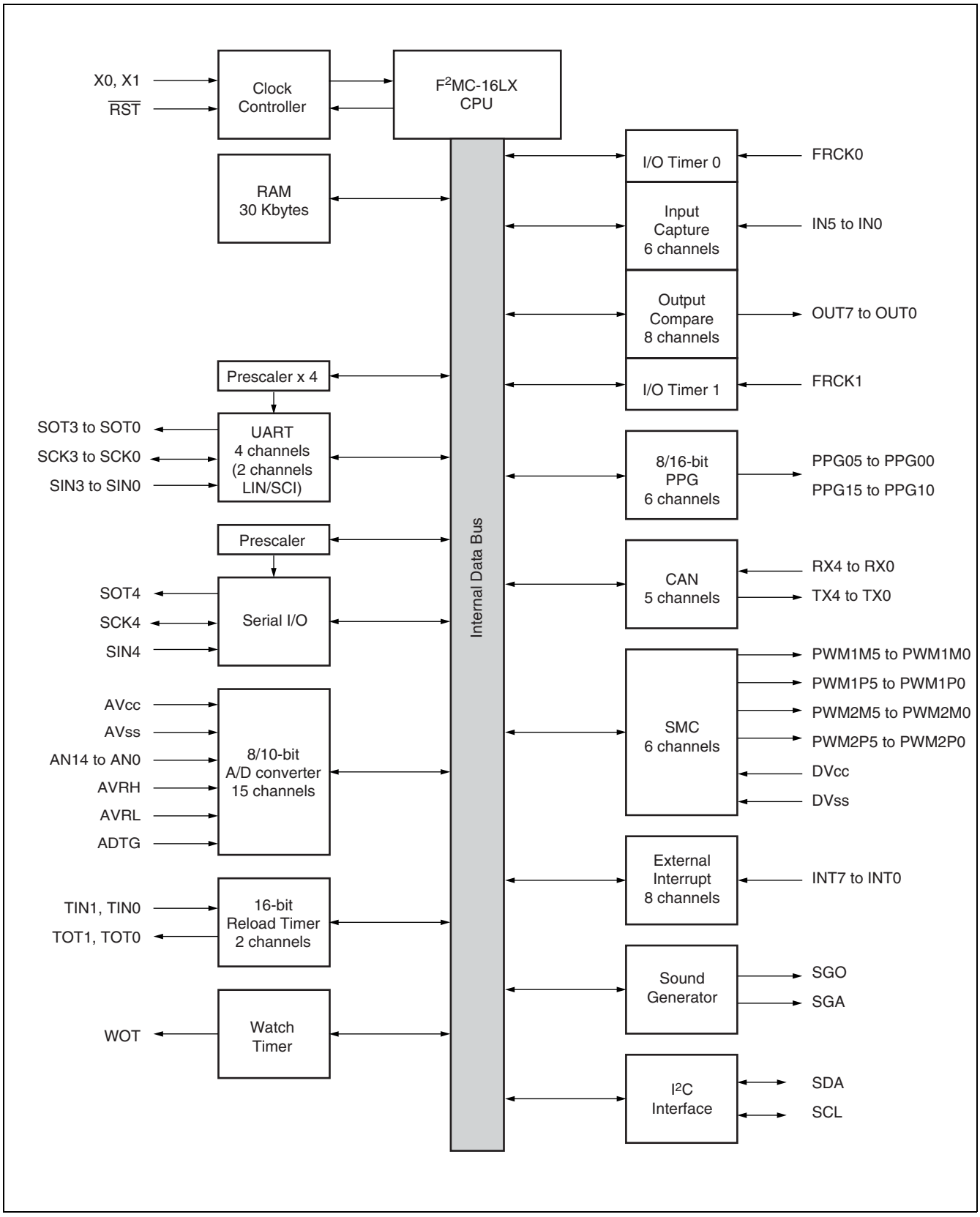
- **MB90F394H/MB90F394HA**



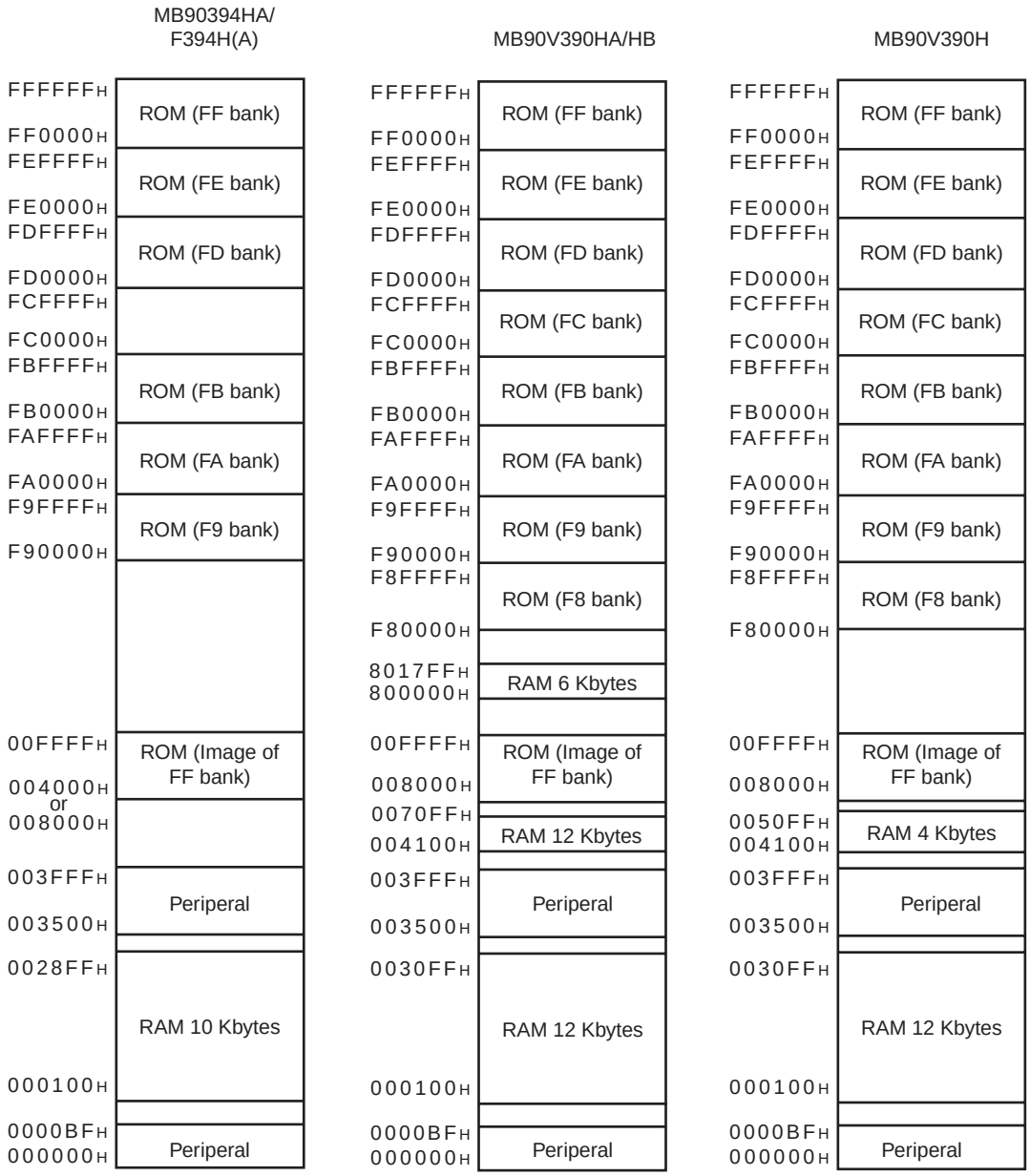
- **MB90V390H**


X0, X1
RST
Clock Controller
F2MC-16LX CPU
RAM 16 Kbytes
Prescaler x 3
SOT3,SOT1,SOT0
SCK3,SCK1,SCK0
SIN3,SIN1,SIN0
UART 3 channels (1 channel LIN/SCI)
Prescaler
SOT4
SCK4
SIN4
Serial I/O
AVCC
AVSS
AN14 to AN0
AVRH
AVRL
ADTG
8/10-bit A/D converter 15 channels
TIN1, TIN0
TOT1, TOT0
16-bit Reload Timer 2 channels
WOT
Watch Timer
Internal Data Bus
I/O Timer 0
FRCK0
Input Capture 6 channels
IN5 to IN0
Output Compare 8 channels
OUT7 to OUT0
I/O Timer 1
FRCK1
8/16-bit PPG 6 channels
PPG05 to PPG00
PPG15 to PPG10
CAN 5 channels
RX4 to RX0
TX4 to TX0
SMC 6 channels
PWM1M5 to PWM1M0
PWM1P5 to PWM1P0
PWM2M5 to PWM2M0
PWM2P5 to PWM2P0
DVCC
DVSS
External Interrupt 8 channels
INT7 to INT0
Sound Generator
SGO
SGA
I2C Interface
SDA
SCL

- **MB90V390HA/MB90V390HB**



■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32/48 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF4000H/FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF3FFFH/FF7FFFH is visible only in bank FF.
In MB90V390H/HA/HB, the image for only ROM data between FF8000H to FFFFFFH is visible in bank 00.
As for MB90F394H(A) and MB90394HA, it is possible to set the FF bank area which looks the 00 bank image in the ROM mirror function select register (ROMM) .

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
08_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 Data Register	PDR9	R/W	Port 9	$XXXXXXXX_B$
$0A_H$	Port A Data Register	PDRA	R/W	Port A	$XXXXXXXX_B$
$0B_H$	Port B Data Register	PDRB	R/W	Port B	$XXXXXXXX_B$
$0C_H$	Analog Input Enable 0	ADER0	R/W	Port 6, A/D	11111111_B
$0D_H$	Analog Input Enable 1/ ADC Select	ADER1	R/W	Port B, A/D	01111111_B
$0E_H$	Input Level Select Register	ILSR	R/W	Ports	00000000_B
$0F_H$	Input Level Select Register	ILSR	R/W	Ports	00000000_B
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
18_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000_B
$1A_H$	Port A Direction Register	DDRA	R/W	Port A	00000000_B
$1B_H$	Port B Direction Register	DDRB	R/W	Port B	00000000_B
$1C_H$ to $1F_H$	Reserved				
20_H	Serial Mode Control 0	UMC0	R/W	UART0	00000100_B
21_H	Status 0	USR0	R/W		00010000_B
22_H	Input/Output Data 0	UIDR0/ UODR0	R/W		$XXXXXXXX_B$
23_H	Rate and Data 0	URD0	R/W		$0000000X_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
24H	Serial Mode Control 1	UMC1	R/W	UART1	00000100B
25H	Status 1	USR1	R/W		00010000B
26H	Input/Output Data 1	UIDR1/ UODR1	R/W		XXXXXXXXB
27H	Rate and Data 1	URD1	R/W		0000000XB
28H to 2BH	Reserved				
2CH	Serial Mode Control 4	SMCS4	R/W	Serial I/O	XXXX0000B
2DH	Serial Mode Control 4	SMCS4	R/W		00000010B
2EH	Serial Data 4	SDR4	R/W		XXXXXXXXB
2FH	Serial I/O Prescaler/Edge Selector 4	CDCR4	R/W		0 X 0 X 0000B
30H	External Interrupt Enable	ENIR	R/W	External Interrupt	00000000B
31H	External Interrupt Request	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level	ELVR	R/W		00000000B
33H	External Interrupt Level	ELVR	R/W		00000000B
34H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00000000B
35H	A/D Control Status 1	ADCS1	R/W		00000000B
36H	A/D Data 0	ADCR0	R		XXXXXXXXB
37H	A/D Data 1	ADCR1	R/W		000010XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0X000XX1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0X000001B
3AH	PPG0 and PPG1 Clock Select Register	PPG01	R/W		000000XXB
3BH	Address Detection Control Register 1	PACSR1	R/W	Address Match Detection Function 1	00000000B
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0X000XX1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0X000001B
3EH	PPG2 and PPG3 Clock Select Register	PPG23	R/W		000000XXB
3FH	Clock Output Enable Register	CKOE	R/W	Clock Output	XXXXXX00B
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0X000XX1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0X000001B
42H	PPG4 and PPG5 Clock Select Register	PPG45	R/W		000000XXB
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0X000001B
46H	PPG6 and PPG7 Clock Select Register	PPG67	R/W		000000XXB

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0X000001B
4AH	PPG8 and PPG9 Clock Select Register	PPG89	R/W		000000XXB
4BH	Reserved				
4CH	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0X000XX1B
4DH	PPGB Operation Mode Control Register	PPGCB	R/W		0X000001B
4EH	PPGA and PPGB Clock Select Register	PPGAB	R/W		000000XXB
4FH	Reserved				
50H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000B
51H	Timer Control Status 0	TMCSR0	R/W		XXXX0000B
52H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000B
53H	Timer Control Status 1	TMCSR1	R/W		XXXX0000B
54H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000B
55H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000B
56H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000B
57H	Reserved				
58H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00B
59H	Output Compare Control Status 1	OCS1	R/W		0XX00000B
5AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00B
5BH	Output Compare Control Status 3	OCS3	R/W		0XX00000B
5CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00B
5DH	Output Compare Control Status 5	OCS5	R/W		0XX00000B
5EH	Sound Control	SGCR	R/W	Sound Generator	00000000B
5FH	Sound Control	SGCR	R/W		0XXXXXX0B
60H	Watch Timer Control	WTCR	R/W	Watch Timer	000XX000B
61H	Watch Timer Control	WTCR	R/W		00000000B
62H	PWM Control 0	PWC0	R/W	Stepping Motor Controller 0	00000XX0B
63H	Reserved				
64H	PWM Control 1	PWC1	R/W	Stepping Motor Controller 1	00000XX0B
65H	Reserved				
66H	PWM Control 2	PWC2	R/W	Stepping Motor Controller 2	00000XX0B
67H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
68H	PWM Control 3	PWC3	R/W	Stepping Motor Controller 3	00000XX0B
69H	Reserved				
6AH	PWM Control 4	PWC4	R/W	Stepping Motor Controller 4	00000XX0B
6BH	Reserved				
6CH	PWM Control 5	PWC5	R/W	Stepping Motor Controller 5	00000XX0B
6DH	Reserved				
6EH	Reserved				
6FH	ROM Mirror	ROMM	W	ROM Mirror	XXXXXXX1B
70H to 8FH	Reserved for CAN Interface 0/1. Refer to "■ CAN CONTROLLERS"				
90H to 9DH	Reserved				
9EH	Address Detection Control Register 0	PACSR0	R/W	Address Match Detection Function 0	00000000B
9FH	Delayed Interrupt/Release	DIRR	R/W	Delayed Interrupt	XXXXXXX0B
A0H	Low-power Mode	LPMCR	R/W	Low Power Controller	00011000B
A1H	Clock Selector	CKSCR	R/W	Low Power Controller	11111100B
A2H to A7H	Reserved				
A8H	Watchdog Control	WDTC	R/W	Watchdog Timer	XXXXX111B
A9H	Time Base Timer Control	TBTC	R/W	Time Base Timer	1XX00100B
AAH to ADH	Reserved				
AEH	Flash Control Status (Flash devices only. Otherwise reserved)	FMCS	R/W	Flash Memory	000X0XX0B
AFH	Reserved				
B0H	Interrupt Control Register 00	ICR00	R/W	Interrupt Controller	00000111B
B1H	Interrupt Control Register 01	ICR01	R/W		00000111B
B2H	Interrupt Control Register 02	ICR02	R/W		00000111B
B3H	Interrupt Control Register 03	ICR03	R/W		00000111B
B4H	Interrupt Control Register 04	ICR04	R/W		00000111B
B5H	Interrupt Control Register 05	ICR05	R/W		00000111B
B6H	Interrupt Control Register 06	ICR06	R/W		00000111B
B7H	Interrupt Control Register 07	ICR07	R/W		00000111B
B8H	Interrupt Control Register 08	ICR08	R/W		00000111B
B9H	Interrupt Control Register 09	ICR09	R/W		00000111B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
BA$_H$	Interrupt Control Register 10	ICR10	R/W	Interrupt Controller	00000111$_B$
BB$_H$	Interrupt Control Register 11	ICR11	R/W		00000111$_B$
BC$_H$	Interrupt Control Register 12	ICR12	R/W		00000111$_B$
BD$_H$	Interrupt Control Register 13	ICR13	R/W		00000111$_B$
BE$_H$	Interrupt Control Register 14	ICR14	R/W		00000111$_B$
BF$_H$	Interrupt Control Register 15	ICR15	R/W		00000111$_B$
C0$_H$ to FF$_H$	Reserved				
3500$_H$	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX$_B$
3501$_H$	Reload H	PRLH0	R/W		XXXXXXXX$_B$
3502$_H$	Reload L	PRLL1	R/W		XXXXXXXX$_B$
3503$_H$	Reload H	PRLH1	R/W		XXXXXXXX$_B$
3504$_H$	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX$_B$
3505$_H$	Reload H	PRLH2	R/W		XXXXXXXX$_B$
3506$_H$	Reload L	PRLL3	R/W		XXXXXXXX$_B$
3507$_H$	Reload H	PRLH3	R/W		XXXXXXXX$_B$
3508$_H$	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX$_B$
3509$_H$	Reload H	PRLH4	R/W		XXXXXXXX$_B$
350A$_H$	Reload L	PRLL5	R/W		XXXXXXXX$_B$
350B$_H$	Reload H	PRLH5	R/W		XXXXXXXX$_B$
350C$_H$	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX$_B$
350D$_H$	Reload H	PRLH6	R/W		XXXXXXXX$_B$
350E$_H$	Reload L	PRLL7	R/W		XXXXXXXX$_B$
350F$_H$	Reload H	PRLH7	R/W		XXXXXXXX$_B$
3510$_H$	Reload L	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX$_B$
3511$_H$	Reload H	PRLH8	R/W		XXXXXXXX$_B$
3512$_H$	Reload L	PRLL9	R/W		XXXXXXXX$_B$
3513$_H$	Reload H	PRLH9	R/W		XXXXXXXX$_B$
3514$_H$	Reload L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX$_B$
3515$_H$	Reload H	PRLHA	R/W		XXXXXXXX$_B$
3516$_H$	Reload L	PRLLB	R/W		XXXXXXXX$_B$
3517$_H$	Reload H	PRLHB	R/W		XXXXXXXX$_B$
3518$_H$	Serial Mode Register	SMR3	R/W	UART3 (LIN/SCI)	00000000$_B$
3519$_H$	Serial Control Register	SCR3	R/W		00000000$_B$
351A$_H$	Reception/Transmission Data Register	RDR3/ TDR3	R/W		00000000$_B$

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
351B$_H$	Serial Status Register	SSR3	R/W	UART3 (LIN/SCI)	00001000$_B$
351C$_H$	Extended Communication Control Reg.	ECCR3	R/W		000000XX$_B$
351D$_H$	Extended Status/Control Register	ESCR3	R/W		00000X00$_B$
351E$_H$	Baud Rate Register 0	BGR03	R/W		00000000$_B$
351F$_H$	Baud Rate Register 1	BGR13	R/W		00000000$_B$
3520$_H$	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX$_B$
3521$_H$	Input Capture 0	IPCP0	R		XXXXXXXX$_B$
3522$_H$	Input Capture 1	IPCP1	R		XXXXXXXX$_B$
3523$_H$	Input Capture 1	IPCP1	R		XXXXXXXX$_B$
3524$_H$	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX$_B$
3525$_H$	Input Capture 2	IPCP2	R		XXXXXXXX$_B$
3526$_H$	Input Capture 3	IPCP3	R		XXXXXXXX$_B$
3527$_H$	Input Capture 3	IPCP3	R		XXXXXXXX$_B$
3528$_H$	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX$_B$
3529$_H$	Input Capture 4	IPCP4	R		XXXXXXXX$_B$
352A$_H$	Input Capture 5	IPCP5	R		XXXXXXXX$_B$
352B$_H$	Input Capture 5	IPCP5	R		XXXXXXXX$_B$
352C$_H$	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000$_B$
352D$_H$	Timer Data 0	TCDT0	R/W		00000000$_B$
352E$_H$	Timer Control 0	TCCS0	R/W		00000000$_B$
352F$_H$	Timer Control 0	TCCS0	R/W		0XXXXXXX$_B$
3530$_H$	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX$_B$
3531$_H$	Output Compare 0	OCCP0	R/W		XXXXXXXX$_B$
3532$_H$	Output Compare 1	OCCP1	R/W		XXXXXXXX$_B$
3533$_H$	Output Compare 1	OCCP1	R/W		XXXXXXXX$_B$
3534$_H$	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
3535$_H$	Output Compare 2	OCCP2	R/W		XXXXXXXX$_B$
3536$_H$	Output Compare 3	OCCP3	R/W		XXXXXXXX$_B$
3537$_H$	Output Compare 3	OCCP3	R/W		XXXXXXXX$_B$
3538$_H$	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
3539$_H$	Output Compare 4	OCCP4	R/W		XXXXXXXX$_B$
353A$_H$	Output Compare 5	OCCP5	R/W		XXXXXXXX$_B$
353B$_H$	Output Compare 5	OCCP5	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
353C$_H$	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000$_B$
353D$_H$	Timer Data 1	TCDT1	R/W		00000000$_B$
353E$_H$	Timer Control 1	TCCS1	R/W		00000000$_B$
353F$_H$	Timer Control 1	TCCS1	R/W		0XXXXXXX$_B$
3540$_H$	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
3541$_H$	Timer 0/Reload 0	TMR0/ TMRLR0	R/W		XXXXXXXX$_B$
3542$_H$	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
3543$_H$	Timer 1/Reload 1	TMR1/ TMRLR1	R/W		XXXXXXXX$_B$
3544$_H$, 3545$_H$	Reserved				
3546$_H$	Frequency Data	SGFR	R/W	Sound Generator	XXXXXXXX$_B$
3547$_H$	Amplitude Data	SGAR	R/W		XXXXXXXX$_B$
3548$_H$	Decrement Grade	SGDR	R/W		XXXXXXXX$_B$
3549$_H$	Tone Count	SGTR	R/W		XXXXXXXX$_B$
354A$_H$	Sub-second Data	WTBR	R/W	Watch Timer	XXXXXXXX$_B$
354B$_H$	Sub-second Data	WTBR	R/W		XXXXXXXX$_B$
354C$_H$	Sub-second Data	WTBR	R/W		XXXXXXXX$_B$
354D$_H$	Second Data	WTSR	R/W		XX000000$_B$
354E$_H$	Minute Data	WTMR	R/W		XX000000$_B$
354F$_H$	Hour Data	WTHR	R/W		XXX00000$_B$
3550$_H$	PWM1 Compare 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
3551$_H$	PWM2 Compare 0	PWC20	R/W		XXXXXXXX$_B$
3552$_H$	PWM1 Select 0	PWS10	R/W		00000000$_B$
3553$_H$	PWM2 Select 0	PWS20	R/W		X0000000$_B$
3554$_H$	PWM1 Compare 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
3555$_H$	PWM2 Compare 1	PWC21	R/W		XXXXXXXX$_B$
3556$_H$	PWM1 Select 1	PWS11	R/W		00000000$_B$
3557$_H$	PWM2 Select 1	PWS21	R/W		X0000000$_B$
3558$_H$	PWM1 Compare 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
3559$_H$	PWM2 Compare 2	PWC22	R/W		XXXXXXXX$_B$
355A$_H$	PWM1 Select 2	PWS12	R/W		00000000$_B$
355B$_H$	PWM2 Select 2	PWS22	R/W		X0000000$_B$

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
355C$_H$	PWM1 Compare 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
355D$_H$	PWM2 Compare 3	PWC23	R/W		XXXXXXXX$_B$
355E$_H$	PWM1 Select 3	PWS13	R/W		00000000$_B$
355F$_H$	PWM2 Select 3	PWS23	R/W		X0000000$_B$
3560$_H$	PWM1 Compare 4	PWC14	R/W	Stepping Motor Controller 4	XXXXXXXX$_B$
3561$_H$	PWM2 Compare 4	PWC24	R/W		XXXXXXXX$_B$
3562$_H$	PWM1 Select 4	PWS14	R/W		00000000$_B$
3563$_H$	PWM2 Select 4	PWS24	R/W		X0000000$_B$
3564$_H$	PWM1 Compare 5	PWC15	R/W	Stepping Motor Controller 5	XXXXXXXX$_B$
3565$_H$	PWM2 Compare 5	PWC25	R/W		XXXXXXXX$_B$
3566$_H$	PWM1 Select 5	PWS15	R/W		00000000$_B$
3567$_H$	PWM2 Select 5	PWS25	R/W		X0000000$_B$
3568$_H$	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00$_B$
3569$_H$	Output Compare Control Status 7	OCS7	R/W		XXX00000$_B$
356A$_H$	Output Compare 6	OCCP6	R/W		XXXXXXXX$_B$
356B$_H$	Output Compare 6	OCCP6	R/W		XXXXXXXX$_B$
356C$_H$	Output Compare 7	OCCP7	R/W		XXXXXXXX$_B$
356D$_H$	Output Compare 7	OCCP7	R/W		XXXXXXXX$_B$
356E$_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0$_B$
356F$_H$	CAN RX/TX redirect register	CANSWR	R/W	CAN 0/1/2/3	XXXX0000$_B$
3570$_H$ to 359F$_H$	Reserved for CAN Interface 2/3/4. Refer to “■ CAN CONTROLLERS”				
35A0$_H$	I^{2}C Bus Status Register	IBSR	R	I^{2}C Interface*4	00000000$_B$
35A1$_H$	I^{2}C Bus Control Register	IBCR	R/W		00000000$_B$
35A2$_H$	I^{2}C Ten Bit Slave Address Register	ITBAL	R/W		00000000$_B$
35A3$_H$		ITBAH	R/W		XXXXXX00$_B$
35A4$_H$	I^{2}C Ten Bit Address Mask Register	ITMKL	R/W		11111111$_B$
35A5$_H$		ITMKH	R/W		00XXXX11$_B$
35A6$_H$	I^{2}C Seven Bit Slave Address Register	ISBA	R/W		X0000000$_B$
35A7$_H$	I^{2}C Seven Bit Address Mask Register	ISMK	R/W		01111111$_B$
35A8$_H$	I^{2}C Data Register	IDAR	R/W		00000000$_B$
35A9$_H$	I^{2}C Noise Filter Configuration Register*2	INFCR	R/W		XXXXXX01$_B$
35AA$_H$	Reserved				
35AB$_H$	I^{2}C Clock Control Register	ICCR	R/W	I^{2}C Interface*4	X0011111$_B$
35AC$_H$ to 35BF$_H$	Reserved				
35C0$_H$	Parameter Register Low Byte	CMPRL	R/W	Clock Modulator	11111101$_B$

(Continued)

Address	Register	Abbrevi-ation	Access	Resource name	Initial value
35C1H	Parameter Register High Byte	CMPRH	R/W	Clock Modulator	XX000010B
35C2H	Clock Modulator Control Register	CMCR	R/W		00010000B
35C3H to 35C8H	Reserved				
35C9H	Input Capture Edge 0/1	ICE01	R/W	Input Capture 0/1	XXXXX0XXB
35CAH	Input Capture Edge 2/3*3	ICE23	R	Input Capture 2/3	XXXXXXXXB
35CBH	Input Capture Edge 4/5	ICE45	R/W	Input Capture 4/5	XXXXX0XXB
35CCH to 35CEH	Reserved				
35CFH	PLL and special configuration control resister	PSCCR	W	PLL	XXXX0000B
35D0H to 35D7H	Reserved				
35D8H	Serial Mode Register	SMR2	R/W	UART2*1 (LIN/SCI)	00000000B
35D9H	Serial Control Register	SCR2	R/W		00000000B
35DAH	Reception/Transmission Data Register	RDR2/ TDR2	R/W		00000000B
35DBH	Serial Status Register	SSR2	R/W		00001000B
35DCH	Extended Communication Control Register	ECCR2	R/W		000000XXB
35DDH	Extended Status/Control Register	ESCR2	R/W		00000X00B
35DEH	Baud Rate Register 0	BGR02	R/W		00000000B
35DFH	Baud Rate Register 1	BGR12	R/W		00000000B
35E0H	Detection Address Setting Register 0 (Low-order)	PADR0	R/W	Address Match Detection Function 0	XXXXXXXXB
35E1H	Detection Address Setting Register 0 (Middle-order)	PADR0	R/W		XXXXXXXXB
35E2H	Detection Address Setting Register 0 (High-order)	PADR0	R/W		XXXXXXXXB
35E3H	Detection Address Setting Register 1 (Low-order)	PADR1	R/W		XXXXXXXXB
35E4H	Detection Address Setting Register 1 (Middle-order)	PADR1	R/W		XXXXXXXXB
35E5H	Detection Address Setting Register 1 (High-order)	PADR1	R/W		XXXXXXXXB
35E6H to 35EFH	Reserved				
35F0H	Detection Address Setting Register 3 (Low-order)	PADR3	R/W	Address Match Detection Function 1	XXXXXXXXB
35F1H	Detection Address Setting Register 3 (Middle-order)	PADR3	R/W		XXXXXXXXB

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
35F2H	Detection Address Setting Register 3 (High-order)	PADR3	R/W	Address Match Detection Function 1	XXXXXXXXB
35F3H	Detection Address Setting Register 4 (Low-order)	PADR4	R/W		XXXXXXXXB
35F4H	Detection Address Setting Register 4 (Middle-order)	PADR4	R/W		XXXXXXXXB
35F5H	Detection Address Setting Register 4 (High-order)	PADR4	R/W		XXXXXXXXB
35F6H	Detection Address Setting Register 5 (Low-order)	PADR5	R/W		XXXXXXXXB
35F7H	Detection Address Setting Register 5 (Middle-order)	PADR5	R/W		XXXXXXXXB
35F8H	Detection Address Setting Register 5 (High-order)	PADR5	R/W		XXXXXXXXB
35F9H to 35FFH	Reserved				
3600H to 37FFH	Reserved for CAN Interface 0. Refer to “■ CAN CONTROLLERS”				
3800H to 39FFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
3A00H to 3BFFH	Reserved for CAN Interface 2. Refer to “■ CAN CONTROLLERS”				
3C00H to 3DFFH	Reserved for CAN Interface 3. Refer to “■ CAN CONTROLLERS”				
3E00H to 3FFFH	Reserved for CAN Interface 4. Refer to “■ CAN CONTROLLERS”				

*1 : UART2 (LIN/SCI) is only available in MB90V390HA/HB.

*2 : I^2C Noise Filter Configuration Register is only available in the devices MB90V390HA/HB, MB90394HA.

*3 : Input Capture Edge 2/3 register is different in MB90V390HA/HB, the access is “R/W” and initial value is “XXXXX0XXB”.

*4 : I^2C Interface is not available in MB90F394H(A).

- Explanation on read/write
  R/W : Readable and writable
  R : Read only
  W : Write only

- Explanation on initial values
  0 : Initial value is “0”.
  1 : Initial value is “1”.
  X : Initial value is undefined.

Note : Any write access to reserved addresses in I/O map should not be performed. A read access to reserved address results in reading “X”.

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance mask register 0/acceptance mask register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
000070H	000080H	003570H	003580H	003590H	Message buffer valid register	BVALR	R/W	00000000B 00000000B
000071H	000081H	003571H	003581H	003591H				
000072H	000082H	003572H	003582H	003592H	Transmit request register	TREQR	R/W	00000000B 00000000B
000073H	000083H	003573H	003583H	003593H				
000074H	000084H	003574H	003584H	003594H	Transmit cancel register	TCANR	W	00000000B 00000000B
000075H	000085H	003575H	003585H	003595H				
000076H	000086H	003576H	003586H	003596H	Transmit complete register	TCR	R/W	00000000B 00000000B
000077H	000087H	003577H	003587H	003597H				
000078H	000088H	003578H	003588H	003598H	Receive complete register	RCR	R/W	00000000B 00000000B
000079H	000089H	003579H	003589H	003599H				
00007AH	00008AH	00357AH	00358AH	00359AH	Remote request receiving register	RRTRR	R/W	00000000B 00000000B
00007BH	00008BH	00357BH	00358BH	00359BH				
00007CH	00008CH	00357CH	00358CH	00359CH	Receive overrun register	ROVRR	R/W	00000000B 00000000B
00007DH	00008DH	00357DH	00358DH	00359DH				
00007EH	00008EH	00357EH	00358EH	00359EH	Receive interrupt enable register	RIER	R/W	00000000B 00000000B
00007FH	00008FH	00357FH	00358FH	00359FH				

List of Control Registers (2)

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003700H	003900H	003B00H	003D00H	003F00H	Control status register	CSR	R/W, R	00XXX000B 0XXXX0X1B
003701H	003901H	003B01H	003D01H	003F01H				
003702H	003902H	003B02H	003D02H	003F02H	Last event indicator register	LEIR	R/W	XXXXXXXXB 000X0000B
003703H	003903H	003B03H	003D03H	003F03H				
003704H	003904H	003B04H	003D04H	003F04H	Receive/transmit error counter	RTEC	R	00000000B 00000000B
003705H	003905H	003B05H	003D05H	003F05H				
003706H	003906H	003B06H	003D06H	003F06H	Bit timing register	BTR	R/W	X1111111B 11111111B
003707H	003907H	003B07H	003D07H	003F07H				
003708H	003908H	003B08H	003D08H	003F08H	IDE register	IDER	R/W	XXXXXXXXB XXXXXXXXB
003709H	003909H	003B09H	003D09H	003F09H				
00370AH	00390AH	003B0AH	003D0AH	003F0AH	Transmit RTR register	TRTRR	R/W	00000000B 00000000B
00370BH	00390BH	003B0BH	003D0BH	003F0BH				
00370CH	00390CH	003B0CH	003D0CH	003F0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXXB XXXXXXXXB
00370DH	00390DH	003B0DH	003D0DH	003F0DH				
00370EH	00390EH	003B0EH	003D0EH	003F0EH	Transmit interrupt enable register	TIER	R/W	00000000B 00000000B
00370FH	00390FH	003B0FH	003D0FH	003F0FH				
003710H	003910H	003B10H	003D10H	003F10H	Acceptance mask select register	AMSR	R/W	XXXXXXXXB XXXXXXXXB
003711H	003911H	003B11H	003D11H	003F11H				
003712H	003912H	003B12H	003D12H	003F12H				XXXXXXXXB XXXXXXXXB
003713H	003913H	003B13H	003D13H	003F13H				
003714H	003914H	003B14H	003D14H	003F14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXXB XXXXXXXXB
003715H	003915H	003B15H	003D15H	003F15H				
003716H	003916H	003B16H	003D16H	003F16H				XXXXXXXXB XXXXXXXXB
003717H	003917H	003B17H	003D17H	003F17H				
003718H	003918H	003B18H	003D18H	003F18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXXB XXXXXXXXB
003719H	003919H	003B19H	003D19H	003F19H				
00371AH	00391AH	003B1AH	003D1AH	003F1AH				XXXXXXXXB XXXXXXXXB
00371BH	00391BH	003B1BH	003D1BH	003F1BH				

List of Message Buffers (ID Registers) (1)

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003600H to 00361FH	003800H to 00381FH	003A00H to 003A1FH	003C00H to 003C1FH	003E00H to 003E1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003620H	003820H	003A20H	003C20H	003E20H	ID register 0	IDR0	R/W	XXXXXXXXB XXXXXXXXB
003621H	003821H	003A21H	003C21H	003E21H				
003622H	003822H	003A22H	003C22H	003E22H				XXXXXXXXB XXXXXXXXB
003623H	003823H	003A23H	003C23H	003E23H				
003624H	003824H	003A24H	003C24H	003E24H	ID register 1	IDR1	R/W	XXXXXXXXB XXXXXXXXB
003625H	003825H	003A25H	003C25H	003E25H				
003626H	003826H	003A26H	003C26H	003E26H				XXXXXXXXB XXXXXXXXB
003627H	003827H	003A27H	003C27H	003E27H				
003628H	003828H	003A28H	003C28H	003E28H	ID register 2	IDR2	R/W	XXXXXXXXB XXXXXXXXB
003629H	003829H	003A29H	003C29H	003E29H				
00362AH	00382AH	003A2AH	003C2AH	003E2AH				XXXXXXXXB XXXXXXXXB
00362BH	00382BH	003A2BH	003C2BH	003E2BH				
00362CH	00382CH	003A2CH	003C2CH	003E2CH	ID register 3	IDR3	R/W	XXXXXXXXB XXXXXXXXB
00362DH	00382DH	003A2DH	003C2DH	003E2DH				
00362EH	00382EH	003A2EH	003C2EH	003E2EH				XXXXXXXXB XXXXXXXXB
00362FH	00382FH	003A2FH	003C2FH	003E2FH				
003630H	003830H	003A30H	003C30H	003E30H	ID register 4	IDR4	R/W	XXXXXXXXB XXXXXXXXB
003631H	003831H	003A31H	003C31H	003E31H				
003632H	003832H	003A32H	003C32H	003E32H				XXXXXXXXB XXXXXXXXB
003633H	003833H	003A33H	003C33H	003E33H				
003634H	003834H	003A34H	003C34H	003E34H	ID register 5	IDR5	R/W	XXXXXXXXB XXXXXXXXB
003635H	003835H	003A35H	003C35H	003E35H				
003636H	003836H	003A36H	003C36H	003E36H				XXXXXXXXB XXXXXXXXB
003637H	003837H	003A37H	003C37H	003E37H				
003638H	003838H	003A38H	003C38H	003E38H	ID register 6	IDR6	R/W	XXXXXXXXB XXXXXXXXB
003639H	003839H	003A39H	003C39H	003E39H				
00363AH	00383AH	003A3AH	003C3AH	003E3AH				XXXXXXXXB XXXXXXXXB
00363BH	00383BH	003A3BH	003C3BH	003E3BH				
00363CH	00383CH	003A3CH	003C3CH	003E3CH	ID register 7	IDR7	R/W	XXXXXXXXB XXXXXXXXB
00363DH	00383DH	003A3DH	003C3DH	003E3DH				
00363EH	00383EH	003A3EH	003C3EH	003E3EH				XXXXXXXXB XXXXXXXXB
00363FH	00383FH	003A3FH	003C3FH	003E3FH				

List of Message Buffers (ID Registers) (2)

Address		Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003640H	003840H	003A40H	003C40H	003E40H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
003641H	003841H	003A41H	003C41H	003E41H				
003642H	003842H	003A42H	003C42H	003E42H				XXXXXXXXB XXXXXXXXB
003643H	003843H	003A43H	003C43H	003E43H				
003644H	003844H	003A44H	003C44H	003E44H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
003645H	003845H	003A45H	003C45H	003E45H				
003646H	003846H	003A46H	003C46H	003E46H				XXXXXXXXB XXXXXXXXB
003647H	003847H	003A47H	003C47H	003E47H				
003648H	003848H	003A48H	003C48H	003E48H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
003649H	003849H	003A49H	003C49H	003E49H				
00364AH	00384AH	003A4AH	003C4AH	003E4AH				XXXXXXXXB XXXXXXXXB
00364BH	00384BH	003A4BH	003C4BH	003E4BH				
00364CH	00384CH	003A4CH	003C4CH	003E4CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
00364DH	00384DH	003A4DH	003C4DH	003E4DH				
00364EH	00384EH	003A4EH	003C4EH	003E4EH				XXXXXXXXB XXXXXXXXB
00364FH	00384FH	003A4FH	003C4FH	003E4FH				
003650H	003850H	003A50H	003C50H	003E50H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
003651H	003851H	003A51H	003C51H	003E51H				
003652H	003852H	003A52H	003C52H	003E52H				XXXXXXXXB XXXXXXXXB
003653H	003853H	003A53H	003C53H	003E53H				
003654H	003854H	003A54H	003C54H	003E54H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
003655H	003855H	003A55H	003C55H	003E55H				
003656H	003856H	003A56H	003C56H	003E56H				XXXXXXXXB XXXXXXXXB
003657H	003857H	003A57H	003C57H	003E57H				
003658H	003858H	003A58H	003C58H	003E58H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
003659H	003859H	003A59H	003C59H	003E59H				
00365AH	00385AH	003A5AH	003C5AH	003E5AH				XXXXXXXXB XXXXXXXXB
00365BH	00385BH	003A5BH	003C5BH	003E5BH				
00365CH	00385CH	003A5CH	003C5CH	003E5CH	ID register 15	IDR7	R/W	XXXXXXXXB XXXXXXXXB
00365DH	00385DH	003A5DH	003C5DH	003E5DH				
00365EH	00385EH	003A5EH	003C5EH	003E5EH				XXXXXXXXB XXXXXXXXB
00365FH	00385FH	003A5FH	003C5FH	003E5FH				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003660H	003860H	003A60H	003C60H	003E60H	DLC register 0	DLCR0	R/W	XXXXXXXXB
003661H	003861H	003A61H	003C61H	003E61H				
003662H	003862H	003A62H	003C62H	003E62H	DLC register 1	DLCR1	R/W	XXXXXXXXB
003663H	003863H	003A63H	003C63H	003E63H				
003664H	003864H	003A64H	003C64H	003E64H	DLC register 2	DLCR2	R/W	XXXXXXXXB
003665H	003865H	003A65H	003C65H	003E65H				
003666H	003866H	003A66H	003C66H	003E66H	DLC register 3	DLCR3	R/W	XXXXXXXXB
003667H	003867H	003A67H	003C67H	003E67H				
003668H	003868H	003A68H	003C68H	003E68H	DLC register 4	DLCR4	R/W	XXXXXXXXB
003669H	003869H	003A69H	003C69H	003E69H				
00366AH	00386AH	003A6AH	003C6AH	003E6AH	DLC register 5	DLCR5	R/W	XXXXXXXXB
00366BH	00386BH	003A6BH	003C6BH	003E6BH				
00366CH	00386CH	003A6CH	003C6CH	003E6CH	DLC register 6	DLCR6	R/W	XXXXXXXXB
00366DH	00386DH	003A6DH	003C6DH	003E6DH				
00366EH	00386EH	003A6EH	003C6EH	003E6EH	DLC register 7	DLCR7	R/W	XXXXXXXXB
00366FH	00386FH	003A6FH	003C6FH	003E6FH				
003670H	003870H	003A70H	003C70H	003E70H	DLC register 8	DLCR8	R/W	XXXXXXXXB
003671H	003871H	003A71H	003C71H	003E71H				
003672H	003872H	003A72H	003C72H	003E72H	DLC register 9	DLCR9	R/W	XXXXXXXXB
003673H	003873H	003A73H	003C73H	003E73H				
003674H	003874H	003A74H	003C74H	003E74H	DLC register 10	DLCR10	R/W	XXXXXXXXB
003675H	003875H	003A75H	003C75H	003E75H				
003676H	003876H	003A76H	003C76H	003E76H	DLC register 11	DLCR11	R/W	XXXXXXXXB
003677H	003877H	003A77H	003C77H	003E77H				
003678H	003878H	003A78H	003C78H	003E78H	DLC register 12	DLCR12	R/W	XXXXXXXXB
003679H	003879H	003A79H	003C79H	003E79H				
00367AH	00387AH	003A7AH	003C7AH	003E7AH	DLC register 13	DLCR13	R/W	XXXXXXXXB
00367BH	00387BH	003A7BH	003C7BH	003E7BH				
00367CH	00387CH	003A7CH	003C7CH	003E7CH	DLC register 14	DLCR14	R/W	XXXXXXXXB
00367DH	00387DH	003A7DH	003C7DH	003E7DH				
00367EH	00387EH	003A7EH	003C7EH	003E7EH	DLC register 15	DLCR15	R/W	XXXXXXXXB
00367FH	00387FH	003A7FH	003C7FH	003E7FH				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003680H to 003687H	003880H to 003887H	003A80H to 003A87H	003C80H to 003C87H	003E80H to 003E87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
003688H to 00368FH	003888H to 00388FH	003A88H to 003A8FH	003C88H to 003C8FH	003E88H to 003E8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
003690H to 003697H	003890H to 003897H	003A90H to 003A97H	003C90H to 003C97H	003E90H to 003E97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
003698H to 00369FH	003898H to 00389FH	003A98H to 003A9FH	003C98H to 003C9FH	003E98H to 003E9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
0036A0H to 0036A7H	0038A0H to 0038A7H	003AA0H to 003AA7H	003CA0H to 003CA7H	003EA0H to 003EA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
0036A8H to 0036AFH	0038A8H to 0038AFH	003AA8H to 003AAFH	003CA8H to 003CAFH	003EA8H to 003EAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
0036B0H to 0036B7H	0038B0H to 0038B7H	003AB0H to 003AB7H	003CB0H to 003CB7H	003EB0H to 003EB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
0036B8H to 0036BFH	0038B8H to 0038BFH	003AB8H to 003ABFH	003CB8H to 003CBFH	003EB8H to 003EBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
0036C0H to 0036C7H	0038C0H to 0038C7H	003AC0H to 003AC7H	003CC0H to 003CC7H	003EC0H to 003EC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
0036C8H to 0036CFH	0038C8H to 0038CFH	003AC8H to 003ACFH	003CC8H to 003CCFH	003EC8H to 003ECFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
0036D0H to 0036D7H	0038D0H to 0038D7H	003AD0H to 003AD7H	003CD0H to 003CD7H	003ED0H to 003ED7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
0036D8H to 0036DFH	0038D8H to 0038DFH	003AD8H to 003ADFH	003CD8H to 003CDFH	003ED8H to 003EDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
0036E0H to 0036E7H	0038E0H to 0038E7H	003AE0H to 003AE7H	003CE0H to 003CE7H	003EE0H to 003EE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
0036E8H to 0036EFH	0038E8H to 0038EFH	003AE8H to 003AEFH	003CE8H to 003CEFH	003EE8H to 003EEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
0036F0$_H$ to 0036F7$_H$	0038F0$_H$ to 0038F7$_H$	003AF0$_H$ to 003AF7$_H$	003CF0$_H$ to 003CF7$_H$	003EF0$_H$ to 003EF7$_H$	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
0036F8$_H$ to 0036FF$_H$	0038F8$_H$ to 0038FF$_H$	003AF8$_H$ to 003AFF$_H$	003CF8$_H$ to 003CFF$_H$	003EF8$_H$ to 003EFF$_H$	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
Time Base Timer	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
External Interrupt INT0 to INT7	○	#12	FFFFCC$_H$		
CAN 0 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 0 TX/NS	N/A	#14	FFFFC4$_H$		
CAN 1 RX	N/A	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 1 TX/NS	N/A	#16	FFFFBC$_H$		
PPG 0/1 / (CAN 2 RX)	N/A	#17	FFFFB8$_H$	ICR03	0000B3$_H$
PPG 2/3 / (CAN 2 TX/NS)	N/A	#18	FFFFB4$_H$		
PPG 4/5 / (CAN 3 RX)	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
PPG 6/7 / (CAN 3 TX/NS)	N/A	#20	FFFFAC$_H$		
PPG 8/9 / (CAN 4 RX)	N/A	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG A/B / (CAN 4 TX/NS)	N/A	#22	FFFFA4$_H$		
16-bit Reload Timer 0	○	#23	FFFFA0$_H$	ICR06	0000B6$_H$
16-bit Reload Timer 1	○	#24	FFFF9C$_H$		
Input Capture 0/1	○	#25	FFFF98$_H$	ICR07	0000B7$_H$
Output compare 0/1	○	#26	FFFF94$_H$		
Input Capture 2/3 / Output Compare 6	○	#27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 2/3	○	#28	FFFF8C$_H$		
Input Capture 4/5 / Output Compare 7	○	#29	FFFF88$_H$	ICR09	0000B9$_H$
Output Compare 4/5 /I²C	○	#30	FFFF84$_H$		
A/D Converter	○	#31	FFFF80$_H$	ICR10	0000BA$_H$
I/O Timer 0/1 / Watch Timer	N/A	#32	FFFF7C$_H$		
Serial I/O	○	#33	FFFF78$_H$	ICR11	0000BB$_H$
Sound Generator	N/A	#34	FFFF74$_H$		
UART 0 RX	◎	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	○	#36	FFFF6C$_H$		
UART 1 RX	◎	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX	○	#38	FFFF64$_H$		

(Continued)

(Continued)

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
(UART 2 RX) / UART 3 RX	◎	#39	FFFF60H	ICR14	0000BEH
(UART 2 TX) / UART 3 TX	○	#40	FFFF5CH		
Flash Memory	N/A	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt	N/A	#42	FFFF54H		

○ : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

◎ : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Note : For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH ≥ AVRL
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} \geq DV_{CC}$
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	–4.0	+4.0	mA	*6
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*6
“L” level maximum output current	I_{OL1}	—	15	mA	Normal outputs*4
“L” level average output current	I_{OLAV1}	—	4	mA	Normal outputs, average value
“L” level maximum output current	I_{OL2}	—	40	mA	High current outputs*5
“L” level average output current	I_{OLAV2}	—	30	mA	High current outputs, average value
“L” level maximum overall output current	ΣI_{OL1}	—	100	mA	Sum of all normal outputs
“L” level maximum overall output current	ΣI_{OL2}	—	330	mA	Sum of all high current outputs
“L” level average overall output current	ΣI_{OLAV1}	—	50	mA	Sum of all normal outputs, average value
“L” level average overall output current	ΣI_{OLAV2}	—	250	mA	Sum of all high current outputs, average value
“H” level maximum output current	I_{OH1}	—	–15	mA	Normal outputs*4
“H” level average output current	I_{OHAV1}	—	–4	mA	Normal outputs, average value
“H” level maximum output current	I_{OH2}	—	–40	mA	High current outputs*5
“H” level average output current	I_{OHAV2}	—	–30	mA	High current outputs, average value
“H” level maximum overall output current	ΣI_{OH1}	—	–100	mA	Sum of all normal outputs
“H” level maximum overall output current	ΣI_{OH2}	—	–330	mA	Sum of all high current outputs
“H” level average overall output current	ΣI_{OHAV1}	—	–50	mA	Sum of all normal outputs, average value
“H” level average overall output current	ΣI_{OHAV2}	—	–250	mA	Sum of all high current outputs, average value
Power consumption	P_D	—	800	mW	MB90F394H(A)/MB90394HA
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

(Continued)

(Continued)

*1 : The parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

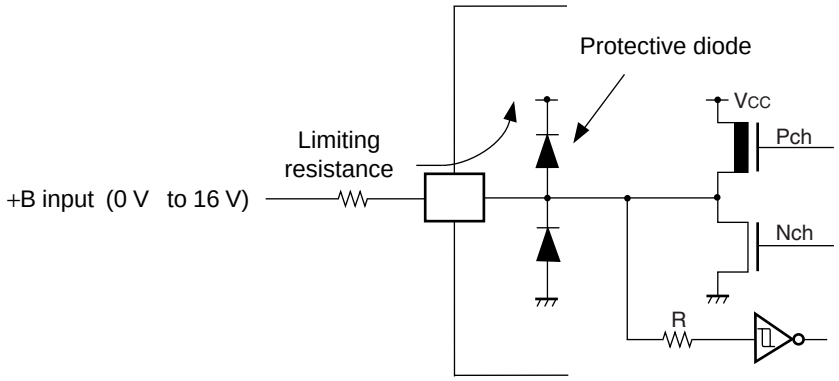
*3 : V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. For ports P70 to P77, P80 to P87 and PA0 to PA7, V_I and V_O should not exceed DV_{CC} + 0.3 V.

*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P90 to P97, PB0 to PB7

*5 : Applicable to pins : P70 to P77, P80 to P87, PA0 to PA7

*6 :
- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67 P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

- Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

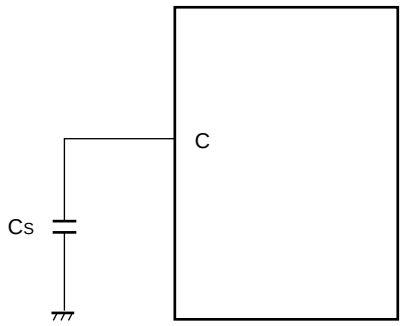
2. Recommended Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation
		4.0	5.0	5.5	V	Under normal operation, when not using the A/D converter
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not programming or erasing Flash
		2.0	—	5.5	V	Retain RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	MB90F394H(A)/MB90394HA*
Operating temperature	T_A	–40	—	+85	°C	

* : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the V_{CC} pin (pin 15) , use a bypass capacitor that has a larger capacity than that of C_S. On the other V_{CC} pin (pin 105) , use a bypass capacitor of about 0.1 µF.
Refer to the following figure for connection of smoothing capacitor C_S.

- **C Pin Connection Diagram**



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS Hysteresis input levels are selected (except SIN and I^2C pins of MB90394HA)
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	MB90394HA : SIN (UART, SIO) and I^2C input pins if CMOS Hysteresis levels are selected
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if AUTOMOTIVE Hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS Hysteresis input levels are selected (except SIN and I^2C pins of MB90394HA)
	V_{ILS}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	MB90394HA : SIN (UART, SIO) and I^2C input pins if CMOS Hysteresis levels are selected
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Port inputs if AUTOMOTIVE Hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Output “H” voltage	V_{OH1}	Normal outputs	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	

(Continued)

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “H” voltage	V_{OH2}	High current outputs	DV_{CC} = 4.5 V, I_{OH2} = –40.0 mA	DV_{CC} – 0.5	—	—	V	T_A = – 40 °C
			DV_{CC} = 4.5 V, I_{OH2} = –30.0 mA					T_A = + 25 °C
			DV_{CC} = 4.5 V, I_{OH2} = –30.0 mA					T_A = + 85 °C
Output “L” voltage	V_{OL1}	Normal outputs	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
Output “L” voltage	V_{OL2}	High current outputs	DV_{CC} = 4.5 V, I_{OL2} = 40.0 mA	—	—	0.5	V	T_A = – 40 °C
			DV_{CC} = 4.5 V, I_{OL2} = 30.0 mA					T_A = + 25 °C
			DV_{CC} = 4.5 V, I_{OL2} = 30.0 mA					T_A = + 85 °C
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	+ 5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 20 MHz, At normal operation.	—	50	70	mA	MB90394HA/ MB90F394H(A)
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	60	85	mA	MB90394HA/ MB90F394H(A)
			V_{CC} = 5.0 V, Internal frequency : 20 MHz, At writing Flash memory.	—	65	85	mA	MB90F394H(A)
			V_{CC} = 5.0 V, Internal frequency : 20 MHz, At erasing Flash memory.	—	70	90	mA	MB90F394H(A)
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	27	36	mA	MB90394HA/ MB90F394H(A)

(Continued)

(Continued)

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CTS}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 2 MHz, At Main Timebase timer mode	—	0.3	0.55	mA	MB90394HA/ MB90F394H(A)
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL Timebase timer mode, external frequency = 4 MHz	—	5	7	mA	MB90394HA/ MB90F394H(A)
	I_{CCH}		V_{CC} = 5.0 V, At Stop mode, T_A = +25°C	—	5	30	µA	MB90394HA/ MB90F394H(A)
Input capacitance	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P77, P80 to P87, PA0 to PA7	—	—	5	15	pF	
		P70 to P77, P80 to P87, PA0 to PA7	—	—	15	30	pF	

* : The power supply current is measured with an external clock.

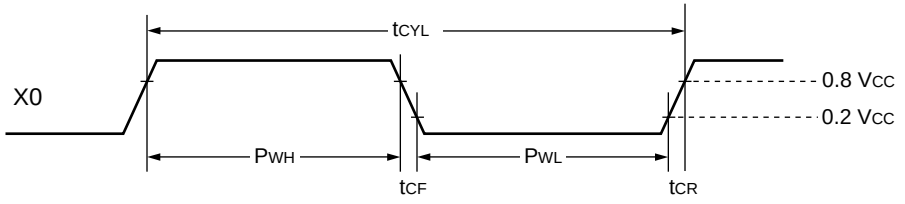
4. AC Characteristics

(1) Clock Timing

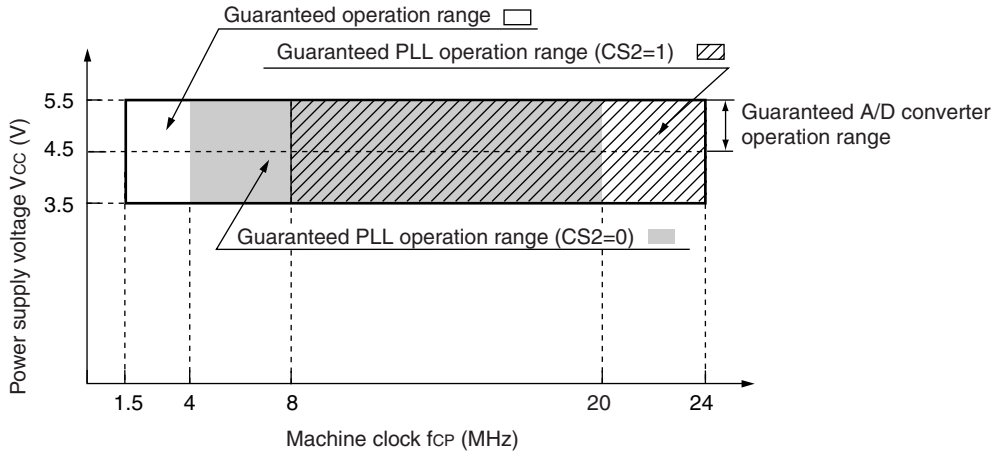
(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	8	MHz	When using a crystal oscillator or a ceramic oscillator
		X0	3	—	12	MHz	When using an external clock
Clock cycle time	t_{CYL}	X0, X1	125	—	333	ns	When using a crystal oscillator or a ceramic oscillator
		X0	83.33	—	333	ns	When using an external clock
Input clock pulse width	P_{WH}, P_{WL}	X0	20	—	—	ns	Duty ratio is about 30% to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	24	MHz	Except programming or erasing Flash memory. When using clock modulation, be sure that the maximum momentary frequency Fmax does not exceed 24 MHz. Refer to the Clock Modulator chapter of the Hardware Manual.
		—	1.5	—	20	MHz	When programming or erasing Flash memory. Be sure that the maximum momentary frequency Fmax does not exceed 20 MHz.
Machine clock cycle time	t_{CP}	—	41.67	—	666	ns	Except programming or erasing Flash memory.
		—	50	—	666	ns	When programming or erasing Flash memory.

- **Clock Timing**

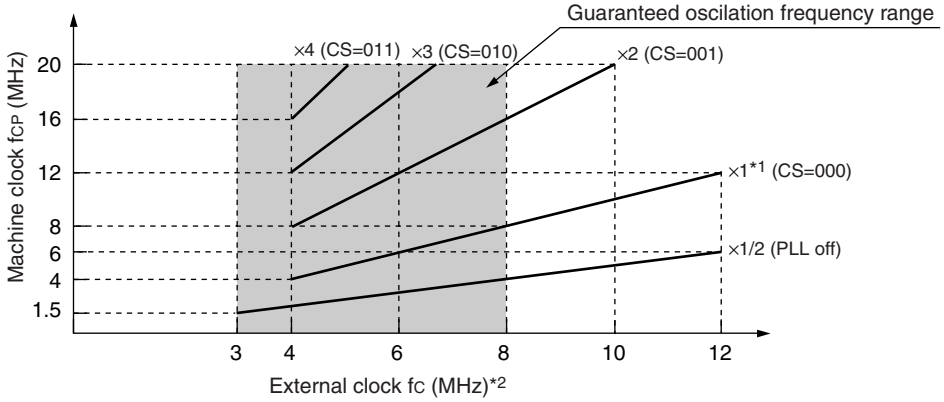


• Guaranteed PLL operation range

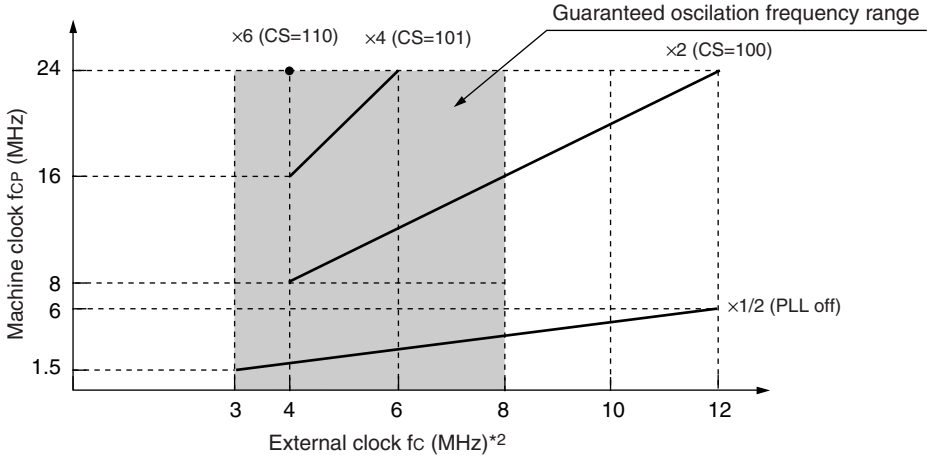


Guaranteed operation range of MB90394HA/MB90F394H(A)

• CS2 (bit 0 in PSCCR register) = 0



• CS2 (bit 0 in PSCCR register) = 1



*1 : PLL × 1 guaranteed operation range is from 4.0 MHz to 12 MHz.

*2 : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 8 MHz

External clock frequency and Machine clock frequency

(2) Reset Standby Input

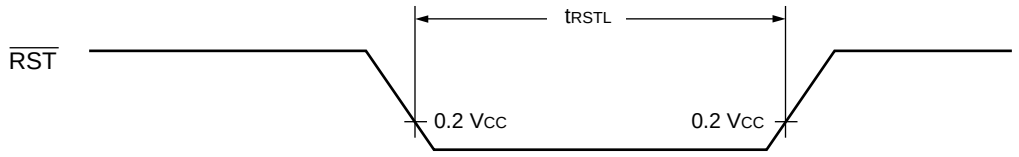
(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 100 µs + 16 t_{CP}*1	—	ns	In Stop mode
			100	—	µs	In Time Base Timer mode

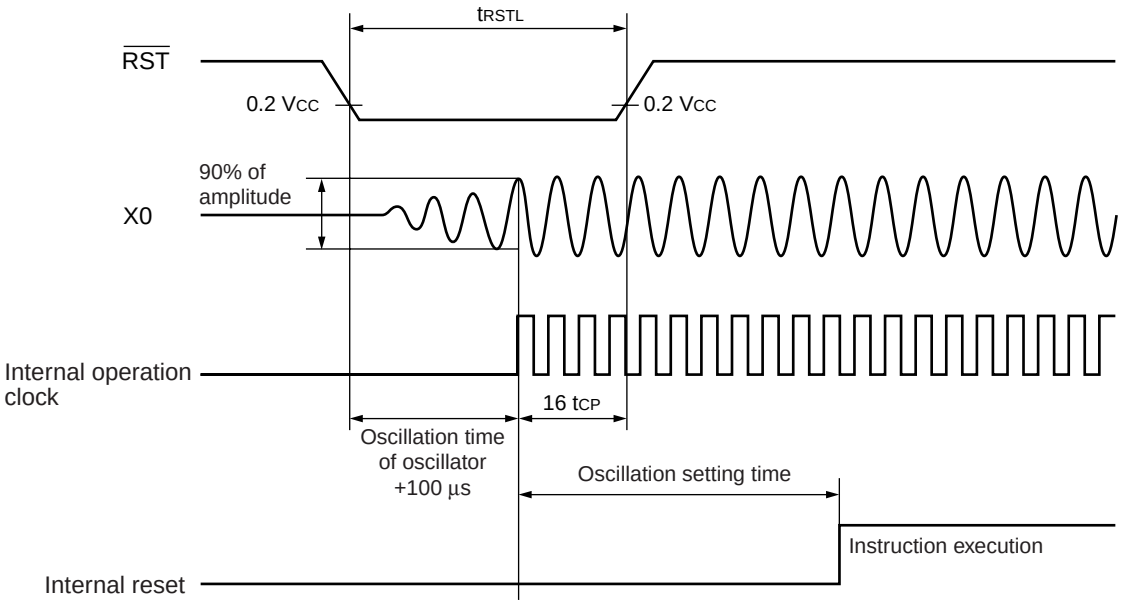
*1 : t_{CP} is the machine clock cycle time. Refer to " (1) Clock timing".
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms.

- **Under Normal Operation**



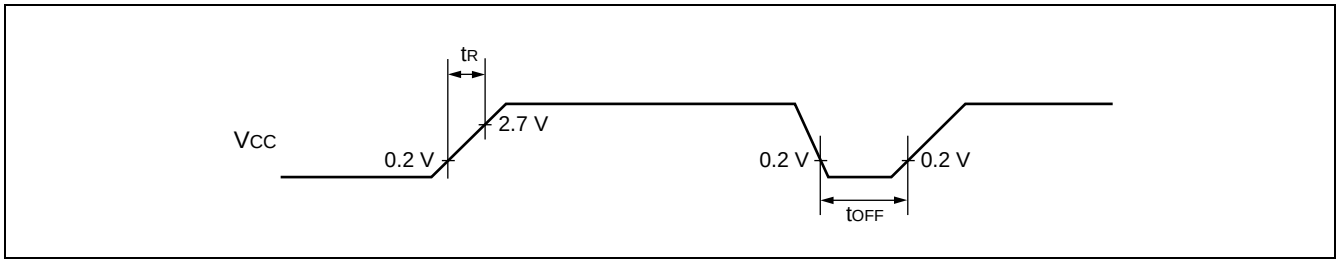
- **In Stop Mode**



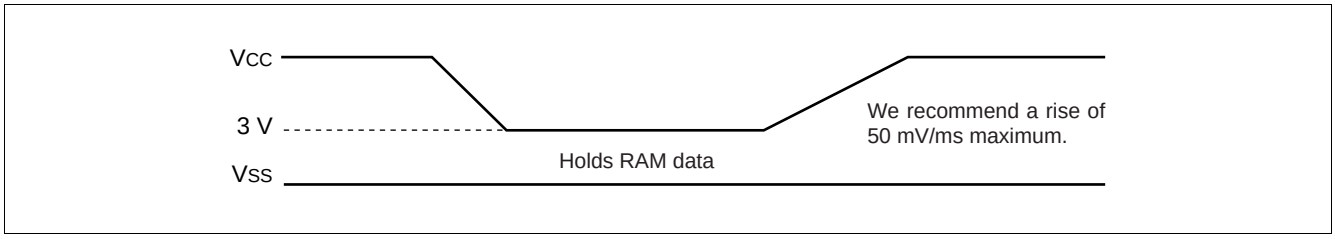
(3) Power On Reset

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Wait time until power on



Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



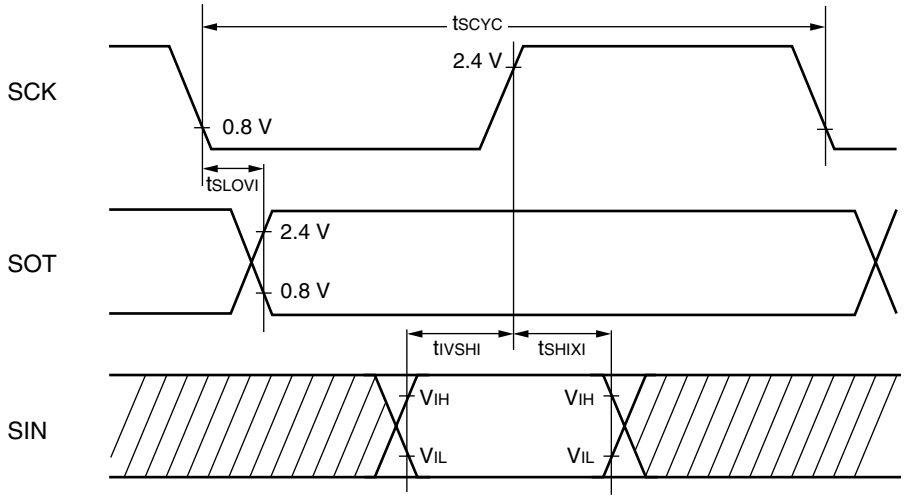
(4) UART0/1 and Serial I/O Timing

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

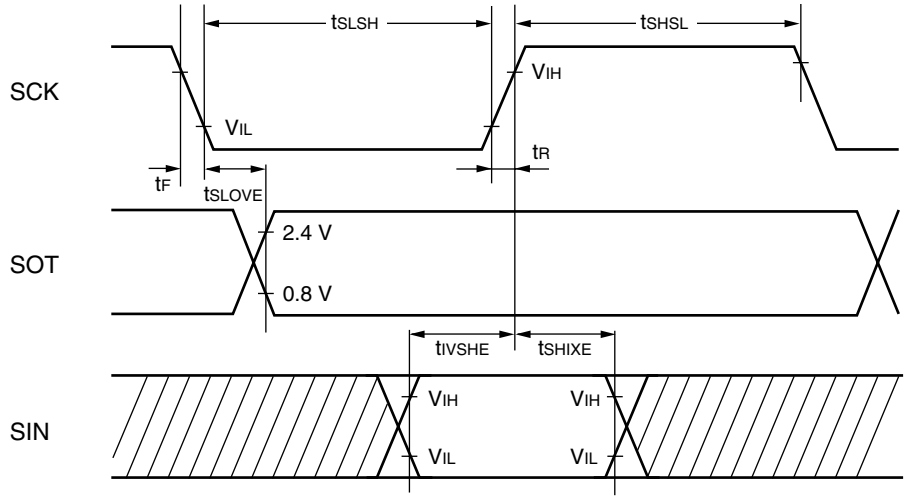
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK4	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SCK4, SOT0, SOT1, SOT4		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSHI}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1, SCK4	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1, SCK4		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0, SCK1, SCK4, SOT0, SOT1, SOT4		—	150	ns	
Valid SIN → SCK ↑	t_{IVSHE}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	

Notes :
- Above rating is the case of CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**



(5) UART2/3 (LIN/SCI)

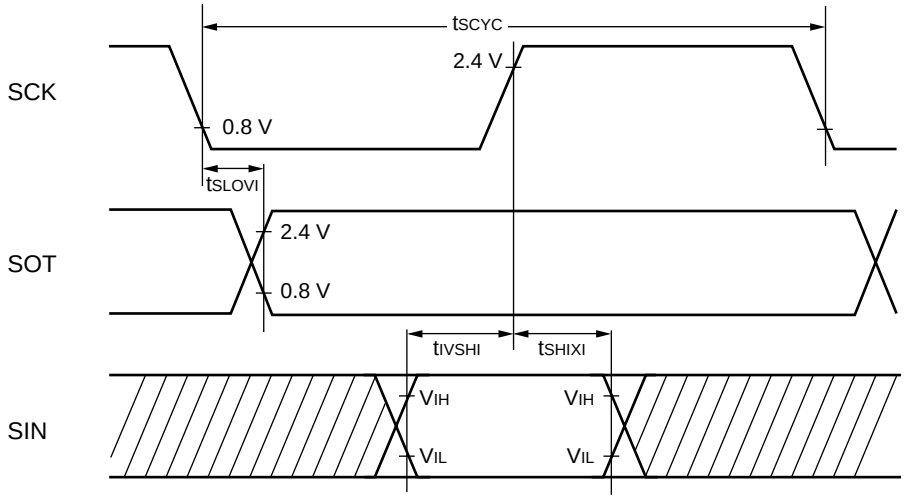
- **Bit setting** : **ESCR2/3** : **SCES** = **0**, **ECCR2/3** : **SCDE** = **0**

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

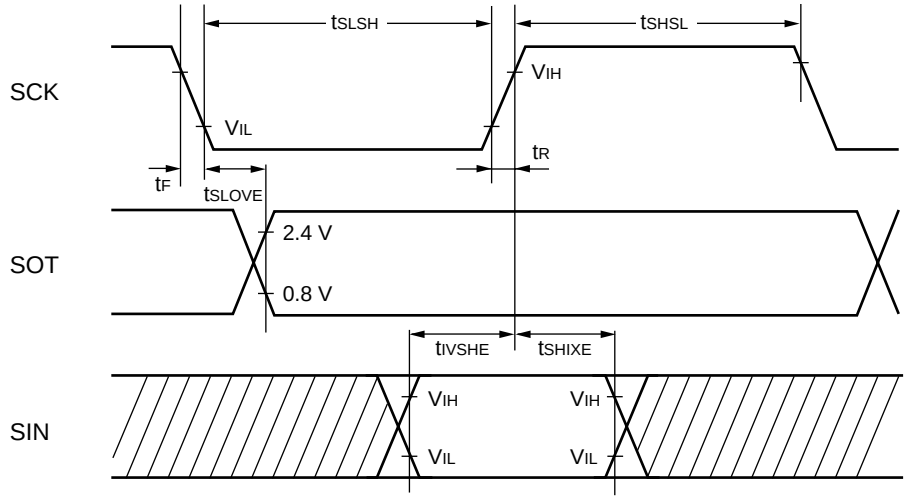
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2/3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2/3, SOT2/3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2/3, SIN2/3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2/3, SIN2/3		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK2/3	External clock operation output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} – t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK2/3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2/3, SOT2/3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK2/3, SIN2/3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK2/3, SIN2/3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK2/3		—	10	ns
SCK rise time	t_R	SCK2/3		—	10	ns

Notes :
- C_L is load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
- t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**



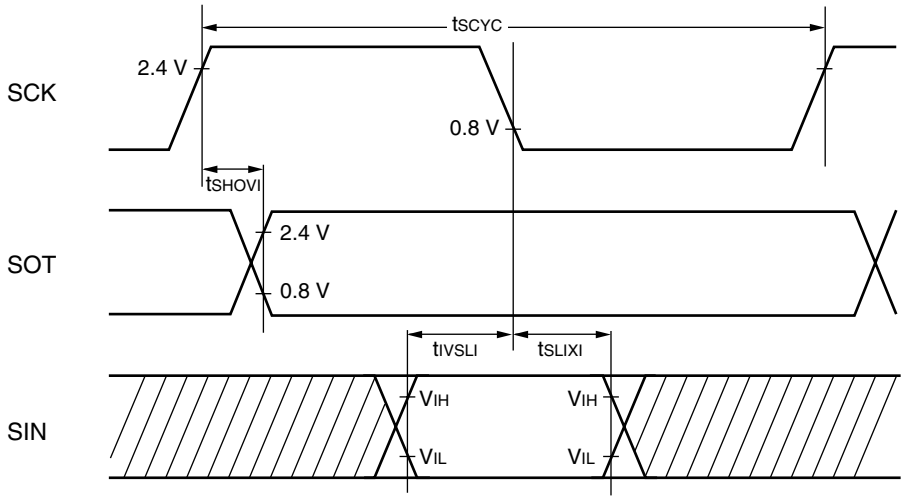
- **Bit setting** : **ESCR2/3** : **SCES** = **1**, **ECCR2/3** : **SCDE** = **0**

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

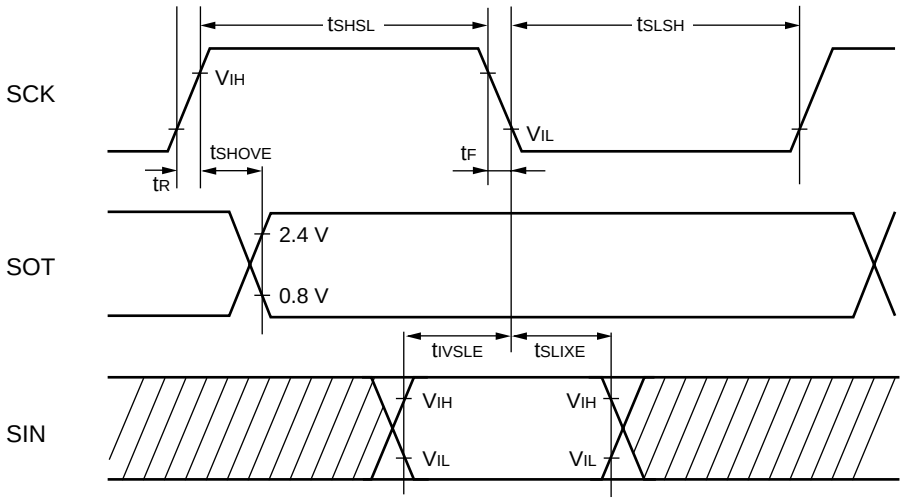
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2/3	Internal clock operation output pins are C_L = 80 pF + 1 TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2/3, SOT2/3		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK2/3, SIN2/3		t_{CP}+80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2/3, SIN2/3		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK2/3	External clock operation output pins are C_L = 80 pF + 1 TTL	3 t_{CP}–t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK2/3		t_{CP}+10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2/3, SOT2/3		—	2 t_{CP}+60	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK2/3, SIN2/3		30	—	ns
SCK↓ →Valid SIN hold time	t_{SLIXE}	SCK2/3, SIN2/3		t_{CP}+30	—	ns
SCK fall time	t_F	SCK2/3		—	10	ns
SCK rise time	t_R	SCK2/3		—	10	ns

Notes :
- C_L is load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
- t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

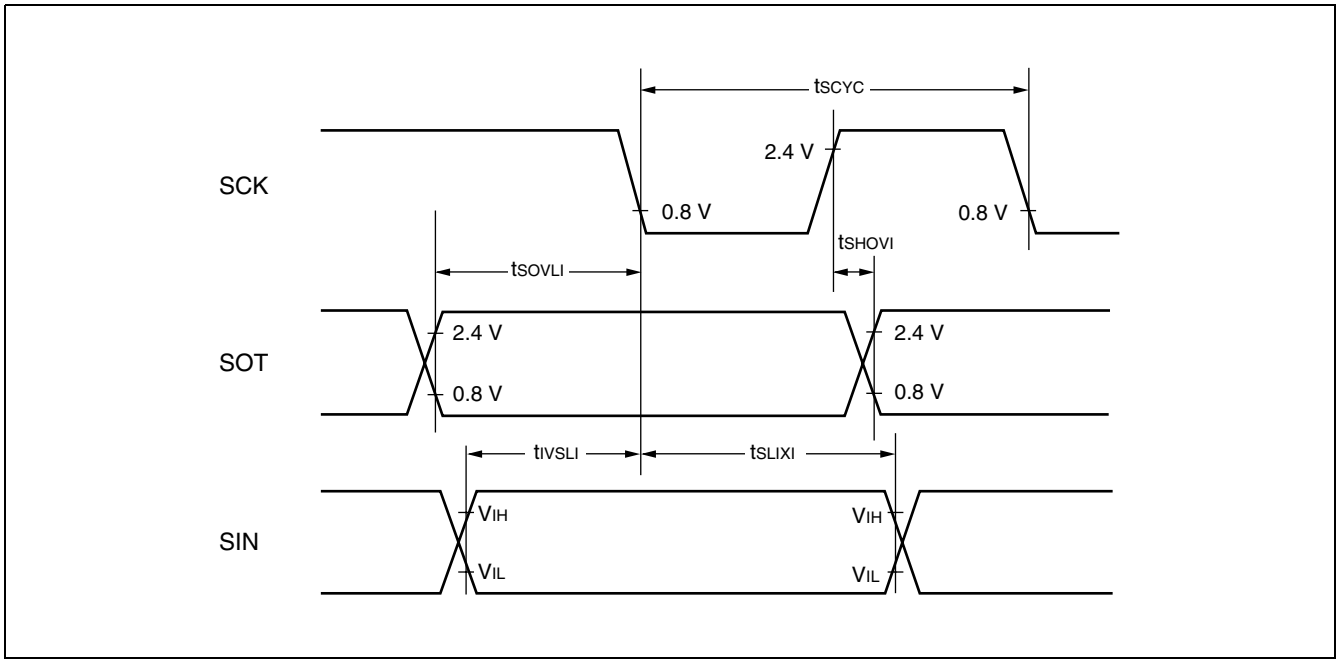


- **Bit setting** : **ESCR2/3** : **SCES** = **0**, **ECCR2/3** : **SCDE** = **1**

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2/3	Internal clock operation output pins are C_L = 80 pF + 1 TTL	5 t_{CP}	—	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2/3, SOT2/3		–50	+50	ns	MB90394HA, MB90V390HA/HB
				t_{CP} – 60	t_{SCYC}/2 + 70 – t_{CP}	ns	MB90F394H(A), MB90V390H
Valid SIN → SCK↓	t_{IVSLI}	SCK2/3, SIN2/3		t_{CP} + 80	—	ns	MB90394HA, MB90V390HA/HB
				100 – t_{CP}	—	ns	MB90F394H(A), MB90V390H
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2/3, SIN2/3		0	—	ns	MB90394HA, MB90V390HA/HB
				t_{SCYC}/2	—	ns	MB90F394H(A), MB90V390H
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2/3, SOT2/3		3 t_{CP} – 70	—	ns	MB90394HA, MB90V390HA/HB
				t_{CP} – 60	—	ns	MB90F394H(A), MB90V390H

Notes :
- C_L is load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
- t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.

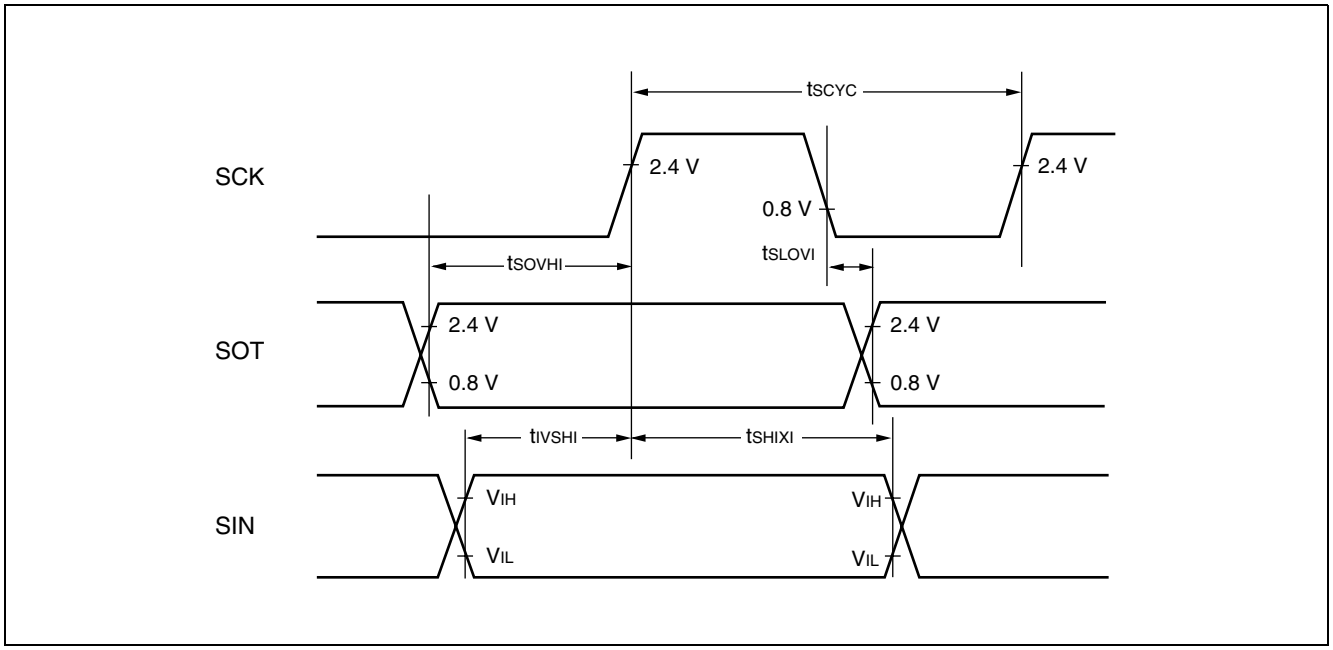


- **Bit setting** : **ESCR2/3** : **SCES** = **1**, **ECCR2/3** : **SCDE** = **1**

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2/3	Internal clock operation output pins are C_L = 80 pF + 1 TTL	5 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2/3, SOT2/3		–50	+50	ns	MB90394HA, MB90V390HA/HB
				t_{CP} – 60	t_{SCYC}/2 + 70 – t_{CP}	ns	MB90F394H(A), MB90V390H
Valid SIN → SCK↓	t_{IVSHI}	SCK2/3, SIN2/3		t_{CP} + 80	—	ns	MB90394HA, MB90V390HA/HB
				100 – t_{CP}	—	ns	MB90F394H(A), MB90V390H
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2/3, SIN2/3		0	—	ns	MB90394HA, MB90V390HA/HB
				t_{SCYC}/2	—	ns	MB90F394H(A), MB90V390H
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2/3, SOT2/3		3t_{CP} – 70	—	ns	MB90394HA, MB90V390HA/HB
				t_{CP} – 60	—	ns	MB90F394H(A), MB90V390H

Notes :
- C_L is load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
- t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.



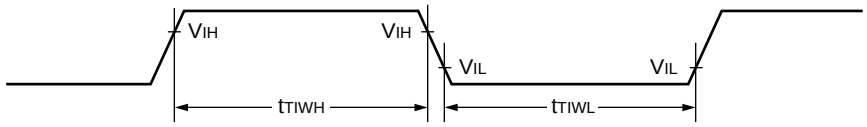
(6) Timer Related Resource Input Timing

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN5					

Note : t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.

- **Timer Input Timing**



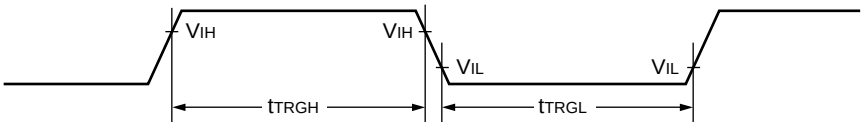
(7) Trigger Input Timing

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7	—	200	—	ns	
	t_{TRGL}	ADTG	—	t_{CP} + 200	—	ns	

Note : t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing”.

- **Trigger Input Timing**

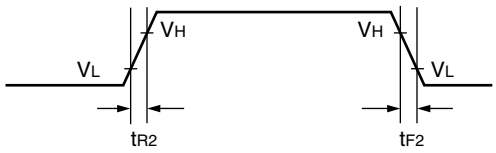


(8) Slew Rate High Current Outputs

(T_A = –40 °C to +85 °C, V_{CC} = DV_{CC} = 3.5 V to 5.5 V, V_{SS} = DV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	P70 to P77, P80 to P87, PA0 to PA7	—	15	—	—	ns	

- **Slew Rate Output Timing**



$V_H = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

$V_L = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$

(9) I²C Timing

(T_A = –40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

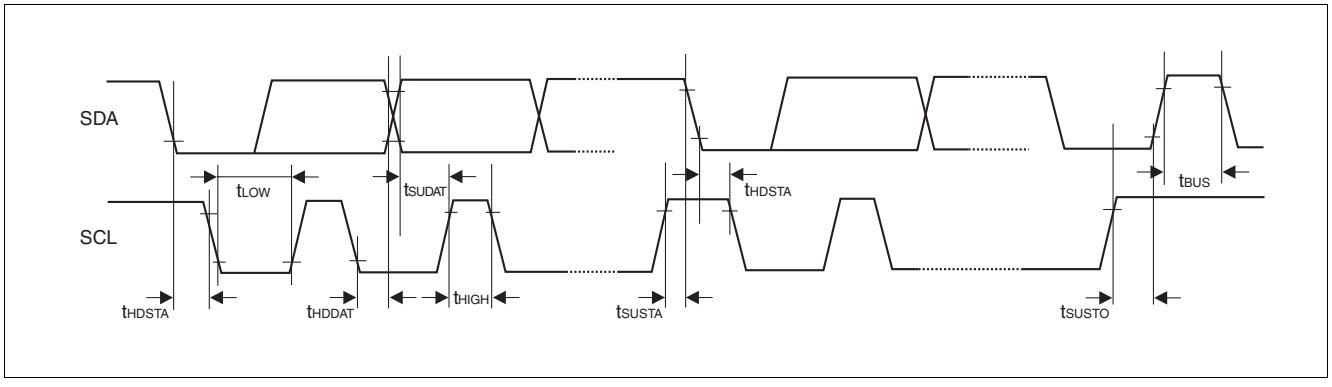
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.3 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



5. A/D Converter

(T_A = –40 °C to +85 °C, 3.0 V ≤ AVRH – AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Compare time	—	—	3.3	—	16500	µs	
			—	3.3 (= 66 t_{CP})	—	µs	f_{CP} = 20 MHz
			—	3.7 (= 88 t_{CP})	—	µs	f_{CP} = 24 MHz
Sampling time	—	—	1.6	—	∞	µs	
			—	1.6 (= 32 t_{CP})	—	µs	f_{CP} = 20 MHz
			—	2 (= 48 t_{CP})	—	µs	f_{CP} = 24 MHz
Analog port input current	I_{AIN}	AN0 to AN14	–1	—	+1	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH – 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	165	250	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Terminology

Conversion error : Absolute maximum conversion deviation with respect to the theoretical conversion line.

Nonlinearity : Relative maximum conversion deviation with respect to the theoretical conversion line connecting to the device unique zero reading voltage and full scale reading voltage.

Differential nonlinearity : Max conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.

Zero reading voltage : Input voltage which results in the minimum conversion value.

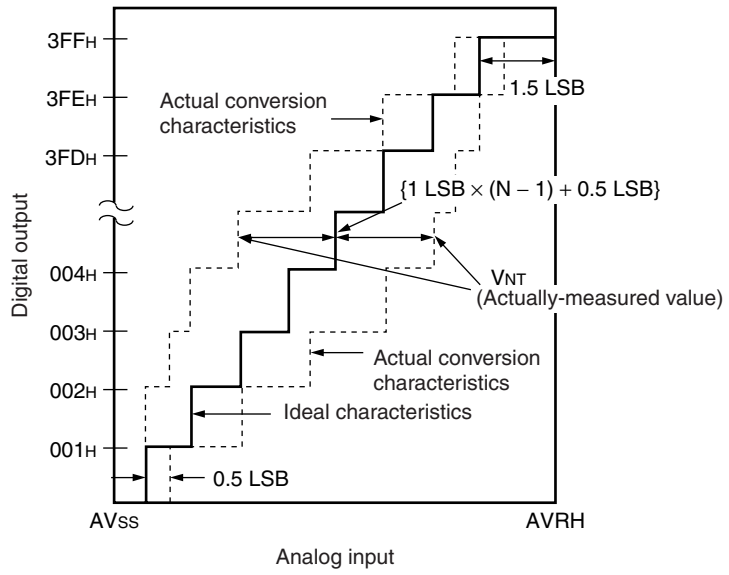
Full scale reading voltage : Input voltage which results in the maximum conversion value.

Notes :
- The accuracy gets worse as AVRH – AVRL becomes smaller.
- t_{CP} is the machine clock cycle time. Refer to “ (1) Clock timing” in “4. AC Characteristics”.

6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Linear error	:	Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.
Differential linear error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVRH - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

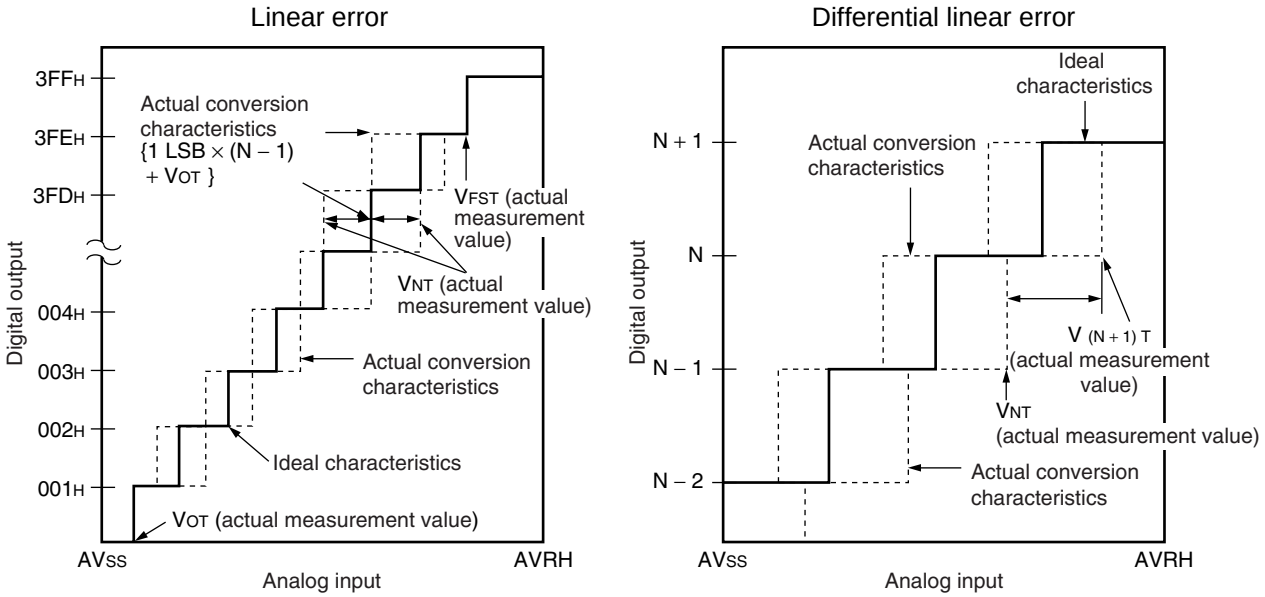
V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

V_{FST} (Ideal value) $= AVRH - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

(Continued)

(Continued)



$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value

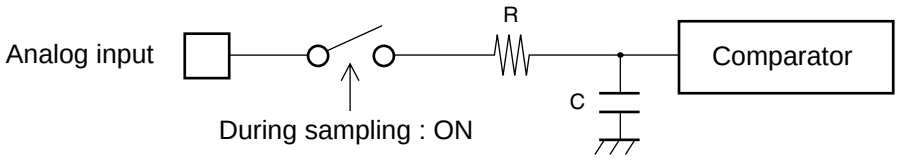
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Notes on A/D Converter Section

• About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

• Analog input circuit model

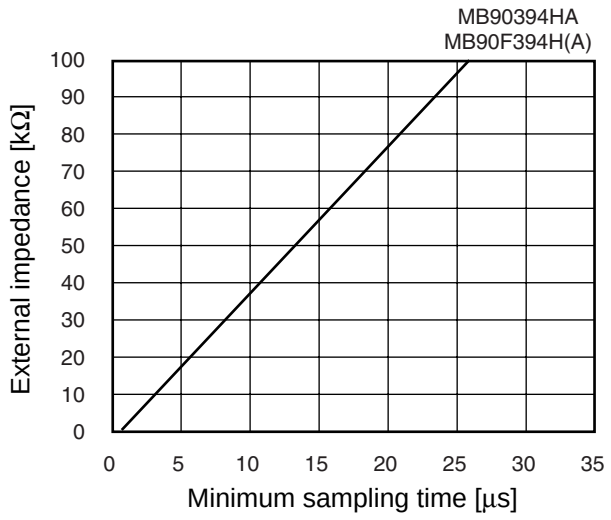


	R	C
MB90394HA/MB90F394H/MB90F394HA	2.4 kΩ (Max)	36.4 pF (Max)

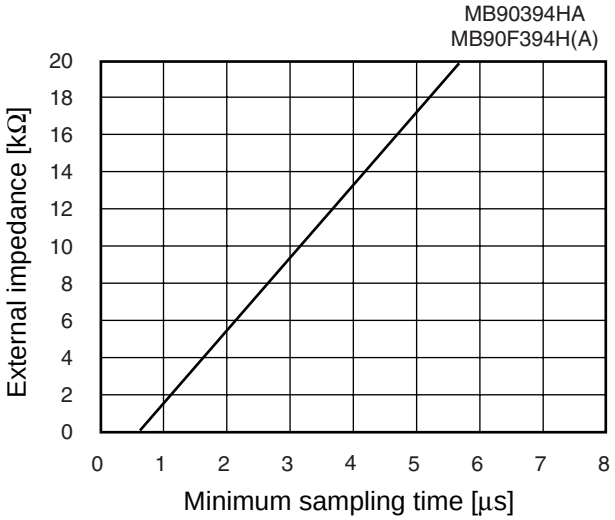
Note : The values are reference values.

• The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



• About the error

The accuracy gets worse as |AVRH − AVRL| becomes smaller.

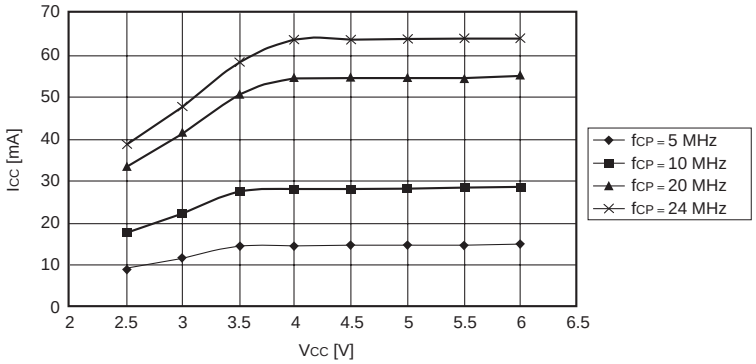
8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Mln	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes 00_H programming prior to erasure.
Chip erase time		—	9	—	s	MB90F394H, Excludes 00_H programming prior to erasure.
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system.
Programs/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

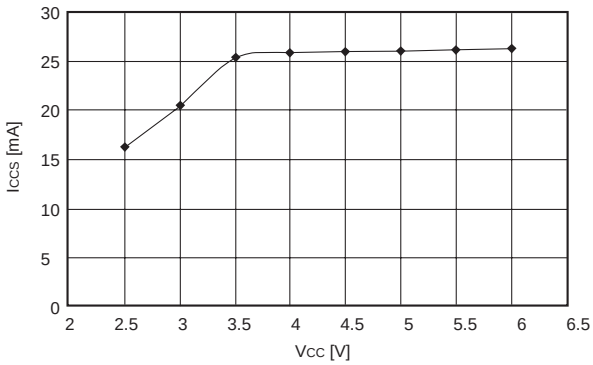
* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ EXAMPLE CHARACTERISTICS

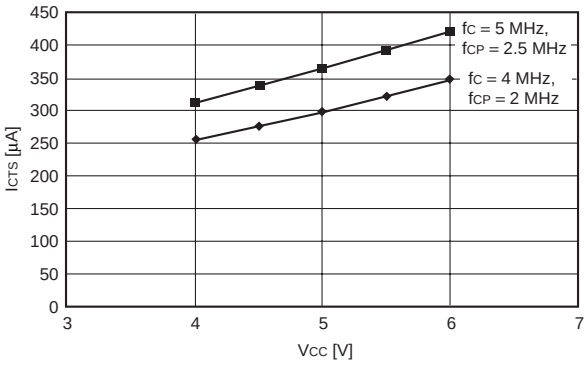
I_{CC} - V_{CC} (T_A = +25 °C)



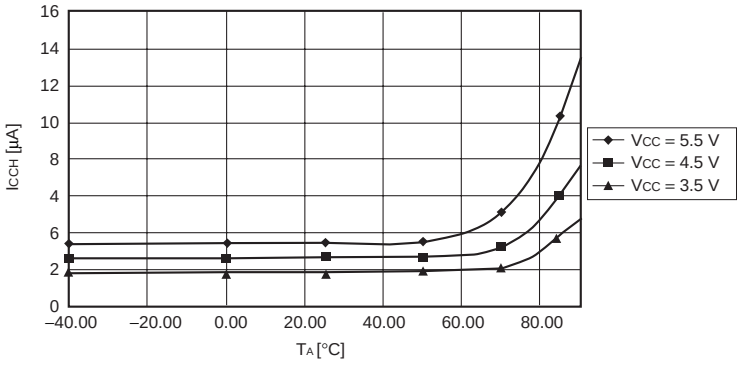
I_{CCS} - V_{CC} (T_A = +25 °C, f_C = 4 MHz, f_{CP} = 24 MHz)



I_{CTS} - V_{CC} (T_A = +25 °C)



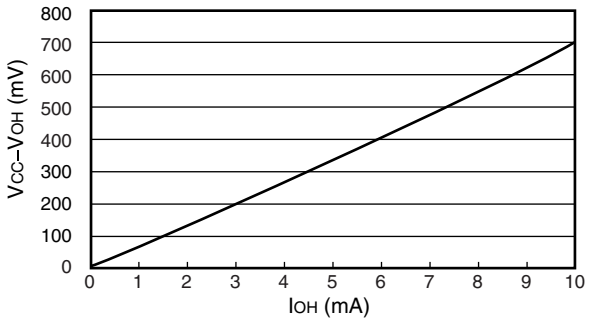
I_{CCH} - T_A



- I/O characteristics

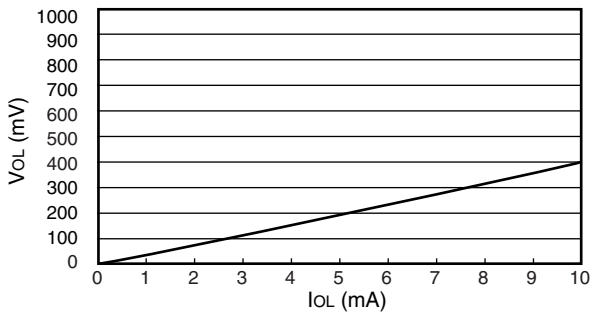
$(V_{CC}–V_{OH})$ – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



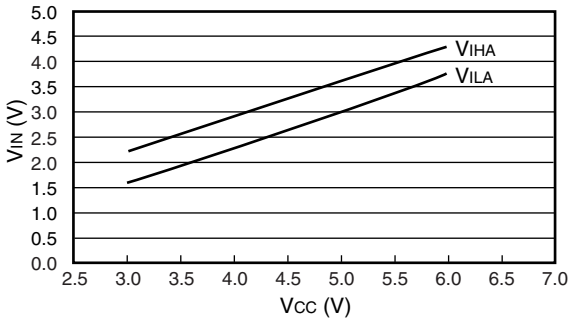
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



Automotive V_{IN} – V_{CC}

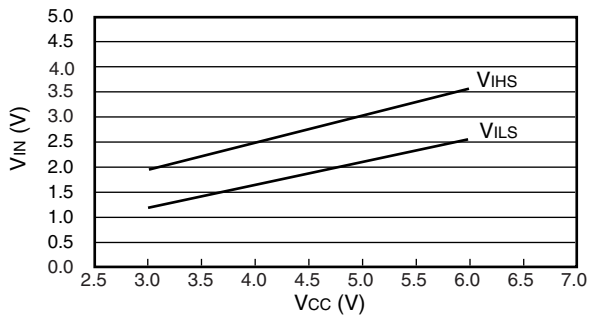
T_A = +25 °C



CMOS V_{IN} – V_{CC}

Except UART-SIN pins and I²C pins of MB90394HA

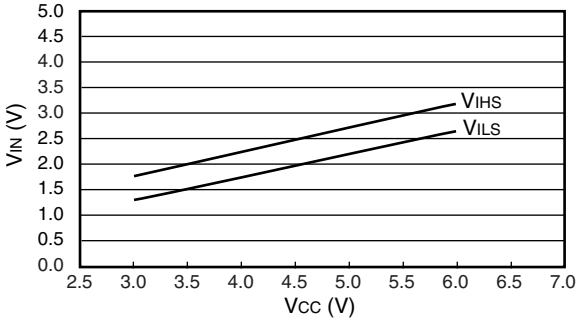
T_A = +25 °C



CMOS V_{IN} – V_{CC}

UART-SIN pins and I²C pins of MB90394HA

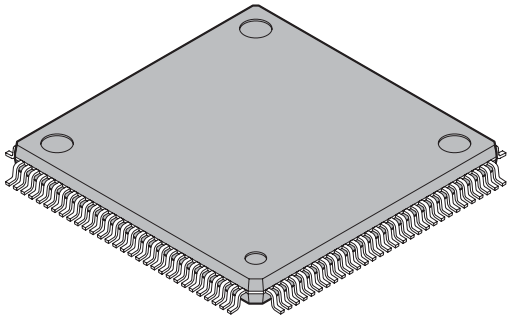
T_A = +25 °C



■ ORDERING INFORMATION

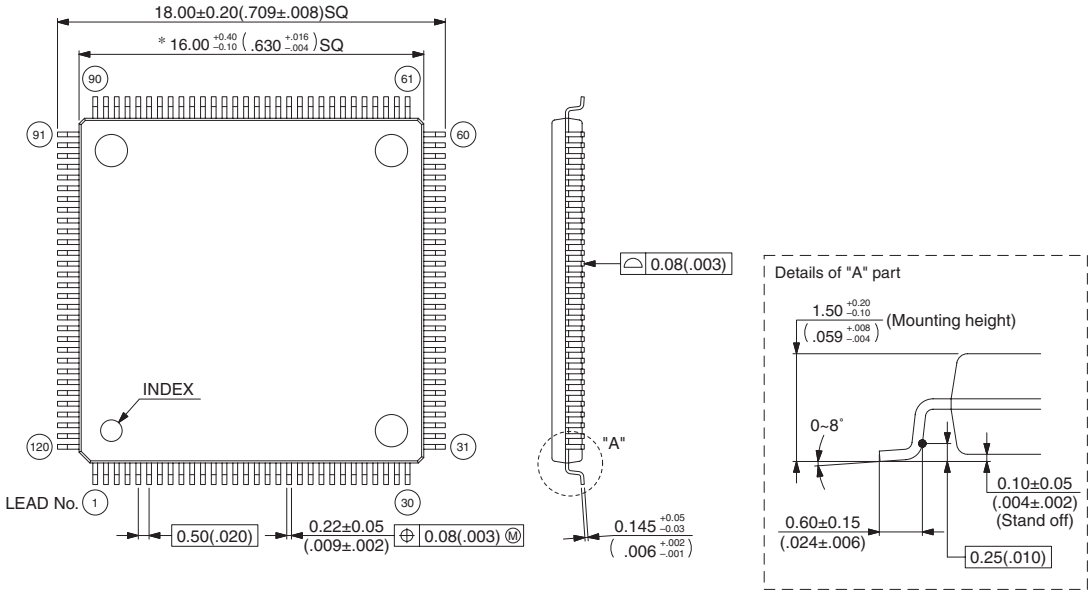
Part number	Package	Remarks
MB90F394HPMT	120-pin Plastic LQFP (FPT-120P-M21)	It is recommended to use MB90F394HA, because MB90F394H does not support frequency modulation, clock modulation and CAN message buffer RAM at the same time.
MB90F394HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90394HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90V390HACR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation It is recommended to use MB90V390HB, because MB90V390HA does not support clock modulation and CAN message buffer RAM at the same time.
MB90V390HBCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation
MB90V390HCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation It is recommended to use MB90V390HB, because MB90V390H does not support clock modulation and CAN message buffer RAM at the same time.

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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