CY8C20180

CapSense Express™ -8 Configurable IOs

Features

- 8 configurable IOs supporting
  - CapSense buttons
  - LED Drive
  - Interrupt outputs
  - WAKE on interrupt input
  - User defined input or output
- 2.4V to 5.25V operating voltage
- Industrial temperature range: –40°C to +85°C
- I^2C slave interface for configuration
  - Selectable to 50 kHz,100 kHz and 400 kHz
- Reduce BOM cost
  - Internal oscillator - no external oscillators or crystal
  - Free development tool - no external tuning components
- Low operating current
  - Active current: continuous sensor scan:1.5 mA
  - Sleep current: no scan, continuous sleep: 2.6 uA
- Available in 16-pin COL and 16-pin SOIC packages

Overview

The CapSense Express™ controller allows the control of 8 IOs configurable as capacitive sensing buttons or as GPIOs for driving LEDs or interrupt signals based on various button conditions. The GPIOs are also configurable for waking up the device from sleep based on an interrupt input.

The user has the ability to configure buttons, outputs, and parameters through specific commands sent to the I^2C port. The IOs have the flexibility in mapping to capacitive buttons and as standard GPIO functions such as interrupt output or input, LED drive and digital mapping of input to output using simple logical operations. This enables easy PCB trace routing and reduces the PCB size and stack up. CapSense Express products are designed for easy integration into complex products.

Architecture

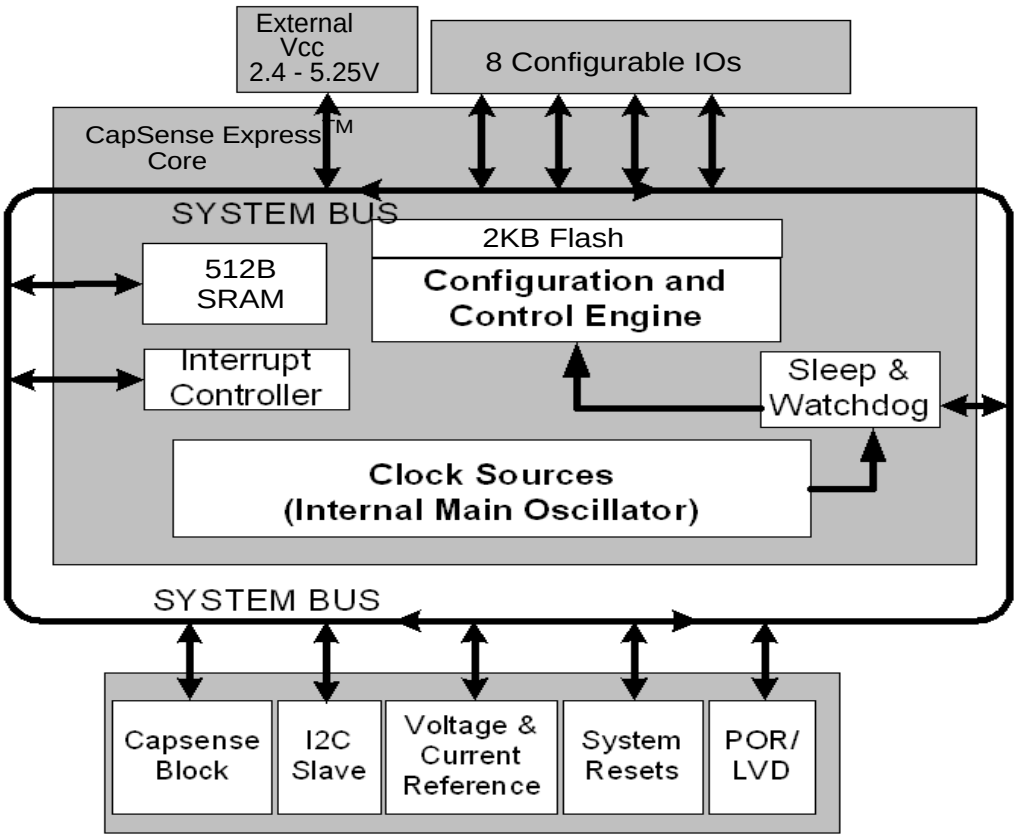
The logic block diagram illustrates the internal architecture of CY8C20180.

The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense system. CY8C20180 supports a standard I^2C serial communications interface that allows the host to configure the device and to read sensor information in real time through easy register access.

The CapSense Express Core

The CapSense Express Core has a powerful configuration and control block. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers. System resources provide additional capability, such as a configurable I^2C slave communication interface and various system resets. The Analog System is composed of the CapSense PSoC block which supports capacitive sensing of up to eight inputs.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 16 Pin COL

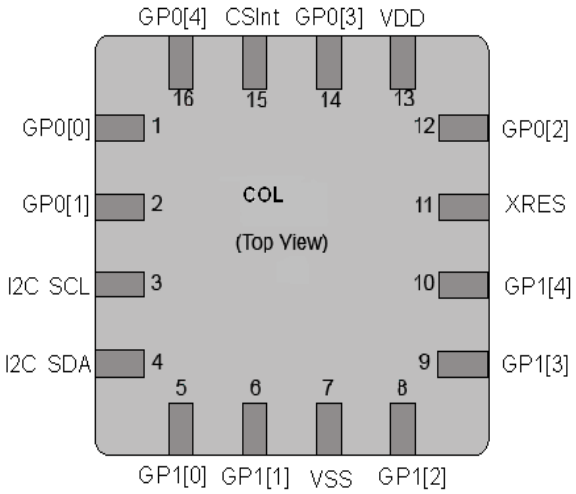


Table 1. Pin Definitions - 16 Pin COL

Pin Number	Name	Description
1	GP0[0]	Configurable as CapSense or GPIO
2	GP0[1]	Configurable as CapSense or GPIO
3	I^2C SCL	I^2C clock
4	I^2C SDA	I^2C data
5	GP1[0]	Configurable as CapSense or GPIO
6	GP1[1]	Configurable as CapSense or GPIO
7	VSS	Ground connection
8	GP1[2]	Configurable as CapSense or GPIO
9	GP1[3]	Configurable as CapSense or GPIO
10	GP1[4]	Configurable as CapSense or GPIO
11	XRES	Active HIGH external reset with internal pull down
12	GP0[2]	Configurable as CapSense or GPIO
13	V_{DD}	Supply voltage
14	GP0[3]	Configurable as CapSense or GPIO
15	CSInt	Integrating Input.The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 10-100 nF.
16	GP0[4]	Configurable as CapSense or GPIO

Figure 2. Pin Diagram - 16 Pin SOIC

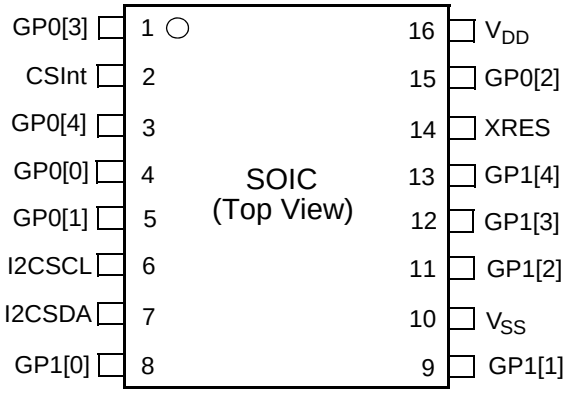


Table 2. Pin Definitions - 16 Pin SOIC

Pin Number	Name	Description
1	GP0[3]	Configurable as CapSense or GPIO
2	CSInt	Integrating Input.The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 10-100 nF.
3	GP0[4]	Configurable as CapSense or GPIO
4	GP0[0]	Configurable as CapSense or GPIO
5	GP0[1]	Configurable as CapSense or GPIO
6	I^2C SCL	I^2C clock
7	I^2C SDA	I^2C data
8	GP1[0]	Configurable as CapSense or GPIO
9	GP1[1]	Configurable as CapSense or GPIO
10	VSS	Ground connection
11	GP1[2]	Configurable as CapSense or GPIO
12	GP1[3]	Configurable as CapSense or GPIO
13	GP1[4]	Configurable as CapSense or GPIO
14	XRES	Active HIGH external reset with internal pull down.
15	GP0[2]	Configurable as CapSense or GPIO
16	V_{DD}	Supply voltage

The CapSense Analog System

The CapSense analog system contains the capacitive sensing hardware. which supports CapSense Successive Approximation (CSA) algorithm.This hardware performs capacitive sensing and scanning without external components. Capacitive sensing is configurable on each pin.

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources are low voltage detection and power on reset (POR).

- The I^2C slave provides 50, 100, or 400 kHz communication over two wires.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels and the advanced POR circuit eliminates the need for a system supervisor.

An internal 1.8V reference provides a stable internal reference so that capacitive sensing functionality is not affected by minor V_{DD} changes.

I^2C Interface

The two modes of operation for the I^2C interface are:

- Device register configuration and status read or write for controller.
- Command execution.

The I^2C address is programmable during configuration. It can be locked to prevent accidental change by setting a flag in a configuration register.

CapSense Express Software Tool

An easy to use software tool integrated with PSoC Express is available for configuring and tuning CapSense Express devices. Refer to the Application Note AN42137 for details of the software tool.

CapSense Express Register Map

CapSense Express supports user configurable registers through which the device functionality and parameters are configured. For details, refer to CY8C201xx Register Reference document.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C (0°C to 50°C). Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient temperature with power applied	–40	–	+85	ºC	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any GPIO pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	

DC Electrical Characteristics

DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0V, T_A = 25°C
I_{SB}	Sleep mode current with POR and LVD active. Mid temperature range	–	2.6	4	µA	V_{DD} = 2.55V, 0°C ≤ T_A ≤ 40°C
I_{SB}	Sleep mode current with POR and LVD active.	–	2.8	5	µA	V_{DD} = 3.3V, –40°C ≤ T_A ≤ 85°C
I_{SB}	Sleep mode current with POR and LVD active.	–	5.2	6.4	µA	V_{DD} = 5.25V, –40°C ≤ T_A ≤ 85°C

5 and 3.3V DC General Purpose IO Specifications

This Table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C≤ TA≤85°C, 3.0V to 3.6V and -40°C≤TA≤85°C respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0 pins	V_{DD} – 0.2	–	–	V	IOH = 10 µA, V_{DD} ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH2}	High output voltage Port 0 pins	V_{DD} – 0.9	–	–	V	IOH = 1 mA, V_{DD} ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH3}	High output voltage Port 1 pins	V_{DD} – 0.2	–	–	V	IOH < 10 µA, V_{DD}≥ 3.0V, maximum of 10 mA source current in all IOs.
V_{OH}	High output voltage Port 1 pins	V_{DD} – 0.9	–	–	V	IOH = 5 mA, V_{DD}≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH5}	High output voltage. Port 1 pins with 3.0V LDO regulator enabled	2.75	3.0	3.2	V	IOH < 10 µA, V_{DD}≥ 3.1V, maximum of 4 IOs all sourcing 5mA.
V_{OH6}	High Output Voltage Port 1 pins with 3.0V LDO regulator enabled	2.2	–	–	V	IOH = 5 mA, V_{DD}≥ 3.1V, maximum of 20 mA source current in all IOs.
V_{OH7}	High Output Voltage. Port 1 pins with 2.4V LDO regulator enabled	2.1	2.4	2.5	V	IOH < 10 µA, V_{DD}≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OH8}	High Output Voltage. Port 1 pins with 2.4V LDO regulator enabled	2	–	–	V	IOH < 200 µA, V_{DD} ≥ 3.0V, maximum of 20 mA source current in all IOs.
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 20 mA, V_{DD} > 3V, maximum of 60 mA sink current on even port pins and 60 mA sink current on odd port pins
VIL	Input low voltage	–	–	0.75	V	V_{DD} = 3 to 3.6V
VIH	Input high voltage	1.6	–	–	V	V_{DD} = 3 to 3.6V
V_{IL}	Input low voltage	–	–	0.8	V	V_{DD} = 3.6 to 5.25V.
V_{IH}	Input high voltage	2.0	–	–	V	V_{DD} = 3.6 to 5.25V.
V_H	Input hysteresis voltage	–	140	–	mV	

5 and 3.3V DC General Purpose IO Specifications (continued)

This Table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C≤ TA≤85°C, 3.0V to 3.6V and -40°C≤TA≤85°C respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
IL	Input leakage	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C

2.7 V DC General Purpose IO Specifications

This Table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 3.0V and -40°C≤. TA ≤85°C, respectively. Typical parameters apply to 2.7V at 25°C. These are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0 pins	V_{DD} – 0.2	–	–	V	IOH ≤ 10 µA, maximum of 10 mA source current in all IOs.
V_{OH2}	High output voltage Port 0 pins	V_{DD} – 0.5	–	–	V	IOH = 0.2 mA, maximum of 10 mA source current in all IOs.
V_{OH3}	High output voltage Port 1 pins	V_{DD} – 0.2	–	–	V	IOH < 10 µA, maximum of 10 mA source current in all IOs.
V_{OH4}	High output voltage Port 1 pins	V_{DD} – 0.5	–	–	V	IOH = 2 mA, maximum of 10 mA source current in all IOs.
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 10 mA, maximum of 30 mA sink current on even port pins and 30 mA sink current on odd port pins
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	IOL=5mA Maximum of 50mA sink current on even port pins and 50mA sink current on odd port pins 2.4≤Vdd≤3.6V
V_{IL}	Input low voltage	–	–	0.75	V	V_{DD} = 2.4 to 3.6V.
V_{IH1}	Input high voltage	1.4	–	–	V	V_{DD} = 2.4 to 2.7V.
V_{IH2}	Input high voltage	1.6			V	V_{DD} = 2.7 to 3.6V.
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load On Pins As Input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C.

DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	V_{DD} Value PPOR Trip V_{DD}= 2.7V V_{DD}= 3.3V,5V	 – –	 2.36 2.60	 2.40 2.65	 V V	V_{DD} must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
VLVD0 VLVD2 VLVD6	V_{DD} Value for LVD trip V_{DD}= 2.7V V_{DD}= 3.3V V_{DD}= 5V	 2.39 2.75 3.98	 2.45 2.92 4.05	 2.51 2.99 4.12	 V V V	

AC Electrical Characteristics

5.0V and 3.3V AC General Purpose IO Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise0	Rise time, strong mode, Cload = 50pF, Port 0	15	80	ns	V_{DD} = 3.0V to 3.6V and 4.75V to 5.25V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50pF, Port 1	10	50	ns	V_{DD} = 3.0V to 3.6V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50pF, all ports	10	50	ns	V_{DD} = 3.0V to 3.6V and 4.75V to 5.25V, 10% - 90%

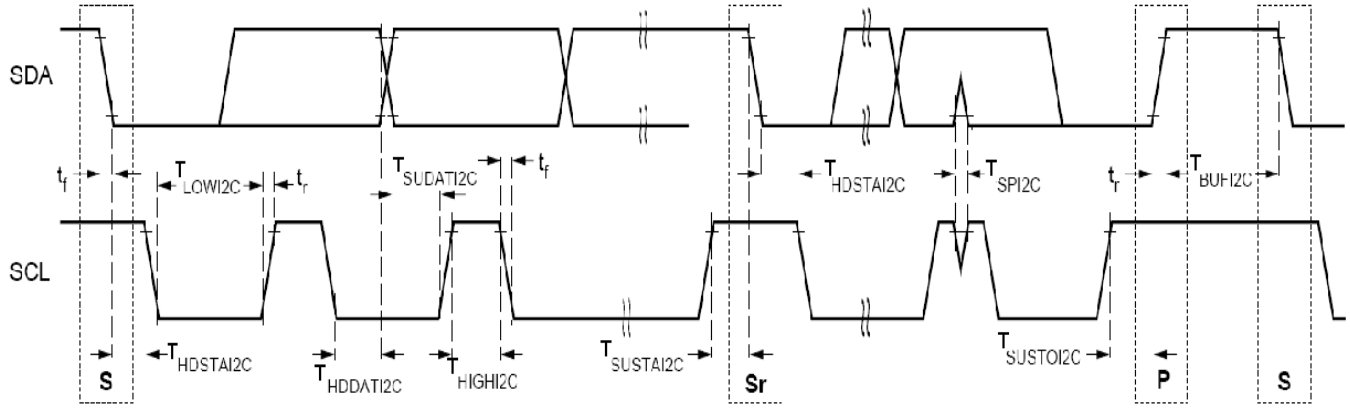
2.7V AC General Purpose IO Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise0	Rise time, strong mode, Cload = 50pF, Port 0	15	100	ns	V_{DD} = 2.4V to 3.0V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50pF, Port 1	10	70	ns	V_{DD} = 2.4V to 3.0V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50pF, all ports	10	70	ns	V_{DD} = 2.4V to 3.0V, 10% - 90%

AC I^2C Specifications

Parameter	Description	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	KHz	Fast mode not supported for V_{DD} < 3.0V
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data setup time	250	–	100	–	ns	
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	BUS free time between a STOP and START condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	

Figure 3. Definition for Timing for Fast/Standard Mode on the I2C Bus



Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature
CY8C20180-LDX2I	001-09116	16 COL[3]	Industrial
CY8C20180-SX2I	51-85068	16 SOIC	Industrial

Thermal Impedances by Package

Package	Typical θ_{JA}[1]
16 COL[3]	46 °C
16 SOIC	79.96 °C

Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[2]	Maximum Peak Temperature
16 COL[3]	240 °C	260 °C
16 SOIC	240 °C	260 °C

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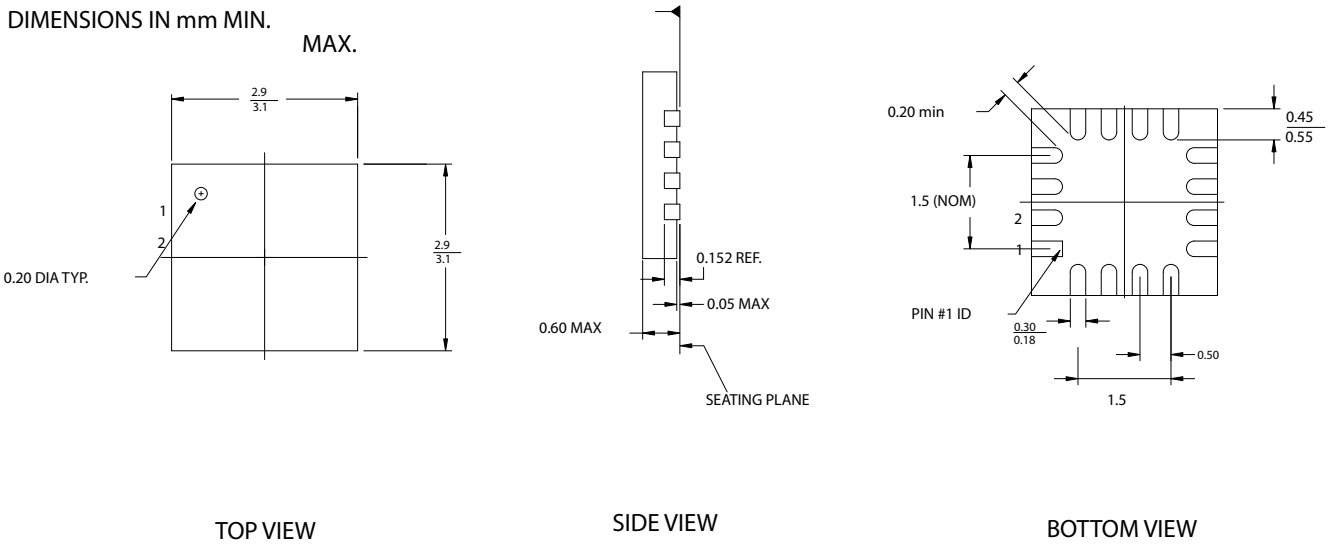
Notes
1. $T_J = T_A$ + Power x $\theta_{JA.}$
2. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.
3. Earlier termed as QFN package.

Package Diagram

Figure 4. 16L Chip On Lead 3 X 3 mm Package Outline (SAWN) - 001-09116 - (Pb-Free)

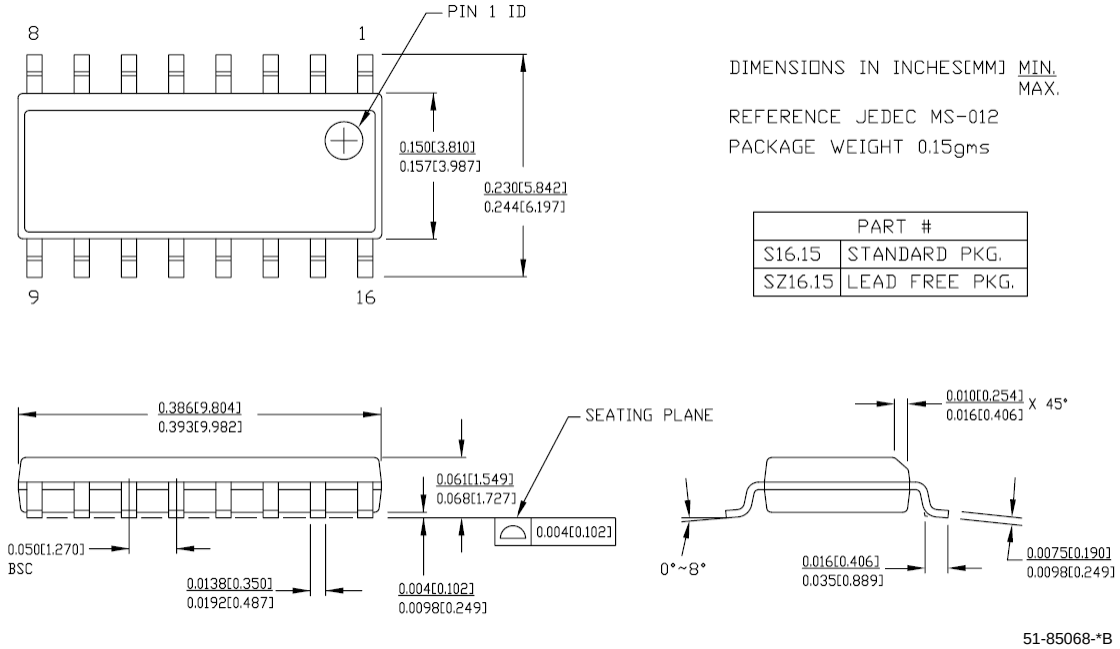


PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

JEDEC # MO-220
Package Weight: 0.014g

001-09116-*C

Figure 5. 16 - Pin (150-Mil) SOIC (51-85068)



51-85068-*B

Document History Page

Document Title: CY8C20180 CapSense Express™ -8 Configurable IOs Document Number: 001-17346			
REV.	**ECN.**	**Orig. of Change**	**Description of Change**
**	1341766	TUP/FSU	New Data Sheet
*A	1494145	TUP/AESA	Changed to FINAL Datasheet Removed table - 2.7V DC General Purpose IO Specifications - Open Drain with a pull up to 1.8V Updated Logic Block Diagram
*B	1773608	TUP/AESA	Removed table - 3V DC General Purpose IO Specifications Updated Logic Block Diagram Updated table - DC POR and LVD Specifications Updated table - DC Chip Level Specifications Updated table - 5V and 3.3V DC General Purpose IO Specifications Updated table - 2.7V DC General Purpose IO Specifications Updated table - AC GPIO Specifications and split it into two tables for 5V/3.3V and 2.7V Added section on CapSense Express™ Software tool Updated 16-QFN Package Diagram
*C	2091026	DZU/MOHD /AESA	Updated table-DC Chip Level Specifications Updated table-Pin Definitions 16 pin COL Updated table-Pin Definitions 16 pin SOIC Updated table-5V and 3.3V DC General Purpose IO Specifications Updated table - 2.7V DC General Purpose IO Specifications Changed definition for Timing for Fast/Standard Mode on the I2C Bus diagram