

HVD362

Variable Capacitance Diode for VCO

REJ03G0056-0200
Rev.2.00
Jan 24, 2006

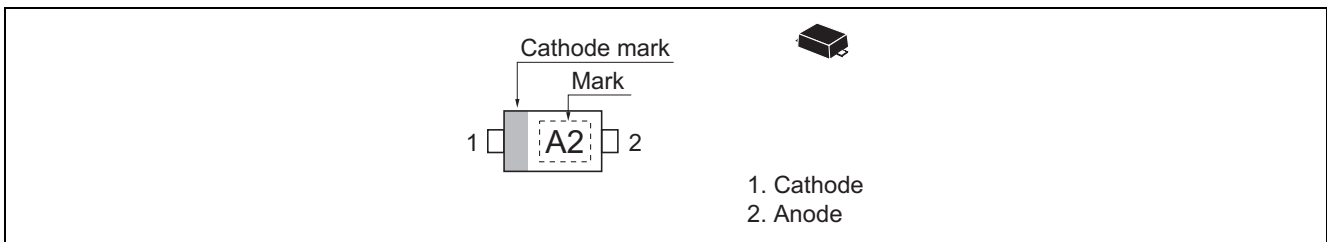
Features

- High capacitance ratio. (n = 3.0 min)
- Good C-V linearity.
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code
HVD362	A2	SFP	PUSF002ZB-A

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V_R	15	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I_{R1}	—	—	10	nA	$V_R = 10\text{ V}$
	I_{R2}	—	—	100		$V_R = 10\text{ V}, T_a = 60^\circ\text{C}$
Capacitance	C_1	41.6	—	49.9	pF	$V_R = 1\text{ V}, f = 1\text{ MHz}$
	C_4	10.1	—	14.8		$V_R = 4\text{ V}, f = 1\text{ MHz}$
Capacitance ratio	n	3.0	—	—	—	C_1 / C_4
Series resistance	r_s	—	—	2.0	Ω	$V_R = 4\text{ V}, f = 100\text{ MHz}$
ESD-Capability ^{*1}	—	80	—	—	V	C = 200pF, Both forward and reverse direction 1 pulse.

Notes: 1. Failure criterion ; $I_R \geq 20\text{nA}$ at $V_R = 10\text{ V}$

2. For SFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

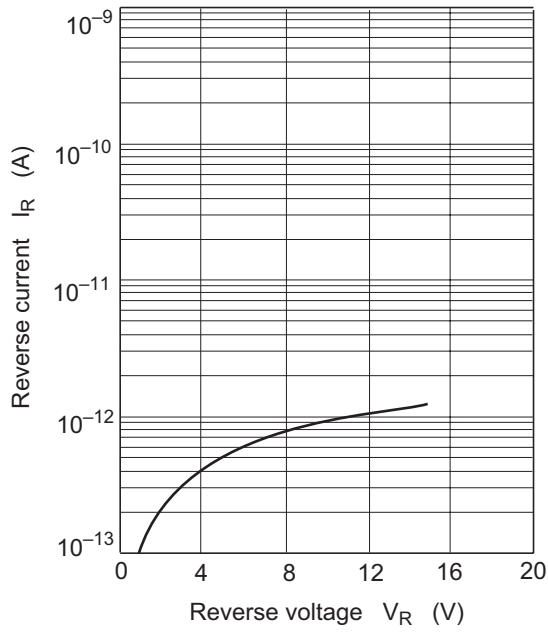


Fig.1 Reverse current vs. Reverse voltage

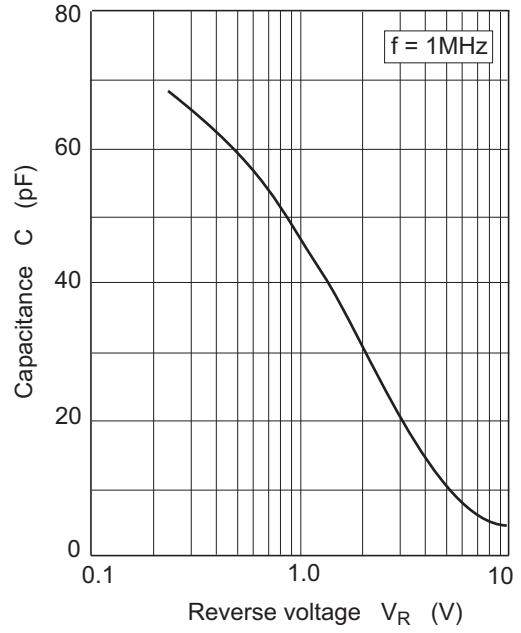


Fig.2 Capacitance vs. Reverse voltage

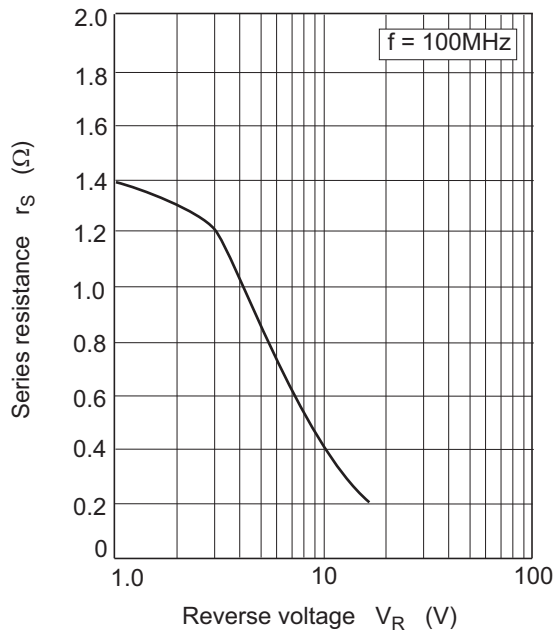


Fig.3 Series resistance vs. Reverse voltage

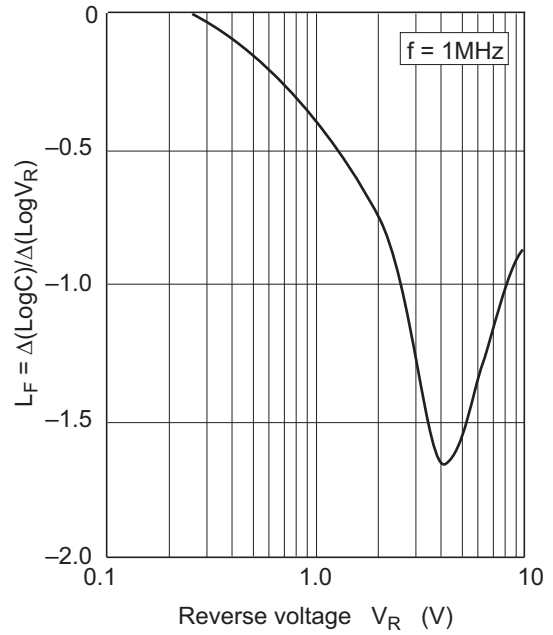
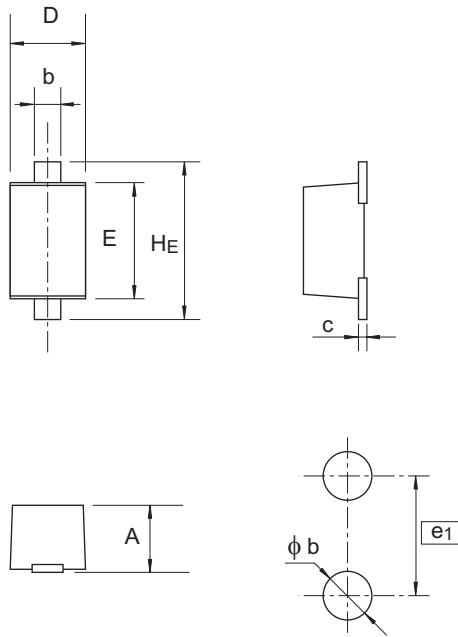


Fig.4 Linearity factor vs. Reverse voltage

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SFP	—	PUSF0002ZB-A	SFP / SFPV	0.0010g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	—	0.55
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.90	1.00	1.10
H_E	1.30	1.40	1.50
ϕb	—	0.50	—
e_1	—	1.40	—

Keep safety first in your circuit designs!

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