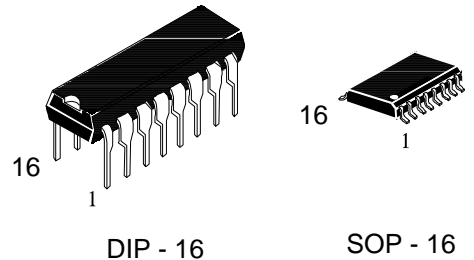


Description

The IW4049B is hex buffers and feature logic-level conversion using only one supply (voltage V_{CC}). The input- signal high (V_{ih}) can exceed the V_{CC} supply voltage when these devices are used for logic -level conversions. These devices are intended for use as CMOS to DTL/TTL converters

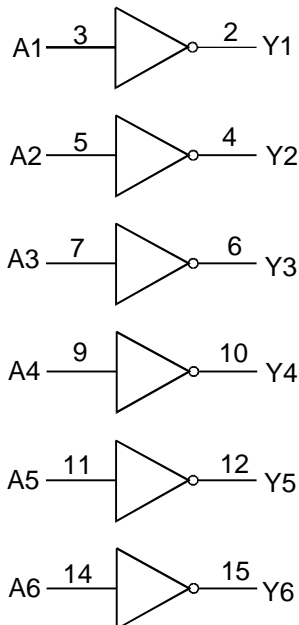
Features

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 at 18 V over full package-temperature range ;100 nA at 18 V and 25 C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



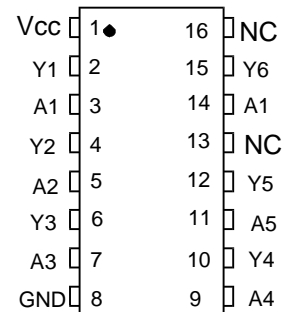
Package

Logic Diagram



PINS 13, 16 = NO CONNECTION
 PIN 1 = V_{CC}
 PIN 8 = GND

Pin Assignment



NC = NO CONNECTION

Function Table

Inputs	Output
A	Y
H	L
L	H

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to 20	V
V_{IN}	DC Input Voltage (Referenced to GND)	to +18	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Derating - Plastic DIP: - 10 mW/ °C from 65° to 125 °C

SOIC Package °C from 65° to 125 °C

The IW4049B has high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{in} \geq V_{cc}$

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	V_{CC}	18	V
V_{OUT}	DC Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	125	°C

The IW4049B has high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{in} \geq V_{cc}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND (V_{IN} or V_{OUT}) V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics

(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥ -55°C	25°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5 V V _{OUT} =1.0 V V _{OUT} =1.5 V	5.0	4	4	4	V
			10	8	8	8	
			15	12.5	12.5	12.5	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.5 V V _{OUT} =1.0 V V _{OUT} =1.5 V	5.0	1	1	1	V
			10	2	2	2	
			15	2.5	2.5	2.5	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	± 0.1	± 0.1	± 1.0	μA
I _{CC} Quiescent	Maximum Quiescent (per Package)	V _{IN} = GND or V _{CC}	5.0 10 15 20	1.0 2.0 4.0 20	1.0 2.0 4.0 20	30 60 120 600	μA
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} V _{OL} =0.4 V V _{OL} =0.4 V V _{OL} =0.5 V V _{OL} =1.5 V	4.5	3.3	2.6	1.8	
			5.0	4	3.2	2.4	
			10	10	8	5.6	
			15	26	24	18	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} V _{OH} =2.5 V V _{OH} =4.6 V V _{OH} =9.5 V V _{OH} =13.5 V	5.0	-2.6	-2.1	-	mA
			5.0	-0.81	-0.65	-	
			10	-2.0	-1.65	-1.18	
			15	-5.2	-4.3	-3.1	

AC Electrical Characteristics

($C_L=50\text{pF}$, $R=200\text{ k}\Omega$, Input $t_r=t_f=20$

Symbol	Parameter	ns)					Unit
		V	V	$\geq -55^\circ\text{C}$	$25^\circ\text{C} \leq 125^\circ\text{C}$		
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5	5	120	120	240	ns
		10	10	65	65	130	
		10	5	90	90	180	
		15	15	50	50		
		15	5	90	90	100	
t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5	5	65	65	180	ns
		10	10	40	40	130	
		10	5	40	30	80	
		15	15	30	30	60	
		15	5	30	20	60	
t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5	5		160	40	ns
		10	10	20	80	320	
		15	15	160	60	160	
t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5	5	80	60	120	ns
		10	10	60	40	120	
		15	15	60	30	80	
C_{IN}	Maximum Input Capacitance	-	-		22.5		pF

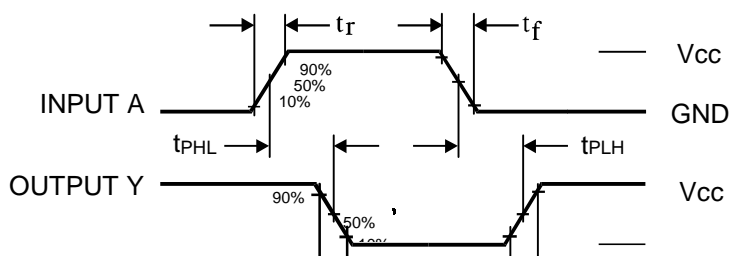
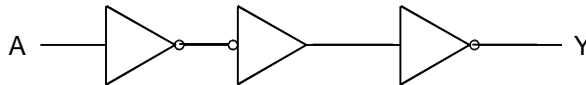


Figure 1. Switching Waveforms

Expanded Logic Diagram (1/6 of the Device)

Address : 北京市海淀区永定路 88 号长银大厦 6A06--6A07

Rm 6A07,Changyin Office Building ,No.88,Yong Ding Road,Hai Dian District ,Beijing

Postalcode:100039

Tel: 86-010-58895780 / 81 / 82 / 83 / 84 Fax : 010-58895793

[Http://www.estek.com.cn](http://www.estek.com.cn)

Email:sales@estek.com.cn

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