19-4322; Rev 0; 10/08

RS-485 Transceivers with Low-Voltage Logic Interface

General Description

The MAX13430E–MAX13433E are full- and half-duplex RS-485 transceivers that feature an adjustable low-voltage logic interface for operation in multivoltage systems. This allows direct interfacing to low-voltage ASIC/FPGAs without extra components. The MAX13430E–MAX13433E RS-485 transceivers operate with a V_{CC} voltage supply from +3V to +5V. The low-voltage logic interface operates with a voltage supply from +1.62V to V_{CC}.

The MAX13430E/MAX13432E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps. The MAX13431E/MAX13433E driver slew rates are not limited, enabling data transmission up to 16Mbps. The MAX13430E/MAX13431E are intended for half-duplex communications, and the MAX13432E/MAX13433E are intended for full-duplex communications.

The MAX13430E/MAX13431E are available in 10-pin µMAX® and 10-pin TDFN packages. The MAX13432E/MAX13433E are available in 14-pin TDFN and 14-pin SO packages.

Applications

Industrial Control Systems

Portable Industrial Equipment

Motor Control

HVAC

Features

- **Wide +3V to +5V Input Supply Range**
- **Low-Voltage Logic Interface +1.62V (min)**
- **Ultra-Low Supply Current in Shutdown Mode 10µA I_{CC} (max), 1µA I_L (max)**
- **Thermal Shutdown Protection**
- **Hot-Swap Input Structures on DE and $\overline{RE}$**
- **1/8-Unit Load Allows Up to 256 Transceivers on the Bus**
- **Enhanced Slew-Rate Limiting (MAX13430E/MAX13432E)**
- **Extended ESD Protection for RS-485 I/O Pins**
  - **±30kV Human Body Model**
  - **±15kV Air-Gap Discharge per IEC 61000-4-2**
  - **±10kV Contact Discharge per IEC 61000-4-2**
- **Extended -40°C to +85°C Operating Temperature Range**
- **Space-Saving TDFN and µMAX Packages**

Pin Configurations and Functional Diagrams appear at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	FULL/HALF DUPLEX	DATA RATE (Mbps)	SLEW RATE LIMITED	TRANSCEIVERS ON BUS	TOP MARK	PACKAGE CODE
MAX13430EETB+	10 TDFN-EP* (3mm x 3mm)	Half	0.5	Yes	256	AUS	T1033-1
MAX13430EEUB+**	10 µMAX (3mm x 3mm)	Half	0.5	Yes	256	—	U10-2
MAX13431EETB+	10 TDFN-EP* (3mm x 3mm)	Half	16	No	256	AUT	T1033-1
MAX13431EEUB+**	10 µMAX (3mm x 3mm)	Half	16	No	256	—	U10-2
MAX13432EESD+	14 SO	Full	0.5	Yes	256	—	S14-1
MAX13432EETD+**	14 TDFN-EP* (3mm x 3mm)	Full	0.5	Yes	256	AEG	T1433-2
MAX13433EESD+	14 SO	Full	16	No	256	—	S14-1
MAX13433EETD+**	14 TDFN-EP** (3mm x 3mm)	Full	16	No	256	AEH	T1433-2

Note: *All devices are specified over the extended -40°C to +85°C operating temperature range.*

+Denotes a lead-free/RoHS-compliant package.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

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RS-485 Transceivers with Low-Voltage Logic Interface

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
Supply Voltage (V_{CC}) .....-0.3V to +6V
Logic Supply Voltage (V_L) .....-0.3V to +6V
Control Input Voltage ($\overline{RE}$) .....-0.3V to (V_L+0.3V)
Control Input Voltage (DE) .....-0.3V to +6V
Driver Input Voltage (DI) .....-0.3V to +6V
Driver Output Voltage (Y, Z, A, B) .....-8V to +13V
Receiver Input Voltage (A, B)
(MAX13430E/MAX13431E).....-8V to +13V
Receiver Input Voltage (A, B)
(MAX13432E/MAX13433E).....-25V to +25V
Receiver Output Voltage (RO) .....-0.3V to (V_L + 0.3V)
Driver Output Current .....±250mA
Short-Circuit Duration (RO, A, B) to GND .....Continuous
Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 8.8mW/°C above +70°C) 707mW
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
14-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
14-Pin SO (derate 11.9mW/°C above +70°C) 952mW
Junction-to-Ambient Thermal Resistance (Θ_{JA}) (Note 1)
10-Pin µMAX .....113.1°C/W
10-Pin TDFN.....41°C/W
14-Pin TDFN .....41°C/W
14-Pin SO .....84°C/W
Junction-to-Ambient Thermal Resistance (Θ_{JC}) (Note 1)
10-Pin µMAX .....42°C/W
10-Pin TDFN.....9°C/W
14-Pin TDFN .....8°C/W
14-Pin SO .....34°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **http://www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +5.5V, V_L = +1.8V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +5V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{CC} Supply-Voltage Range	V_{CC}		3		5.5	V
V_L Supply-Voltage Range	V_L		1.62		V_{CC}	V
I_{CC} Supply Current	I_{CC}	DE = $\overline{RE}$ = high, no load DE = $\overline{RE}$ = low, no load DE = high, $\overline{RE}$ = low, no load			2	mA
I_{CC} Supply Current in Shutdown Mode	I_{SHDN}	DE = low, $\overline{RE}$ = high, no load			10	µA
V_L Supply Current	I_L	RO = no load			1	µA
DRIVER						
Differential Driver Output (Figure 1)	V_{OD}	R_L = 100Ω, V_{CC} = +3V	2		V_{CC}	V
		R_L = 54Ω, V_{CC} = +3V	1.5		V_{CC}	
		R_L = 100Ω, V_{CC} = +4.5V	2.25		V_{CC}	
		R_L = 54Ω, V_{CC} = +4.5V	2.25		V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1 (Note 4)			0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1		$V_{CC}/2$	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 4)			0.2	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +5.5V, V_L = +1.8V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +5V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Leakage Current (Y and Z)	I_{OLK}	DE = GND, V_{CC} = GND or +5.5V	V_{IN} = +12V			125	µA
			V_{IN} = -7V	-100			
Driver Short-Circuit Output Current (Note 5)	I_{OSD}	0 ≤ V_{OUT} ≤ +12V				+250	mA
		-7V ≤ V_{OUT} ≤ V_{CC}		-250			
Driver Short-Circuit Output Foldback Current (Note 5)	I_{OSDF}	(V_{CC} - 1V) ≤ V_{OUT} ≤ +12V		15			mA
		-7V ≤ V_{OUT} ≤ +1V				-15	
Thermal Shutdown Threshold	T_{TS}				+150		°C
Thermal Shutdown Hysteresis	T_{TSH}				15		°C
RECEIVER							
Input Current (A and B)	$I_{A, B}$	DE = GND, V_{CC} = GND or +5.5V	V_{CM} = +12V			125	µA
			V_{CM} = -7V	-100			
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V		-200		-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0			15		mV
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		96			kΩ
LOGIC INTERFACE							
Input High Logic Level (DI, DE, $\overline{RE}$)	V_{IH}			2/3 x V_L			V
Input Low Logic Level (DI, DE, $\overline{RE}$)	V_{IL}					1/3 x V_L	V
Input Current (DI, DE, $\overline{RE}$)	I_{IN}	V_{DI} = V_{DE} = $V_{\overline{RE}}$ = V_L = +5.5V				±1	µA
Input Impedance on First Transition	$R_{DE, \overline{RE}}$			1		10	kΩ
Output High Logic Level (RO)	V_{OH}	I_O = -1mA, V_A - V_B = V_{TH}		V_L - 0.4			V
Output Low Logic Level (RO)	V_{OL}	I_O = 1mA, V_A - V_B = -V_{TH}				0.4	V
Receiver Three-State Output Current (RO)	I_{OZR}	0 ≤ V_{RO} ≤ V_L		-1	0.01	+1	µA
Receiver Output Short-Circuit Current (RO)	I_{OSR}	0 ≤ V_{RO} ≤ V_L		-110		+110	mA
ESD PROTECTION							
A, B, Y, Z to GND		IEC 61000-4-2 Air Gap Discharge			±15		kV
		IEC 61000-4-2 Contact Discharge			±10		
		Human Body Model			±30		
All Other Pins (Except A, B, Y, and Z)		Human Body Model			±2		kV

SWITCHING CHARACTERISTICS (MAX13431E/MAX13433E (16 Mbps))

(V_{CC} = +3V to +5.5V, V_L = +1.8V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +5V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay (Figures 2 and 3)	t_{DPLH}	C_L = 50pF, R_{DIFF} = 54Ω			50	ns
	t_{DPHL}				50	
Driver Differential Output Rise or Fall Time	t_R, t_F	C_L = 50pF, R_L = 54Ω, Figures 2 and 3			15	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	C_L = 50pF, R_L = 54Ω, Figures 2 and 3			8	ns
Maximum Data Rate			16			Mbps
Driver Enable to Output High	t_{DZH}	C_L = 50pF, R_L = 500Ω, Figure 4			150	ns
Driver Enable to Output Low	t_{DZL}	C_L = 50pF, R_L = 500Ω, Figure 5			150	ns
Driver Disable Time from Low	t_{DLZ}	C_L = 50pF, R_L = 500Ω, Figure 4			100	ns
Driver Disable Time from High	t_{DHZ}	C_L = 50pF, R_L = 500Ω, Figure 5			120	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	C_L = 50pF, R_L = 500Ω, Figure 4			5	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	C_L = 50pF, R_L = 500Ω, Figure 5			5	µs
RECEIVER						
Receiver Propagation Delay (Figures 6 and 7)	t_{RPLH}	C_L = 15pF			80	ns
	t_{RPHL}				80	
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figures 6 and 7			13	ns
Maximum Data Rate			16			Mbps
Receiver Enable to Output Low	t_{RZL}	Figure 8			50	ns
Receiver Enable to Output High	t_{RZH}	Figure 8			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 8			50	ns
Receiver Disable Time from High	t_{RHZ}	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figure 8			5	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figure 8			5	µs
DRIVER/RECEIVER						
Time to Shutdown	t_{SHDN}		50	340	700	ns

DRIVER SWITCHING CHARACTERISTICS (MAX13430E/MAX13432E (500 kbps))

(V_{CC} = +3V to +5.5V, V_L = +1.8V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +5V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay (Figures 2 and 3)	t_{DPLH}	C_L = 50pF, R_L = 54Ω	180		800	ns
	t_{DPHL}		180		800	
Driver Differential Output Rise or Fall Time	t_R, t_F	C_L = 50pF, R_L = 54Ω, Figures 2 and 3	200		800	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	C_L = 50pF, R_L = 54Ω, Figures 2 and 3			100	ns
Maximum Data Rate			500			kbps
Driver Enable to Output High	t_{DZH}	C_L = 50pF, R_L = 500Ω, Figure 4			2.5	µs
Driver Enable to Output Low	t_{DZL}	C_L = 50pF, R_L = 500Ω, Figure 5			2.5	µs
Driver Disable Time from Low	t_{DLZ}	C_L = 50pF, R_L = 500Ω, Figure 4			100	ns
Driver Disable Time from High	t_{DHZ}	C_L = 50pF, R_L = 500Ω, Figure 5			120	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	C_L = 50pF, R_L = 500Ω, Figure 4			5	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	C_L = 50pF, R_L = 500Ω, Figure 5			5	µs
RECEIVER						
Receiver Propagation Delay (Figures 6 and 7)	t_{RPLH}	C_L = 15pF			200	ns
	t_{RPHL}				200	
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figures 6 and 7			30	ns
Maximum Data Rate			500			kbps
Receiver Enable to Output Low	t_{RZL}	Figure 8			50	ns
Receiver Enable to Output High	t_{RZH}	Figure 8			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 8			50	ns
Receiver Disable Time from High	t_{RHZ}	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figure 8			5	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figure 8			5	µs

RS-485 Transceivers with Low-Voltage Logic Interface

DRIVER SWITCHING CHARACTERISTICS (MAX13430E/MAX13432E (500 kbps)) (continued)

(V_{CC} = +3V to +5.5V, V_L = +1.8V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +5V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER/RECEIVER						
Time to Shutdown	t_{SHDN}		50	340	700	ns

Note 2: Parameters are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over temperature are guaranteed by design.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.

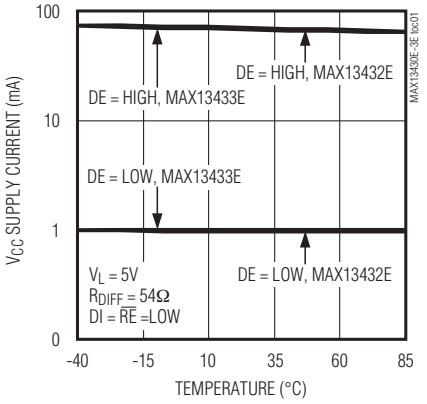
Note 4: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 5: The short-circuit output current is the peak current just prior to current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

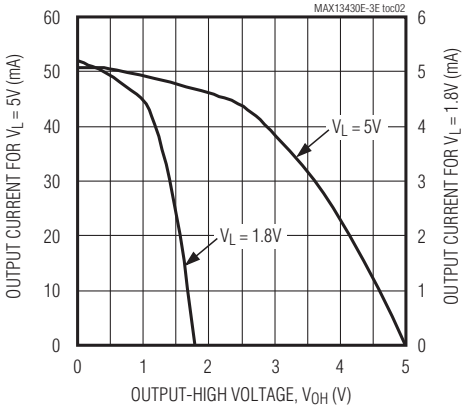
Typical Operating Characteristics

(V_{CC} = +5V, V_L = +5V, T_A = +25°C, unless otherwise noted.)

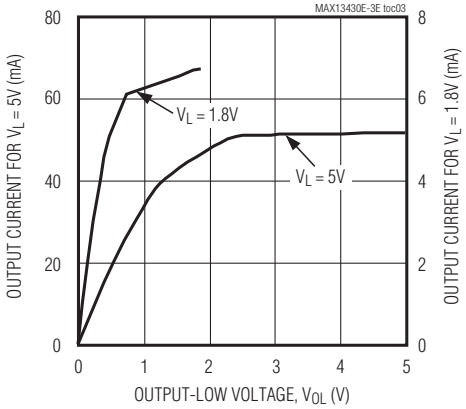
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



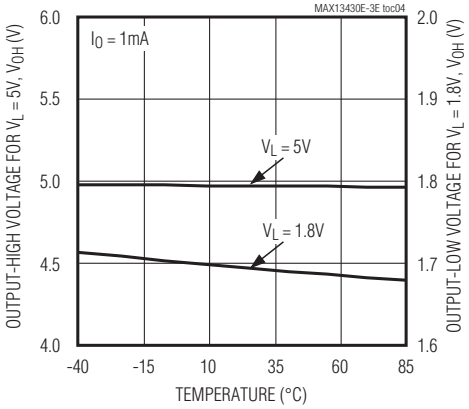
OUTPUT CURRENT vs. RECEIVER OUTPUT-HIGH VOLTAGE



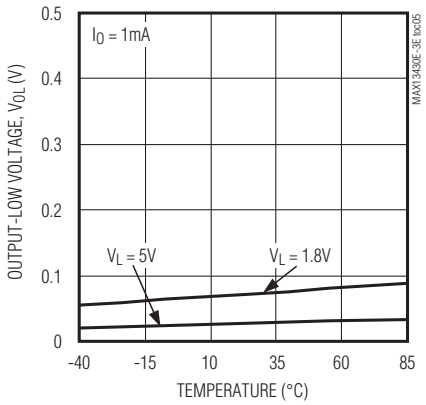
OUTPUT CURRENT vs. RECEIVER OUTPUT-LOW VOLTAGE



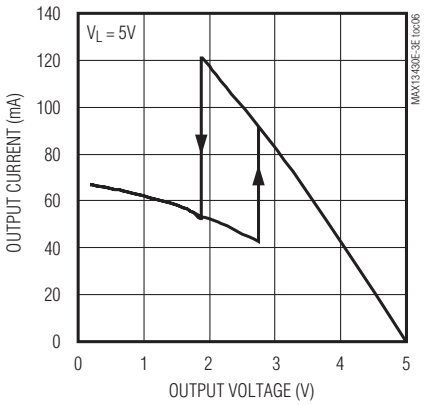
RECEIVER OUTPUT-HIGH VOLTAGE vs. TEMPERATURE



RECEIVER OUTPUT-LOW VOLTAGE vs. TEMPERATURE



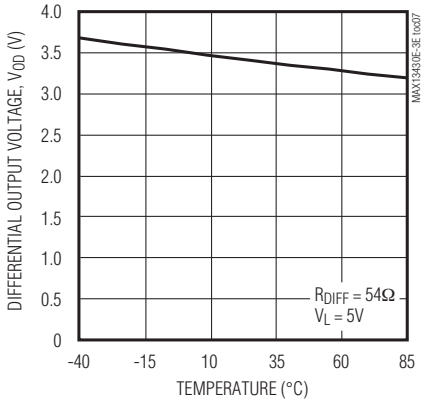
DIFFERENTIAL OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



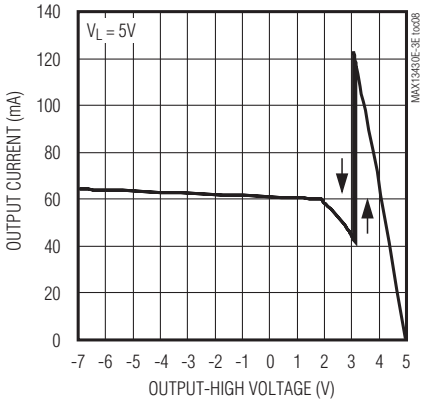
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_L = +5V, T_A = +25°C, unless otherwise noted.)

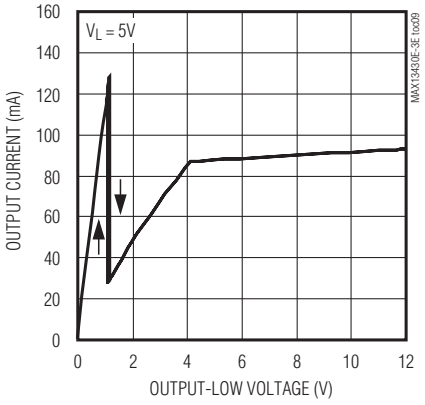
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



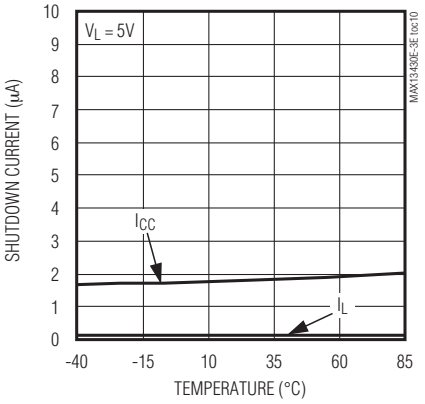
OUTPUT CURRENT vs. TRANSMITTER OUTPUT-HIGH VOLTAGE



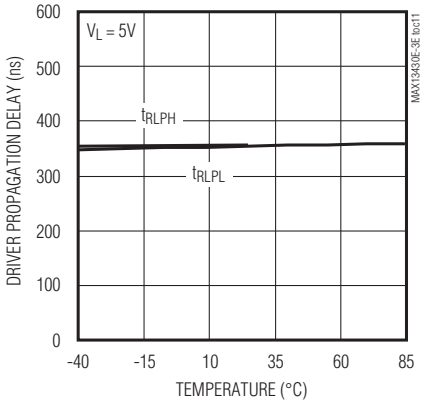
OUTPUT CURRENT vs. TRANSMITTER OUTPUT-LOW VOLTAGE



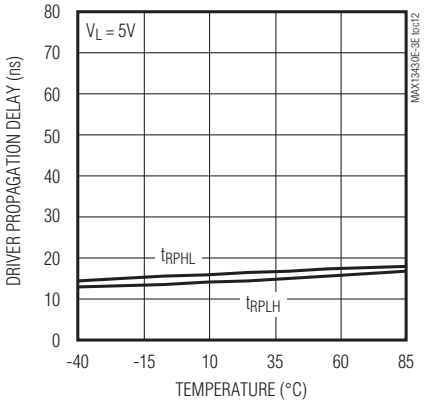
SHUTDOWN CURRENT vs. TEMPERATURE



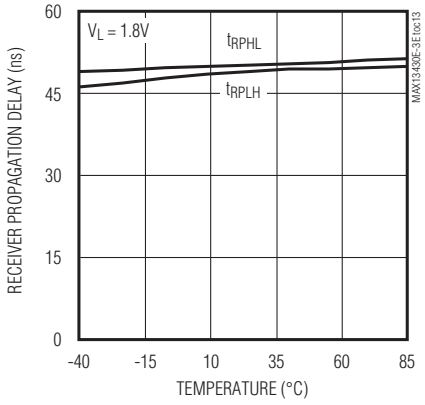
DRIVER PROPAGATION vs. TEMPERATURE (MAX13432E)



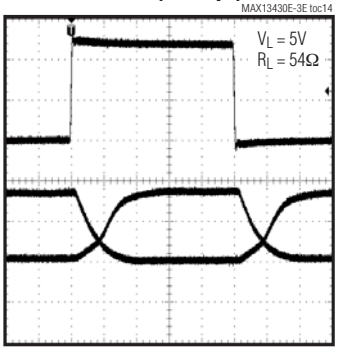
DRIVER PROPAGATION vs. TEMPERATURE (MAX13433E)



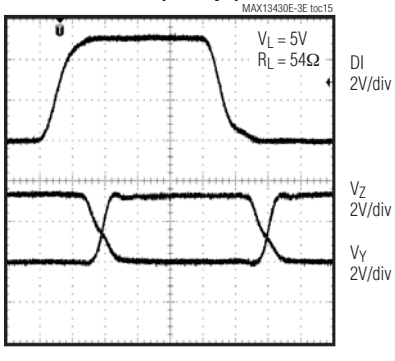
RECEIVER PROPAGATION vs. TEMPERATURE



MAX13432E DRIVER PROPAGATION DELAY (500kbps)



MAX13433E DRIVER PROPAGATION DELAY (20Mbps)



RS-485 Transceivers with Low-Voltage Logic Interface

Test Circuits and Waveforms

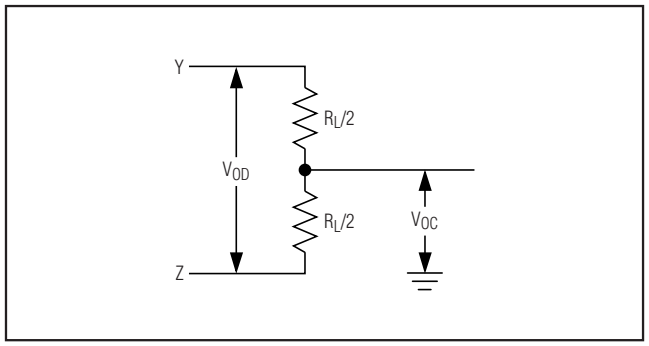


Figure 1. Driver DC Test Load

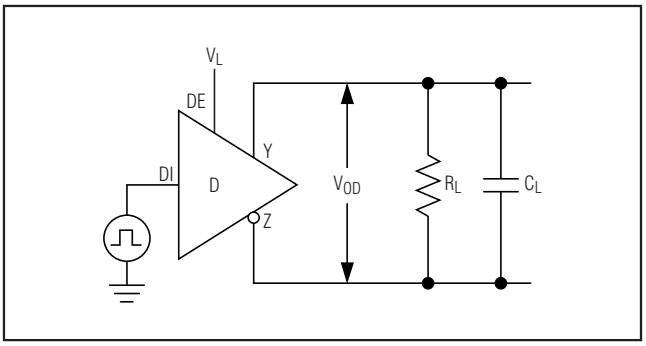


Figure 2. Driver Timing Test Circuit

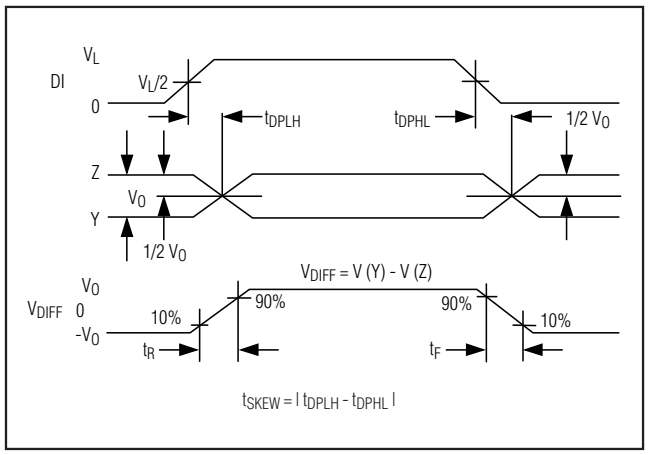


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

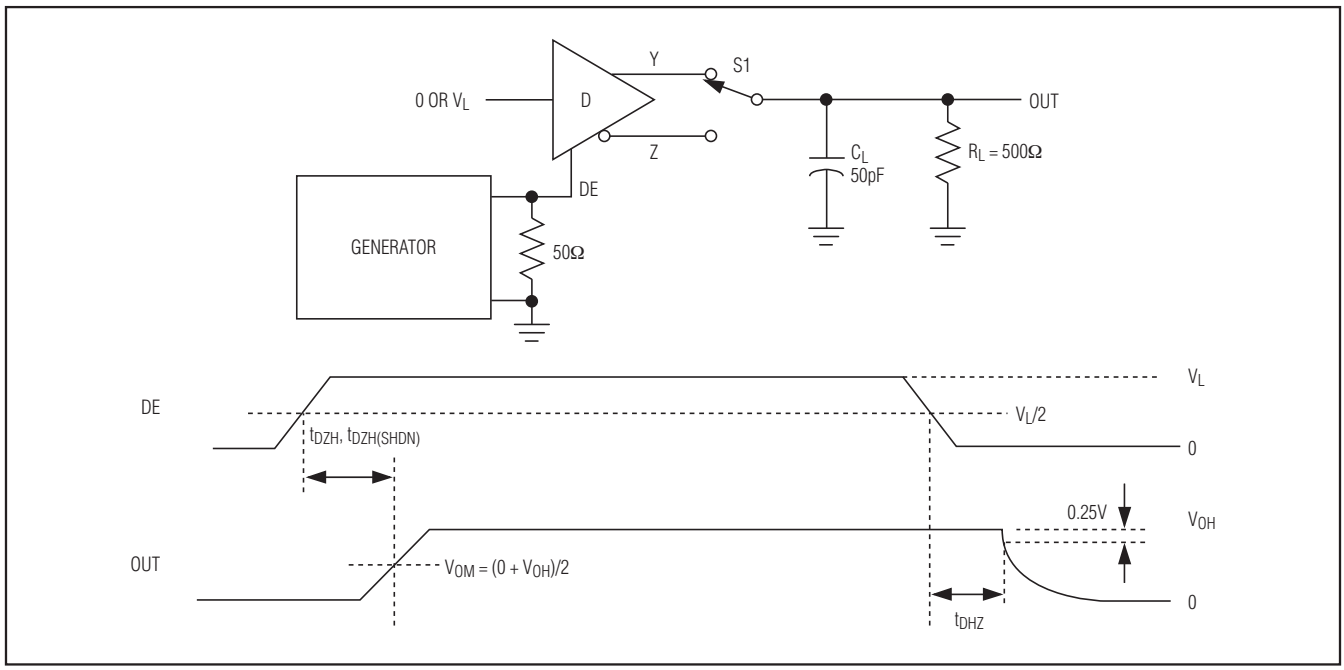


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, and $t_{DZHZ(SHDN)}$)

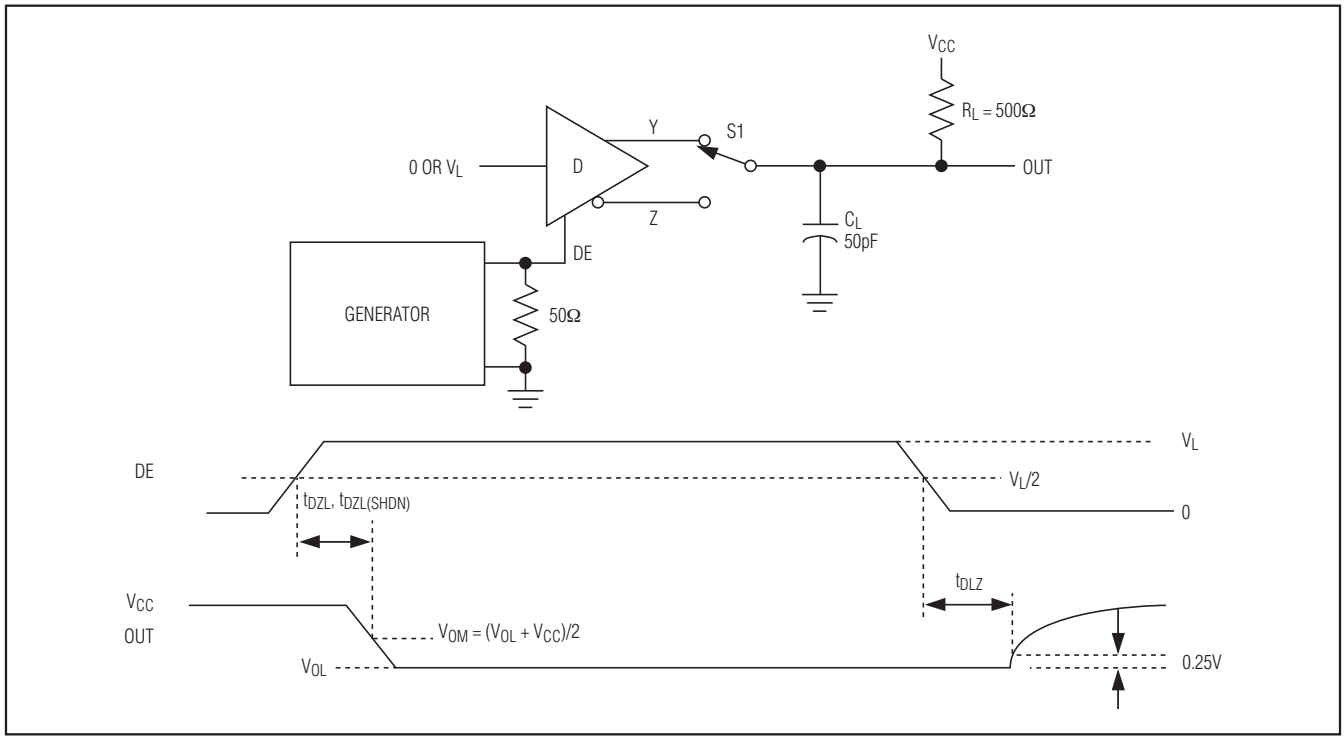


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ}, and $t_{DLZ(SHDN)}$)

RS-485 Transceivers with Low-Voltage Logic Interface

Test Circuits and Waveforms (continued)

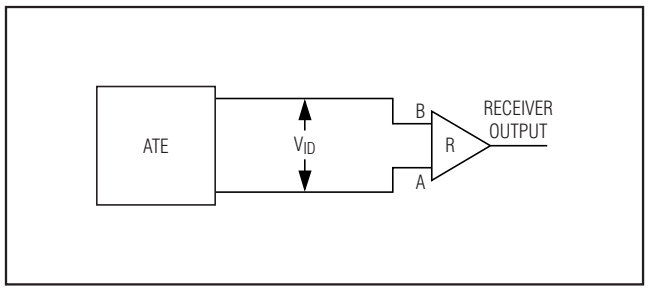


Figure 6. Receiver Propagation Delay Test Circuit

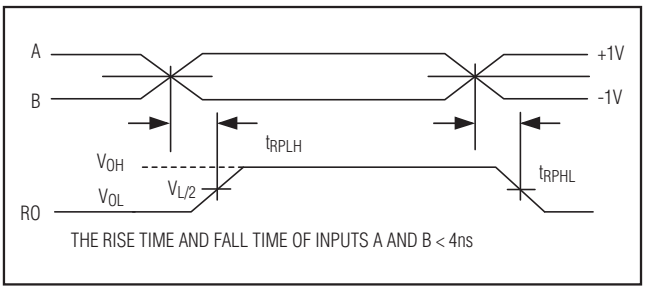


Figure 7. Receiver Propagation Delays

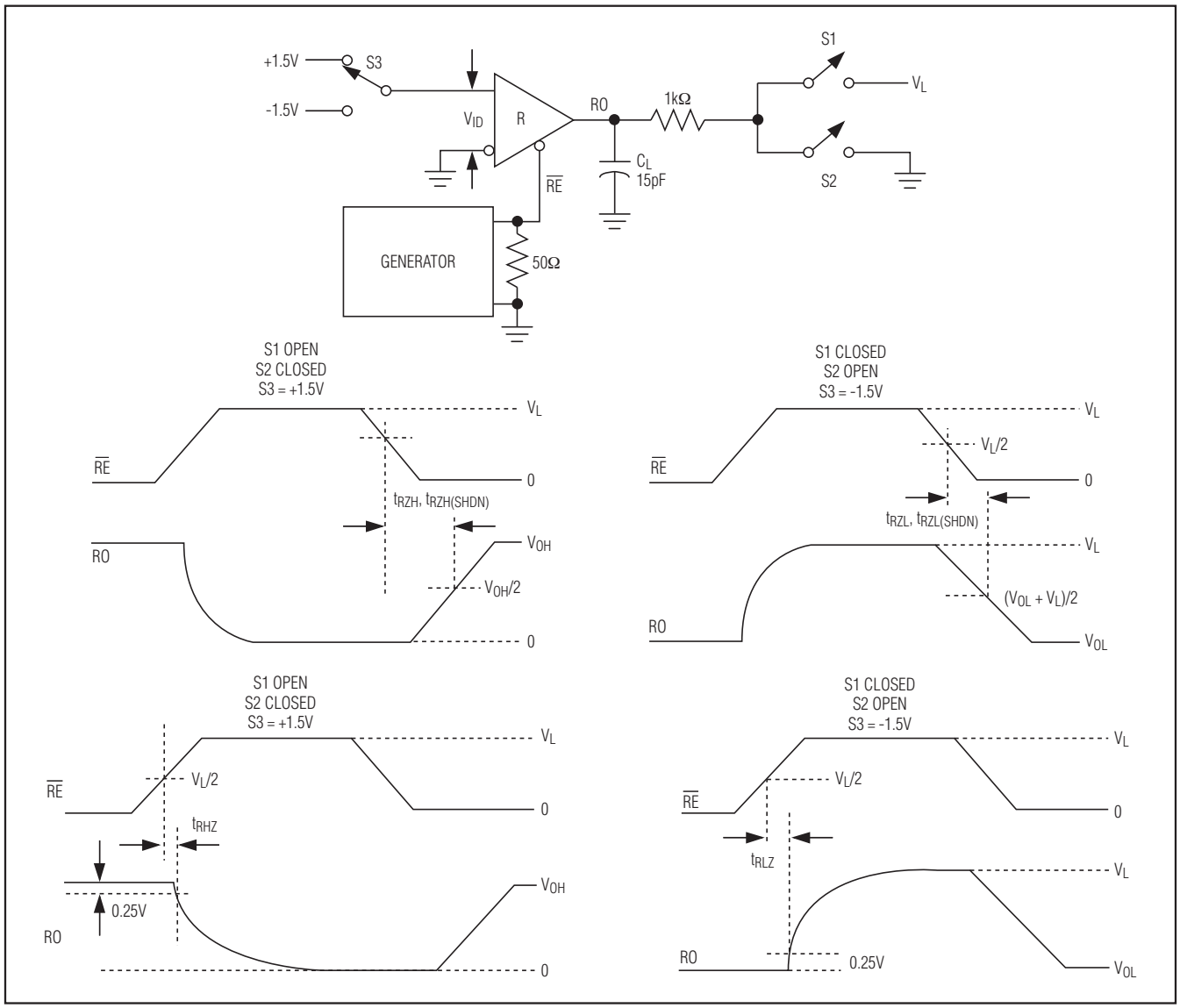


Figure 8. Receiver Enable and Disable Times

Pin Description

PIN		NAME	FUNCTION
MAX13430E/MAX13431E			
µMAX	TDFN-EP		
1	1	V_L	V_L Input Logic-Supply Voltage. Bypass V_L with a 0.1µF ceramic capacitor located as close as possible to the input.
2	2	RO	Receiver Output. When $\overline{RE}$ is low and if (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low.
3	3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the *Hot-Swap Capability* section for details.)
4	4	$\overline{RE}$	Active-Low Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when RE is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input (see the *Hot-Swap Capability* section for details.)
5	5	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces noninverting output high and inverting output low.
6	6	GND	Ground
7	7	N.C.	No Connection. Not internally connected. N.C. can be connected to GND.
8	8	A	Noninverting Receiver Input and Noninverting Driver Output
9	9	B	Inverting Receiver Input and Inverting Driver Output
10	10	V_{CC}	V_{CC} Input Supply Voltage. Bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass V_{CC} with a 0.1µF ceramic capacitor.
—	EP	EP	Exposed Pad. Connect EP to GND (TDFN-EP only).

RS-485 Transceivers with Low-Voltage Logic Interface

Pin Description (continued)

PIN		NAME	FUNCTION
MAX13432E/MAX13433E			
SO	TDFN-EP		
1	1	V_L	V_L Input Logic Supply Voltage. Bypass V_L with a 0.1µF ceramic capacitor located as close as possible to the input.
2	2	RO	Receiver Output. When $\overline{RE}$ is low and if (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low.
3	3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the *Hot-Swap Capability* section for details.)
4	4	$\overline{RE}$	Active-Low Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when RE is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input (see the *Hot-Swap Capability* section for details.)
5	5	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces noninverting output high and inverting output low.
6	6	GND	Ground
7, 13	7, 13	N.C.	No Connection. Not internally connected. N.C. can be connected to GND.
8	8	GND	Ground
9	9	Y	Noninverting Driver Output
10	10	Z	Inverting Driver Output
11	11	B	Inverting Receiver Input
12	12	A	Noninverting Receiver Input
14	14	V_{CC}	V_{CC} Input Supply Voltage. Bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass V_{CC} with a 0.1µF ceramic capacitor.
—	EP	EP	Exposed Pad. Connect EP to GND (TDFN-EP only).

Function Tables

MAX13430E/MAX13431E (Full Duplex)

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Impedance	High-Impedance
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ -50mV	1
0	X	≤ -200mV	0
0	X	Open/ Shorted	1
1	1	X	High-Impedance
1	0	X	Shutdown

MAX13432E/MAX13433E (Half Duplex)

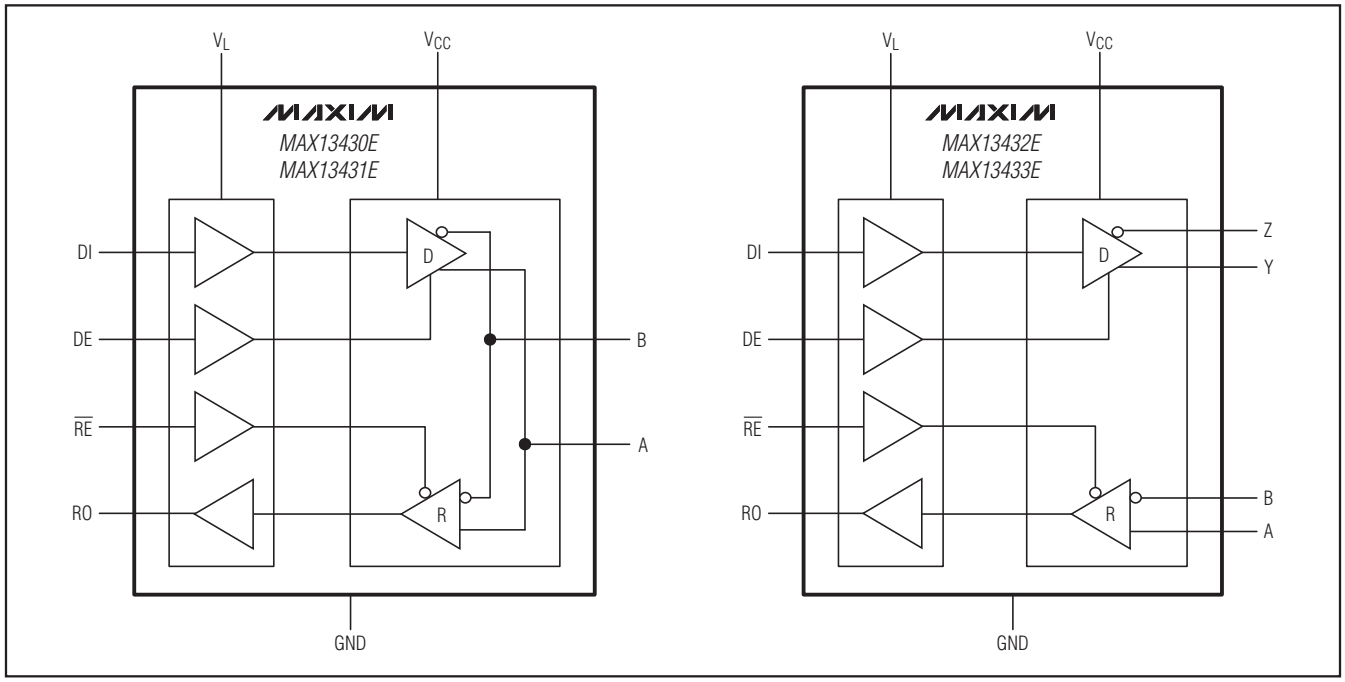
TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
1	0	X	High-Impedance	High-Impedance
0	0	X	Shutdown*	

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ -50mV	1
0	X	≤ -200mV	0
0	X	Open/ Shorted	1
1	1	X	High-Impedance
1	0	X	Shutdown*

X = Don't care.

**Shutdown mode, driver and receiver outputs are in high impedance.*

Functional Diagrams



RS-485 Transceivers with Low-Voltage Logic Interface

Detailed Description

The MAX13430E–MAX13433E are full- and half-duplex RS-485 transceivers that feature an adjustable low-voltage logic interface for application in multivoltage systems. This allows direct interfacing to low-voltage ASIC/FPGAs without extra components. The MAX13430E–MAX13433E RS-485 transceivers operate with a V_{CC} voltage supply from +3V to +5V. The low-voltage logic interface operates with a voltage supply from +1.62V to V_{CC}.

The MAX13430E–MAX13433E are ±30kV ESD-protected RS-485 transceivers with one driver and one receiver. All devices have a 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. These devices include fail-safe circuitry, guaranteeing a logic-high receiver output when receiver inputs are open or shorted. The receivers output a logic-high if all transmitters on a terminated bus are disabled (high impedance). All devices feature hot-swap capability to eliminate false transitions on the bus during power-up or hot insertion.

The MAX13430E/MAX13432E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps. The MAX13431E/MAX13433E driver slew rates are not limited, enabling data transmission up to 16Mbps.

The MAX13430E–MAX13433E transceivers draw 2mA of supply current when unloaded or when fully loaded with the drivers disabled. The MAX13430E/MAX13431E are intended for half-duplex communications, and the MAX13432E/MAX13433E are intended for full-duplex communications.

Low-Voltage Logic Interface

V_L is the voltage supply for the low-voltage logic interface and receiver output. V_L operates with voltage supply from +1.62V to V_{CC}.

Fail Safe

The MAX13430E family guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high.

If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX13430E family, this results in a logic-high with a 50mV minimum noise margin. The -50mV to -200mV threshold complies with the ±200mV EIA/TIA/RS-485 standard.

Hot-Swap Capability

When circuit boards are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit-board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of these devices to a defined logic level. Leakage currents up to ±10µA from the high-impedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit-board capacitance could cause coupling of V_L or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver. When V_L rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

±30kV ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13430E family of devices have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±30kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13430E–MAX13433E keep working without latchup or damage. ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13430E–MAX13433E are characterized for protection to the following limits:

- ±30kV using the Human Body Model
- ±10kV using the Contact Discharge method specified in IEC 61000-4-2
- ±15kV using the Air Gap Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13430E family of devices helps you design equipment to meet IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 61000-4-2 model, and Figure 10d shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

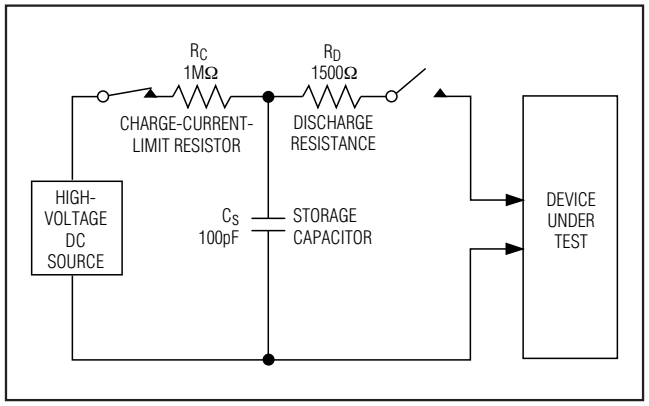


Figure 10a. Human Body ESD Test Model

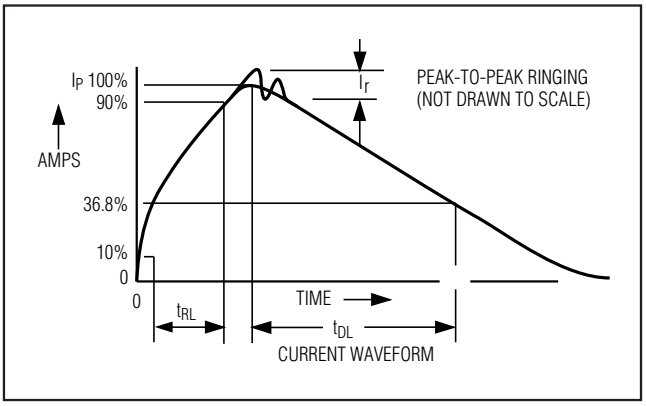


Figure 10b. Human Body Current Waveform

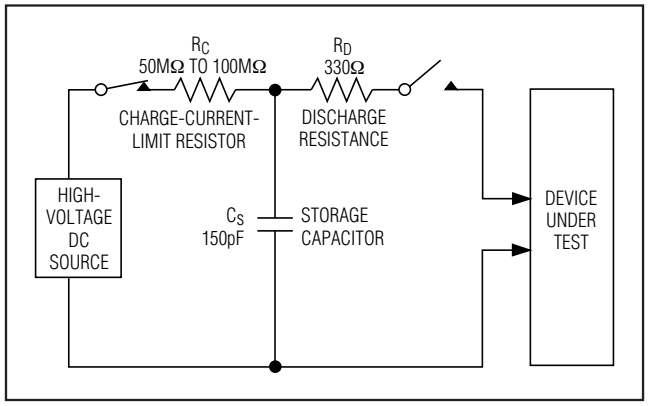


Figure 10c. IEC 61000-4-2 ESD Test Model

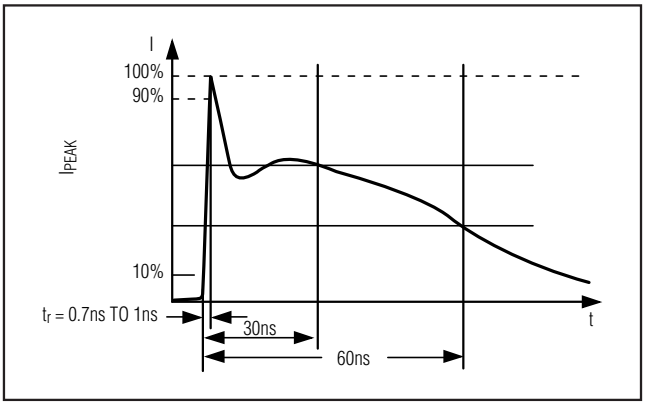


Figure 10d. IEC 61000-4-2 ESD Generator Current Waveform

RS-485 Transceivers with Low-Voltage Logic Interface

Applications Information

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is a one-unit load (12kΩ), and the standard driver can drive up to 32 unit loads. The MAX13430E family of transceivers has a 1/8-unit load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices, as well as other RS-485 transceivers with a total of 32-unit loads or less, can be connected to the line.

Reduced EMI and Reflections

The MAX13430E/MAX13432E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*.) The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +150°C (typ).

Typical Applications

The MAX13430E/MAX13433E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 12 and 13 show typical network applications circuits. To minimize reflections, terminate the line at both ends with its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX13430E/MAX13432E allow the RS-485 network to be more tolerant of imperfect termination.

Typical Application Circuits

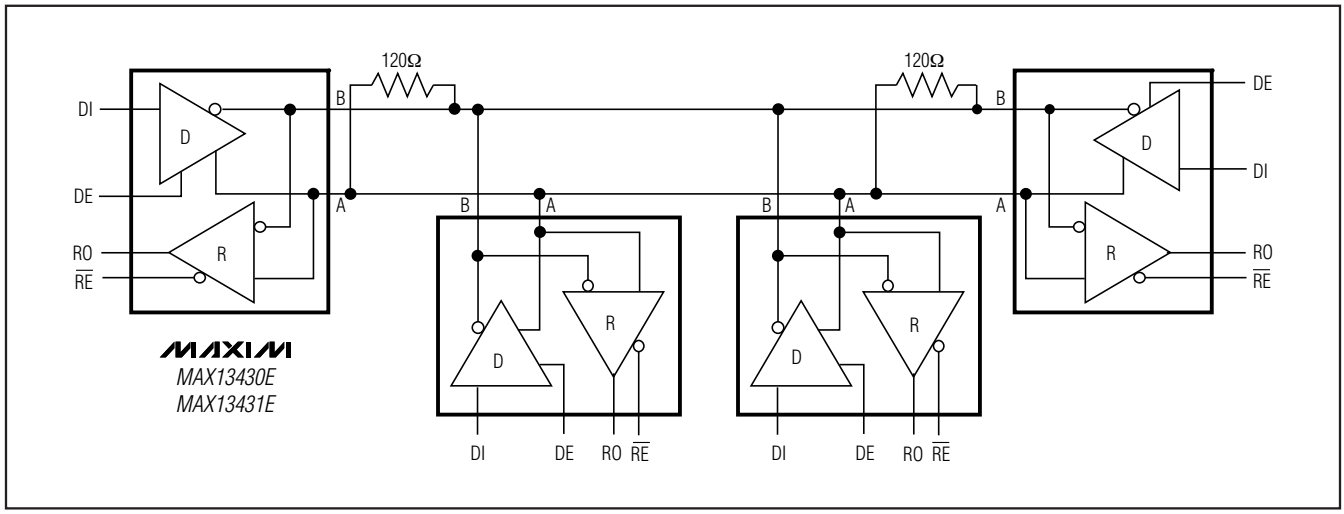


Figure 11. Typical Half-Duplex RS-485 Network

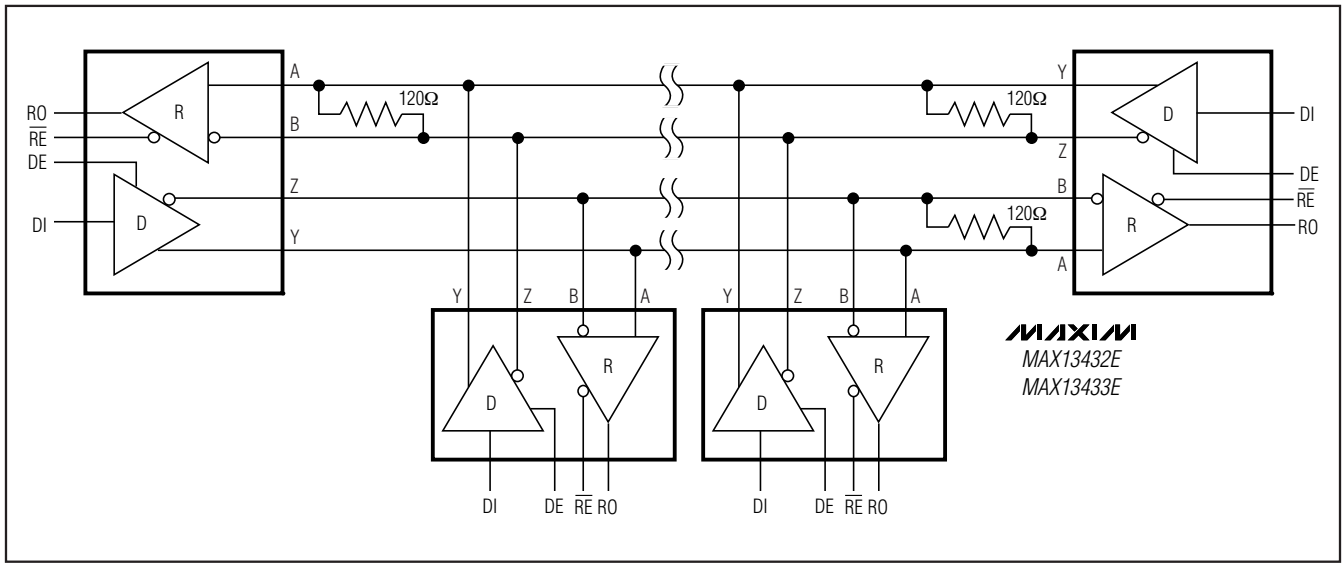
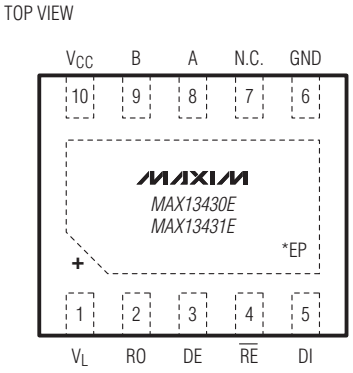


Figure 12. Typical Full-Duplex RS-485 Network

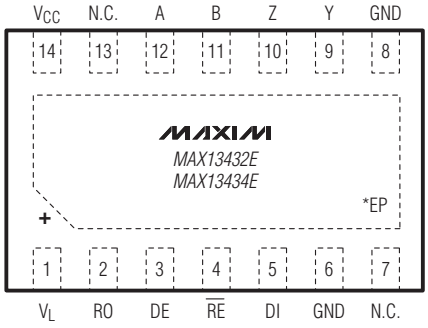
RS-485 Transceivers with Low-Voltage Logic Interface

Pin Configurations



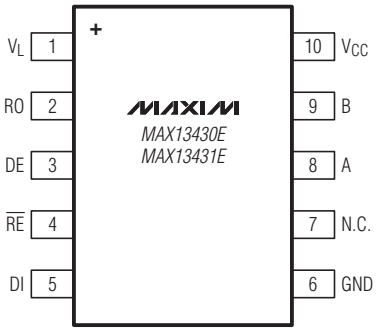
TDFN

* EXPOSED PAD CONNECT TO GND.

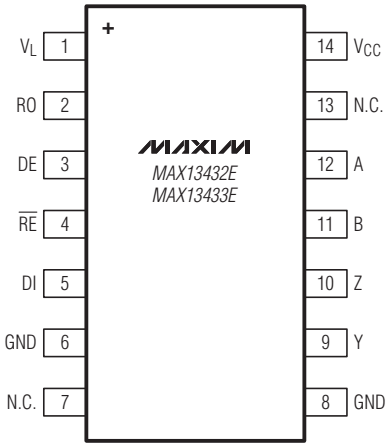


TDFN

* EXPOSED PAD CONNECT TO GND.



µMAX



SO

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 µMAX	U10-2	**21-0061**
14 TDFN	T1433-2	**21-0137**
10 TDFN	T1033-1	**21-0137**
14 SO	S14-1	**21-0041**