Rev 0; 11/07

1024-Bit, 1-Wire EEPROM for Automotive Applications

General Description

The DS2431-A1 is an AEC-Q100 Grade 1 qualified version of the DS2431. The logical behavior of both versions is identical. The DS2431-A1 is a 1024-bit, 1-Wire® EEPROM chip organized as four memory pages of 256 bits each. Data is written to an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four memory pages can individually be write protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. The DS2431-A1 communicates over the single-conductor 1-Wire bus. The communication follows the standard 1-Wire protocol. Each device has its own unalterable and unique 64-bit ROM registration number that is factory lasered into the chip. The registration number is used to address the device in a multidrop 1-Wire net environment.

Applications

Automotive Sensor Identification and Calibration Data Storage

Automotive Cable Assembly Identification

Accessory/PCB Identification

Commands and modes are capitalized for clarity.

Features

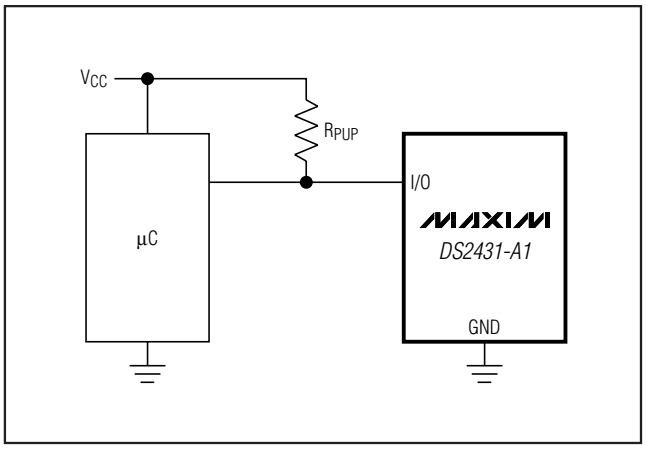
- **1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits**
- **Individual Memory Pages Can Be Permanently Write Protected or Put in EPROM-Emulation Mode (“Write to 0”)**
- **Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise**
- **IEC 1000-4-2 Level 4 ESD Protection (8kV Contact, 15kV Air, Typ)**
- **Reads and Writes Over a 4.5V to 5.25V Voltage Range from -40°C to +125°C**
- **Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps Using 1-Wire Protocol**
- **Meets AEC-Q100 Grade 1 Qualification Requirements**
- **Also Available as Standard Version for Industrial Temperature Range (DS2431)**

Ordering Information

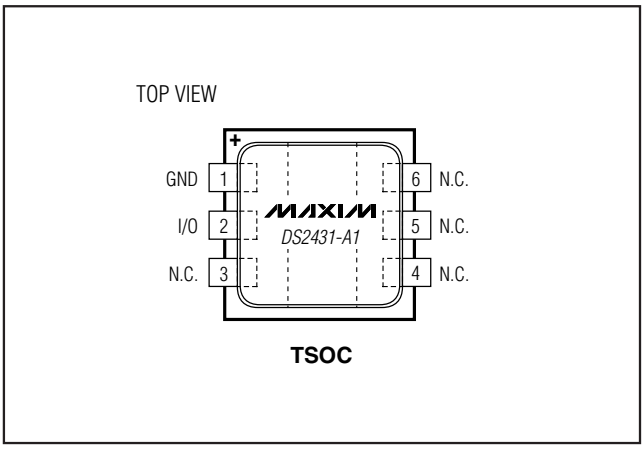
PART	TEMP RANGE	PIN-PACKAGE
DS2431P-A1+	-40°C to +125°C	6 TSOC
DS2431P-A1+T	-40°C to +125°C	6 TSOC

+Denotes a lead-free package.
T = Tape and reel.

Typical Operating Circuit



Pin Configuration



TSOC

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1024-Bit, 1-Wire EEPROM for Automotive Applications

ABSOLUTE MAXIMUM RATINGS

I/O Voltage to GND .....-0.5V, +6V
I/O Sink Current 20mA
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +125°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O PIN GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	4.5		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)			1000	pF
Input Load Current	I_L	I/O pin at V_{PUP}	0.05		10	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	0.5		V_{PUP} - 1.8	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	1.0		V_{PUP} - 1.0	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.21		1.70	V
Output Low Voltage	V_{OL}	At 4mA (Note 11)			0.4	V
Recovery Time (Notes 2, 12)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-Off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Time Slot Duration (Notes 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
I/O PIN, 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
I/O PIN, 1-Wire WRITE						
Write-0 Low Time (Notes 2, 16, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	5		**15.5**	
Write-1 Low Time (Notes 2, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
I/O PIN, 1-Wire READ						
Read Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +125°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	$t_{RL} + \delta$		15	µs
		Overdrive speed	$t_{RL} + \delta$		2	
EEPROM						
Programming Current	I_{PROG}	(Notes 5, 19)			0.8	mA
Programming Time	t_{PROG}	(Note 20)			10	ms
Write/Erase Cycles (Endurance) (Notes 21, 22)	N_{CY}	At +25°C	200k			—
		At +85°C	50k			
		At +125°C	1k			
Data Retention (Notes 23, 24, 25)	t_{DR}	At +125°C (worst case)	10			Years

Note 1: Specifications at T_A = -40°C are guaranteed by design only and not production tested.

Note 2: System requirement.

Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.

Note 4: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied, the parasite capacitance does not affect normal communications.

Note 5: Guaranteed by design, characterization, and/or simulation only. Not production tested.

Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on I/O. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 7: Voltage below which, during a falling edge on I/O, a logic 0 is detected.

Note 8: The voltage on I/O needs to be less than or equal to V_{ILMAX} at all times the master is driving I/O to a logic-0 level.

Note 9: Voltage above which, during a rising edge on I/O, a logic 1 is detected.

Note 10: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O must drop by at least V_{HY} to be detected as logic 0.

Note 11: The I-V characteristic is linear for voltages less than 1V.

Note 12: Applies to a single device attached to a 1-Wire line.

Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.

Note 14: Defines maximum possible bit rate. Equal to $t_{W0LMIN} + t_{RECMIN}$.

Note 15: Interval after t_{RSTL} during which a bus master is guaranteed to sample a logic 0 on I/O if there is a DS2431-A1 present. Minimum limit is t_{PDHMAX}; maximum limit is $t_{PDHMIN} + t_{PDLMIN}$.

Note 16: Bolded numbers are NOT in compliance with legacy 1-Wire product standards. See *Comparisons Table*.

Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.

Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Note 19: Current drawn from I/O during the EEPROM programming interval. The pullup circuit on I/O during the programming interval should be such that the voltage at I/O is greater than or equal to V_{PUPMIN}. If V_{PUP} in the system is close to V_{PUPMIN}, a low-impedance bypass of R_{PUP}, which can be activated during programming, may need to be added.

Note 20: Interval begins t_{REHMAX} after the trailing rising edge on I/O for the last time slot of the E/S byte for a valid Copy Scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.

Note 21: Write-cycle endurance is degraded as T_A increases.

Note 22: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 23: Data retention is degraded as T_A increases.

Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.

Note 25: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.

1024-Bit, 1-Wire EEPROM for Automotive Applications

Comparisons Table

PARAMETER	LEGACY VALUES				DS2431-A1 VALUES			
	STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)		STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (including t_{REC})	61	(undefined)	7	(undefined)	65*	(undefined)	8*	(undefined)
t_{RSTL}	480	(undefined)	48	80	480	640	48	80
t_{PDH}	15	60	2	6	15	60	2	6
t_{PDL}	60	240	8	24	60	240	8	24
t_{W0L}	60	120	6	16	60	120	6	**15.5**

**Intentional change, longer recovery time requirement due to modified 1-Wire front-end.*

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground Reference
2	I/O	1-Wire Bus Interface. Open drain, requires external pullup resistor.
3–6	N.C.	No Connection

General Description

The DS2431-A1 combines 1024 bits of EEPROM, an 8-byte register/control page with up to seven user read/write bytes, and a fully featured 1-Wire interface in a single chip. Each DS2431-A1 has its own 64-bit ROM registration number that is factory lasered into the chip to provide a guaranteed unique identity for absolute traceability. Data is transferred serially through the 1-Wire protocol, which requires only a single data lead and a ground return. The DS2431-A1 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory or the register page. Data is first written to the scratchpad from which it can be read back. After the data has been verified, a Copy Scratchpad command transfers the data to its final memory location. The DS2431-A1 applications include sensor, cable, accessory, or PCB identification in environments that demand automotive AEC-Q100 Grade 1 reliability.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2431-A1. The DS2431-A1 has four main data components: 64-bit lasered ROM, 64-bit scratchpad, four 32-byte pages of EEPROM, and 64-bit register page.

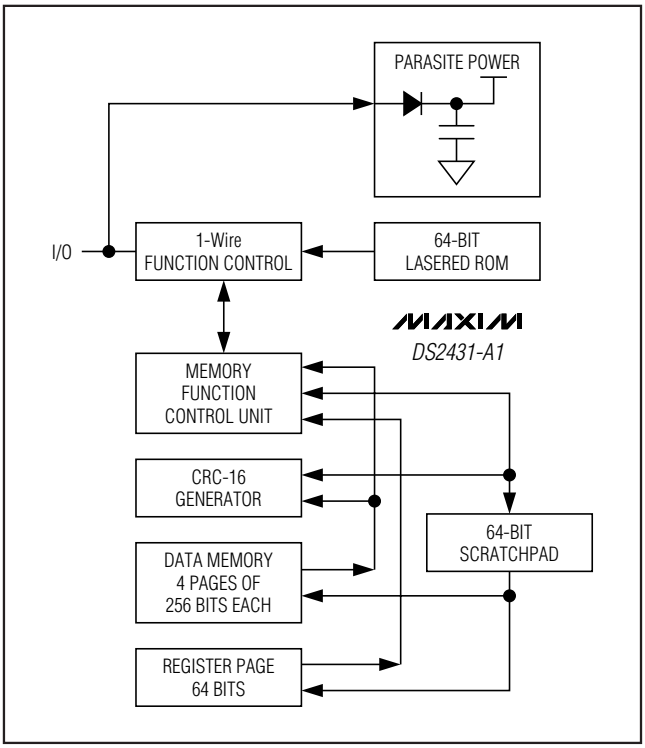


Figure 1. Block Diagram

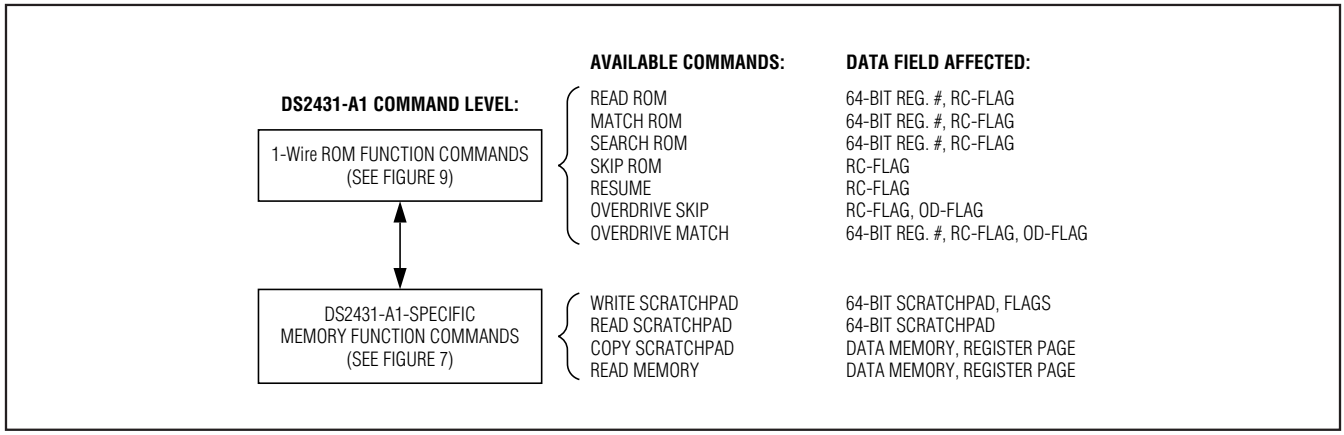


Figure 2. Hierarchical Structure for 1-Wire Protocol

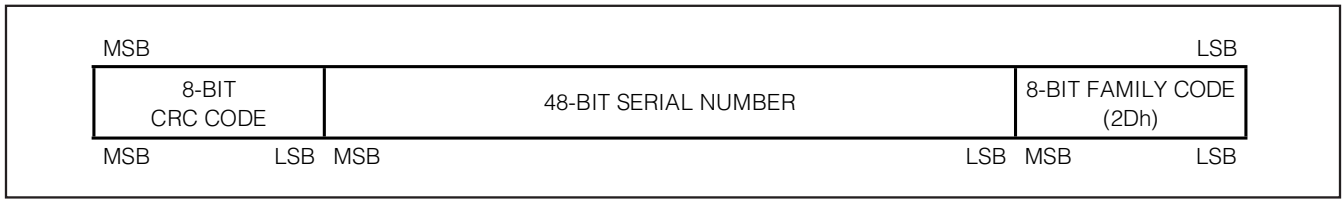


Figure 3. 64-Bit Lasered ROM

The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume, Overdrive Skip ROM, Overdrive Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters Overdrive Mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master can provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. **All data is read and written least significant bit first.**

64-Bit Lasered ROM

Each DS2431-A1 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC (cyclic redundancy check) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in *Application Note 27*.

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

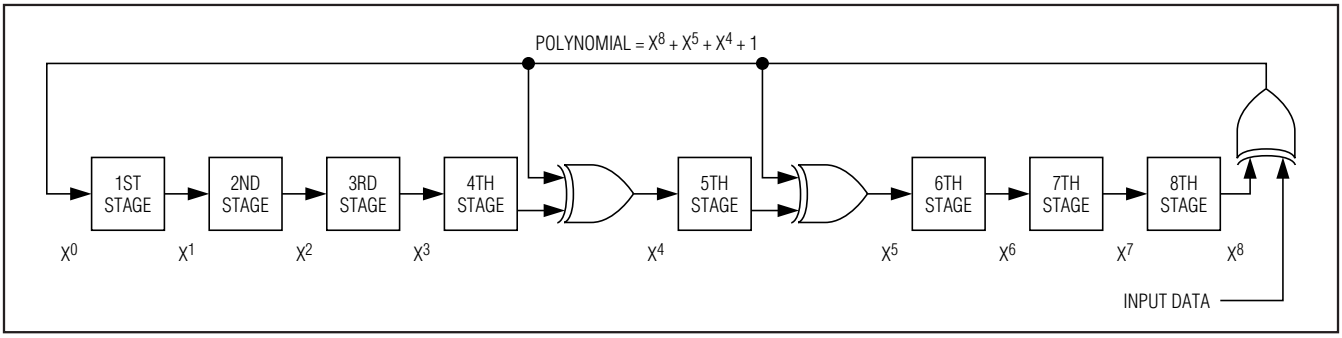


Figure 4. 1-Wire CRC Generator

Memory

Data memory and registers are located in a linear address space, as shown in Figure 5. The data memory and the registers have unrestricted read access. The DS2431-A1 EEPROM array consists of 18 rows of 8 bytes each. The first 16 rows are divided equally into four memory pages (32 bytes each). These four pages are the primary data memory. Each page can be individually set to open (unprotected), write protected, or EPROM mode by setting the associated protection byte in the register row. The last two rows contain protection registers and reserved bytes. The register row consists of four protection control bytes, a copy protection byte, the factory byte, and two user byte/manufacture ID bytes. The manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS2431-A1 is associated with. Contact the factory to set up and reg-

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES
0000h to 001Fh	R/(W)	Data Memory Page 0	—
0020h to 003Fh	R/(W)	Data Memory Page 1	—
0040h to 005Fh	R/(W)	Data Memory Page 2	—
0060h to 007Fh	R/(W)	Data Memory Page 3	—
0080h*	R/(W)	Protection Control Byte Page 0	55h: Write Protect P0; AAh: EPROM Mode P0; 55h or AAh: Write Protect 80h
0081h*	R/(W)	Protection Control Byte Page 1	55h: Write Protect P1; AAh: EPROM Mode P1; 55h or AAh: Write Protect 81h
0082h*	R/(W)	Protection Control Byte Page 2	55h: Write Protect P2; AAh: EPROM Mode P2; 55h or AAh: Write Protect 82h
0083h*	R/(W)	Protection Control Byte Page 3	55h: Write Protect P3; AAh: EPROM Mode P3; 55h or AAh: Write Protect 83h
0084h*	R/(W)	Copy Protection Byte	55h or AAh: Copy Protect 0080:008Fh, and Any Write-Protected Pages
0085h	R	Factory Byte. Set at Factory.	AAh: Write Protect 85h, 86h, 87h; 55h: Write Protect 85h, Unprotect 86h, 87h
0086h	R/(W)	User Byte/Manufacturer ID	—
0087h	R/(W)	User Byte/Manufacturer ID	—
0088h to 008Fh	N/A	Reserved	—

** Once programmed to AAh or 55h this address becomes read-only. All other codes can be stored, but neither write protect the address nor activate any function.*

Figure 5. Memory Map

ister a custom manufacturer ID. The last row is reserved for future use. It is undefined in terms of R/W functionality and should not be used.

In addition to the main EEPROM array, an 8-byte volatile scratchpad is included. Writes to the EEPROM array are a two-step process. First, data is written to the scratchpad and then copied into the main array. This allows the user to first verify the data written to the scratchpad prior to copying into the main array. The device only supports full row (8-byte) copy operations. For data in the scratchpad to be valid for a copy operation, the address supplied with a Write Scratchpad must start on a row boundary, and 8 full bytes must be written into the scratchpad.

The protection control registers determine how incoming data on a Write Scratchpad command is loaded into the scratchpad. A protection setting of 55h (write protect) causes the incoming data to be ignored and the target address main memory data to be loaded into the scratchpad. A protection setting of AAh (EPROM mode) causes the logical AND of incoming data and target address main memory data to be loaded into the scratchpad. Any other protection control register setting leaves the associated memory page open for unrestricted write access. Protection control byte settings of 55h or AAh also write protect the protection control byte. The protection control byte setting of 55h does not block the copy. This allows write-protected data to be refreshed (i.e., reprogrammed with the current data) in the device.

The copy protection byte is used for a higher level of security, and should only be used after all other protection control bytes, user bytes, and write-protected pages are set to their final value. If the copy protection byte is set to 55h or AAh, all copy attempts to the register row and user byte row are blocked. In addition, all copy attempts to write-protected main memory pages (i.e., refresh) are blocked.

Address Registers and Transfer Status

The DS2431-A1 employs three address registers: TA1, TA2, and E/S (Figure 6). These registers are common to many other 1-Wire devices but operate slightly differently with the DS2431-A1. Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read-only transfer-status register used to verify data integrity with write commands. ES bits E2:E0 are loaded with the incoming T2:T0 on a Write Scratchpad command and increment on each subsequent data byte. This is, in effect, a byte-ending offset counter within the 8-byte scratchpad. Bit 5 of the E/S register, called PF, is a logic 1 if the data in the scratchpad is not valid due to a loss of power or if the master sends less bytes than needed to reach the end of the scratchpad. For a valid write to the scratchpad, T2:T0 must be 0 and the master must have sent 8 data bytes. Bits 3, 4, and 6 have no function; they always read 0. The highest valued bit of the E/S register, called AA or authorization accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

Writing with Verification

To write data to the DS2431-A1, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Note that Copy Scratchpad commands must be performed on 8-byte boundaries, i.e.,

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	0	PF	0	0	E2	E1	E0

Figure 6. Address Registers

the three LSBs of the target address (T2, T1, T0) must be equal to 000b. If T2:T0 are sent with nonzero values, the copy function is blocked. Under certain conditions (see the *Write Scratchpad Command* section) the master receives an inverted CRC-16 of the command, address (actual address sent), and data at the end of the Write Scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC-16, it should send the Read Scratchpad command to verify data integrity. As a preamble to the scratchpad data, the DS2431-A1 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the device did not recognize the Write command. If everything went correctly, both flags are cleared. Now the master can continue reading and verifying every data byte. After the master has verified the data, it can send the Copy Scratchpad command, for example. This command must be followed exactly by the data of the three address registers, TA1, TA2, and E/S. The master should obtain the contents of these registers by reading the scratchpad.

Memory Function Commands

The *Memory Function Flow Chart* (Figure 7) describes the protocols necessary for accessing the memory of the DS2431-A1. An example on how to use these functions to write to and read from the device is included at the end of this document. The communication between master and the DS2431-A1 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the Overdrive mode, the DS2431-A1 assumes standard speed.

Write Scratchpad Command [0Fh]

The Write Scratchpad command applies to the data memory and the writable addresses in the register page. In order for the scratchpad data to be valid for copying to the array, the user must perform a Write Scratchpad command of 8 bytes starting at a valid row boundary. The Write Scratchpad command accepts invalid addresses and partial rows, but subsequent Copy Scratchpad commands are blocked.

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset of T2:T0. The ES bits E2:E0 are loaded with the starting byte offset, and increment with each subsequent byte. Effectively, E2:E0 is the byte offset of the last full byte written to the scratchpad. Only full data bytes are accepted.

When executing the Write Scratchpad command, the CRC generator inside the DS2431-A1 (Figure 13) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte as sent by the master. This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses (TA1 and TA2), and all the data bytes. Note that the CRC-16 calculation is performed with the actual TA1 and TA2 and data sent by the master. The master can end the Write Scratchpad command at any time. However, if the end of the scratchpad is reached (E2:E0 = 111b), the master can send 16 read-time slots and receive the CRC generated by the DS2431-A1.

If a Write Scratchpad is attempted to a write-protected location, the scratchpad is loaded with the data already in memory, rather than the data transmitted. Similarly, if the target address page is in EPROM mode, the scratchpad is loaded with the bitwise logical AND of the transmitted data and data already in memory.

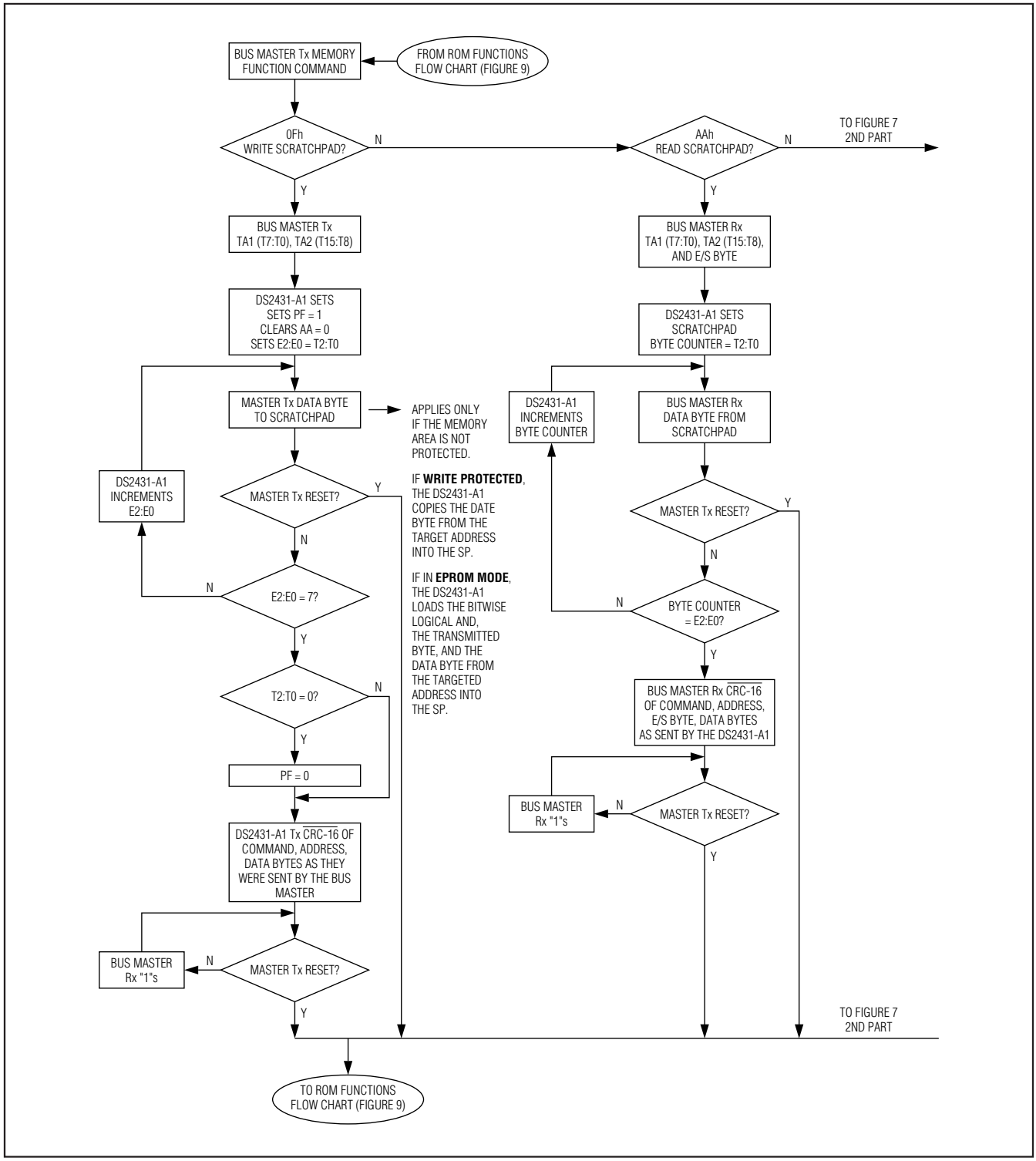


Figure 7. Memory Function Flow Chart

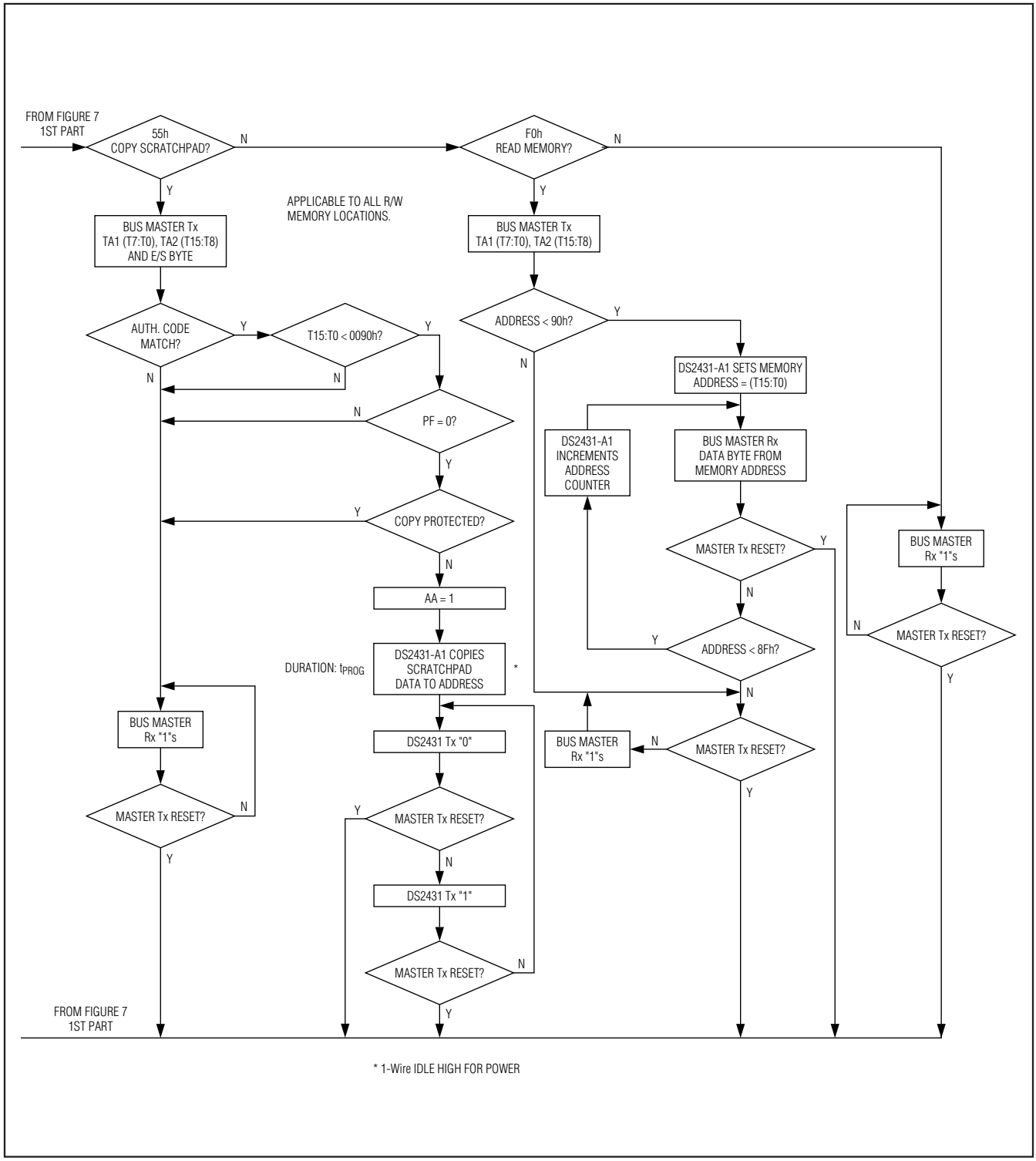


Figure 7. Memory Function Flow Chart (continued)

Read Scratchpad Command [AAh]

The Read Scratchpad command allows verifying the target address and the integrity of the scratchpad data. After issuing the command code, the master begins reading. The first two bytes are the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data, which may be different from what the master originally sent. This is of particular importance if the target address is within the register page or a page in either Write Protection or EPROM modes. See the *Write Scratchpad Command* section for details. The master should read through the scratchpad (E2:E0 - T2:T0 + 1 bytes), after which it receives the inverted CRC, based on data as it was sent by the DS2431-A1. If the master continues reading after the CRC, all data are logic 1s.

Copy Scratchpad [55h]

The Copy Scratchpad command is used to copy data from the scratchpad to writable memory sections. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which should have been obtained by an immediately preceding Read Scratchpad command. This 3-byte pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the target address is valid, the PF flag is not set, and the target memory is not copy protected, then the AA (authorization accepted) flag is set and the copy begins. All eight bytes of scratchpad contents are copied to the target memory location. The duration of the device's internal data transfer is t_{PROG} during which the voltage on the 1-Wire bus must not fall below 2.8V. A pattern of alternating 0s and 1s are transmitted after the data has been copied until the master issues a reset pulse. If the PF flag is set or the target memory is copy protected, the copy does not begin and the AA flag is not set.

Read Memory [F0h]

The Read Memory command is the general function to read data from the DS2431-A1. After issuing the command, the master must provide the 2-byte target address. After these two bytes, the master reads data beginning from the target address and may continue until address 008Fh. If the master continues reading, the result is logic 1s. The device's internal TA1, TA2, E/S, and scratchpad contents are not affected by a Read Memory command.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS2431-A1 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS2431-A1 is open drain with an internal circuit equivalent to that shown in Figure 8.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS2431-A1 supports both a standard and overdrive communication speed of 15.4kbps (max) and 125kbps (max), respectively. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and overdrive of 142kbps. The slightly reduced rates for the DS2431-A1 are a result of additional recovery times, which in turn were driven by a 1-Wire physical interface enhancement to improve noise immunity. The value of the pullup resistor primarily depends on the network size and load conditions. The DS2431-A1 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus might be reset.

Transaction Sequence

The protocol for accessing the DS2431-A1 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

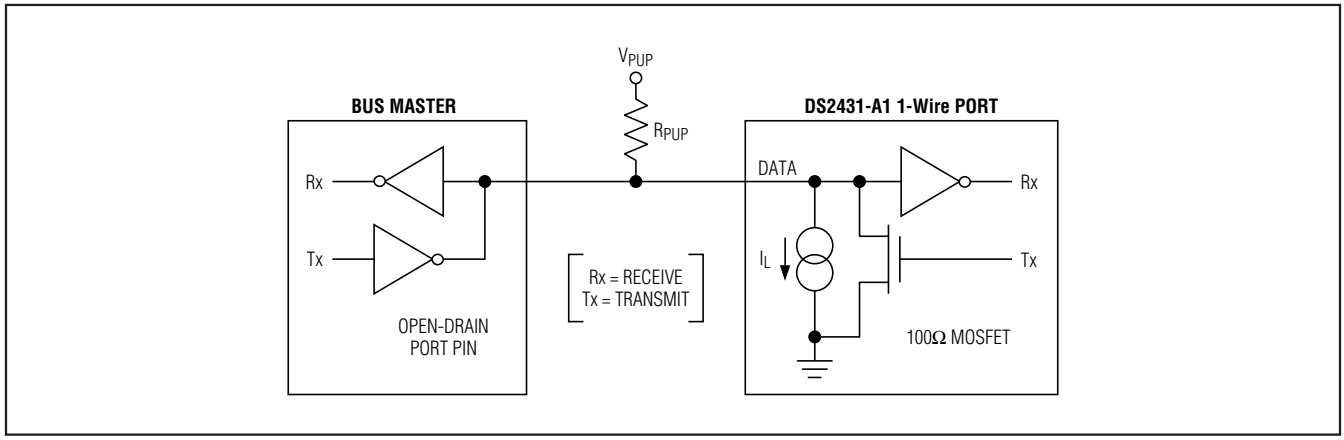


Figure 8. Hardware Configuration

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2431-A1 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS2431-A1 supports. All ROM function commands are 8 bits long. A list of these commands follows (see the flow chart in Figure 9).

Read ROM [33h]

The Read ROM command allows the bus master to read the DS2431-A1's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2431-A1 on a multidrop bus. Only the DS2431-A1 that exactly matches the 64-bit ROM sequence responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the romcode tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a Read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

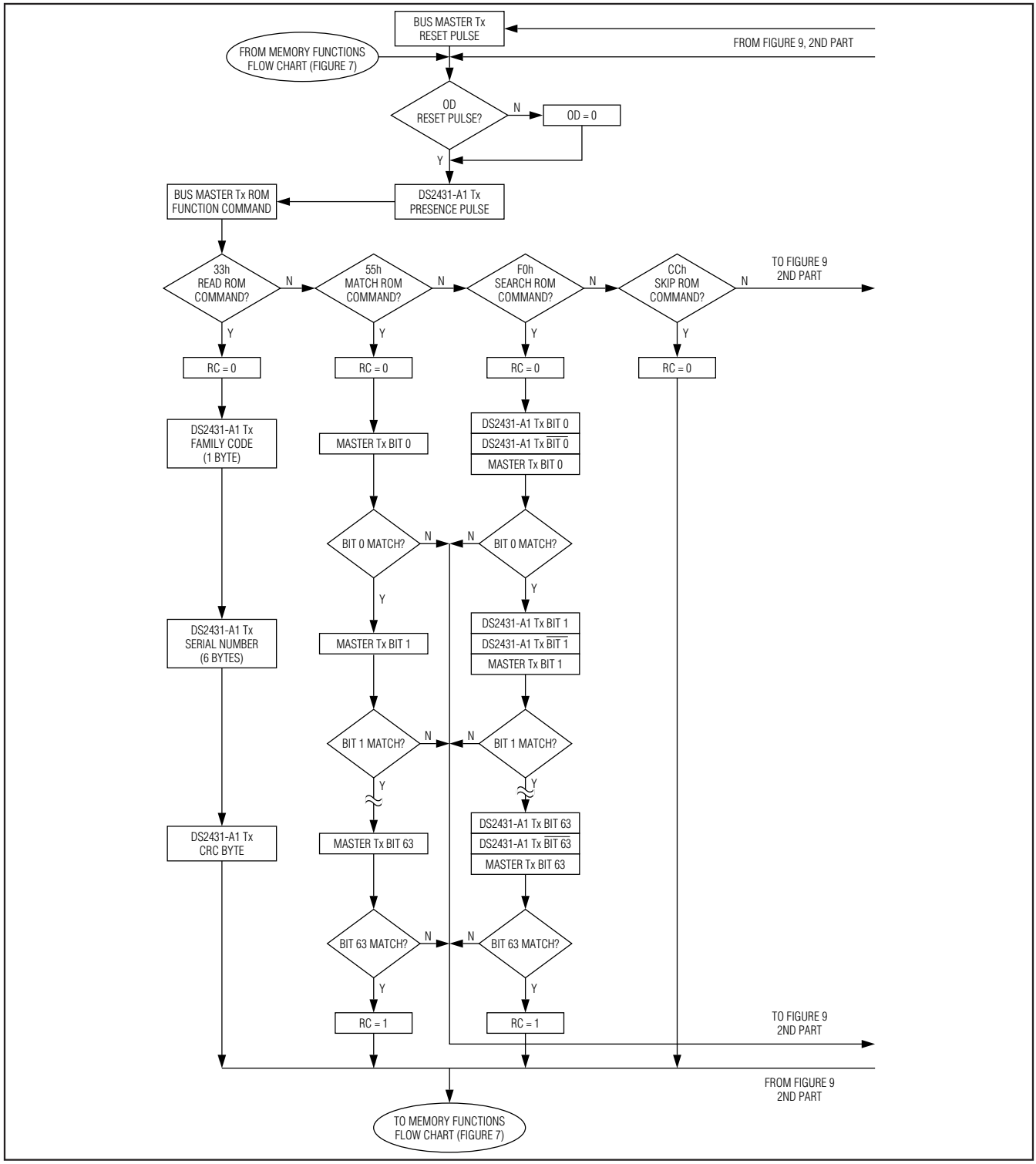
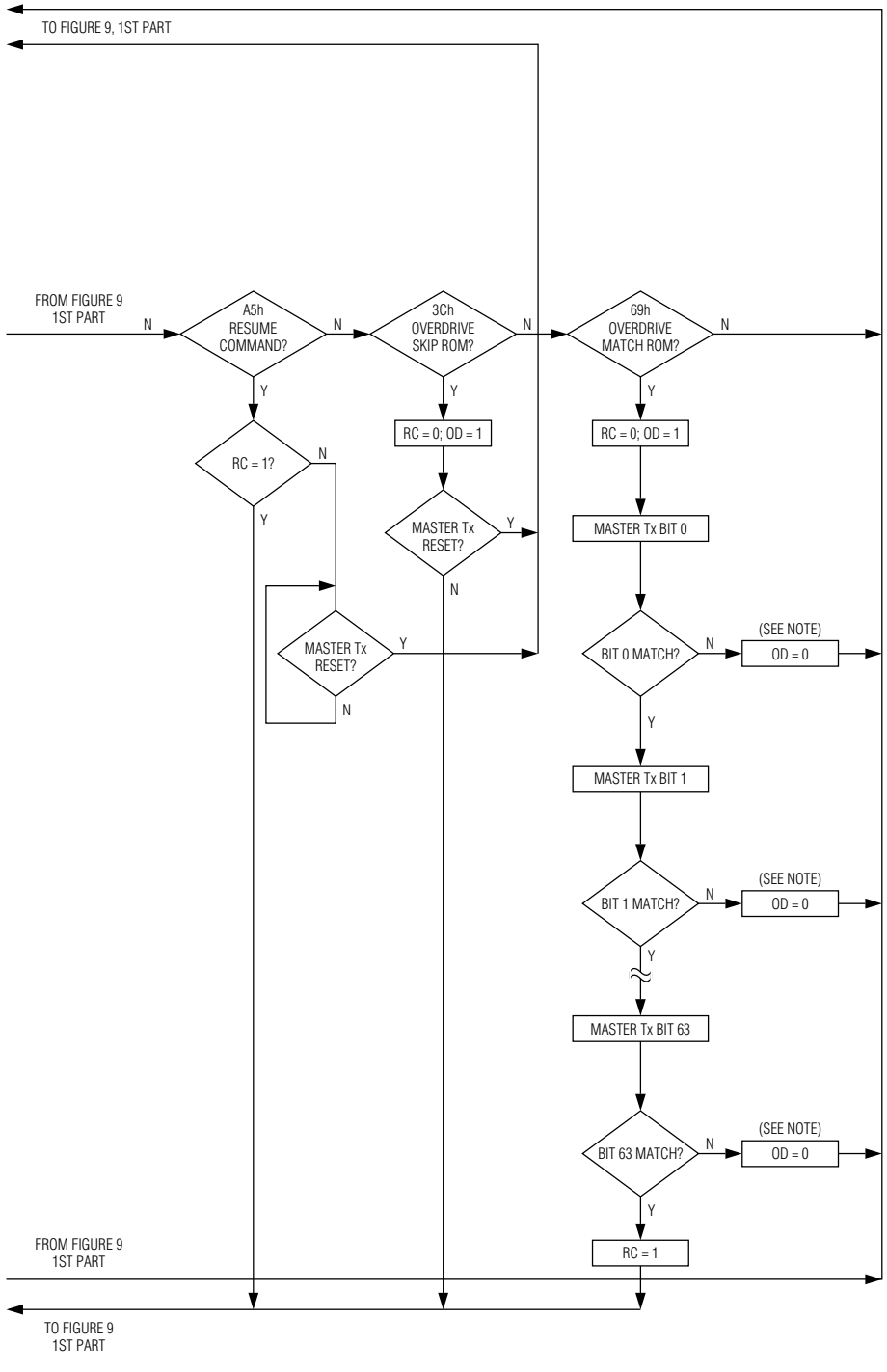


Figure 9. ROM Functions Flow Chart



NOTE: THE OD FLAG REMAINS AT 1 IF THE DEVICE WAS ALREADY AT OVERDRIVE SPEED BEFORE THE OVERDRIVE MATCH ROM COMMAND WAS ISSUED.

Figure 9. ROM Functions Flow Chart (continued)

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume function is available. This function checks the status of the RC bit and, if it is set, directly transfers control to the Memory functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command function.

Overdrive Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS2431-A1 in the Overdrive mode (OD = 1). All communication following this command has to occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into Overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive Match ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS2431-A1 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS2431-A1 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

1-Wire Signaling

The DS2431-A1 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS2431-A1 can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the Overdrive mode, the DS2431-A1 communicates at standard speed. While in Overdrive mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 10 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS2431-A1 when determining a logical level, not triggering any events.

Figure 10 shows the initialization sequence required to begin any communication with the DS2431-A1. A reset pulse followed by a presence pulse indicates that the DS2431-A1 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the Overdrive mode, returning the device to standard speed. If the DS2431 is in Overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive mode. If the device is in Overdrive mode and t_{RSTL} is *between* 80µs and 480µs, the device resets, but the communication speed is undetermined.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor, or in the case of a DS2482-x00 or DS2480B driver, through the active circuitry. When the threshold V_{TH} is crossed, the DS2431-A1 waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS2431-A1 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

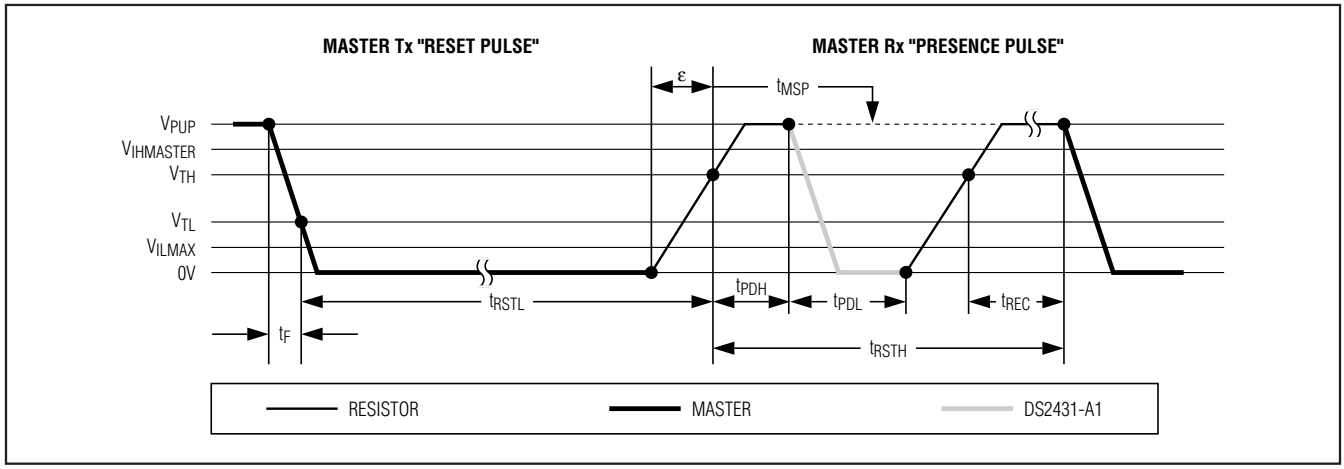


Figure 10. Initialization Procedure: Reset and Presence Pulse

Read-/Write-Time Slots

Data communication with the DS2431-A1 takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. Figure 11 illustrates the definitions of the write- and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS2431-A1 starts its internal timing generator that determines when the data line is sampled during a write-time slot and how long data is valid during a read-time slot.

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS2431-A1 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS2431-A1 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS2431-A1 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS2431-A1 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS2431-A1 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS2431-A1 attached to a 1-Wire line. For multidevice configurations, t_{REC} should be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

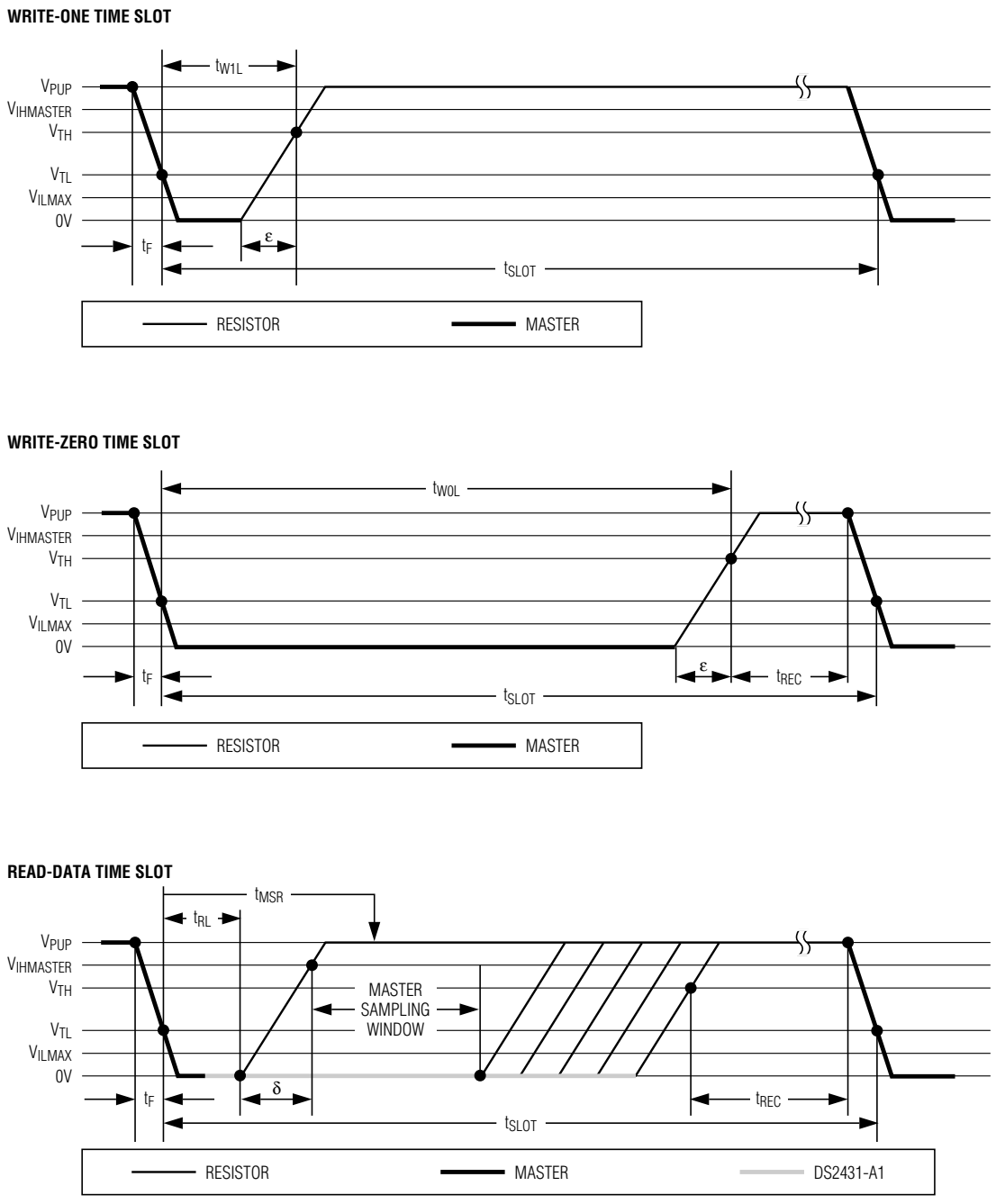


Figure 11. Read/Write Timing Diagrams

1024-Bit, 1-Wire EEPROM for Automotive Applications

Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS2431-A1 uses a new 1-Wire front-end, which makes it less sensitive to noise.

The 1-Wire front-end of the DS2431-A1 differs from traditional slave devices in three characteristics.

1) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TH} - V_{HY}, it will not be recognized (Figure 12, Case A). The hysteresis is effective at any 1-Wire speed.
3) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below the V_{TH} - V_{HY} threshold (Figure 12, Case B, $t_{GL} < t_{REH}$). Deep voltage drops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 12, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters V_{HY} and t_{REH} specified in their electrical characteristics use the improved 1-Wire front-end.

CRC Generation

The DS2431-A1 uses two different types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2431-A1 to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form. It is computed at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $x^{16} + x^{15} + x^2 + 1$. This CRC is used for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS2431-A1 chip (Figure 13) calculates a new 16-bit CRC, as shown in the command flow chart (Figure 7). The bus master compares the CRC value read from the device to the one it calculates from the data, and decides whether to continue with an operation or to reread the portion of the data with the CRC error.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes as they were sent by the bus master. The DS2431-A1 transmits this CRC only if E2:E0 = 111b.

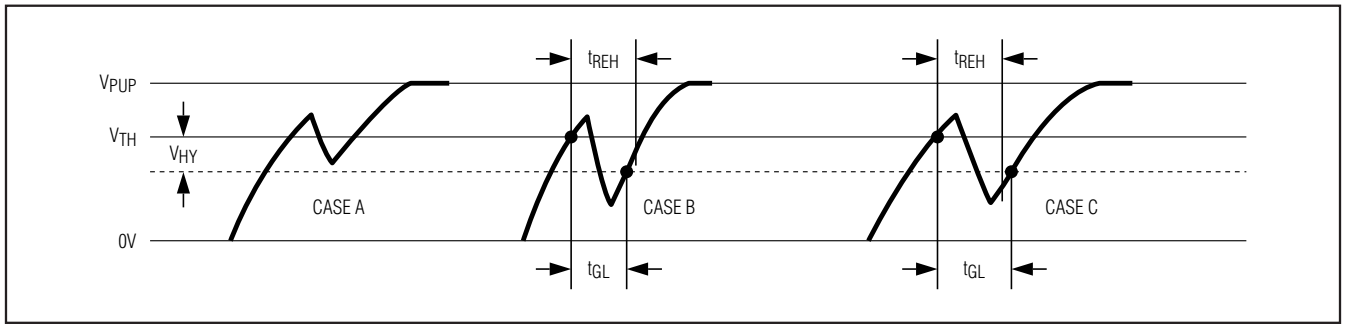


Figure 12. Noise Suppression Scheme

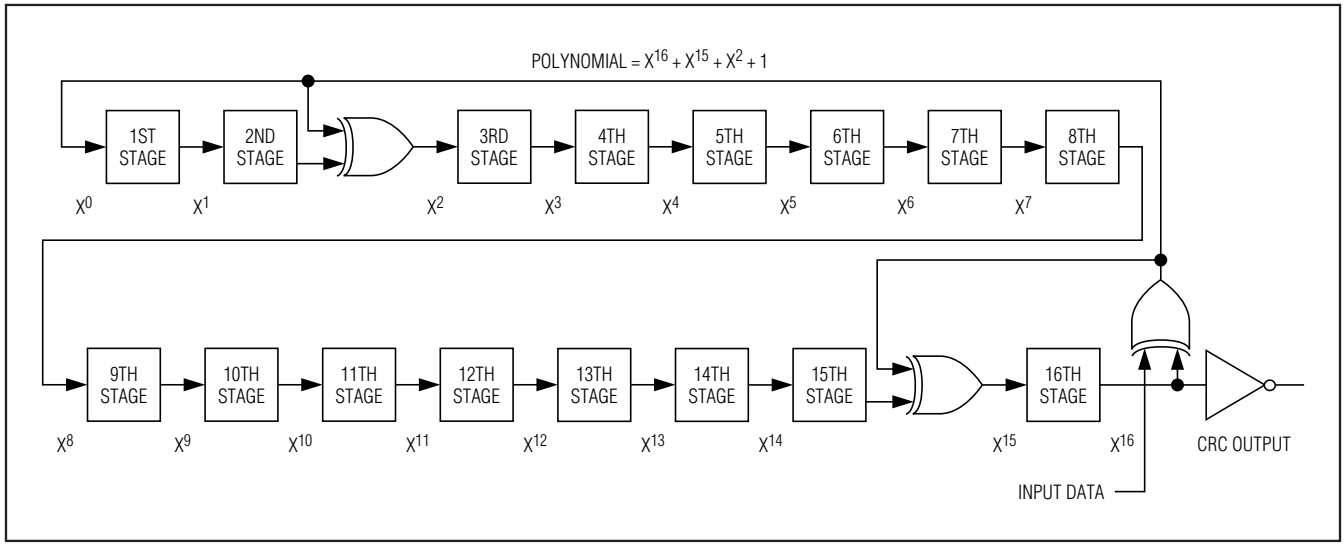


Figure 13. CRC-16 Hardware Description and Polynomial

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data as they were sent by the DS2431-A1. The DS2431-A1 transmits this CRC only if the reading continues through the end of the scratchpad. For more information on generating CRC values, refer to *Application Note 27*.

Command-Specific 1-Wire Communication Protocol—Legend

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master.
PD	1-Wire presence pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol.
WS	Command "Write Scratchpad."
RS	Command "Read Scratchpad."
CPS	Command "Copy Scratchpad."
RM	Command "Read Memory."
TA	Target address TA1, TA2.
TA-E/S	Target address TA1, TA2 with E/S byte.
<8–T2:T0 bytes>	Transfer of as many bytes as needed to reach the end of the scratchpad for a given target address.
<Data to EOM>	Transfer of as many data bytes as are needed to reach the end of the memory.
$\overline{\text{CRC-16}}$	Transfer of an inverted CRC-16.
FF Loop	Indefinite loop where the master reads FF bytes.
AA Loop	Indefinite loop where the master reads AA bytes.
Programming	Data transfer to EEPROM; no activity on the 1-Wire bus permitted during this time.

1024-Bit, 1-Wire EEPROM for Automotive Applications

Command-Specific 1-Wire Communication Protocol—Color Codes

Master to Slave	Slave to Master	Programming

1-Wire Communication Examples

Write Scratchpad

RST	PD	Select	WS	TA	<8–T2:T0 bytes>	$\overline{\text{CRC-16}}$	FF Loop

Read Scratchpad

RST	PD	Select	RS	TA-E/S	<8–T2:T0 bytes>	$\overline{\text{CRC-16}}$	FF Loop

Copy Scratchpad (Success)

RST	PD	Select	CPS	TA-E/S	Programming	AA Loop

Copy Scratchpad (Invalid Address or PF = 1 or Copy Protected)

RST	PD	Select	CPS	TA-E/S	FF Loop

Read Memory (Success)

RST	PD	Select	RM	TA	<Data to EOM>	FF Loop

Read Memory (Invalid Address)

RST	PD	Select	RM	TA	FF Loop

Memory Function Example

Write to the first 8 bytes of memory page 1. Read the entire memory.

With only a single DS2431-A1 connected to the bus master, the communication looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	0Fh	Issue “Write Scratchpad” command
Tx	20h	TA1, beginning offset = 20h
Tx	00h	TA2, address = 0020h
Tx	<8 Data Bytes>	Write 8 bytes of data to scratchpad
Rx	<2 Bytes $\overline{\text{CRC-16}}$>	Read CRC to check for data integrity
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	AAh	Issue “Read Scratchpad” command
Rx	20h	Read TA1, beginning offset = 20h
Rx	00h	Read TA2, address = 0020h
Rx	07h	Read E/S, ending offset = 111b, AA, PF = 0
Rx	<8 Data Bytes>	Read scratchpad data and verify
Rx	<2 Bytes $\overline{\text{CRC-16}}$>	Read CRC to check for data integrity
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	55h	Issue “Copy Scratchpad” command
Tx	20h	TA1 (AUTHORIZATION CODE)
Tx	00h	TA2
Tx	07h	E/S
—	<1-Wire Idle High>	Wait $t_{PROGMAX}$ for the copy function to complete
Rx	AAh	Read copy status, AAh = success
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	F0h	Issue “Read Memory” command
Tx	00h	TA1, beginning offset = 00h
Tx	00h	TA2, address = 0000h
Rx	<144 Data Bytes>	Read the entire memory
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse

Package Information

(For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

PACKAGE TYPE	DOCUMENT NO.
6 TSOC	**56-G2016-001**

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