

# M66310P/FP

## 16-Bit LED Driver with Shift Register and Latch

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### Description

M66310P/FP is a LED array driver having a 16 bit serial-input and parallel output shift-register function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24 mA which is sufficient for cathode common LED drive, capable of flowing 16 bits continuously at the same time.

Parallel output is open drain output.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin layout ensures the realization of an easy printed circuit.

### Features

- Cathode common LED drive
- High output current  
all parallel output  $I_{OH} = -24$  mA  
simultaneous lighting available
- Low power dissipation: 100  $\mu$ W/package (max)  
( $V_{CC} = 5$  V,  $T_a = 25^\circ\text{C}$ , quiescent state)
- High noise margin  
schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output (except serial data output)
- Wide operating temperature range:  $T_a = -40$  to  $+85^\circ\text{C}$
- Pin layout facilitates printed circuit wiring. (This layout facilitates cascade connection and LED connection.)

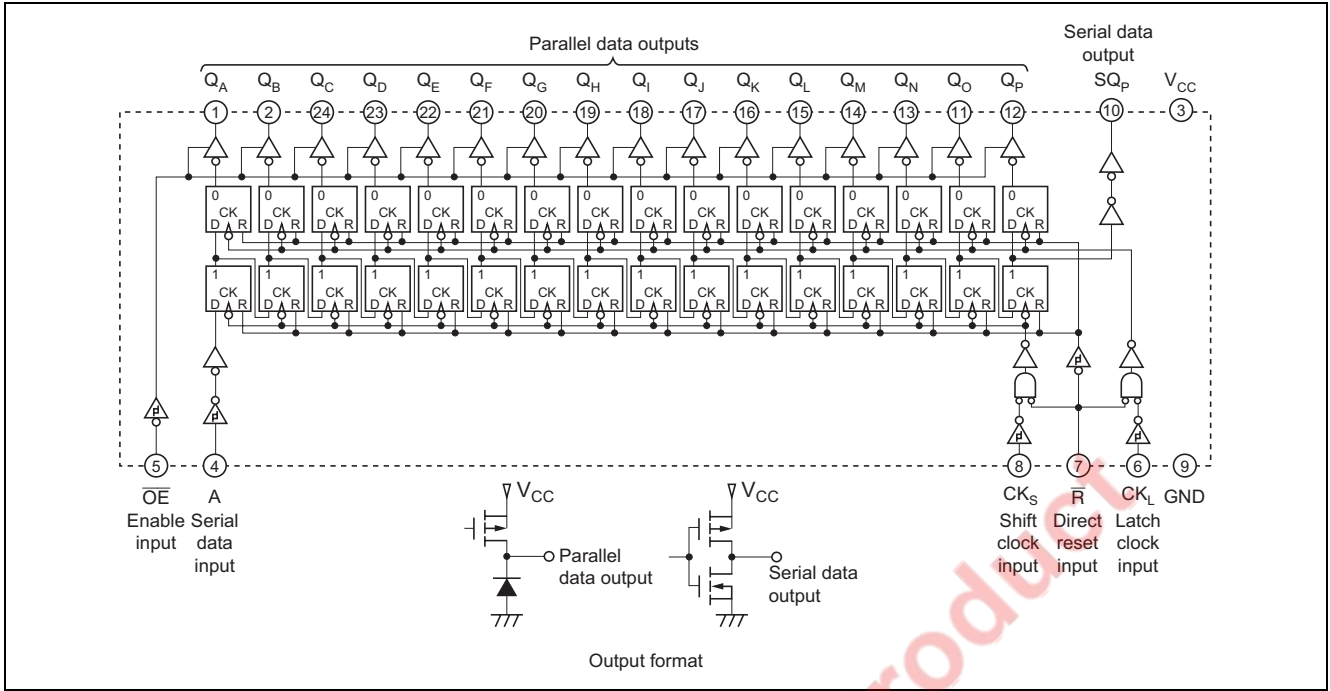
### Application

LED array drive of BUTTON TELEPHONE

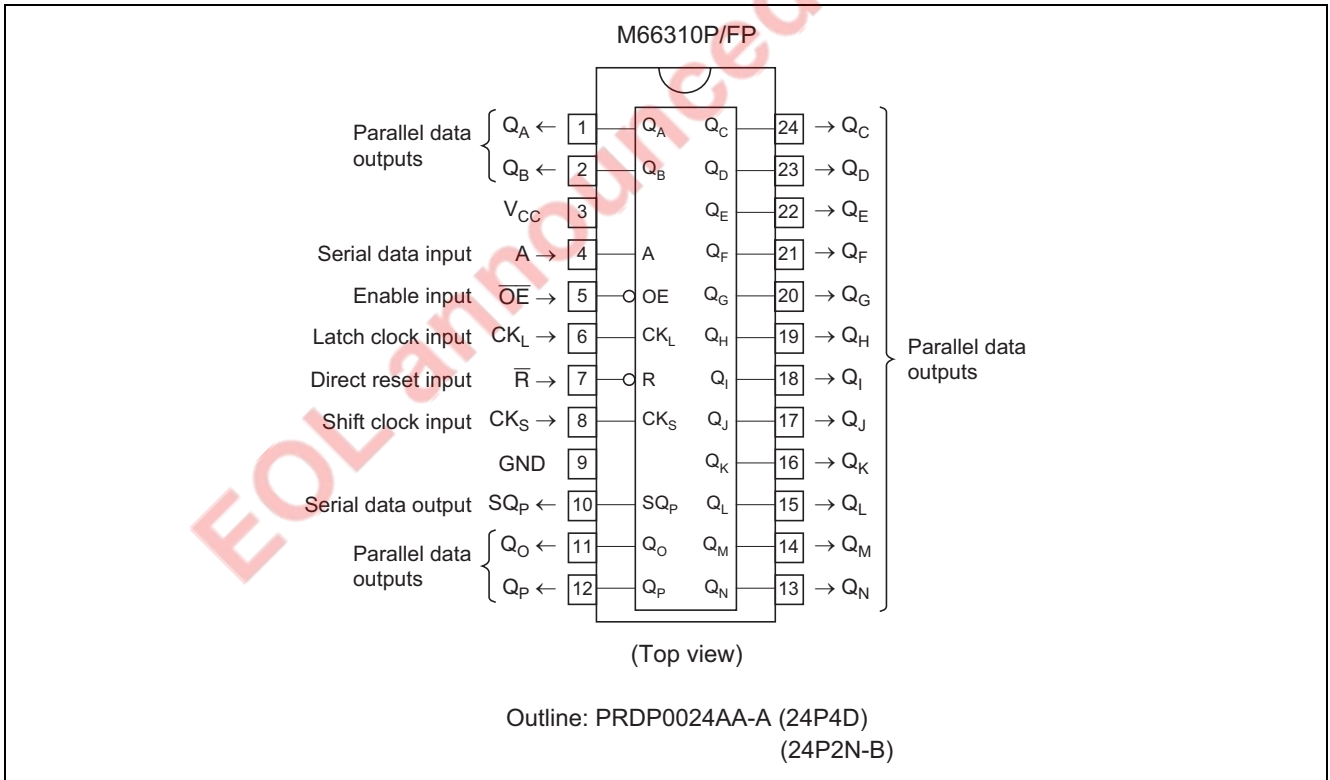
LED array drive of ERASER of a PPC copier

Other various LED modules

### Logic Diagram



### Pin Arrangement



## Functional Description

As M66310P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shift-register consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input  $CK_S$  and latch clock input  $CK_L$  are independent from each other, shift and latch operations being made when “L” changes to “H”.

Serial data input A is the data input of the first-step shift-register and the signal of A shifts shifting registers one by one when a pulse is impressed to  $CK_S$ . When A is “L”, the signal of “L” shifts.

When the pulse is impressed to  $CK_L$ , the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from  $Q_A$  to  $Q_P$ .

Outputs from  $Q_A$  to  $Q_P$  are open drain outputs.

To extend the number of bits, use the serial data output  $SQ_P$  which shows the output of the shifting register of the 16th bit.

If  $CK_S$  and  $CK_L$  are connected, the state of the shifting register with one clock delay is outputted to  $Q_A$  to  $Q_P$ .

When reset input  $\bar{R}$  is changed to “L”,  $Q_A$  to  $Q_P$  and  $SQ_P$  are reset. In this case, shifting and latching registers are reset.

If “H” is impressed to output enable input  $\bar{OE}$ ,  $Q_A$  to  $Q_P$  reaches the high impedance state, but  $SQ_P$  does not reach the high impedance state. Furthermore, change in  $\bar{OE}$  does not affect shift operation.

**Function Table** (Note)

Operation Mode	Input					Parallel Data Output																Serial Data Output $SQ_P$	Remarks		
	$\bar{R}$	$CK_S$	$CK_L$	A	$\bar{OE}$	$Q_A$	$Q_B$	$Q_C$	$Q_D$	$Q_E$	$Q_F$	$Q_G$	$Q_H$	$Q_I$	$Q_J$	$Q_K$	$Q_L$	$Q_M$	$Q_N$	$Q_O$	$Q_P$				
Reset	L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	–	
Shift latch operation	Shift $t_1$	H	↑	X	H	L	$Q_A^0$	$Q_B^0$	$Q_C^0$	$Q_D^0$	$Q_E^0$	$Q_F^0$	$Q_G^0$	$Q_H^0$	$Q_I^0$	$Q_J^0$	$Q_K^0$	$Q_L^0$	$Q_M^0$	$Q_N^0$	$Q_O^0$	$Q_P^0$	$q_O^0$	Output lighting "H"	
	Latch $t_2$	H	X	↑	X	L	H	$q_A^0$	$q_B^0$	$q_C^0$	$q_D^0$	$q_E^0$	$q_F^0$	$q_G^0$	$q_H^0$	$q_I^0$	$q_J^0$	$q_K^0$	$q_L^0$	$q_M^0$	$q_N^0$	$q_O^0$	$q_O^0$	$q_O^0$	Output lights-out "L"
	Shift $t_1$	H	↑	X	L	L	$Q_A^0$	$Q_B^0$	$Q_C^0$	$Q_D^0$	$Q_E^0$	$Q_F^0$	$Q_G^0$	$Q_H^0$	$Q_I^0$	$Q_J^0$	$Q_K^0$	$Q_L^0$	$Q_M^0$	$Q_N^0$	$Q_O^0$	$Q_P^0$	$q_O^0$	Output lights-out "L"	
	Latch $t_2$	H	X	↑	X	L	Z	$q_A^0$	$q_B^0$	$q_C^0$	$q_D^0$	$q_E^0$	$q_F^0$	$q_G^0$	$q_H^0$	$q_I^0$	$q_J^0$	$q_K^0$	$q_L^0$	$q_M^0$	$q_N^0$	$q_O^0$	$q_O^0$	$q_O^0$	–
Output disable	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	$q_P$	–	

Note    ↑: Change from low-level to high-level  
 $Q^0$ : Output state Q before  $CK_L$  changed  
 X: Irrelevant  
 $q^0$ : Contents of shift register before  $CK_S$  changed  
 q: Contents of shift register  
 $t_1, t_2$ :  $t_2$  is set after  $t_1$  is set  
 Z: High impedance

## Absolute Maximum Ratings

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	-0.5 to +7.0	V	
Input voltage	V <sub>I</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Output voltage	V <sub>O</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Input protection diode current	I <sub>IK</sub>	-20	mA	V <sub>I</sub> < 0 V
		20		V <sub>I</sub> > V <sub>CC</sub>
Output parasitic diode current	I <sub>OK</sub>	-20	mA	V <sub>O</sub> < 0 V
		20		V <sub>O</sub> > V <sub>CC</sub>
Output current per output pin	Q <sub>A</sub> to Q <sub>P</sub>	I <sub>O</sub>	mA	
	SQ <sub>P</sub>			±25
Supply/GND current	I <sub>CC</sub>	-410, +20	mA	V <sub>CC</sub> , GND
Power dissipation	P <sub>d</sub>	500	mW	(Note)
Storage temperature range	T <sub>stg</sub>	-65 to +150	°C	

Note: M66310FP; Ta = -40 to +70°C, Ta = 70 to 85°C are derated at -6 mW/°C.

## Recommended Operating Conditions

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V <sub>CC</sub>	4.5	5	5.5	V
Input voltage	V <sub>I</sub>	0	—	V <sub>CC</sub>	V
Output voltage	V <sub>O</sub>	0	—	V <sub>CC</sub>	V
Operating temperature range	T <sub>opr</sub>	-40	—	+85	°C

## Electrical Characteristics

(V<sub>CC</sub> = 4.5 to 5.5 V, unless otherwise noted)

Item	Symbol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = -40 to +85°C				
		Min	Typ	Max	Min	Max			
Positive-going threshold voltage	V <sub>T+</sub>	0.35×V <sub>CC</sub>	—	0.7×V <sub>CC</sub>	0.35×V <sub>CC</sub>	0.7×V <sub>CC</sub>	V	V <sub>O</sub> = 0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>   = 20 μA	
Negative-going threshold voltage	V <sub>T-</sub>	0.2×V <sub>CC</sub>	—	0.55×V <sub>CC</sub>	0.2×V <sub>CC</sub>	0.55×V <sub>CC</sub>	V	V <sub>O</sub> = 0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>   = 20 μA	
High-level output voltage Q <sub>A</sub> to Q <sub>P</sub>	V <sub>OH</sub>	V <sub>CC</sub> -0.1	—	—	V <sub>CC</sub> -0.1	—	V	V <sub>I</sub> = V <sub>T+</sub> , V <sub>T-</sub> V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -20 μA
		3.83	—	—	3.66	—			I <sub>OH</sub> = -24 mA
		3.50	—	—	3.25	—			I <sub>OH</sub> = -40 mA <sup>(Note)</sup>
High-level output voltage SQ <sub>P</sub>	V <sub>OH</sub>	V <sub>CC</sub> -0.1	—	—	V <sub>CC</sub> -0.1	—	V	V <sub>I</sub> = V <sub>T+</sub> , V <sub>T-</sub> V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -20 μA
		3.83	—	—	3.66	—			I <sub>OH</sub> = -4 mA
Low-level output voltage SQ <sub>P</sub>	V <sub>OL</sub>	—	—	0.1	—	0.1	V	V <sub>I</sub> = V <sub>T+</sub> , V <sub>T-</sub> V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 μA
		—	—	0.44	—	0.53			I <sub>OL</sub> = 4 mA
High-level input current	I <sub>IH</sub>	—	—	0.5	—	5.0	μA	V <sub>I</sub> = V <sub>CC</sub> , V <sub>CC</sub> = 5.5 V	
Low-level input current	I <sub>IL</sub>	—	—	-0.5	—	-5.0	μA	V <sub>I</sub> = GND, V <sub>CC</sub> = 5.5 V	
Maximum output leakage current Q <sub>A</sub> to Q <sub>P</sub>	I <sub>O</sub>	—	—	1.0	—	10.0	μA	V <sub>I</sub> = V <sub>T+</sub> , V <sub>T-</sub> V <sub>CC</sub> = 5.5 V	V <sub>O</sub> = V <sub>CC</sub>
		—	—	-1.0	—	-10.0			V <sub>O</sub> = GND
Quiescent supply current	I <sub>CC</sub>	—	—	20.0	—	200.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND, V <sub>CC</sub> = 5.5 V	

Note: M66310 is used under the condition of an output current I<sub>OH</sub> = -40 mA, the number of simultaneous drive outputs are restricted as shown in the Duty Cycle-I<sub>OH</sub> of Standard characteristics.

## Switching Characteristics

(V<sub>CC</sub> = 5V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = -40 to +85°C			
		Min	Typ	Max	Min	Max		
Maximum clock frequency	f <sub>max</sub>	5	—	—	4	—	MHz	C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ (Note 2)
Low-level to high-level and high-level to low-level output propagation time (CK <sub>S</sub> -SQ <sub>P</sub> )	t <sub>PLH</sub>	—	—	100	—	130	ns	
	t <sub>PHL</sub>	—	—	100	—	130	ns	
High-level to low-level output propagation time ( $\bar{R}$ -SQ <sub>P</sub> )	t <sub>PHL</sub>	—	—	100	—	130	ns	
High-level to low-level output propagation time ( $\bar{R}$ -Q <sub>A</sub> to Q <sub>P</sub> )	t <sub>PHZ</sub>	—	—	150	—	200	ns	
Low-level to high-level and high-level to low-level output propagation time (CK <sub>L</sub> -Q <sub>A</sub> to Q <sub>P</sub> )	t <sub>PZH</sub>	—	—	100	—	130	ns	
	t <sub>PHZ</sub>	—	—	150	—	200	ns	
Output enable time to low-level and high-level ( $\bar{OE}$ -Q <sub>A</sub> to Q <sub>P</sub> )	t <sub>PZH</sub>	—	—	100	—	130	ns	
	t <sub>PHZ</sub>	—	—	150	—	200	ns	
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF	
Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF	$\bar{OE} = V_{CC}$
Power dissipation Capacitance (Note 1)	C <sub>PO</sub>	—	11	—	—	—	pF	

Note: 1. C<sub>PD</sub> is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)

The power dissipated during operation under no-load conditions is calculated using the following formula:

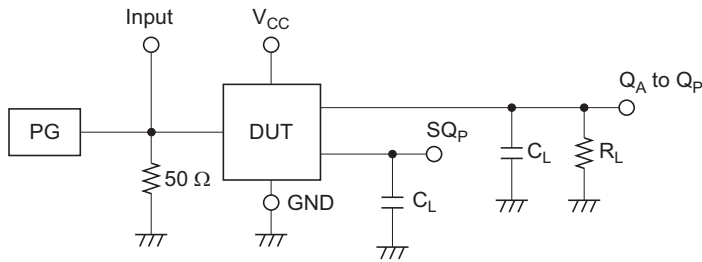
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$

## Timing Requirements

(V<sub>CC</sub> = 5 V)

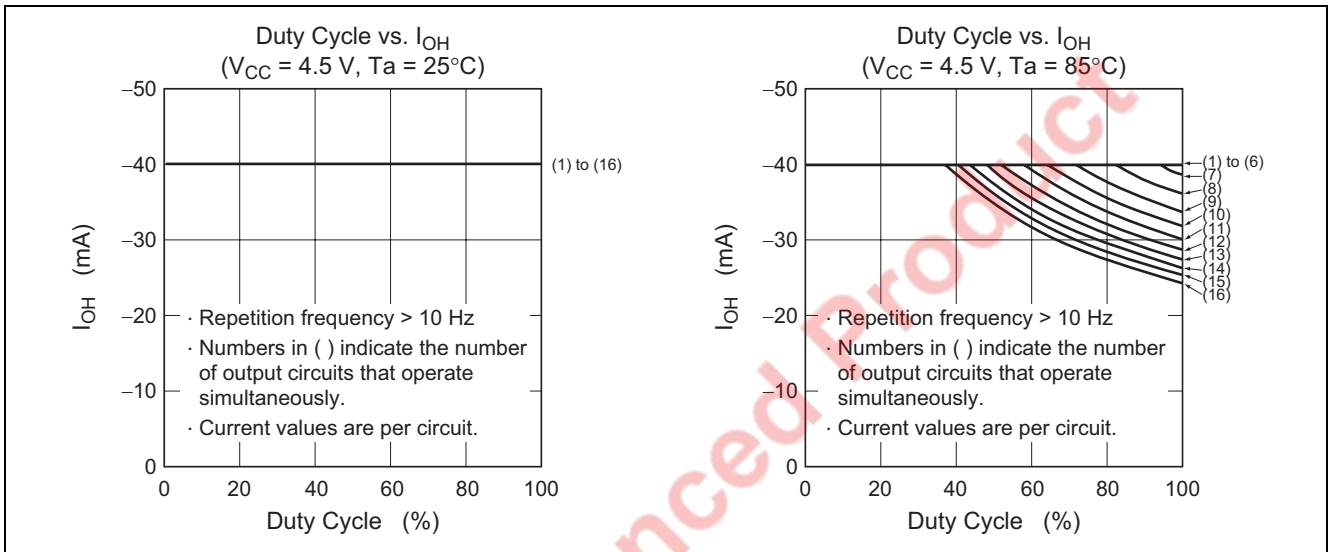
Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = -40 to +85°C			
		Min	Typ	Max	Min	Max		
CK <sub>S</sub> , CK <sub>L</sub> , $\bar{R}$ pulse width	t <sub>w</sub>	100	—	—	130	—	ns	(Note 2)
A setup time with respect to CK <sub>S</sub>	t <sub>su</sub>	100	—	—	130	—	ns	
CK <sub>S</sub> setup time with respect to CK <sub>L</sub>	t <sub>su</sub>	100	—	—	130	—	ns	
A hold time with respect to CK <sub>S</sub>	t <sub>h</sub>	10	—	—	15	—	ns	
$\bar{R}$ , recovery time with respect to CK <sub>S</sub> , CK <sub>L</sub>	t <sub>rec</sub>	50	—	—	70	—	ns	

Note: 2. Test Circuit



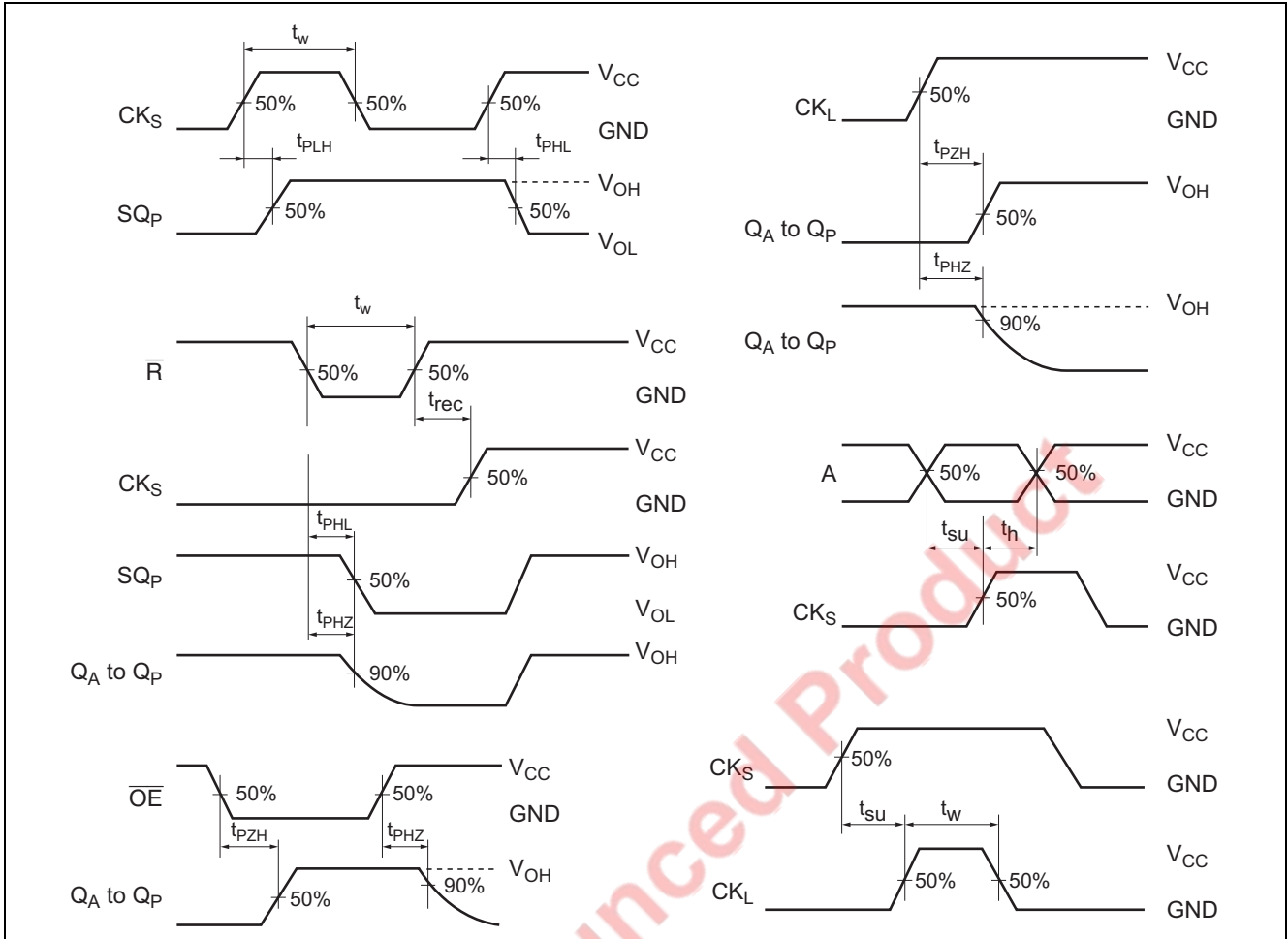
- (1) The pulse generator (PG) has the following characteristics (10% to 90%):  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$
- (2) The capacitance  $C_L$  includes stray wiring capacitance and the probe input capacitance.

### Typical Characteristics



EOL announced Product

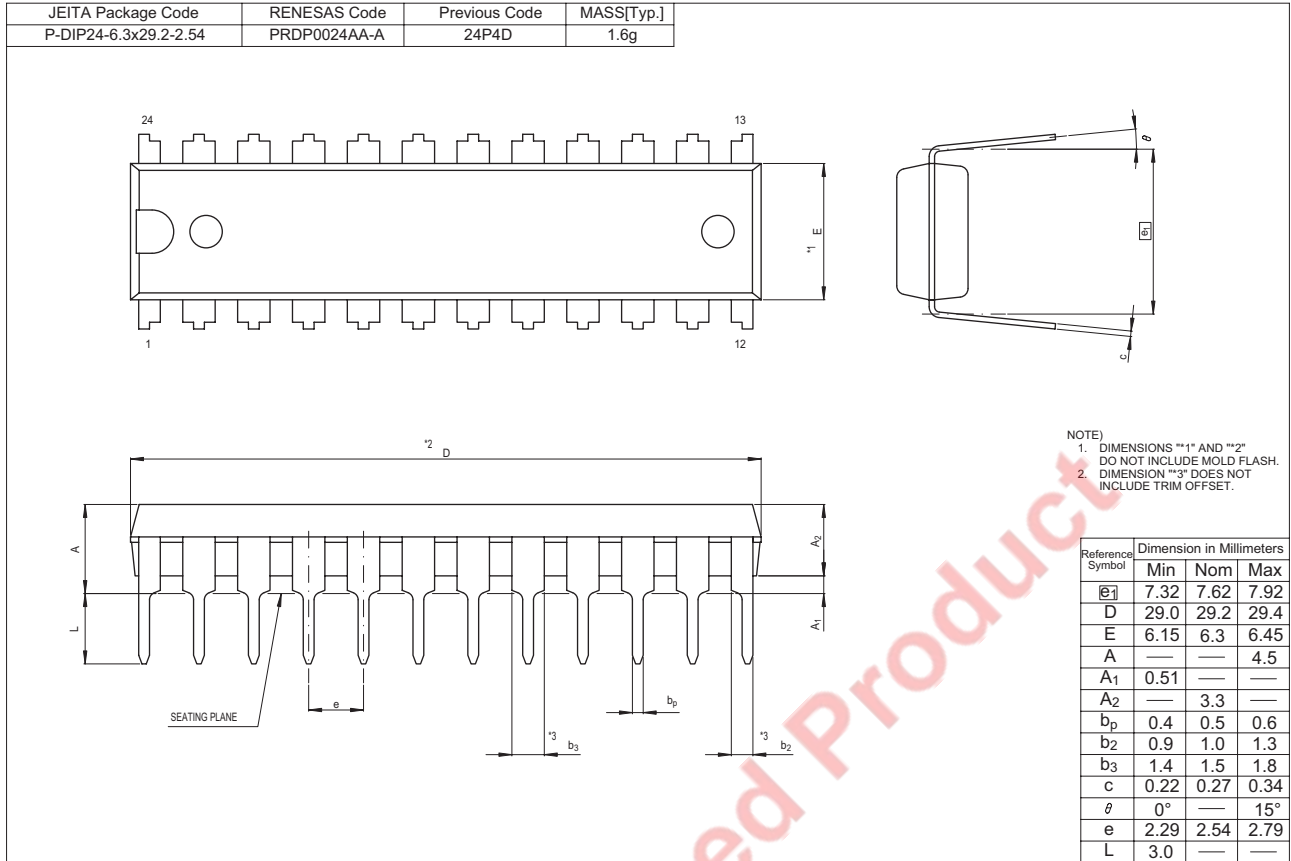
Timing Chart



EOL announced Product

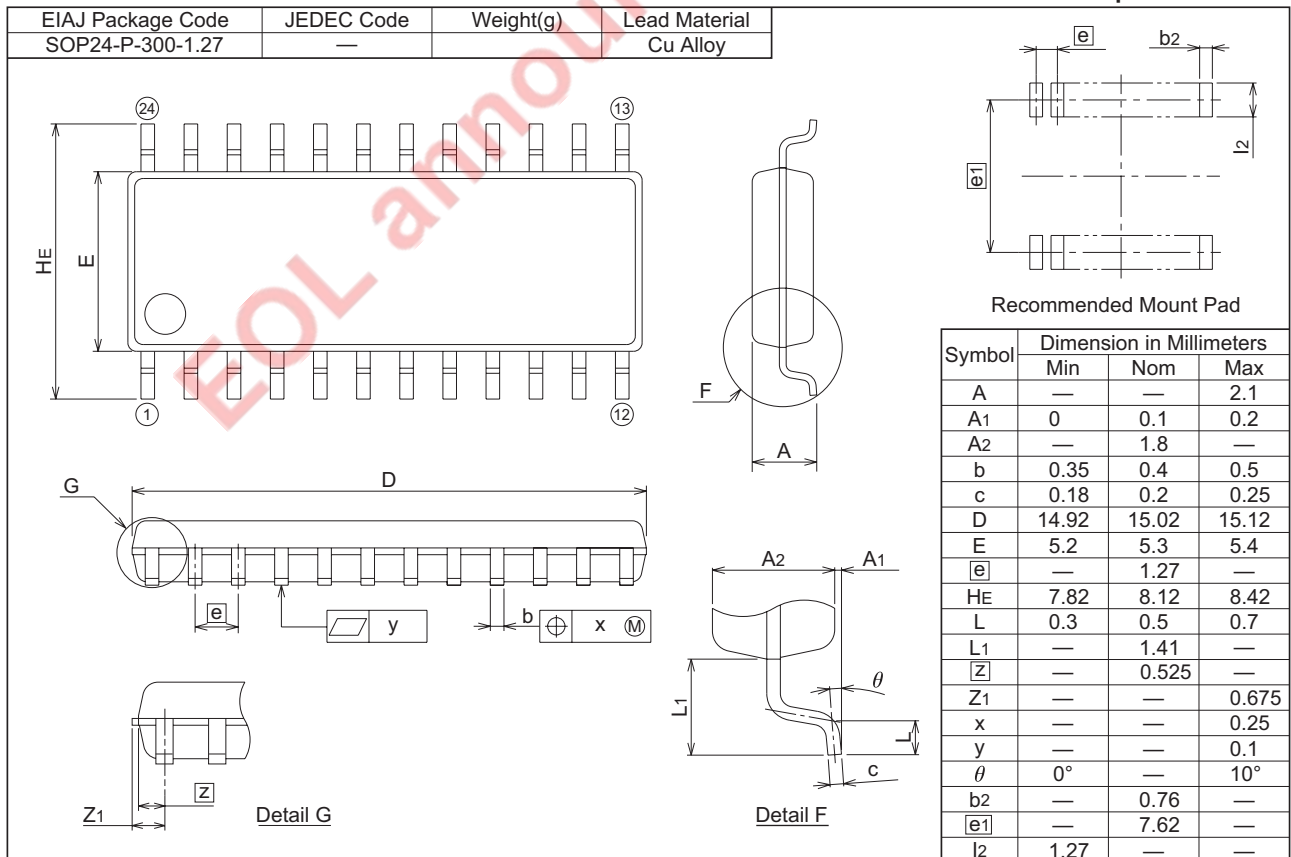


Package Dimensions



24P2N-B

Plastic 24pin 300mil SOP



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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
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Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

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7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2377-3473

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10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

**Renesas Technology Singapore Pte. Ltd.**  
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510