M66310P/FP

16-Bit LED Driver with Shift Register and Latch

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Rev.2.01
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Description

M66310P/FP is a LED array driver having a 16 bit serial-input and parallel output shift-register function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24 mA which is sufficient for cathode common LED drive, capable of flowing 16 bits continuously at the same time.

Parallel output is open drain output.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin layout ensures the realization of an easy printed circuit.

Features

- Cathode common LED drive
- High output current
  all parallel output $I_{OH} = -24$ mA
  simultaneous lighting available
- Low power dissipation: 100 μW/package (max)
  ($V_{CC} = 5$ V, Ta = 25°C, quiescent state)
- High noise margin
  schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output (except serial data output)
- Wide operating temperature range: Ta = –40 to +85°C
- Pin layout facilitates printed circuit wiring. (This layout facilitates cascade connection and LED connection.)

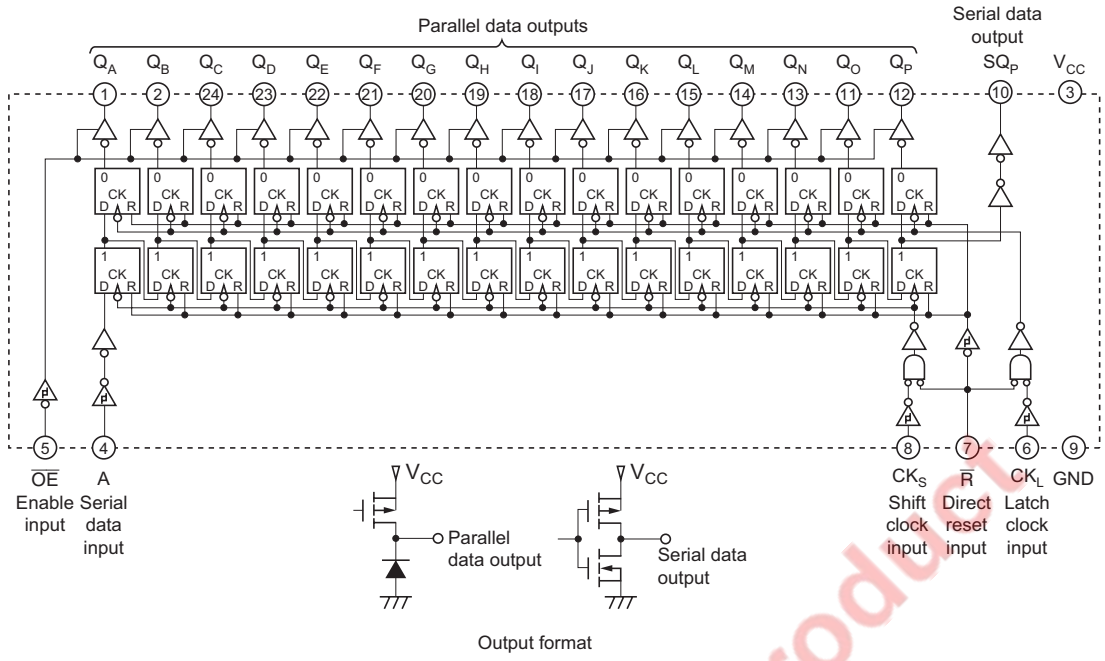
Application

LED array drive of BUTTON TELEPHONE

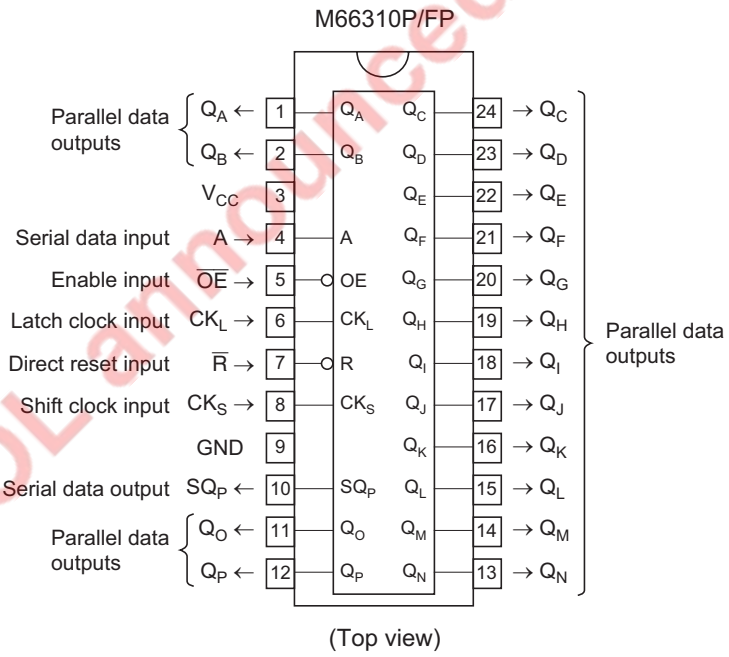
LED array drive of ERASER of a PPC copier

Other various LED modules

Logic Diagram



Pin Arrangement



Outline: PRDP0024AA-A (24P4D)
(24P2N-B)

Functional Description

As M66310P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shift-register consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when “L” changes to “H”.

Serial data input A is the data input of the first-step shift-register and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S. When A is “L”, the signal of “L” shifts.

When the pulse is impressed to CK_L, the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from Q_A to Q_P.

Outputs from Q_A to Q_P are open drain outputs.

To extend the number of bits, use the serial data output SQ_P which shows the output of the shifting register of the 16th bit.

If CK_S and CK_L are connected, the state of the shifting register with one clock delay is outputted to Q_A to Q_P.

When reset input $\overline{R}$ is changed to “L”, Q_A to Q_P and SQ_P are reset. In this case, shifting and latching registers are reset.

If “H” is impressed to output enable input $\overline{OE}$, Q_A to Q_P reaches the high impedance state, but SQ_P does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

Function Table (Note)

Operation Mode		Input					Parallel Data Output																Serial Data Output	Remarks
		$\overline{R}$	CK_S	CK_L	A	$\overline{OE}$	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	Q_I	Q_J	Q_K	Q_L	Q_M	Q_N	Q_O	Q_P	SQ_P	
Reset		L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	–
Shift latch operation	Shift t1	H	↑	X	H	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	Q_P^0	q_O^0	Output lighting "H"
	Latch t2	H	X	↑	X	L	H	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_H^0	q_I^0	q_J^0	q_K^0	q_L^0	q_M^0	q_N^0	q_O^0	q_O^0	
	Shift t1	H	↑	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	Q_I^0	Q_J^0	Q_K^0	Q_L^0	Q_M^0	Q_N^0	Q_O^0	Q_P^0	q_O^0	Output lights-out "L"
	Latch t2	H	X	↑	X	L	Z	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_H^0	q_I^0	q_J^0	q_K^0	q_L^0	q_M^0	q_N^0	q_O^0	q_O^0	
Output disable		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_P	–

Note ↑: Change from low-level to high-level
Q^0: Output state Q before CK_L changed
X: Irrelevant
q^0: Contents of shift register before CK_S changed
q: Contents of shift register
t_1, t_2: t_2 is set after t_1 is set
Z: High impedance

Absolute Maximum Ratings

(Ta = –40 to +85°C, unless otherwise noted)

Item		Symbol	Ratings	Unit	Conditions
Supply voltage		V_{CC}	–0.5 to +7.0	V	
Input voltage		V_I	–0.5 to V_{CC} + 0.5	V	
Output voltage		V_O	–0.5 to V_{CC} + 0.5	V	
Input protection diode current		I_{IK}	–20	mA	V_I < 0 V
			20		V_I > V_{CC}
Output parasitic diode current		I_{OK}	–20	mA	V_O < 0 V
			20		V_O > V_{CC}
Output current per output pin	Q_A to Q_P	I_O	–50	mA	
	SQ_P		±25		
Supply/GND current		I_{CC}	–410, +20	mA	V_{CC}, GND
Power dissipation		Pd	500	mW	(Note)
Storage temperature range		Tstg	–65 to +150	°C	

Note: M66310FP; Ta = –40 to +70°C, Ta = 70 to 85°C are derated at –6 mW/°C.

Recommended Operating Conditions

(Ta = –40 to +85°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_I	0	—	V_{CC}	V
Output voltage	V_O	0	—	V_{CC}	V
Operating temperature range	Topr	–40	—	+85	°C

Electrical Characteristics

(V_{CC} = 4.5 to 5.5 V, unless otherwise noted)

Item	Symbol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = –40 to +85°C				
		Min	Typ	Max	Min	Max			
Positive-going threshold voltage	V_{T+}	0.35×V_{CC}	—	0.7×V_{CC}	0.35×V_{CC}	0.7×V_{CC}	V	V_O = 0.1V, V_{CC}–0.1V $\lvert I_O \rvert$ = 20 µA	
Negative-going threshold voltage	V_{T-}	0.2×V_{CC}	—	0.55×V_{CC}	0.2×V_{CC}	0.55×V_{CC}	V	V_O = 0.1V, V_{CC}–0.1V $\lvert I_O \rvert$ = 20 µA	
High-level output voltage Q_A to Q_P	V_{OH}	V_{CC}–0.1	—	—	V_{CC}–0.1	—	V	V_I = V_{T+}, V_{T-} V_{CC} = 4.5 V	I_{OH} = –20 µA
		3.83	—	—	3.66	—			I_{OH} = –24 mA
		3.50	—	—	3.25	—			I_{OH} = –40 mA (Note)
High-level output voltage SQ_P	V_{OH}	V_{CC}–0.1	—	—	V_{CC}–0.1	—	V	V_I = V_{T+}, V_{T-} V_{CC} = 4.5 V	I_{OH} = –20 µA
		3.83	—	—	3.66	—			I_{OH} = –4 mA
Low-level output voltage SQ_P	V_{OL}	—	—	0.1	—	0.1	V	V_I = V_{T+}, V_{T-} V_{CC} = 4.5 V	I_{OL} = 20 µA
		—	—	0.44	—	0.53			I_{OL} = 4 mA
High-level input current	I_{IH}	—	—	0.5	—	5.0	µA	V_I = V_{CC}, V_{CC} = 5.5 V	
Low-level input current	I_{IL}	—	—	–0.5	—	–5.0	µA	V_I = GND, V_{CC} = 5.5 V	
Maximum output leakage current Q_A to Q_P	I_O	—	—	1.0	—	10.0	µA	V_I = V_{T+}, V_{T-} V_{CC} = 5.5 V	V_O = V_{CC}
		—	—	–1.0	—	–10.0			V_O = GND
Quiescent supply current	I_{CC}	—	—	20.0	—	200.0	µA	V_I = V_{CC}, GND, V_{CC} = 5.5 V	

Note: M66310 is used under the condition of an output current I_{OH} = –40 mA, the number of simultaneous drive outputs are restricted as shown in the Duty Cycle-I_{OH} of Standard characteristics.

Switching Characteristics

(V_{CC} = 5V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = –40 to +85°C			
		Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	5	—	—	4	—	MHz	C_L = 50 pF, R_L = 1 kΩ (Note 2)
Low-level to high-level and high-level to low-level output propagation time (CK_S-SQ_P)	t_{PLH}	—	—	100	—	130	ns	
	t_{PHL}	—	—	100	—	130	ns	
High-level to low-level output propagation time ($\overline{R}$-SQ_P)	t_{PHL}	—	—	100	—	130	ns	
High-level to low-level output propagation time ($\overline{R}$-Q_A to Q_P)	t_{PHZ}	—	—	150	—	200	ns	
Low-level to high-level and high-level to low-level output propagation time (CK_L–Q_A to Q_P)	t_{PZH}	—	—	100	—	130	ns	
	t_{PHZ}	—	—	150	—	200	ns	
Output enable time to low-level and high-level ($\overline{OE}$–Q_A to Q_P)	t_{PZH}	—	—	100	—	130	ns	
	t_{PHZ}	—	—	150	—	200	ns	
Input Capacitance	C_I	—	—	10	—	10	pF	
Output Capacitance	C_O	—	—	15	—	15	pF	$\overline{OE}$ = V_{CC}
Power dissipation Capacitance (Note 1)	C_{PO}	—	11	—	—	—	pF	

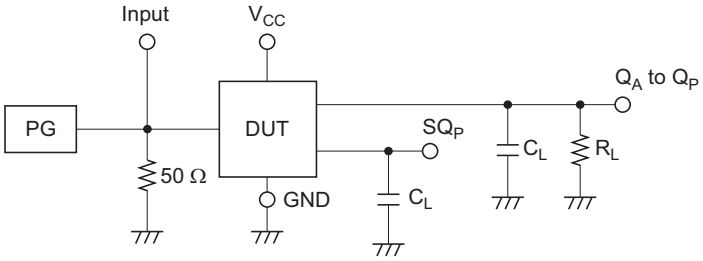
Note: 1. C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no–load conditions is calculated using the following formula:
$P_D = C_{PD} \bullet V_{CC}^2 \bullet f_I + I_{CC} \bullet V_{CC}$

Timing Requirements

(V_{CC} = 5 V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = –40 to +85°C			
		Min	Typ	Max	Min	Max		
CK_S, CK_L, $\overline{R}$ pulse width	t_w	100	—	—	130	—	ns	(Note 2)
A setup time with respect to CK_S	t_{su}	100	—	—	130	—	ns	
CK_S setup time with respect to CK_L	t_{su}	100	—	—	130	—	ns	
A hold time with respect to CK_S	t_h	10	—	—	15	—	ns	
$\overline{R}$, recovery time with respect to CK_S, CK_L	t_{rec}	50	—	—	70	—	ns	

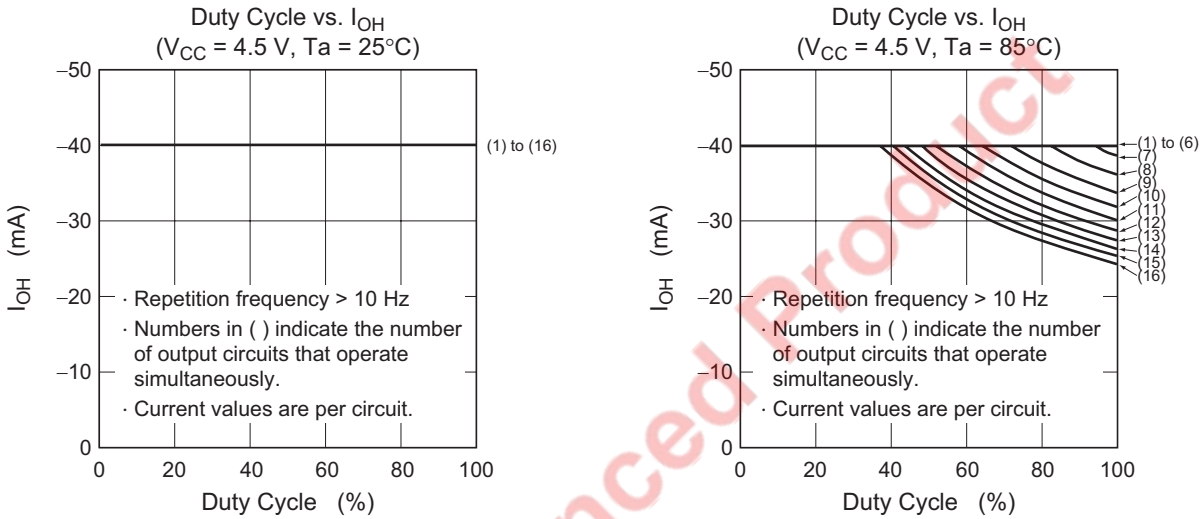
Note: 2. Test Circuit



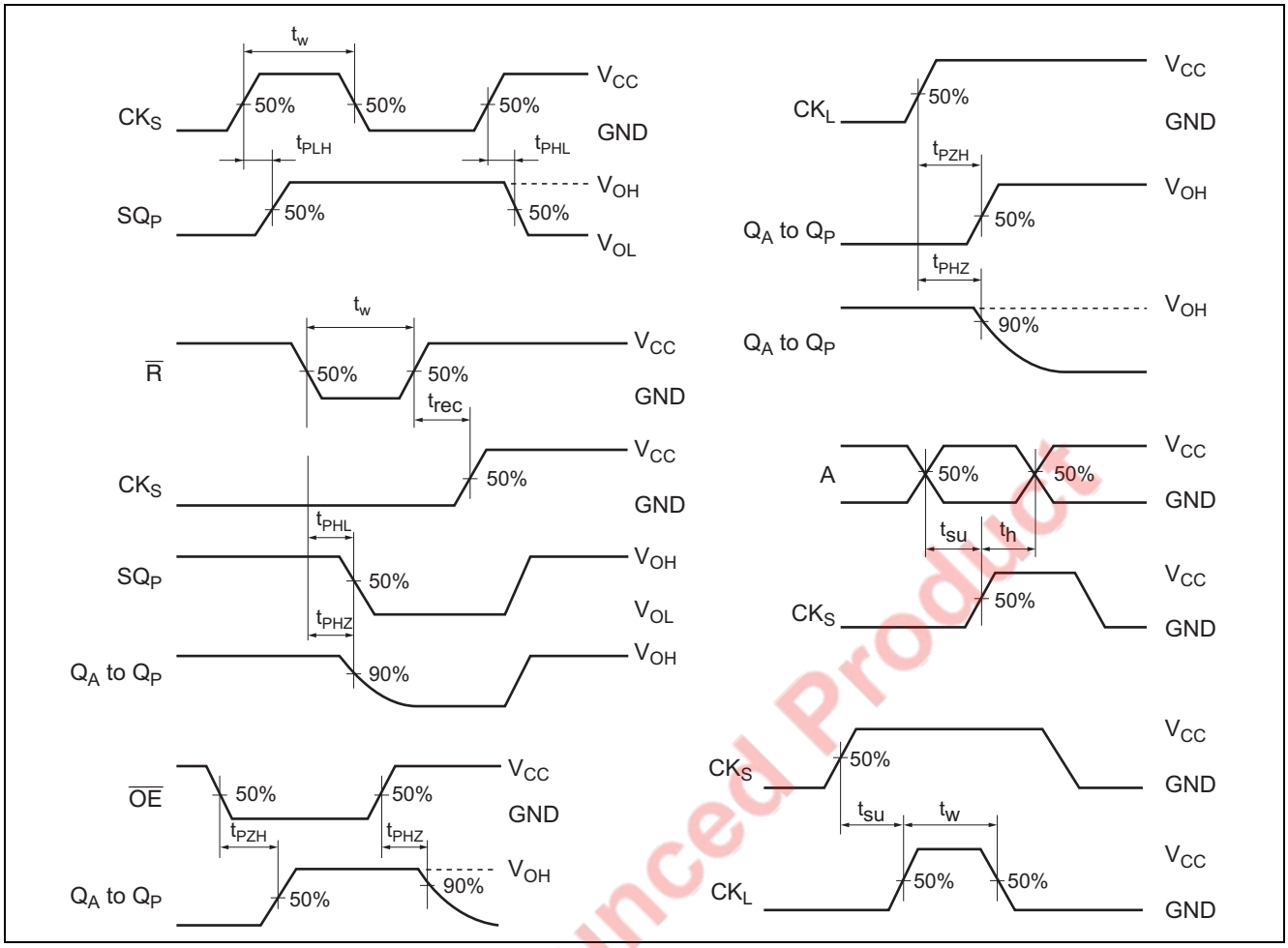
(1) The pulse generator (PG) has the following characteristics (10% to 90%): tr = 6 ns, tf = 6 ns

(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

Typical Characteristics

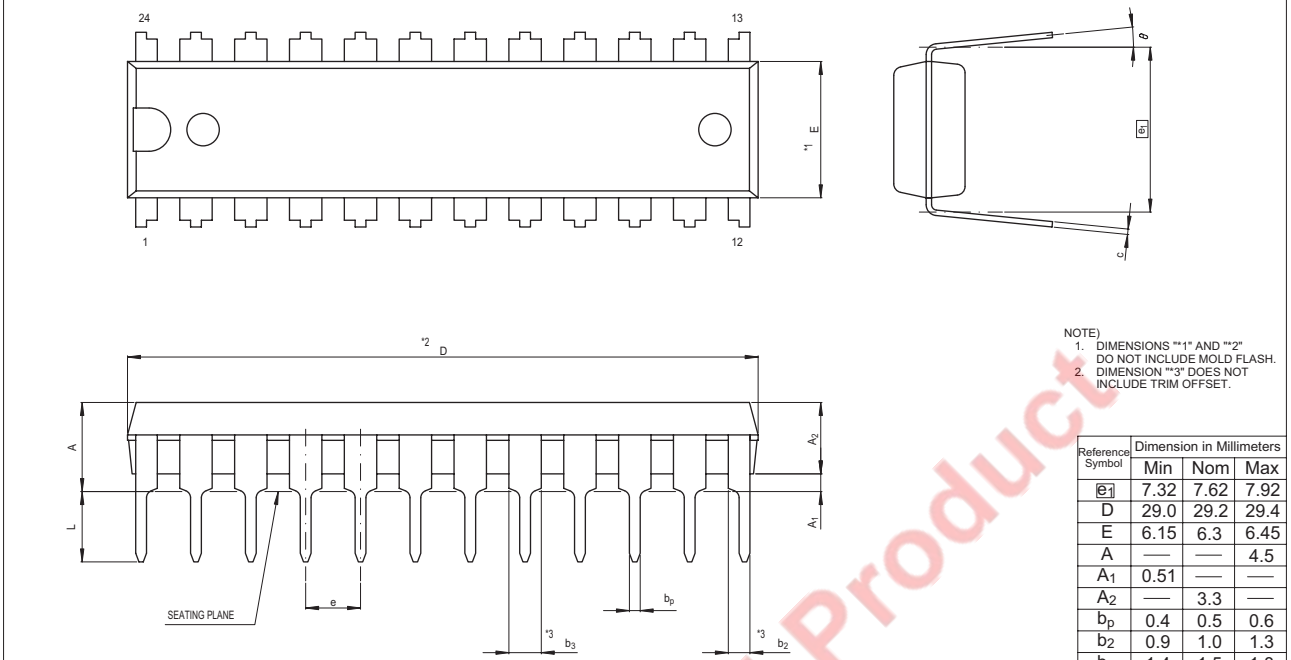


Timing Chart



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP24-6.3x29.2-2.54	PRDP0024AA-A	24P4D	1.6g



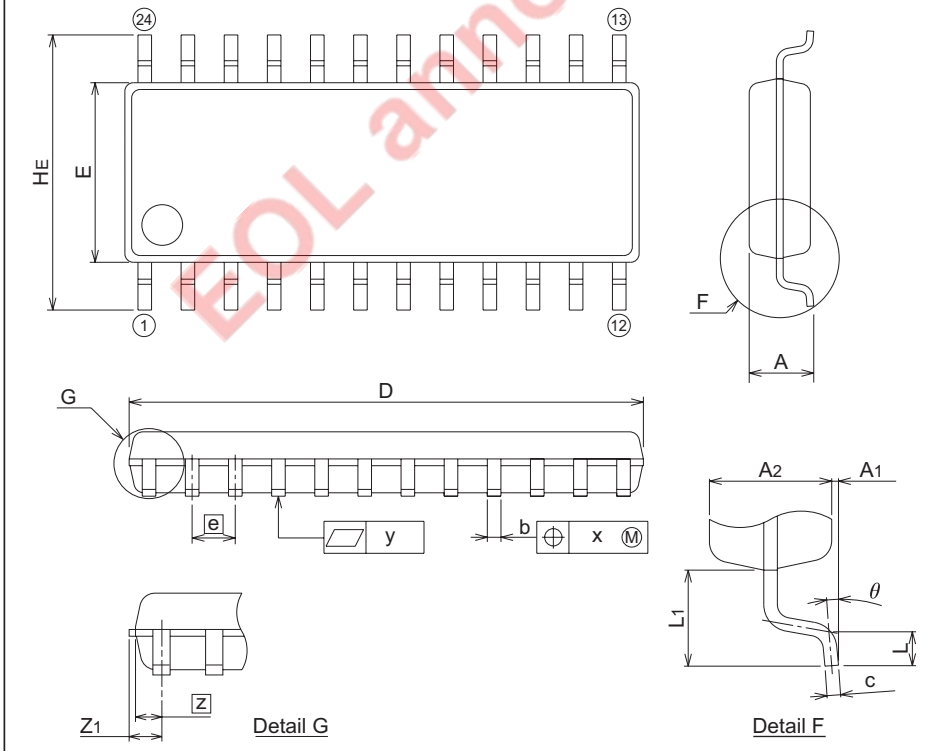
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

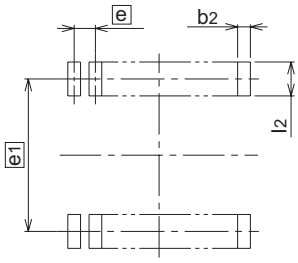
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	7.32	7.62	7.92
D	29.0	29.2	29.4
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

24P2N-B

Plastic 24pin 300mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP24-P-300-1.27	—		Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A_1	0	0.1	0.2
A_2	—	1.8	—
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	14.92	15.02	15.12
E	5.2	5.3	5.4
e	—	1.27	—
HE	7.82	8.12	8.42
L	0.3	0.5	0.7
L_1	—	1.41	—
Z	—	0.525	—
Z_1	—	—	0.675
x	—	—	0.25
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.76	—
e1	—	7.62	—
l_2	1.27	—	—

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