

HAT2173N

Silicon N Channel Power MOS FET Power Switching

REJ03G1684-0100

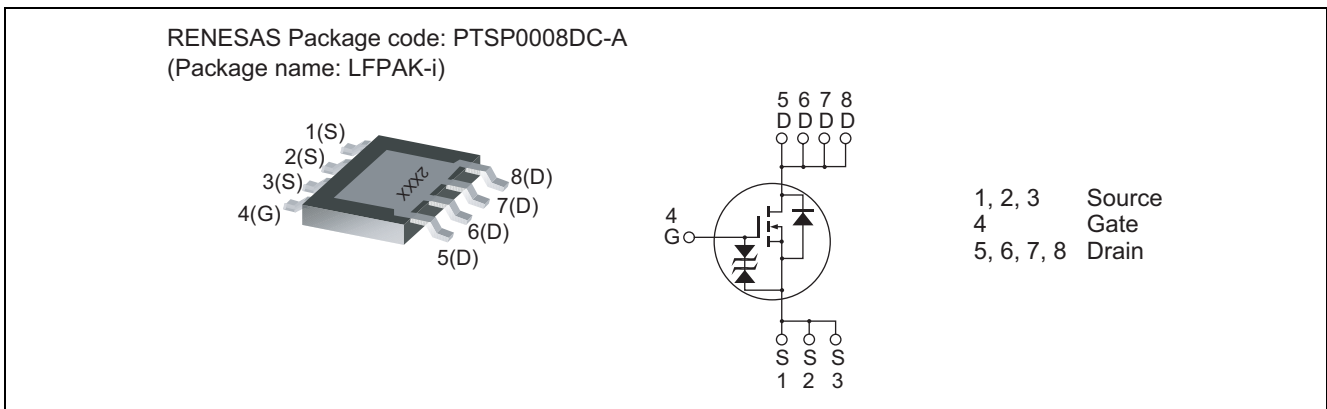
Rev.1.00

May 28, 2008

Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 12.3 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} ^{Note 2}	25	A
Avalanche energy	E_{AR} ^{Note 2}	62.5	mJ
Channel dissipation	P_{ch} ^{Note 3}	30	W
Channel to case thermal resistance	θ_{ch-C}	4.17	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

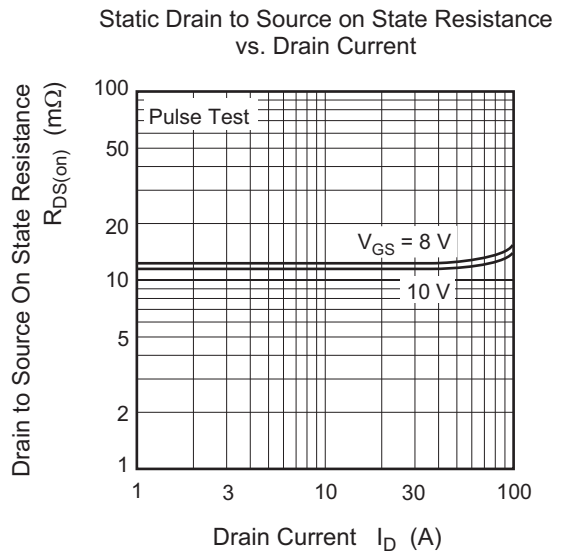
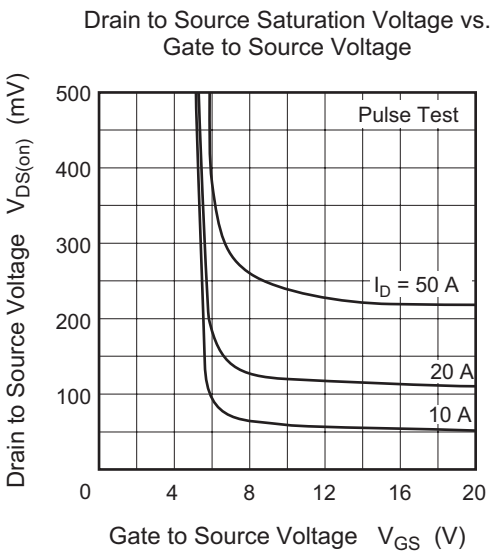
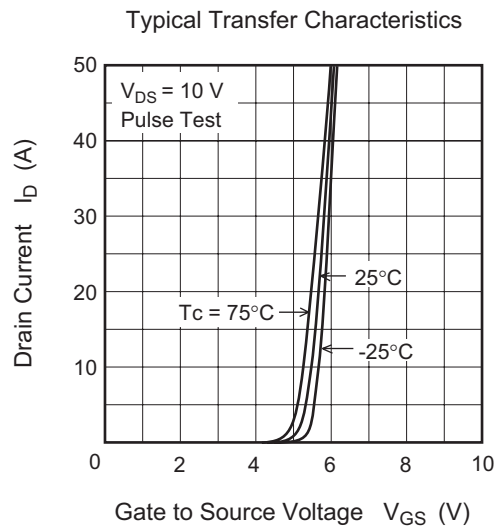
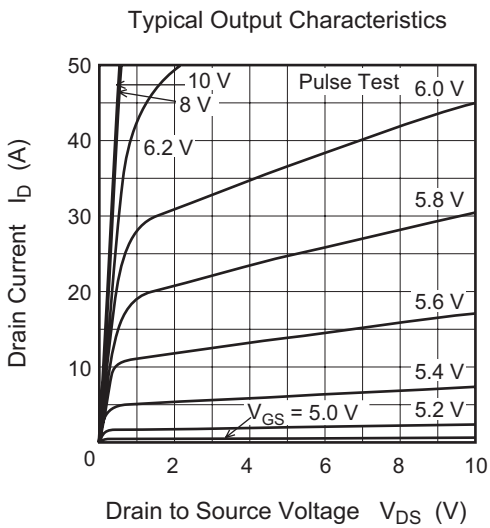
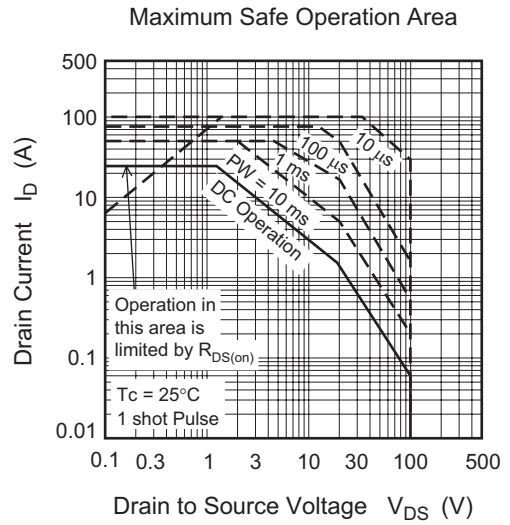
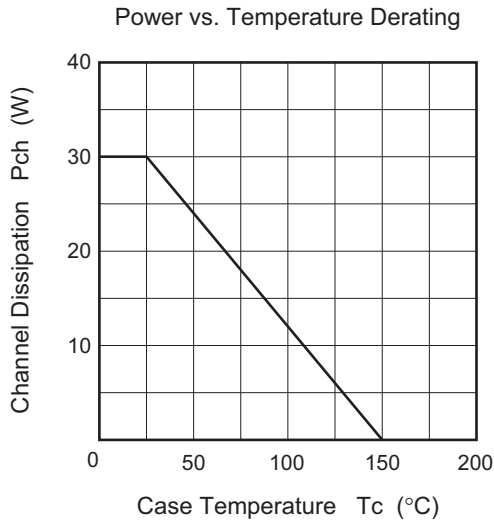
Electrical Characteristics

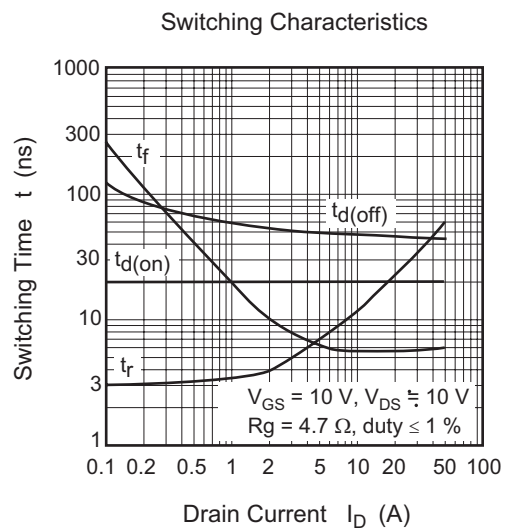
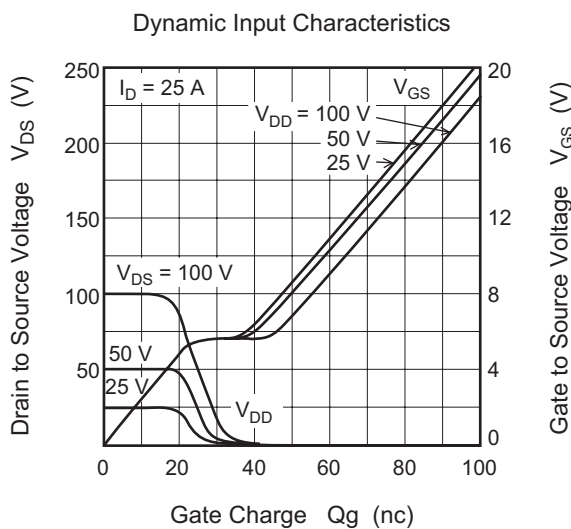
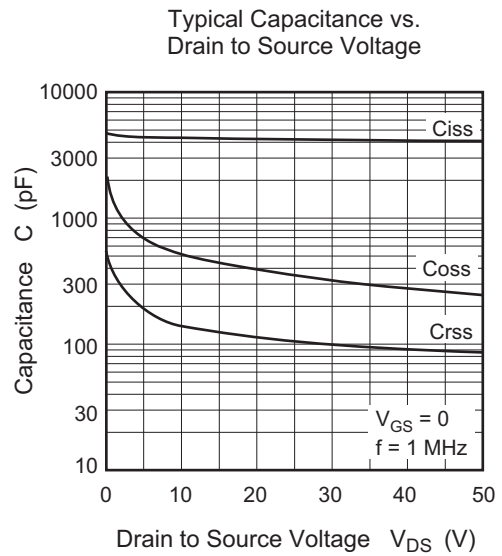
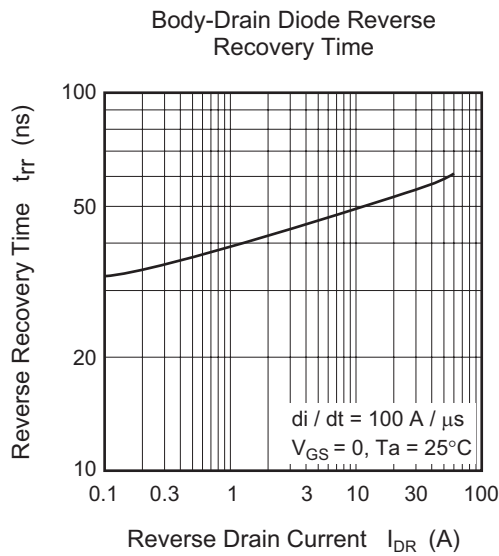
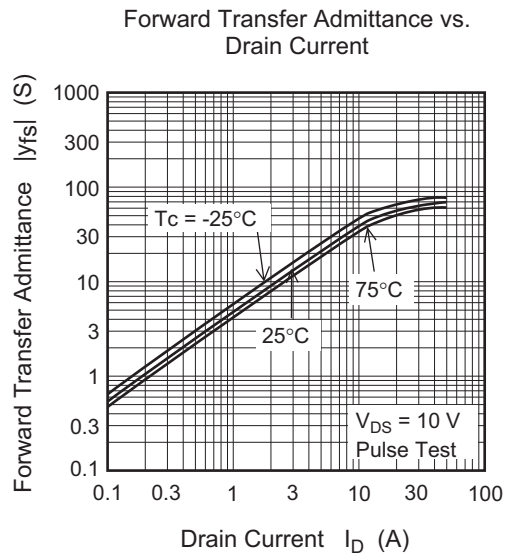
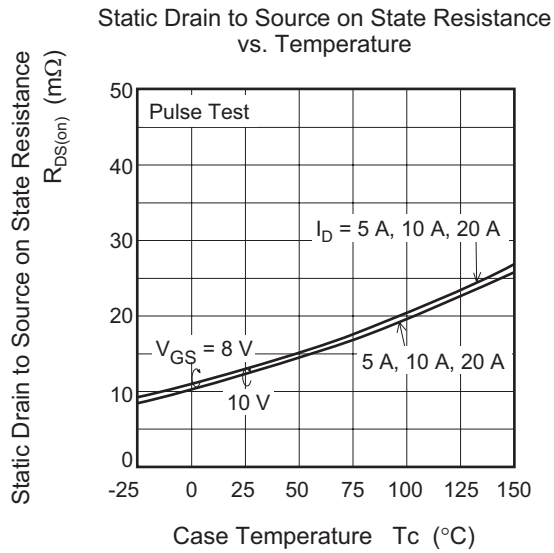
(Ta = 25°C)

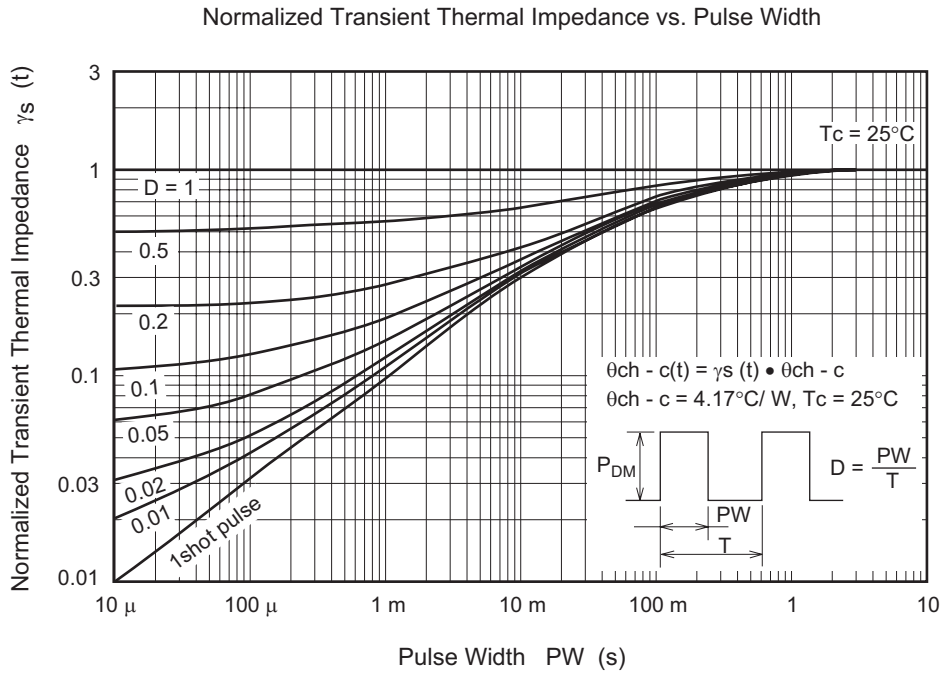
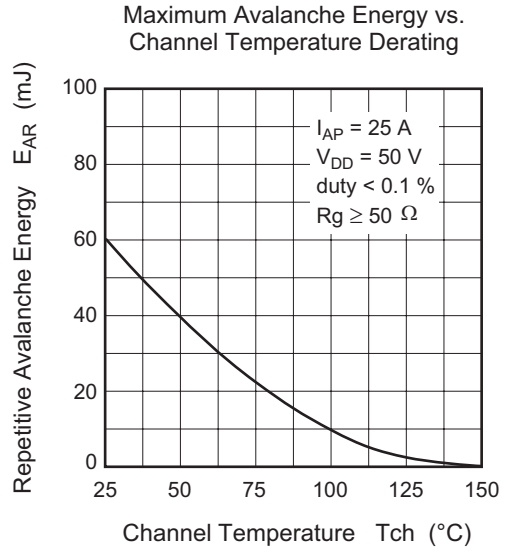
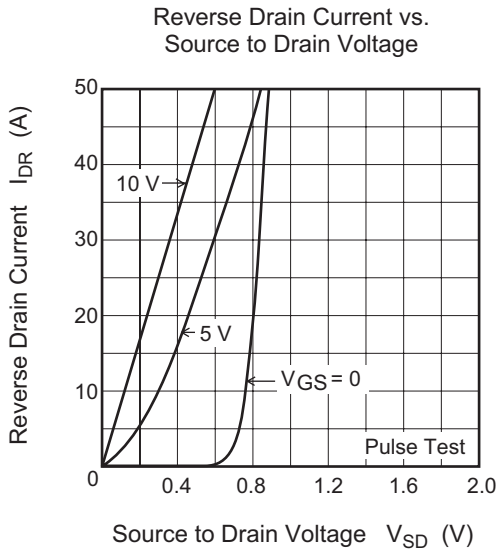
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	4.0	—	6.0	V	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	12.3	15.3	$\text{m}\Omega$	$I_D = 12.5 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	13.3	17.8	$\text{m}\Omega$	$I_D = 12.5 \text{ A}, V_{GS} = 8 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = 12.5 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4350	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	520	—	pF	
Reverse transfer capacitance	C_{rss}	—	150	—	pF	
Gate resistance	R_g	—	0.5	—	Ω	
Total gate charge	Q_g	—	61	—	nC	$V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 25 \text{ A}$
Gate to source charge	Q_{gs}	—	23	—	nC	
Gate to drain charge	Q_{gd}	—	14.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}, I_D = 12.5 \text{ A},$ $V_{DD} \cong 30 \text{ V}, R_L = 2.4 \text{ }\Omega,$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	15	—	ns	
Turn-off delay time	$t_{d(off)}$	—	37	—	ns	
Fall time	t_f	—	5.7	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.82	1.07	V	$I_F = 25 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	55	—	ns	$I_F = 25 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

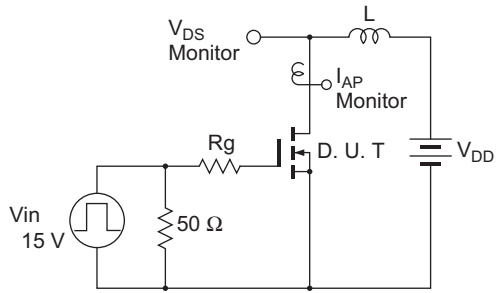
Main Characteristics





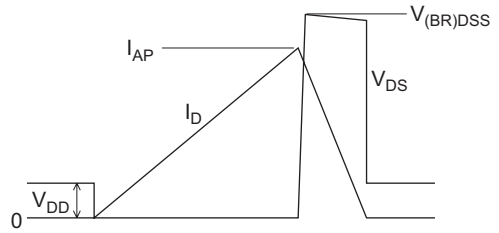


Avalanche Test Circuit

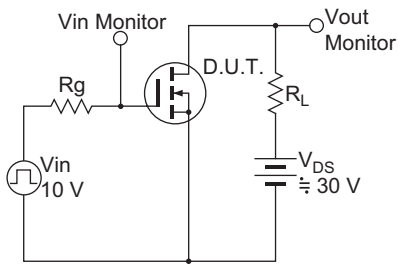


Avalanche Waveform

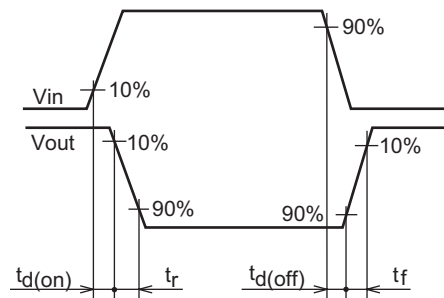
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

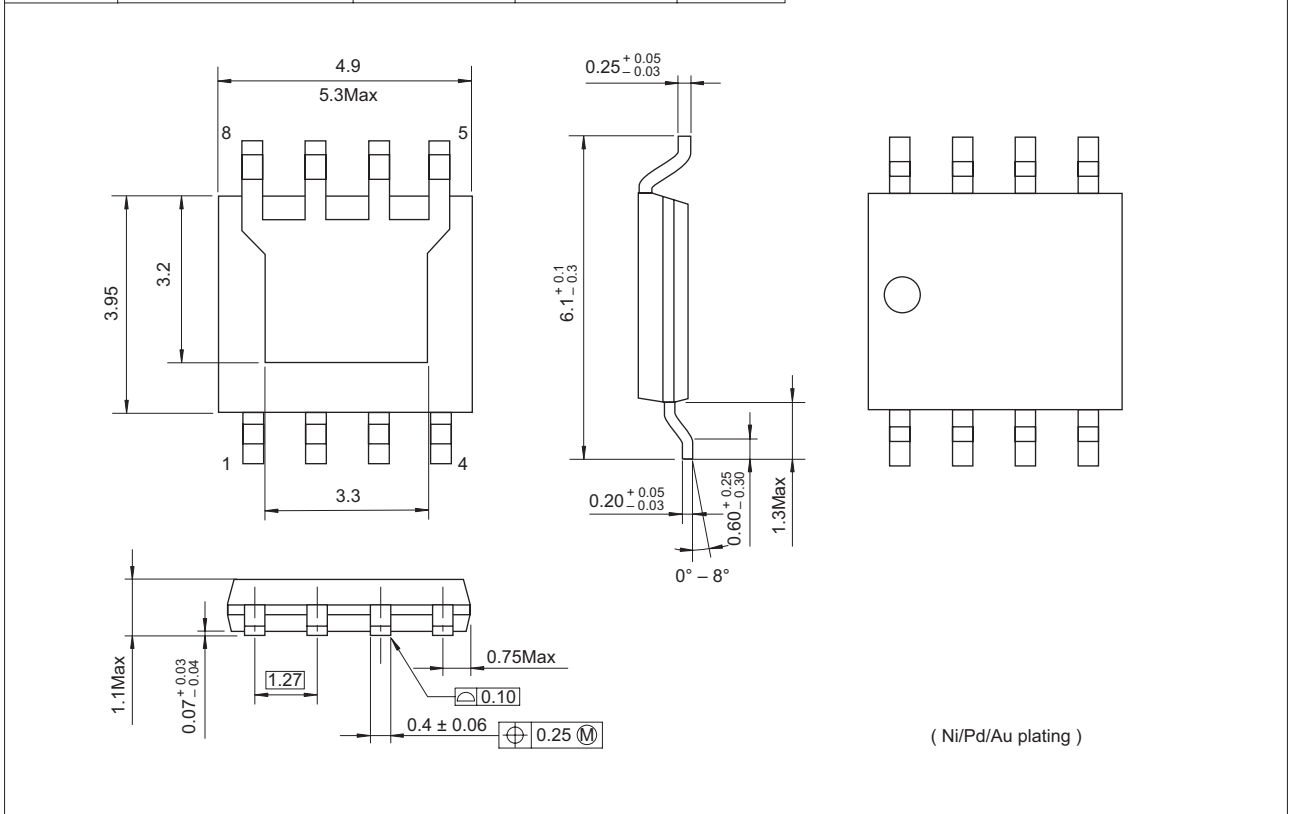


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LFPAK-I	—	PTSP0008DC-A	LFPAK-IV	0.080g



Ordering Information

Part No.	Quantity	Shipping Container
HAT2173N-EL-E	2500 pcs	Taping

Notes:

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