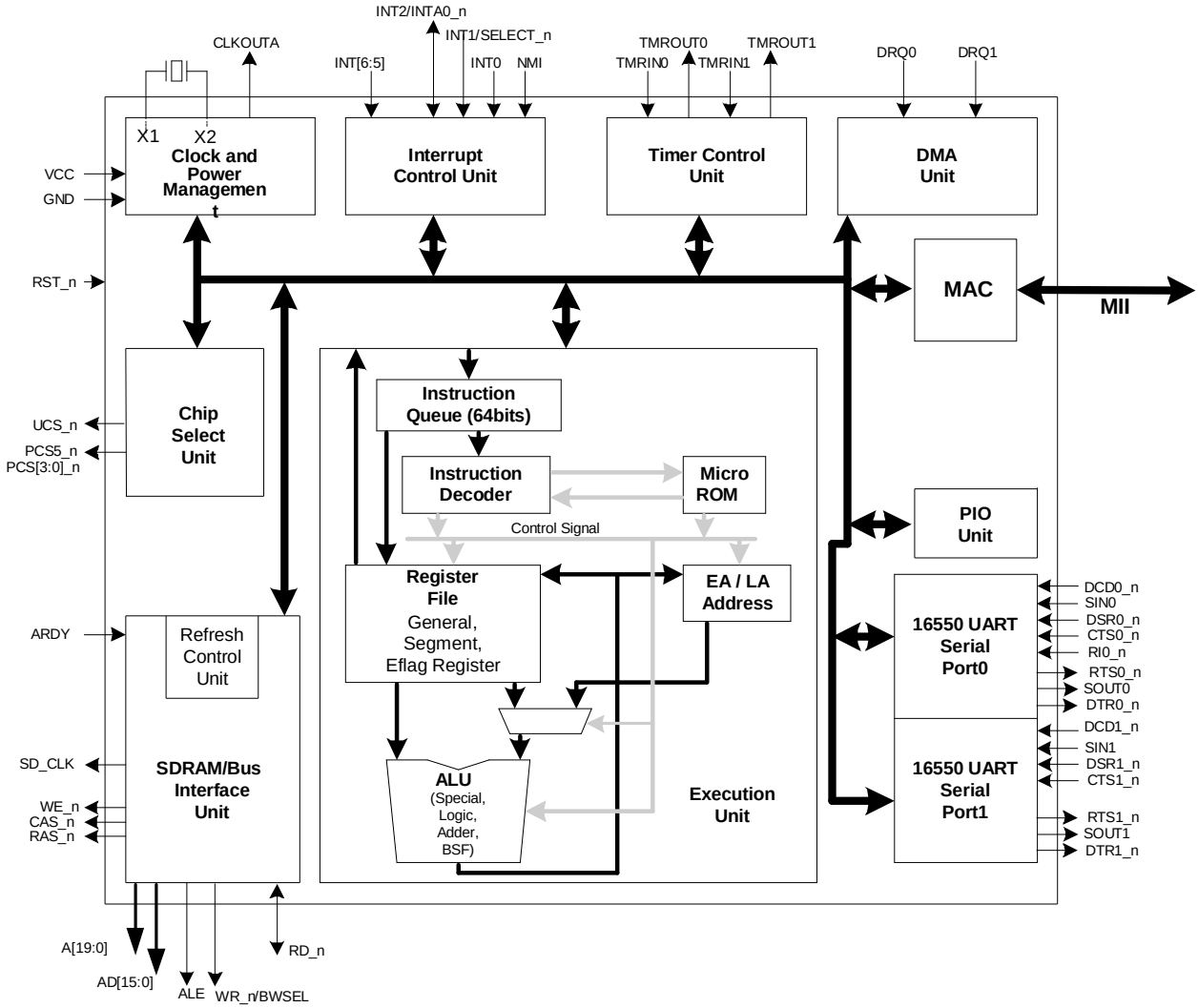
R1610
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

- Five-stage pipeline
- RISC architecture
- Bus interface
  - Multiplexed address and data bus
  - Supports non-multiplexed address bus A[19:0]
  - 8-bit or 16-bit external bus dynamic access
  - 1M-byte memory address space
  - 64K-byte I/O space
  - Supports an independent bus for the slower I/O device
- Software is compatible with the 80C186 microprocessor
- Supports two 16550 UART serial channels with 16-byte FIFO
- Supports CPU ID
- Supports 18 PIO pins
- SDRAM control Interface
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with five maskable external interrupts and one non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for memory or I/O bus cycle decoder
- Programmable wait-state generators
- With 8-bit or 16-bit boot ROM bus size
- 1-port Fast Ethernet MAC with MII interface
- With 25MHz input frequency and up to 4x25MHz maximum internal frequency
- Compatible with 3.3V I/O
- With 128-pin PQFP package type

2. Block Diagram



3. Package Information

PQFP 128 pins