

Silicon PNP Power Transistors

2SB1145

DESCRIPTION

- With TO-220F package
- High DC current gain.
- DARLINGTON
- Low collector saturation voltage

APPLICATIONS

- For high current driver and power driver applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

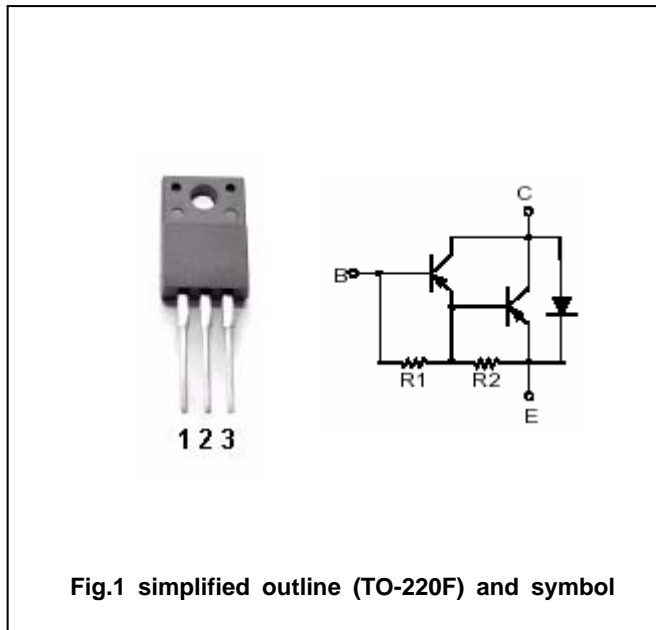


Fig.1 simplified outline (TO-220F) and symbol

Absolute maximum ratings (Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-120	V
V _{CEO}	Collector-emitter voltage	Open base	-120	V
V _{EBO}	Emitter-base voltage	Open collector	-6	V
I _C	Collector current		-3	A
I _{CM}	Collector current-peak		-5	A
P _C	Collector dissipation	T _C =25	20	W
		T _a =25	2	
T _j	Junction temperature		150	
T _{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

 $T_j=25$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	$I_C=-100\ \mu A; I_E=0$	-120			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	$I_C=-5mA; I_B=0$	-120			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=-1.5A; I_B=-3mA$			-1.5	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=-1.5A; I_B=-3mA$			-2.0	V
I_{CBO}	Collector cut-off current	$V_{CB}=-120V; I_E=0$			-50	μA
I_{EBO}	Emitter cut-off current	$V_{EB}=-5V; I_C=0$			-3.0	mA
h_{FE}	DC current gain	$I_C=-1.5A; V_{CE}=-3V$	2000			

固电半导体

INCHANGE SEMICONDUCTOR

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PACKAGE OUTLINE

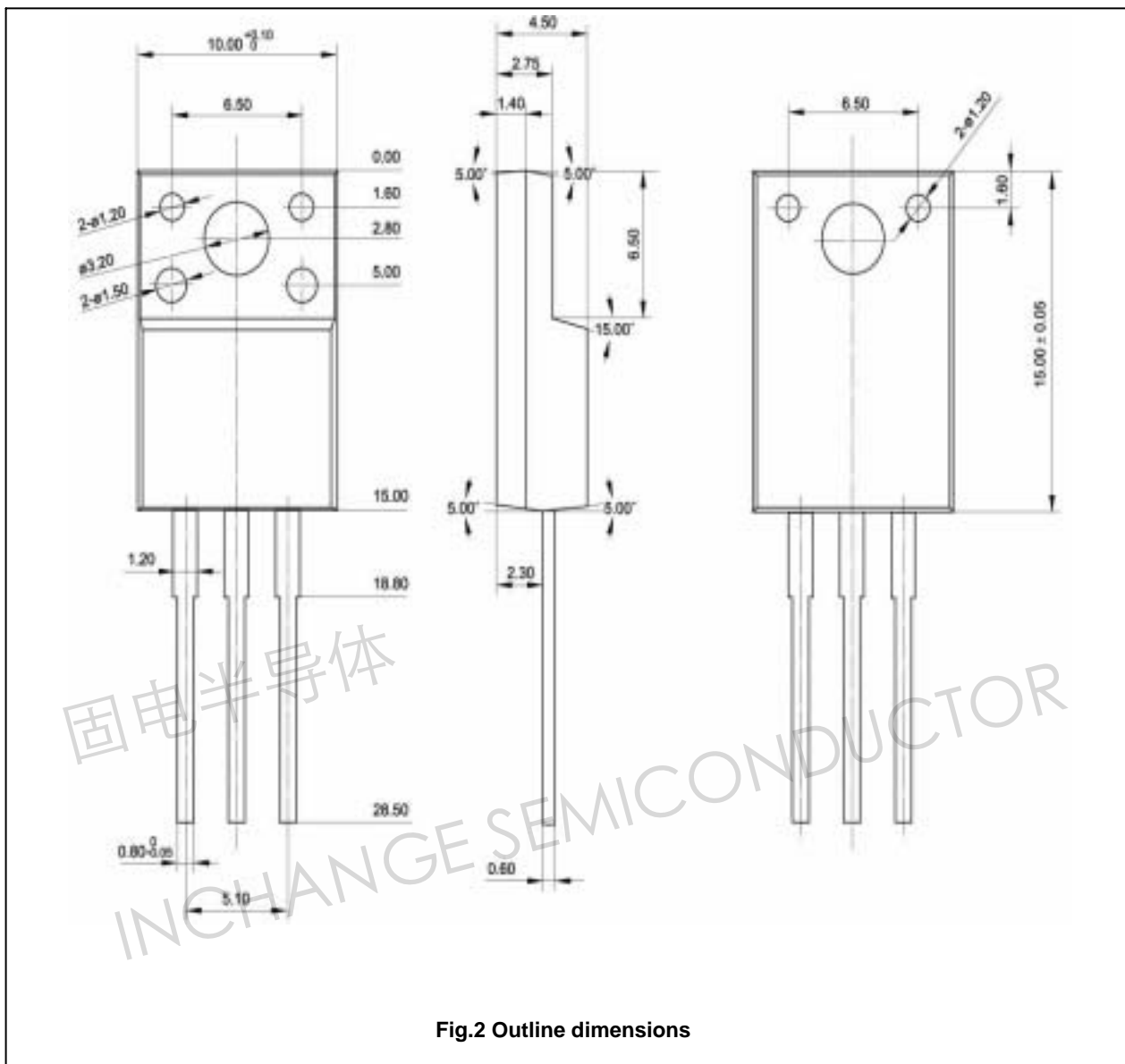


Fig.2 Outline dimensions