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128MB DDR SDRAM S.O. DIMM

EBD13UB6ALS (16M words × 64 bits, 2 Banks)

Description

The EBD13UB6ALS is 16M words × 64 bits, 2 banks Double Data Rate (DDR) SDRAM module, mounted 8 pieces of 128M bits DDR SDRAM (EDD1216ALTA) sealed in TSOP package. Read and write operations are performed at the cross points of the CLK and the /CLK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 200-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 200-pin socket type package (dual lead out)
— Outline: 67.6mm (Length) × 31.75mm (Height) × 3.80mm (Thickness)
— Lead pitch: 0.6mm
- 2.5V power supply
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 133MHz/100MHz (max.)
- Data inputs and outputs are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2, 4, 8
— Burst read stop capability
- Programmable burst sequence
— Sequential
— Interleave
- Start addressing capability
— Even and Odd
- Programmable /CAS latency (CL): 2, 2.5
- 4096 refresh cycles: 15.6μs (4096/64ms)
- 2 variations of refresh
— Auto refresh
— Self refresh

Ordering Information

Part number	Clock frequency MHz (max.)	/CAS latency	Package	Contact pad	Mounted devices
EBD13UB6ALS-7A	133	2.0	200-pin S.O. DIMM	Gold	EDD1216ALTA
EBD13UB6ALS-75	133	2.5			
EBD13UB6ALS-1A	100	2.0			

Pin Configurations
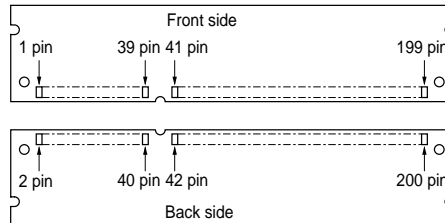
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	51	VSS	2	VREF	52	VSS
3	VSS	53	DQ19	4	VSS	54	DQ23
5	DQ0	55	DQ24	6	DQ4	56	DQ28
7	DQ1	57	VDD	8	DQ5	58	VDD
9	VDD	59	DQ25	10	VDD	60	DQ29
11	DQS0	61	DQS3	12	DM0	62	DM3
13	DQ2	63	VSS	14	DQ6	64	VSS
15	VSS	65	DQ26	16	VSS	66	DQ30
17	DQ3	67	DQ27	18	DQ7	68	DQ31
19	DQ8	69	VDD	20	DQ12	70	VDD
21	VDD	71	NC	22	VDD	72	NC
23	DQ9	73	NC	24	DQ13	74	NC
25	DQS1	75	VSS	26	DM1	76	VSS
27	VSS	77	NC	28	VSS	78	NC
29	DQ10	79	NC	30	DQ14	80	NC
31	DQ11	81	VDD	32	DQ15	82	VDD
33	VDD	83	NC	34	VDD	84	NC
35	CLK0	85	NC	36	VDD	86	NC
37	/CLK0	87	VSS	38	VSS	88	VSS
39	VSS	89	CLK2	40	VSS	90	VSS
41	DQ16	91	/CLK2	42	DQ20	92	VDD
43	DQ17	93	VDD	44	DQ21	94	VDD
45	VDD	95	NC	46	VDD	96	CKE0
47	DQS2	97	NC	48	DM2	98	NC
49	DQ18	99	NC	50	DQ22	100	A11

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	A9	151	DQ42	102	A8	152	DQ46
103	VSS	153	DQ43	104	VSS	154	DQ47
105	A7	155	VDD	106	A6	156	VDD
107	A5	157	VDD	108	A4	158	/CLK1
109	A3	159	VSS	110	A2	160	CLK1
111	A1	161	VSS	112	A0	162	VSS
113	VDD	163	DQ48	114	VDD	164	DQ52
115	A10/AP	165	DQ49	116	BA1	166	DQ53
117	BA0	167	VDD	118	/RAS	168	VDD
119	/WE	169	DQS6	120	/CAS	170	DM6
121	/CS0	171	DQ50	122	/CS1	172	DQ54
123	NC	173	VSS	124	NC	174	VSS
125	VSS	175	DQ51	126	VSS	176	DQ55
127	DQ32	177	DQ56	128	DQ36	178	DQ60
129	DQ33	179	VDD	130	DQ37	180	VDD
131	VDD	181	DQ57	132	VDD	182	DQ61
133	DQS4	183	DQS7	134	DM4	184	DM7
135	DQ34	185	VSS	136	DQ38	186	VSS
137	VSS	187	DQ58	138	VSS	188	DQ62
139	DQ35	189	DQ59	140	DQ39	190	DQ63
141	DQ40	191	VDD	142	DQ44	192	VDD
143	VDD	193	SDA	144	VDD	194	SA0
145	DQ41	195	SCL	146	DQ45	196	SA1
147	DQS5	197	VDDSPD	148	DM5	198	SA2
149	VSS	199	VDDID	150	VSS	200	NC

Pin Description

Pin name	Function
A0 to A11	Address input Row address A0 to A11 Column address A0 to A8
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0, /CS1	Chip select
CKE0, CKE1	Clock enable
CLK0 to CLK2	Clock input
/CLK0 to /CLK2	Differential clock input
DQS0 to DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0 to SA2	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
VDDID	VDD indentication flag
NC	No connection

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Serial PD Matrix

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	0	1	1	1	07H	DDR SDRAM
3	Number of row address	0	0	0	0	1	1	0	0	0CH	12
4	Number of column address	0	0	0	0	1	0	0	1	09H	9
5	Number of DIMM banks	0	0	0	0	0	0	1	0	02H	2
6	Module data width	0	1	0	0	0	0	0	0	40H	64
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04H	SSTL2
9	DDR SDRAM cycle time, CL = 2.5 -7A	0	1	1	1	0	1	0	1	75H	7.5ns
	-75	0	1	1	1	0	1	0	1	75H	7.5ns
	-1A	1	0	1	0	0	0	0	0	A0H	10ns
10	SDRAM access from clock (tAC) -7A	0	1	1	1	0	1	0	1	75H	0.75ns
	-75	0	1	1	1	0	1	0	1	75H	0.75ns
	-1A	1	0	0	0	0	0	0	0	80H	0.8ns
11	DIMM configuration type	0	0	0	0	0	0	0	0	00H	None.
12	Refresh rate/type	1	0	0	0	0	0	0	0	80H	Norm
13	Primary SDRAM width	0	0	0	1	0	0	0	0	10H	× 16
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00H	None.
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0EH	2,4,8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	1	1	0	0	0CH	2, 2.5
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	1	0	02H	1
21	SDRAM module attributes	0	0	1	0	0	0	0	0	20H	Differential Clock
22	SDRAM device attributes: General	0	0	0	0	0	0	0	0	00H	VDD ± 0.2V
23	Minimum clock cycle time at CL = 2 -7A	0	1	1	1	0	1	0	1	75H	7.5ns
	-75	1	0	1	0	0	0	0	0	A0H	10ns
	-1A	1	0	1	0	0	0	0	0	A0H	10ns
24	Maximum data access time (tAC) from clock at CL = 2 -7A	1	0	0	0	0	0	0	0	80H	0.80ns
	-75	0	1	1	1	0	1	0	1	75H	0.75ns
	-1A	1	0	0	0	0	0	0	0	80H	0.8ns
25 to 26		0	0	0	0	0	0	0	0	00H	

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Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
27	Minimum row precharge time (tRP) -7A	0	1	0	1	0	0	0	0	50H	20ns
	-75	0	1	0	1	0	0	0	0	50H	20ns
	-1A	0	1	0	1	0	0	0	0	50H	20ns
28	Minimum row active to row active delay (tRRD) -7A	0	0	1	1	1	1	0	0	3CH	15ns
	-75	0	0	1	1	1	1	0	0	3CH	15ns
	-1A	0	0	1	1	1	1	0	0	3CH	15ns
29	Minimum /RAS to /CAS delay (tRCD) -7A	0	1	0	1	0	0	0	0	50H	20ns
	-75	0	1	0	1	0	0	0	0	50H	20ns
	-1A	0	1	0	1	0	0	0	0	50H	20ns
30	Minimum active to precharge time (tRAS) -7A	0	0	1	0	1	1	0	1	2DH	45ns
	-75	0	0	1	0	1	1	0	1	2DH	45ns
	-1A	0	0	1	1	0	0	1	0	32H	50ns
31	Module bank density	0	0	0	1	0	0	0	0	10H	64M bytes
32	Address and command setup time before clock (tIS) -7A	1	0	0	1	0	0	0	0	90H	0.9ns
	-75	1	0	0	1	0	0	0	0	90H	0.9ns
	-1A	1	0	1	1	0	0	0	0	B0H	1.1ns
33	Address and command hold time after clock (tIH) -7A	1	0	0	1	0	0	0	0	90H	0.9ns
	-75	1	0	0	1	0	0	0	0	90H	0.9ns
	-1A	1	0	1	1	0	0	0	0	B0H	1.1ns
34	Data input setup time before clock (tDS) -7A	0	1	0	1	0	0	0	0	50H	0.5ns
	-75	0	1	0	1	0	0	0	0	50H	0.5ns
	-1A	0	1	1	0	0	0	0	0	60H	0.6ns
35	Data input hold time after clock (tDH) -7A	0	1	0	1	0	0	0	0	50H	0.5ns
	-75	0	1	0	1	0	0	0	0	50H	0.5ns
	-1A	0	1	1	0	0	0	0	0	60H	0.6ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00H	
62	SPD Revision	0	0	0	0	0	0	0	0	00H	
63	Checksum for bytes 0 to 62 -7A	0	1	1	1	0	1	0	0	74H	
	-75	1	0	0	1	0	1	0	0	94H	
	-1A	0	0	1	1	1	0	1	0	3AH	
64	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location										
73 to 90	Manufacturer's part number										
91 to 92	Revision code										
93 to 94	Manufacturing date										

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| Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
95 to 98	Module serial number										
99 to 127	Manufacture specific data										

Block Diagram
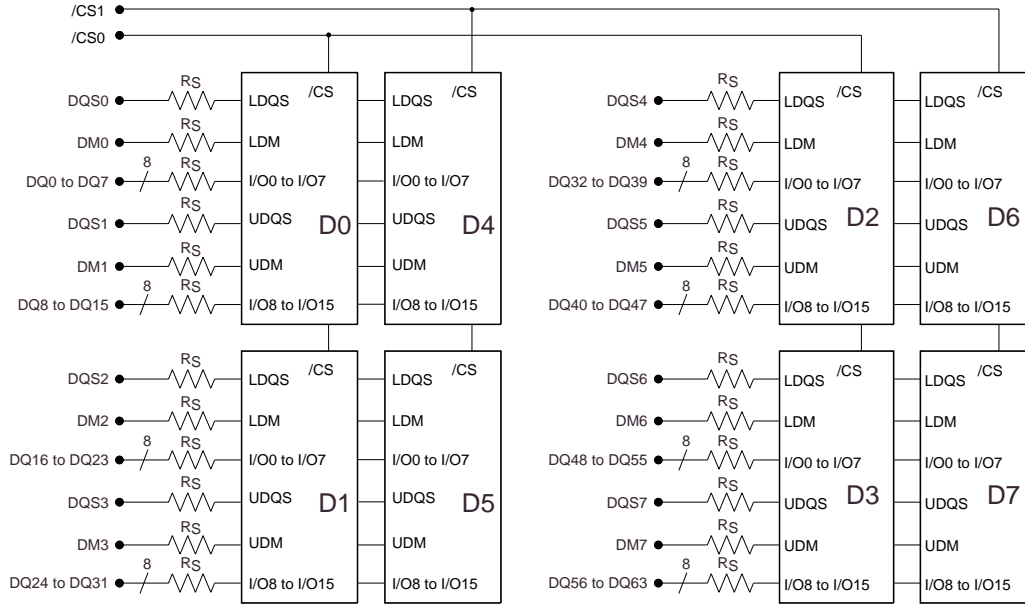
* D0 to D7 : EDD1216ALTA
U0 : 2k bits EEPROM
Rs : 22Ω
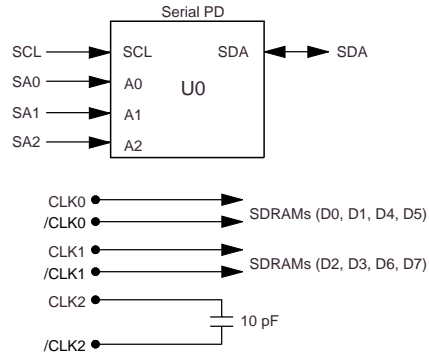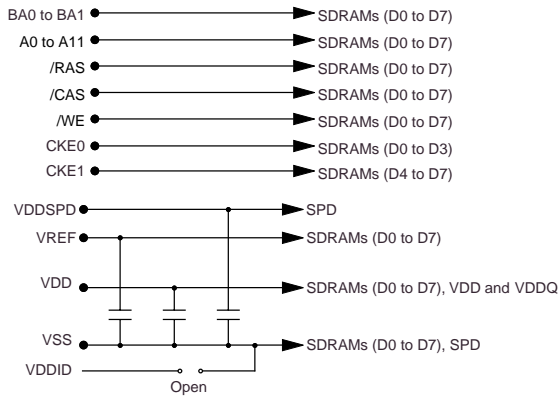
Notes :
1. DQ wiring may differ from that described
   in this drawing; however DQ/DM/DQS
   relationships are maintained as shown.
   VDDID strap connections:
   (for memory device VDD, VDDQ)
      Strap out (open): VDD = VDDQ
      Strap in (closed): VDD ≠ VDDQ
2. The SDA pull-up registor is required due to
   the open-drain/open-collector output.
3. The SCL pull-up registor is recommended,
   because of the normal SCL lime inactive
   "high" state.

Logical Clock Net Structure
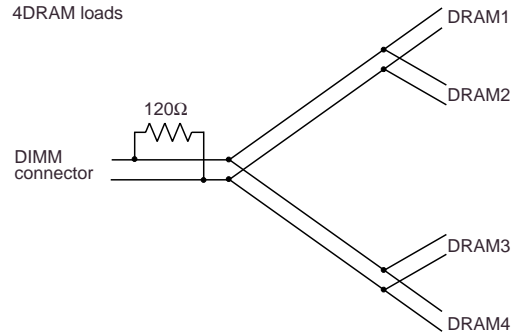
Pin Functions (1)

CLK, /CLK (input pin): The CLK and the /CLK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CLK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CLK and the /CLK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CLK and the /CLK.

/CS (input pin): When /CS is Low, commands and data can be input. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A11 (input pins): Row address (AX0 to AX11) is determined by the A0 to the A11 level at the cross point of the CLK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY8) is loaded via the A0 to the A8 at the cross point of the CLK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin): A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0, BA1 (input pin): BA0/BA1 are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 = Low and BA0 = Low, bank 0 is selected. If BA1 = High and BA0 = Low, bank 1 is selected. If BA1 = Low and BA0 = High, bank 2 is selected. If BA1 = High and BA0 = High, bank 3 is selected.

CKE (input pin): CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CLK cycle (= LCKEPW) at least, that is, if CKE changes at the cross point of the CLK rising edge and the VREF level with proper setup time tIS, at the next CLK rising edge CKE level must be kept with proper hold time tIH.

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Pin Functions (2)

DQ (input and output pins): Data are input to and output from these pins.

DQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input).

DM (input pins): DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and VREF

VDD (power supply pins): 2.5V is applied.

VDDSPD (power supply pin): 2.5V is applied (For serial EEPROM).

VSS (power supply pin): Ground is connected.

Detailed Operation Part, AC Characteristics and Timing Waveforms

Refer to the EDD1204ALTA, EDD1208ALTA, EDD1216ALTA Series datasheet (E0136E).

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Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 1ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +3.6	V	
Supply voltage relative to VSS	VDD	–0.5 to +3.6	V	
Short circuit output current	IO	50	mA	
Power dissipation	PD	8	W	
Operating temperature	TA	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution   **Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

DC Operating Conditions (TA = 0 to +70°C)

Parameter	Symbol	min.	Typ	max.	Unit	Notes
Supply voltage	VDD	2.3	2.5	2.7	V	1
	VSS	0	0	0	V	
Input reference voltage	VREF	$0.49 \times$ VDD	—	$0.51 \times$ VDD	V	1
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	1
DC Input high voltage	VIH	VREF + 0.18	—	VDD + 0.3	V	1, 2
DC Input low voltage	VIL	–0.3	—	VREF – 0.18	V	1, 3
DC Input signal voltage	VIN (dc)	–0.3	—	VDD+ 0.3	V	4
DC differential input voltage	VSWING (dc)	0.36	—	VDD + 0.6	V	5

Notes: 1. All parameters are referred to VSS, when measured.
2. VIH is allowed to exceed VDD up to 4.6V for the period shorter than or equal to 5ns.
3. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.
4. VIN (dc) specifies the allowable dc execution of each differential input.
5. VSWING (dc) specifies the input differential voltage required for switching.

DC Characteristics 1 (TA = 0 to +70°C, VDD = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (ACTV-PRE)	ICC0	-7A -75 -1A	TBD	mA	CKE ≥ VIH, tRC = tRC (min.)	1, 2, 5
Operating current (ACTV-READ-PRE)	ICC1	-7A -75 -1A	TBD	mA	CKE ≥ VIH, BL = 2, CL = 3.5, tRC = tRC (min.)	1, 2, 5
Idle power down standby current	ICC2P	-7A -75 -1A	TBD	mA	CKE ≤ VIL	4
Idle standby current	ICC2N	-7A -75 -1A	TBD	mA	CKE ≥ VIH, /CS ≥ VIH	4
Active power down standby current	ICC3P	-7A -75 -1A	TBD	mA	CKE ≤ VIL	3
Active standby current	ICC3N	-7A -75 -1A	TBD	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = tRAS (max.)	3
Operating current (Burst read operation)	ICC4R	-7A -75 -1A	TBD	mA	CKE ≥ VIH, BL = 2, CL = 3.5	1, 2, 5, 6
Operating current (Burst write operation)	ICC4W	-7A -75 -1A	TBD	mA	CKE ≥ VIH, BL = 2, CL = 3.5	1, 2, 5, 6
Auto refresh current	ICC5	-7A -75 -1A	TBD	mA	tRFC = tRFC (min.) Input ≤ VIL or ≥ VIH	
Self refresh current	ICC6	-7A -75 -1A	TBD	mA	Input ≥ VDD – 0.2V Input ≤ 0.2V.	

Notes. 1. These ICC data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. The ICC data on this table are measured with regard to tCK = tCK (min.) in general.

DC Characteristics 2 (TA = 0 to +70°C, VDD = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–16	16	µA	VDD ≥ VIN ≥ VSS	
Output leakage current	ILO	–10	10	µA	VDD ≥ VOUT ≥ VSS	
Output high current	IOH	–15.2	—	mA	VOUT = 1.95V	
Output low current	IOL	15.2	—	mA	VOUT = 0.35V	

Pin Capacitance (TA = 25°C, VDD = 2.5V ± 0.2V)

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE, /CS, CKE	TBD	pF	
Input capacitance	CI2	CLK, /CLK	TBD	pF	
Data and DQS input/output capacitance	CO	DQ, DQS	TBD	pF	

AC Characteristics (TA = 0 to +70°C, VDD = 2.5V ± 0.2V, VSS = 0V)

Synchronous Characteristics

Parameter	Symbol	-7A min.	-7A max.	-75 min.	-75 max.	-1A min.	-1A max.	Unit	Note
Clock cycle time CL = 2.5	tCK	7.5	12	7.5	12	10	12	ns	
CL = 2				10	12	10	12	ns	
CLK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CLK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQ output access time from CLK, /CLK	tAC	−0.75	0.75	−0.75	0.75	−0.8	0.8	ns	
DQS output access time from CLK, /CLK	tDQSCK	−0.75	0.75	−0.75	0.75	−0.8	0.8	ns	
DQS-DQ skew (for DQS and associated DQ signals)	tDQSQ	—	0.5	—	0.5	—	0.6	ns	
DQS-DQ skew (for DQS and all DQ signals)	tDQSQA	—	0.5	—	0.5	—	0.6	ns	
Data out low-impedance time from CLK, /CLK	tLZ	−0.75	0.75	−0.75	0.75	−0.8	0.8	ns	
Data out high-impedance time from CLK, /CLK	tHZ	−0.75	0.75	−0.75	0.75	−0.8	0.8	ns	
Half clock period	tHP	tCH, tCL	—	tCH, tCL	—	tCH, tCL	—	ns	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQ/DQS output hold time from DQS	tQH	tHP – 0.75	—	tHP – 0.75	—	tHP – 1	—	ns	
DQ and DM input setup time	tDS	0.5	—	0.5	—	0.6	—	ns	
DQ and DM input hold time	tDH	0.5	—	0.5	—	0.6	—	ns	
DQ and DM input pulse width (for each input)	tDIPW	1.75	—	1.75	—	2	—	ns	
Write preamble setup time	tWPRES	0	—	0	—	0	—	ns	
Write preamble	tWPRE	0.25	—	0.25	—	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	0.35	—	tCK	
DQS falling edge to CLK setup time	tDSS	0.2	—	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CLK	tDSH	0.2	—	0.2	—	0.2	—	tCK	
Address and control input setup time	tIS	0.9	—	0.9	—	1.1	—	ns	
Address and control input hold time	tIH	0.9	—	0.9	—	1.1	—	ns	
Address and control input pulse width	tIPW	2.2	—	2.2	—	2.5	—	ns	
Internal write to read command delay	tWTR	1	—	1	—	1	—	tCK	

Synchronous Characteristics Example

tCK	7.5 ns		10 ns		
Symbol	min.	max.	min.	max.	Unit
tCH	3.4	4.1	4.5	5.5	ns
tCL	3.4	4.1	4.5	5.5	ns
tRPRE	6.75	8.25	9	11	ns
tRPST	3	4.5	4	6	ns
tWPRE	0.25	—	2.5	—	ns
tWPST	3	4.5	4	6	ns
tDQSS	5.6	9.4	7.5	12.5	ns
tDQSH	2.63	—	3.5	—	ns
tDQSL	2.63	—	3.5	—	ns
tDSS	1.5	—	2	—	ns
tDSH	1.5	—	2	—	ns
tWTR	7.5	—	10	—	ns

Asynchronous Characteristics

Parameter	Symbol	-7A		-75		-1A		Unit
		min.	max.	min.	max.	min.	max.	
ACT to REF/ACT command period (operation)	tRC	65	—	65	—	70	—	ns
REF to REF/ACT command period (refresh)	tRFC	75	—	75	—	80	—	ns
ACT to PRE command period	tRAS	45	120,000	45	120,000	50	120,000	ns
PRE to ACT command period	tRP	20	—	20	—	20	—	ns
ACT to READ/WRITE delay	tRCD	20	—	20	—	20	—	ns
ACT(one) to ACT(another) command period	tRRD	15	—	15	—	15	—	ns
Write recovery time	tWR	2	—	2	—	2	—	CLK
Auto precharge write recovery time + precharge time	tDAL	TBD	—	TBD	—	TBD	—	ns
Mode register set command cycle time	tMRD	15	—	15	—	15	—	ns
Exit self refresh to command	tXSNR	75	—	75	—	80	—	ns
Average periodic Refresh interval	tREF1	—	15.6	—	15.6	—	15.6	µs

Physical Outline

Unit: mm

Detail A

Detail B

ELPIDA
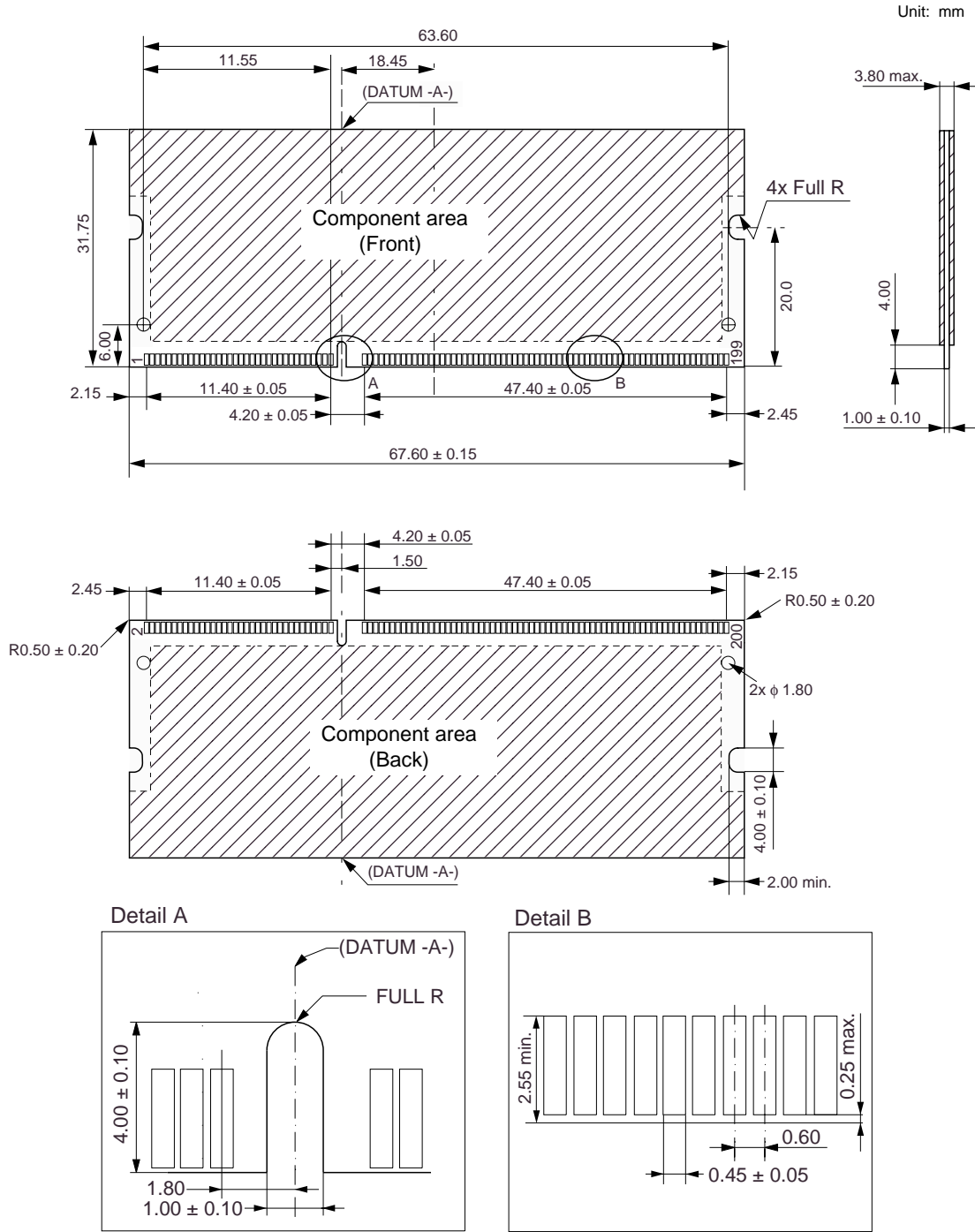
CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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