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# HM5113165LTD-6

128M EDO DRAM (8-Mword × 16-bit)  
4k refresh

**ELPIDA**

E0178H10 (Ver. 1.0)  
Jul. 12, 2001

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## Description

The HM5113165FL is 128M-bit dynamic RAM organized as 8,388,608-word × 16-bit. It has realized high performance and low power by employing CMOS process technology. HM5113165FL offers Extended Data Out (EDO) Page Mode as a high speed access mode. It is packaged in 50-pin plastic TSOPII.

## Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time: 60 ns (max)
- Power dissipation
  - Active: 828 mW (max)
  - Standby : 1.8 mW (max) (CMOS interface) (L-version)
- EDO page mode capability
- Refresh cycles
  - $\overline{\text{RAS}}$ -only refresh  
4096 cycles/64 ms
  - CBR/Hidden refresh  
4096 cycles/64 ms
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)

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## HM5113165FLTD-6

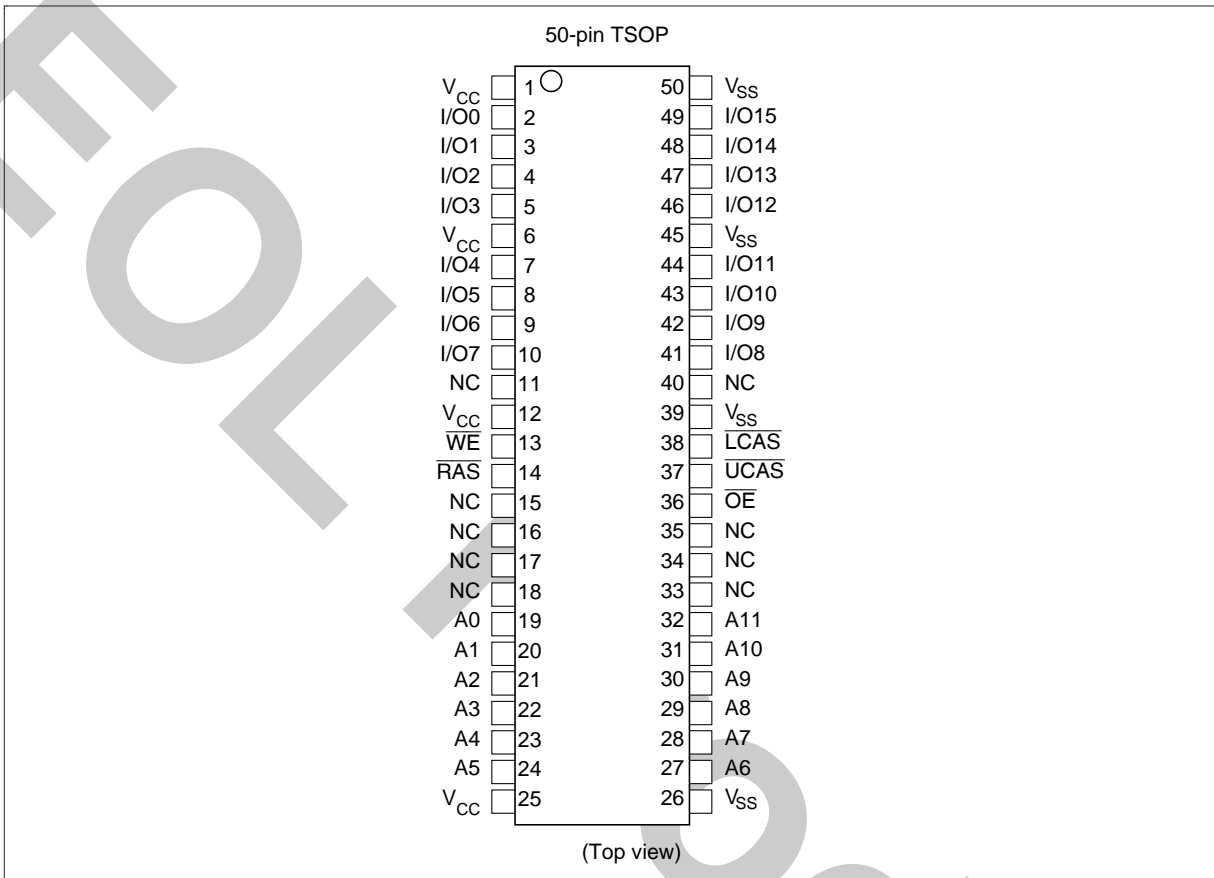
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- $\overline{2CAS}$ -byte control
- Battery backup operation (L-version)

### Ordering Information

Type No.	Access time	Package
HM5113165FLTD-6	60 ns	400-mil 50-pin plastic TSOP II (TTP-50DE)

Pin Arrangement (HM5113165F Series)

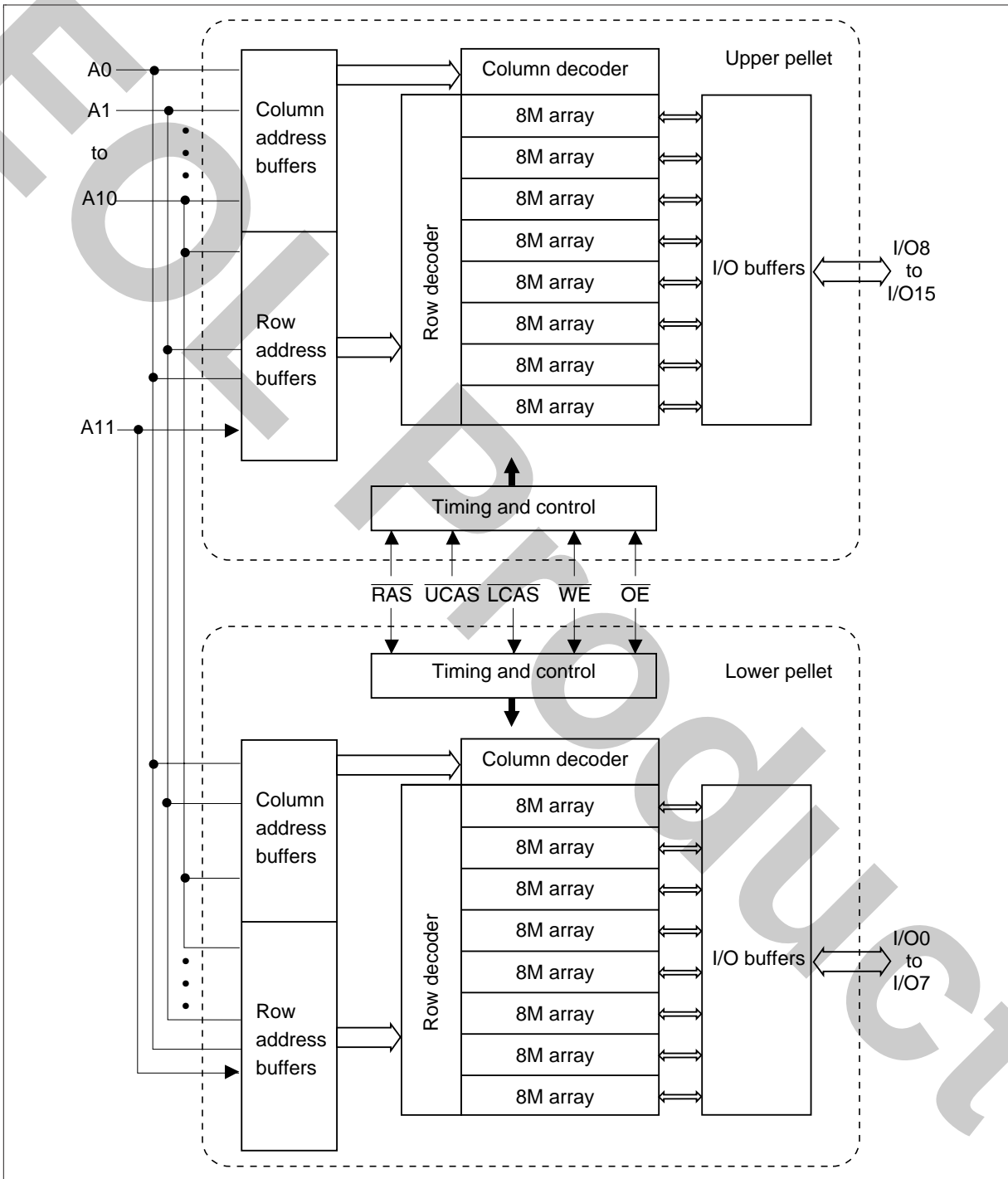


Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A10
I/O0 to I/O15	Data input/output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
$V_{\text{CC}}$	Power supply
$V_{\text{SS}}$	Ground
NC	No connection

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## Block Diagram



Operation Table

RAS	LCAS	UCAS	WE	OE	I/O 0 to I/O 7	I/O 8 to I/O 15	Operation
H	×	×	×	×	High-Z	High-Z	Standby
L	L	H	H	L	Dout	High-Z	Read cycle
L	H	L	H	L	High-Z	Dout	
L	L	L	H	L	Dout	Dout	
L	L	H	L*2	×	Din	×	Early write cycle
L	H	L	L*2	×	×	Din	
L	L	L	L*2	×	Din	Din	
L	L	H	L*2	H	Din	×	Delayed write cycle
L	H	L	L*2	H	×	Din	
L	L	L	L*2	H	Din	Din	
L	L	H	H to L	L to H	Dout/Din	High-Z	Read-modify-write cycle
L	H	L	H to L	L to H	High-Z	Dout/Din	
L	L	L	H to L	L to H	Dout/Din	Dout/Din	
L	H	H	×	×	High-Z	High-Z	RAS-only refresh cycle
H to L	L	L	H	×	High-Z	High-Z	CAS-before-RAS refresh cycle or Self refresh cycle (L-version)
L	L	L	H	H	High-Z	High-Z	Read cycle (Output disabled)

Notes: 1. H:  $V_{IH}$  (inactive) L:  $V_{IL}$  (active) ×:  $V_{IH}$  or  $V_{IL}$

2.  $t_{WCS} \geq 0$  ns: Early write cycle

$t_{WCS} < 0$  ns: Delayed write cycle

3. UCAS controls the upper pellet (I/O 8 to 15) only, and LCAS controls the lower pellet (I/O 0 to 7) only. Therefore, mode, read/write and High-Z control are done independently by each UCAS, LCAS.

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	$-0.5$ to $V_{CC} + 0.5$ ( $\leq 4.6$ V (max))	V
Power supply voltage relative to $V_{SS}$	$V_{CC}$	$-0.5$ to $+4.6$	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Storage temperature	$T_{stg}$	$-55$ to $+125$	$^{\circ}\text{C}$

### DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{CC}$	3.0	3.3	3.6	V	1, 2
	$V_{SS}$	0	0	0	V	2
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	$-0.3$	—	0.8	V	1
Ambient temperature range	$T_a$	0	—	70	$^{\circ}\text{C}$	

Notes: 1. All voltage referred to  $V_{SS}$ .

2. The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all  $V_{SS}$  pins must be on the same level.

DC Characteristics

Parameter	Symbol	HM5113165FL		Unit	Test conditions
		Min	Max		
Operating current* <sup>1, *2</sup>	$I_{CC1}$	—	230	mA	$t_{RC} = \text{min}$
Standby current (L-version)	$I_{CC2}$	—	500	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current* <sup>2</sup>	$I_{CC3}$	—	230	mA	$t_{RC} = \text{min}$
Standby current* <sup>1</sup>	$I_{CC5}$	—	10	mA	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IL}$ Dout = enable
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	$I_{CC6}$	—	230	mA	$t_{RC} = \text{min}$
EDO page mode current* <sup>1, *3</sup>	$I_{CC7}$	—	200	mA	$\overline{\text{RAS}} = V_{IL}, \overline{\text{CAS}} \text{ cycle}, t_{HPC} = t_{HPC} \text{ min}$
Battery backup current* <sup>4</sup> (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	2.5	mA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 15.6 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$
Self refresh mode current (L-version)	$I_{CC11}$	—	1.6	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \leq 0.2 \text{ V}$ Dout = High-Z
Input leakage current	$I_{LI}$	-5	5	$\mu\text{A}$	$0 \text{ V} \leq V_{in} \leq V_{CC} + 0.3 \text{ V}$
Output leakage current	$I_{LO}$	-5	5	$\mu\text{A}$	$0 \text{ V} \leq V_{out} \leq V_{CC}$ Dout = disable
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	V	High Iout = -2 mA
Output low voltage	$V_{OL}$	0	0.4	V	Low Iout = 2 mA

- Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.  
 2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .  
 3. Measured with one sequential address change per EDO cycle,  $t_{HPC}$ .  
 4.  $V_{IH} \geq V_{CC} - 0.2 \text{ V}, 0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ .

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**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{i1}$	—	—	7	pF	1
Input capacitance (Clocks)	$C_{i2}$	—	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{i/O}$	—	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $\overline{\text{RAS}}$ ,  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}} = V_{IH}$  to disable Dout.



**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ) \*<sup>1</sup>, \*<sup>2</sup>, \*<sup>19</sup>

**Test Conditions**

- Input rise and fall time: 2 ns
- Input pulse levels:  $V_{IL} = 0\text{ V}$ ,  $V_{IH} = 3.0\text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

**Read, Write, Read-Modify-Write and Refresh Cycles** (Common parameters)

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Parameter	Symbol	Min	Max	Unit	Notes
Random read or write cycle time	$t_{RC}$	104	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	40	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	—	ns	26
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	60	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	10	10000	ns	
Row address setup time	$t_{ASR}$	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	ns	26
Column address hold time	$t_{CAH}$	10	—	ns	26
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	14	45	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	12	30	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	15	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	40	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	5	—	ns	26
$\overline{\text{OE}}$ to Din delay time	$t_{OED}$	15	—	ns	5
$\overline{\text{OE}}$ delay time from Din	$t_{DZO}$	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	$t_{DZC}$	0	—	ns	6
Transition time (rise and fall)	$t_T$	2	50	ns	7

## HM5113165FLTD-6

### Read Cycle

Parameter	Symbol	HM5113165FL		Unit	Notes
		Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	ns	8, 9
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	ns	9, 10, 17
Access time from address	$t_{\text{AA}}$	—	30	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	15	ns	9
Read command setup time	$t_{\text{RCS}}$	0	—	ns	26
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	ns	12, 26
Read command hold time from $\overline{\text{RAS}}$	$t_{\text{RCHR}}$	60	—	ns	
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	18	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	ns	21
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	ns	13, 21
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	$t_{\text{OHR}}$	3	—	ns	21
Output buffer turn-off to $\overline{\text{RAS}}$	$t_{\text{OFR}}$	—	15	ns	13, 21
Output buffer turn-off to $\overline{\text{WE}}$	$t_{\text{WEZ}}$	—	15	ns	13
$\overline{\text{WE}}$ to Din delay time	$t_{\text{WED}}$	15	—	ns	
$\overline{\text{RAS}}$ to Din delay time	$t_{\text{RDD}}$	15	—	ns	

**Write Cycle**

HM5113165FL					
-6					
Parameter	Symbol	Min	Max	Unit	Notes
Write command setup time	$t_{WCS}$	0	—	ns	14, 26
Write command hold time	$t_{WCH}$	10	—	ns	26
Write command pulse width	$t_{WP}$	10	—	ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	15	—	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	10	—	ns	26
Data-in setup time	$t_{DS}$	0	—	ns	15, 26
Data-in hold time	$t_{DH}$	10	—	ns	15, 26

**Read-Modify-Write Cycle**

HM5113165FL					
-6					
Parameter	Symbol	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	140	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	79	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	34	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	49	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEH}$	15	—	ns	

**Refresh Cycle**

HM5113165FL					
-6					
Parameter	Symbol	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	ns	26
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	ns	26
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	5	—	ns	26

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### EDO Page Mode Cycle

Parameter	Symbol	HM5113165FL		Unit	Notes
		-6			
		Min	Max		
EDO page mode cycle time	$t_{HPC}$	25	—	ns	20
EDO page mode RAS pulse width	$t_{RASP}$	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	35	ns	9, 17, 26
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	35	—	ns	
Output data hold time from $\overline{CAS}$ low	$t_{DOH}$	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	$t_{COL}$	10	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	$t_{COP}$	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	$t_{RCHC}$	35	—	ns	
Write pulse width during $\overline{CAS}$ precharge	$t_{WPE}$	10	—	ns	
$\overline{OE}$ precharge time	$t_{OEP}$	10	—	ns	

### EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5113165FL		Unit	Notes
		-6			
		Min	Max		
EDO page mode read-modify-write cycle time	$t_{HPRWC}$	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	54	—	ns	14, 26

### Refresh

Parameter	Symbol	Max	Unit	Notes
Refresh period (L-version)	$t_{REF}$	64	ms	4096 cycles

Self Refresh Mode (L-version)

Parameter	Symbol	HM5113165FL		Unit	Notes
		Min	Max		
RAS pulse width (self refresh)	$t_{RASS}$	100	—	$\mu s$	25
RAS precharge time (self refresh)	$t_{RPS}$	110	—	ns	25
CAS hold time (self refresh)	$t_{CHS}$	-50	—	ns	26

- Notes:
1. AC measurements assume  $t_T = 2$  ns.
  2. An initial pause of 200  $\mu s$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{RAS}$ -only refresh or  $\overline{CAS}$ -before- $\overline{RAS}$  refresh).
  3. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then the access time is controlled exclusively by  $t_{CAC}$ .
  4. Operation with the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled exclusively by  $t_{AA}$ .
  5. Either  $t_{OED}$  or  $t_{CDD}$  must be satisfied.
  6. Either  $t_{DZO}$  or  $t_{DZC}$  must be satisfied.
  7.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
  8. Assumes that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max). If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
  10. Assumes that  $t_{RCD} \geq t_{RCD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\geq t_{RAD} + t_{AA}$  (max).
  11. Assumes that  $t_{RAD} \geq t_{RAD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\leq t_{RAD} + t_{AA}$  (max).
  12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles.
  13.  $t_{OFF}$  (max),  $t_{OEZ}$  (max),  $t_{WEZ}$  (max) and  $t_{OFR}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  14.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}$  (min),  $t_{CWD} \geq t_{CWD}$  (min), and  $t_{AWD} \geq t_{AWD}$  (min), or  $t_{CWD} \geq t_{CWD}$  (min),  $t_{AWD} \geq t_{AWD}$  (min) and  $t_{CPW} \geq t_{CPW}$  (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  15.  $t_{DS}$  and  $t_{DH}$  are referred to  $\overline{UCAS}$  and  $\overline{LCAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in delayed write or read-modify-write cycles.
  16.  $t_{RASP}$  defines  $\overline{RAS}$  pulse width in EDO page mode cycles.
  17. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$ .
  18. In delayed write or read-modify-write cycles,  $\overline{OE}$  must disable output buffer prior to applying data to the device.
  19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH}$  min/ $V_{IL}$  max level.

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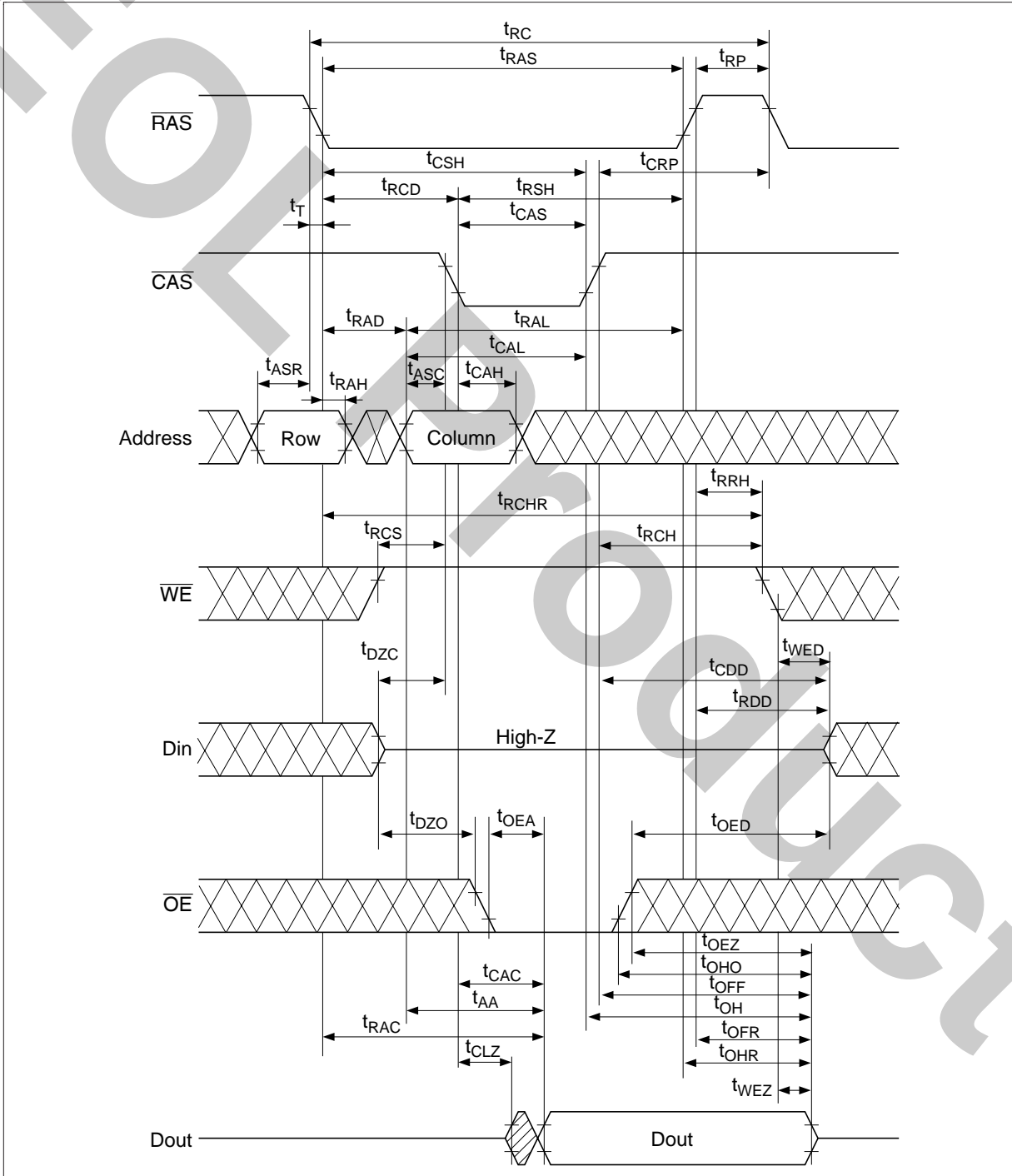
## HM5113165FLTD-6

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20.  $t_{\text{HPC}}$  (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode  $\overline{\text{RAS}}$  cycle (EDO page mode mix cycle (1), (2)), minimum value of  $\overline{\text{CAS}}$  cycle ( $t_{\text{CAS}} + t_{\text{CP}} + 2 t_{\text{T}}$ ) becomes greater than the specified  $t_{\text{HPC}}$  (min) value. The value of  $\overline{\text{CAS}}$  cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . Hold time and turn off time are specified by the timing specifications of later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  between  $t_{\text{OHR}}$  and  $t_{\text{OH}}$  and between  $t_{\text{OFR}}$  and  $t_{\text{OFF}}$ .
22.  $t_{\text{DOH}}$  defines the time at which the output level go cross.  $V_{\text{OL}} = 0.8 \text{ V}$ ,  $V_{\text{OH}} = 2.0 \text{ V}$  of output timing reference level.
23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
- Enter self refresh mode within 15.6  $\mu\text{s}$  after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
  - Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6  $\mu\text{s}$  after exiting from self refresh mode.
24. In case of entering from  $\overline{\text{RAS}}$ -only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 23.
25. At  $t_{\text{RASS}} > 100 \mu\text{s}$ , self refresh mode is activated, and not activated at  $t_{\text{RASS}} < 10 \mu\text{s}$ . It is undefined within the range of  $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$ . For  $t_{\text{RASS}} \geq 10 \mu\text{s}$ , it is necessary to satisfy  $t_{\text{RPS}}$ .
26.  $t_{\text{ASC}}$ ,  $t_{\text{CAH}}$ ,  $t_{\text{RCS}}$ ,  $t_{\text{WCS}}$ ,  $t_{\text{WCH}}$ ,  $t_{\text{CSR}}$ ,  $t_{\text{RPC}}$ ,  $t_{\text{CRP}}$ ,  $t_{\text{CHR}}$ ,  $t_{\text{RCH}}$ ,  $t_{\text{CPA}}$ ,  $t_{\text{CPW}}$ ,  $t_{\text{CWL}}$ ,  $t_{\text{DH}}$ ,  $t_{\text{DS}}$ ,  $t_{\text{CHS}}$  and  $t_{\text{CP}}$  are determined by each of UCAS /LCAS independently.
27. XXX: H or L (H:  $V_{\text{IH}} (\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{max})$ , L:  $V_{\text{IL}} (\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}} (\text{max})$ )  
/////: Invalid Dout  
When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{\text{IH}}$  or  $V_{\text{IL}}$ .

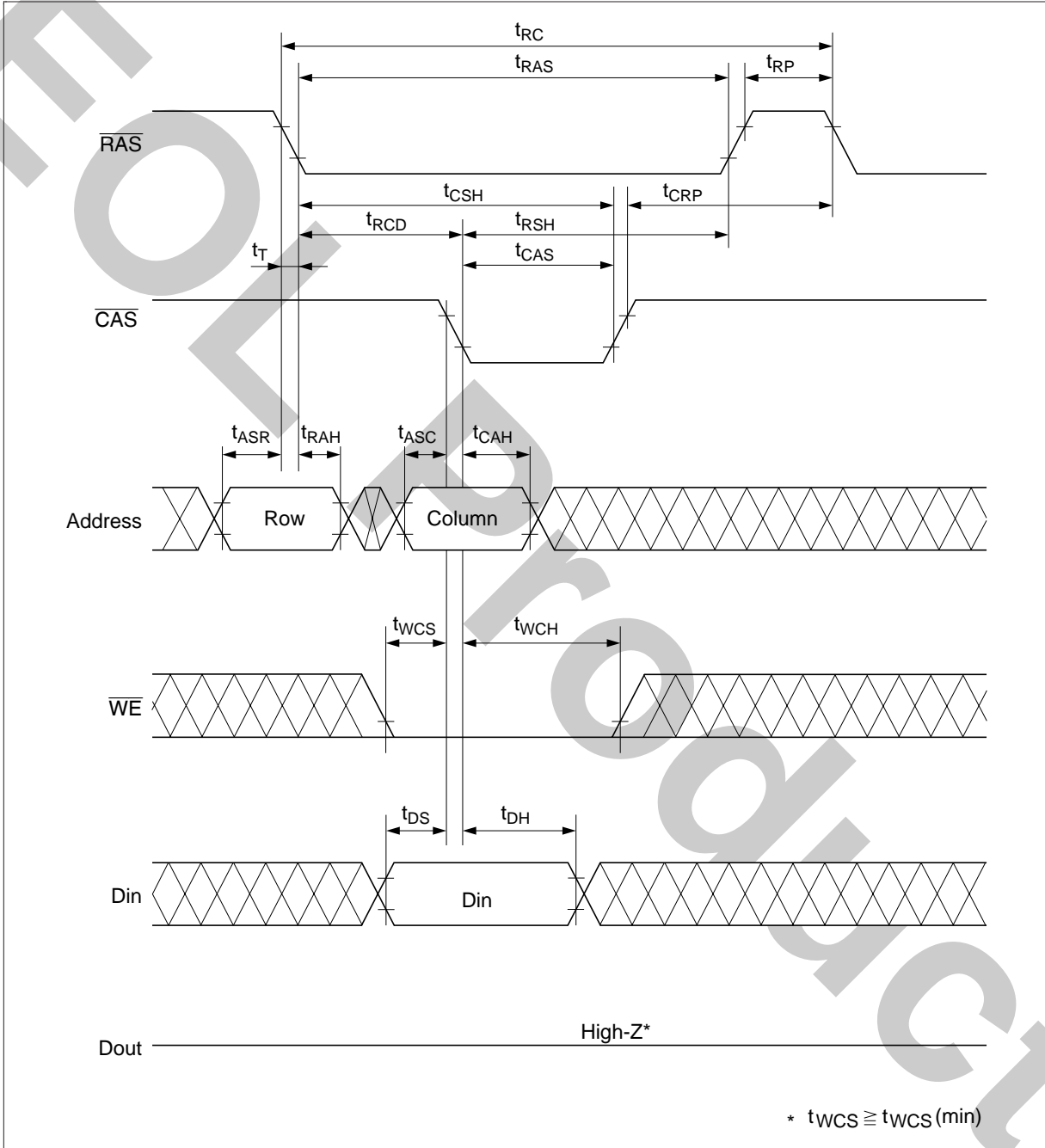
Timing Waveforms\*27

Read Cycle



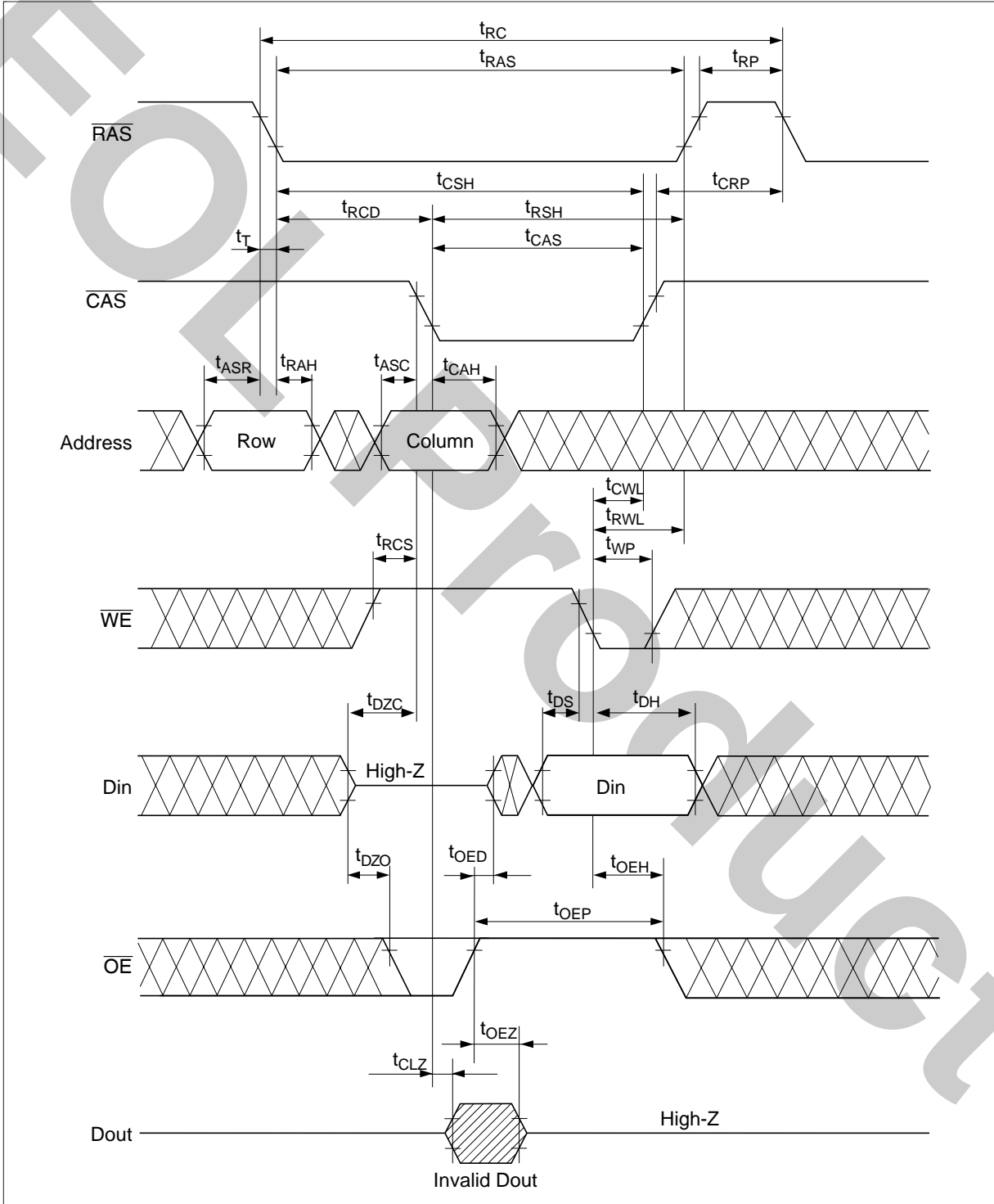
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## Early Write Cycle



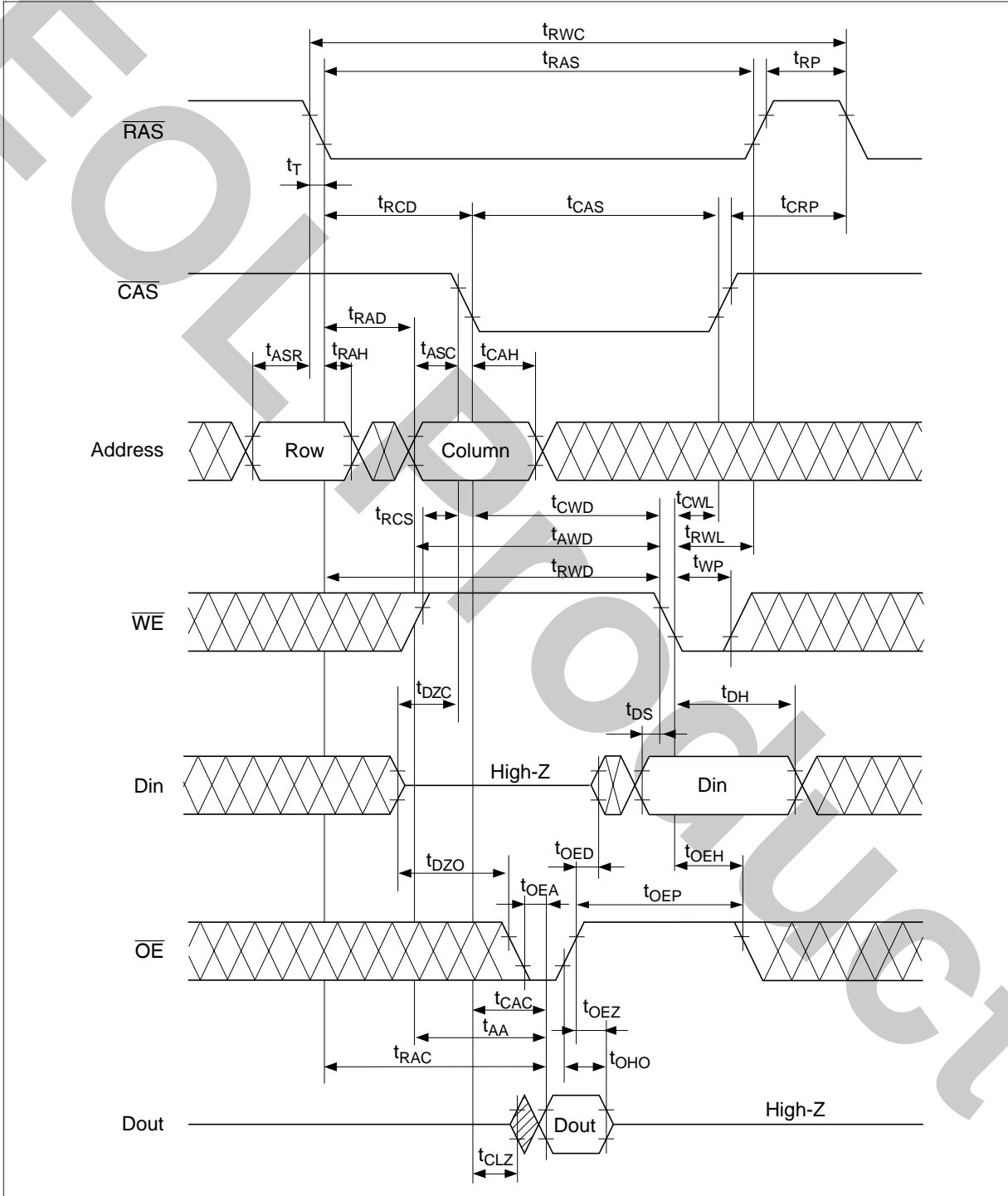


Delayed Write Cycle\*18



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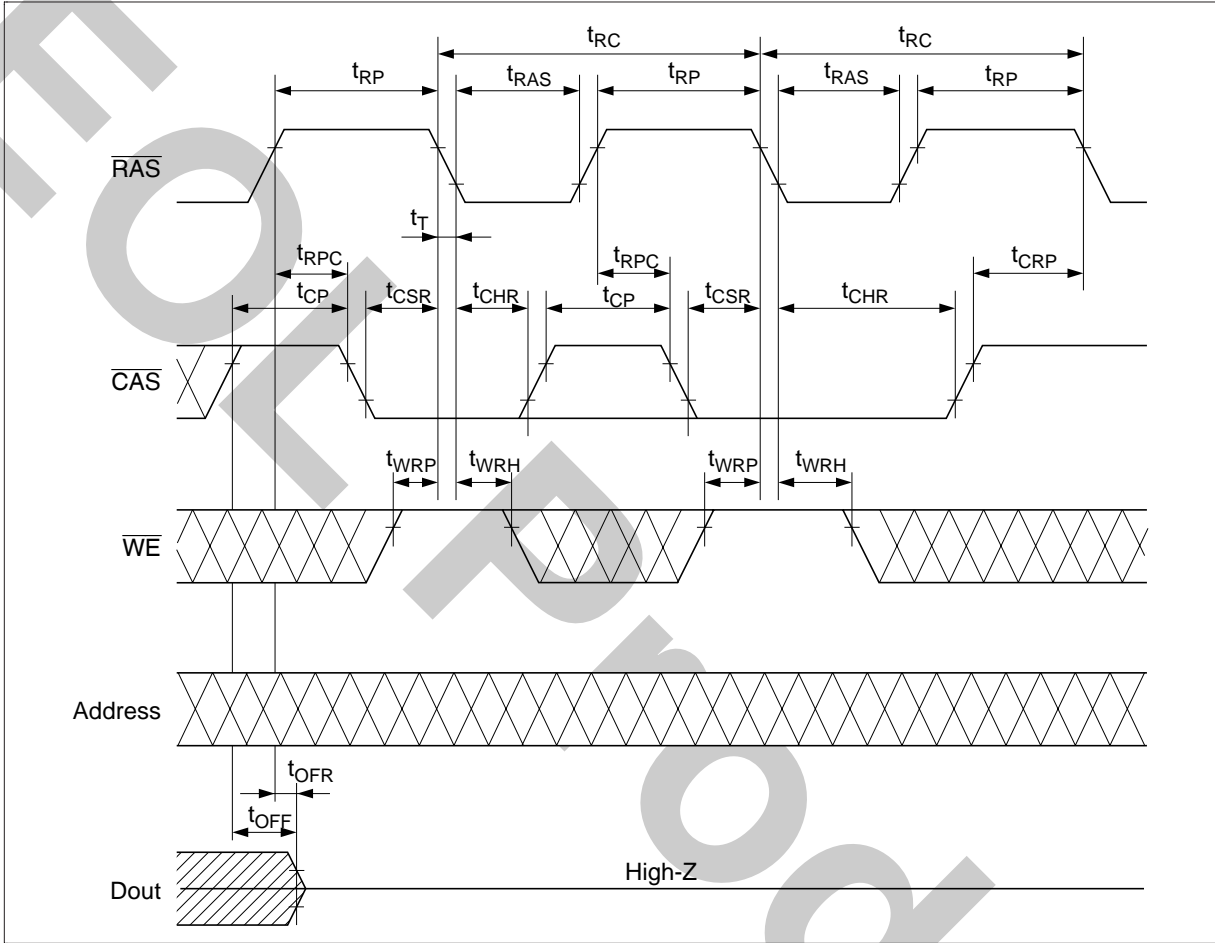
## Read-Modify-Write Cycle<sup>18</sup>



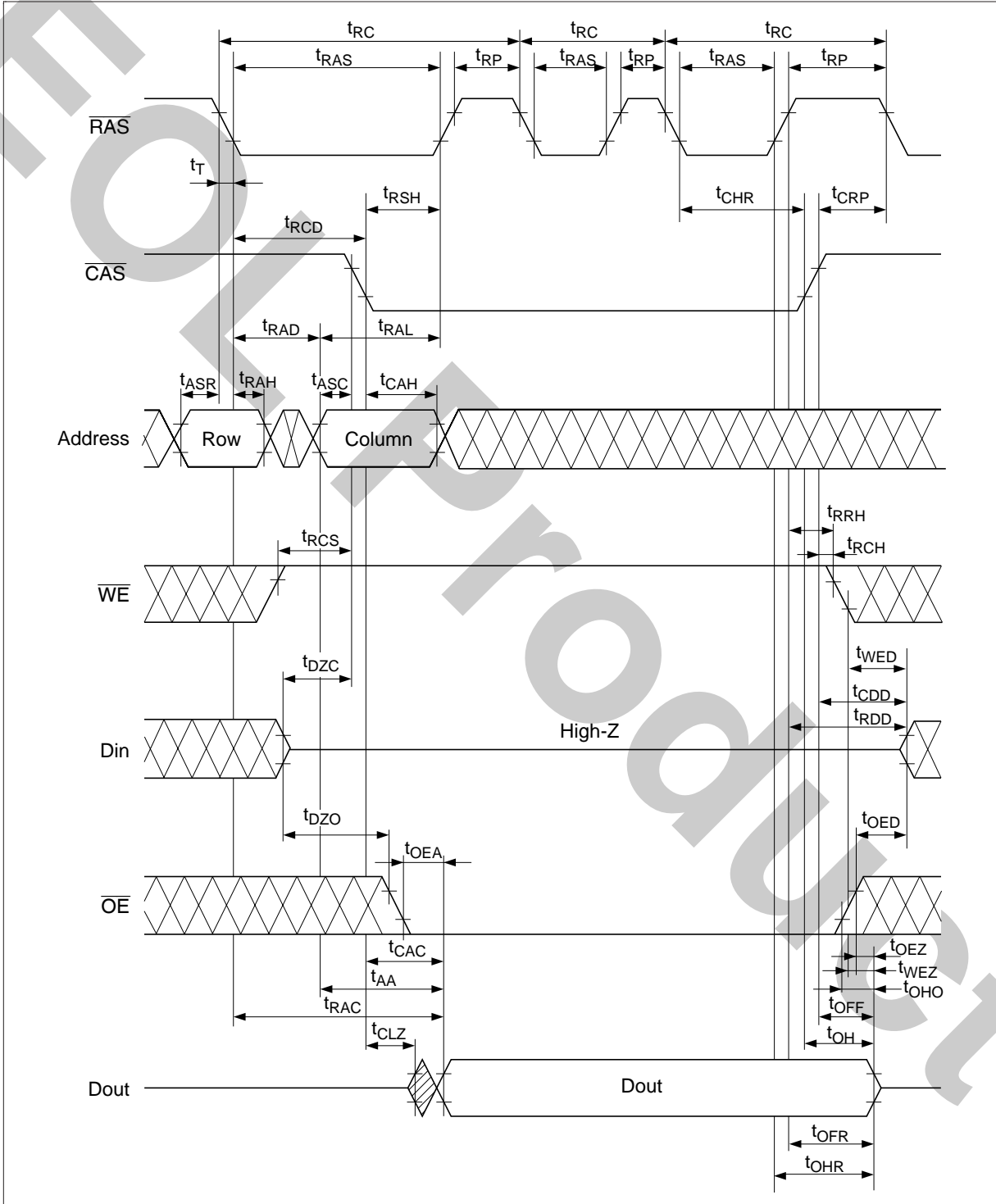


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## $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle



Hidden Refresh Cycle

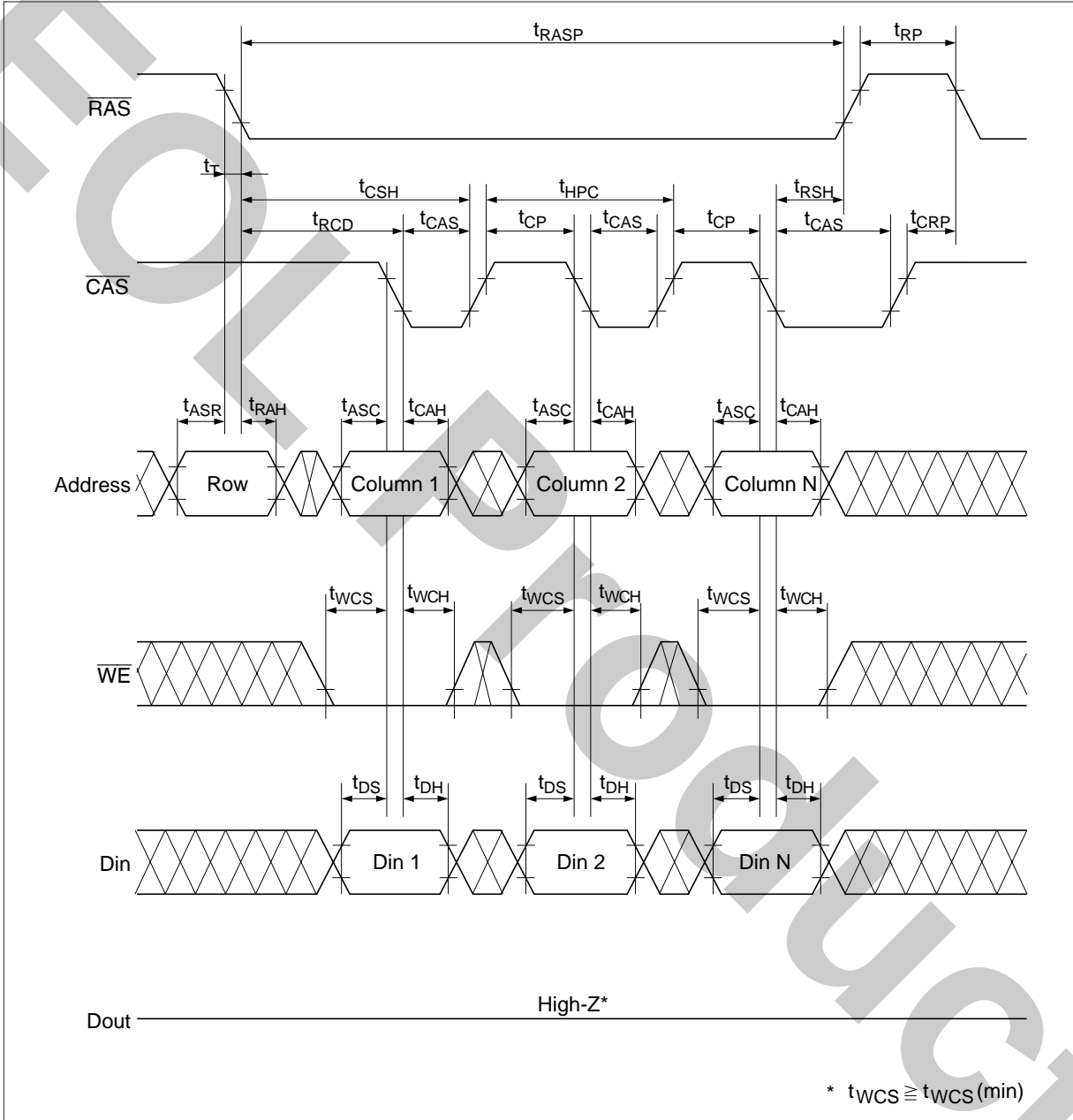






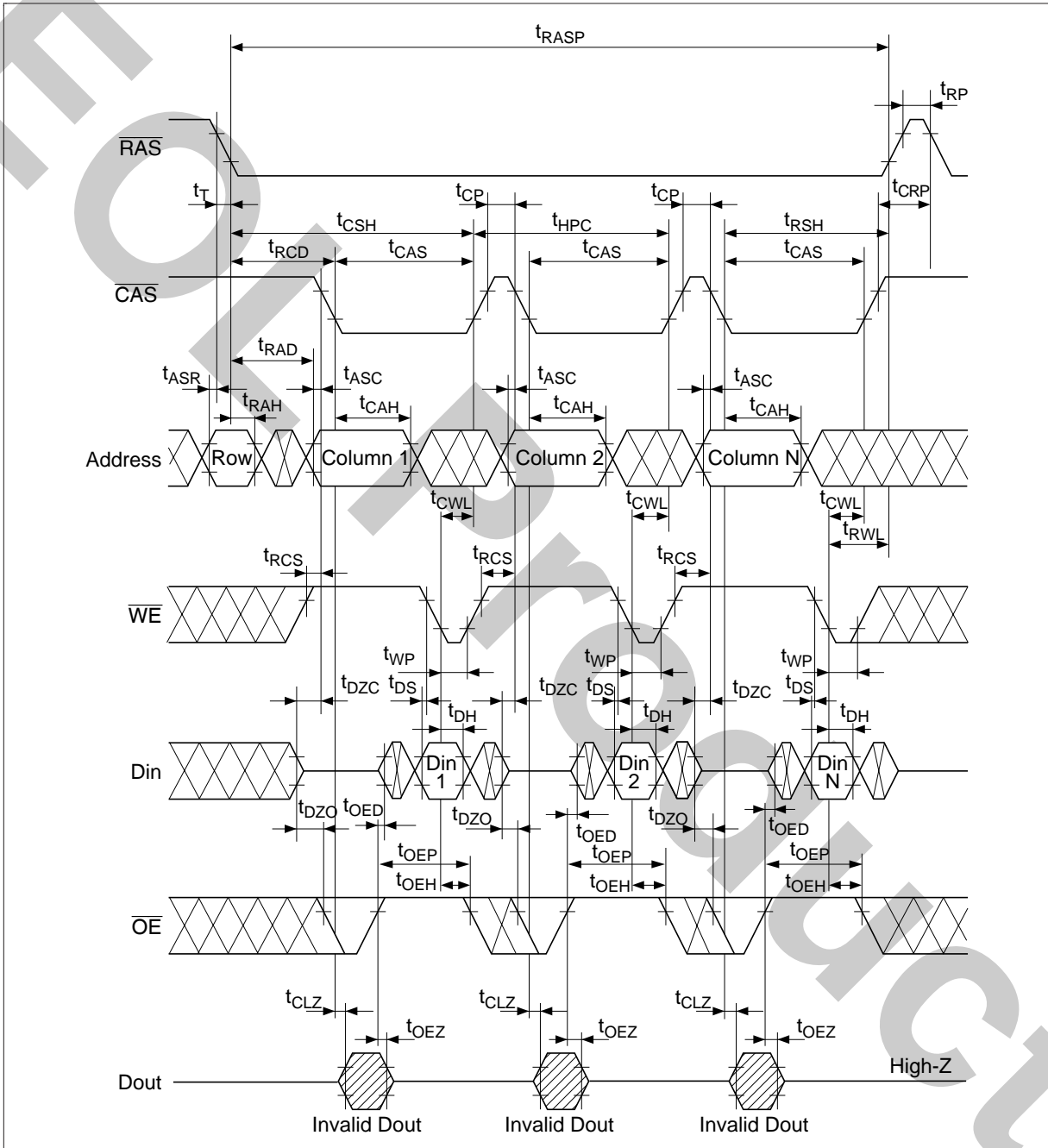
# HM5113165FLTD-6

## EDO Page Mode Early Write Cycle



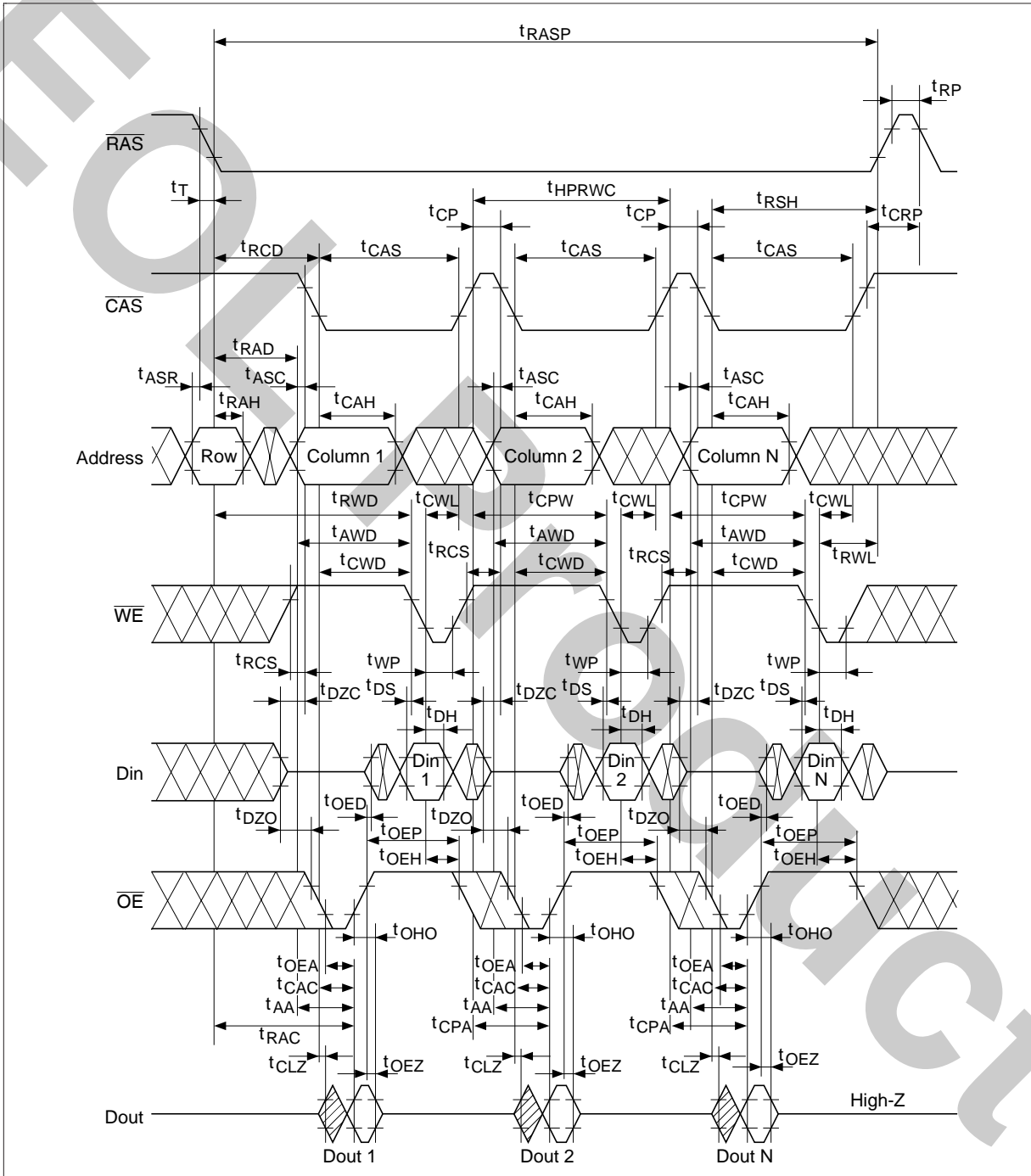


EDO Page Mode Delayed Write Cycle\*18



# HM5113165FLTD-6

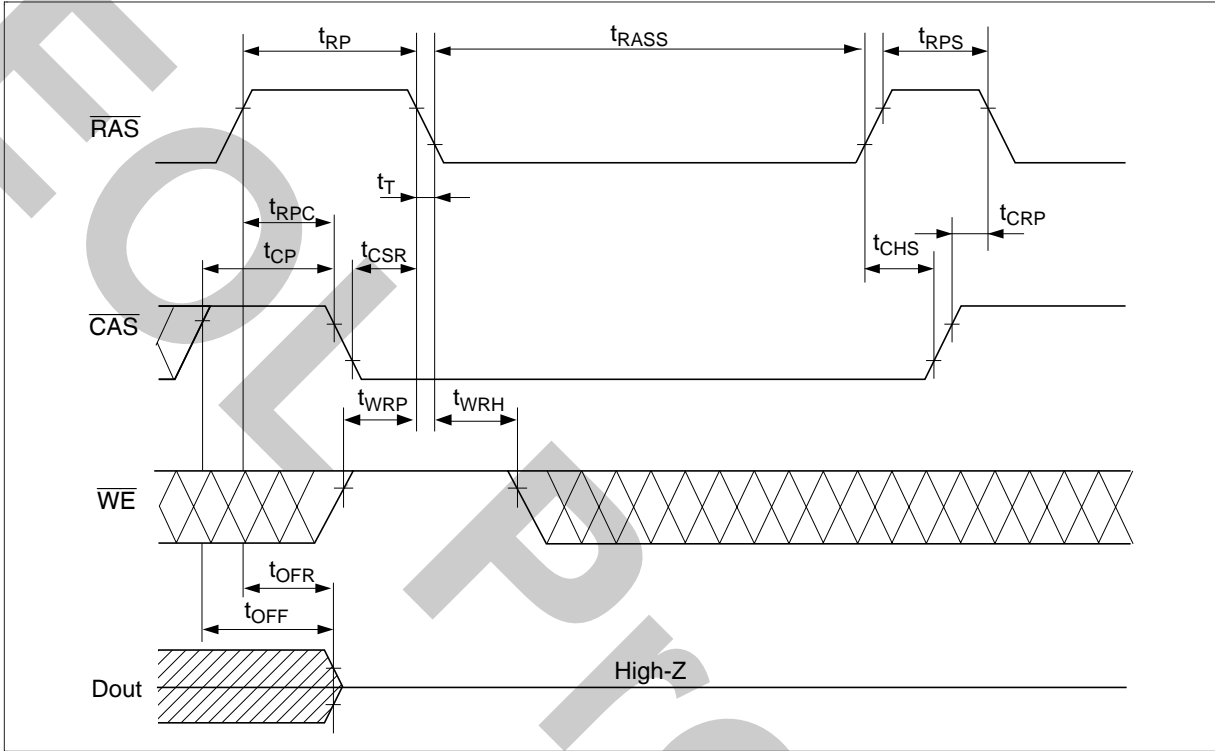
## EDO Page Mode Read-Modify-Write Cycle\*18







Self Refresh Cycle (L-version)\*<sup>23, 24, 25</sup>





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