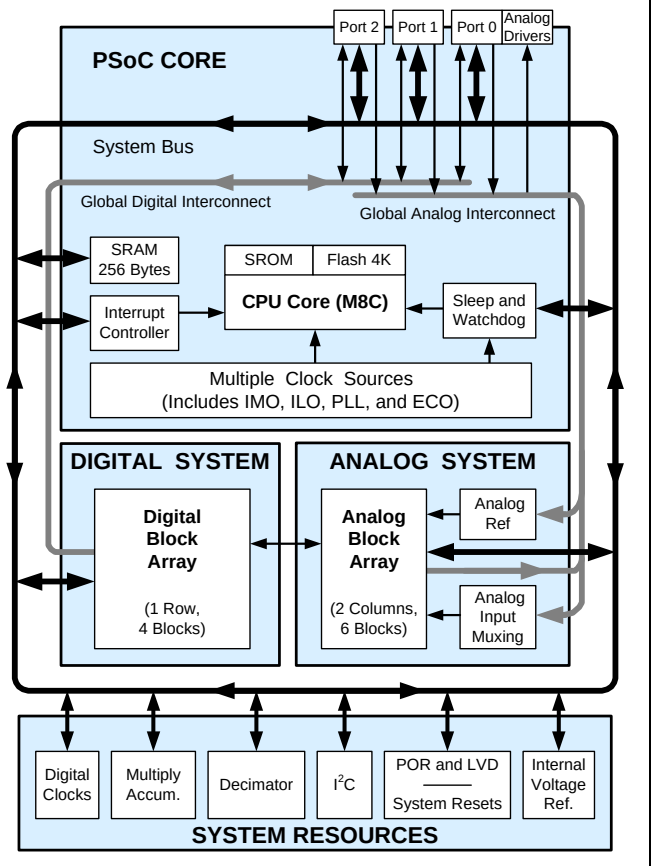
CY8C24423A

Automotive PSoC® Programmable System-on-Chip

Features

- AEC Qualified
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds up to 24 MHz
  - 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 3.0V to 5.25V Operating Voltage
  - Automotive Temperature Range: -40°C to +85°C
- Advanced Peripherals (PSoC® Blocks)
  - Six Rail-to-Rail Analog PSoC Blocks Provide:
    - Up to 14-Bit ADCs
    - Up to 9-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - Four Digital PSoC Blocks Provide:
    - 8- to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Full- or Half-Duplex UART
    - SPI Master or Slave
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- Precision, Programmable Clocking
  - Internal ±5% 24/48 MHz Oscillator
  - High Accuracy 24 MHz with Optional 32 kHz Crystal and PLL
  - Optional External Oscillator, up to 24 MHz
  - Internal Low Speed, Low Power Oscillator for Watchdog and Sleep Functionality
- Flexible On-Chip Memory
  - 4K Bytes Flash Program Storage, 1000 Erase/Write Cycles
  - 256 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 25 mA Sink, 10 mA Drive on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO
  - Up to 12 Analog Inputs on GPIO[1]
  - Two 30 mA Analog Outputs on GPIO
  - Configurable Interrupt on All GPIO
- Additional System Resources
  - I²C™ Slave, Master, or Multi-Master operation up to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory

Logic Block Diagram



Note
1. There are eight standard analog inputs on the GPIO. The other four analog inputs connect from the GPIO directly to specific switched-capacitor block inputs. See the *PSoC Technical Reference Manual* for more details.

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the Logic Block Diagram on page 1, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global buses allow all the device resources to be combined into a complete custom system. Each CY8C24x23A PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 24 general purpose I/O (GPIO) are also included. The GPIO provide access to the global digital and analog interconnects.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with multiple vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep Timer and Watchdog Timer (WDT).

Memory includes 4 KB of Flash for program storage and 256 bytes of SRAM for data storage. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

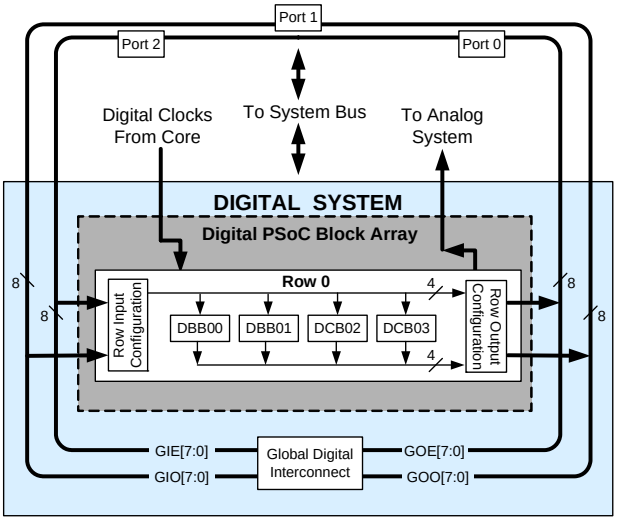
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to ±5% over temperature and voltage. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep Timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt.

Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include:

- PWMs (8 to 32 bit)
- PWMs with Dead Band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full or Half-Duplex 8-bit UART with selectable parity
- SPI master and slave
- I^2C master, slave, or multi-master
- Cyclical Redundancy Checker/Generator (16 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 4.

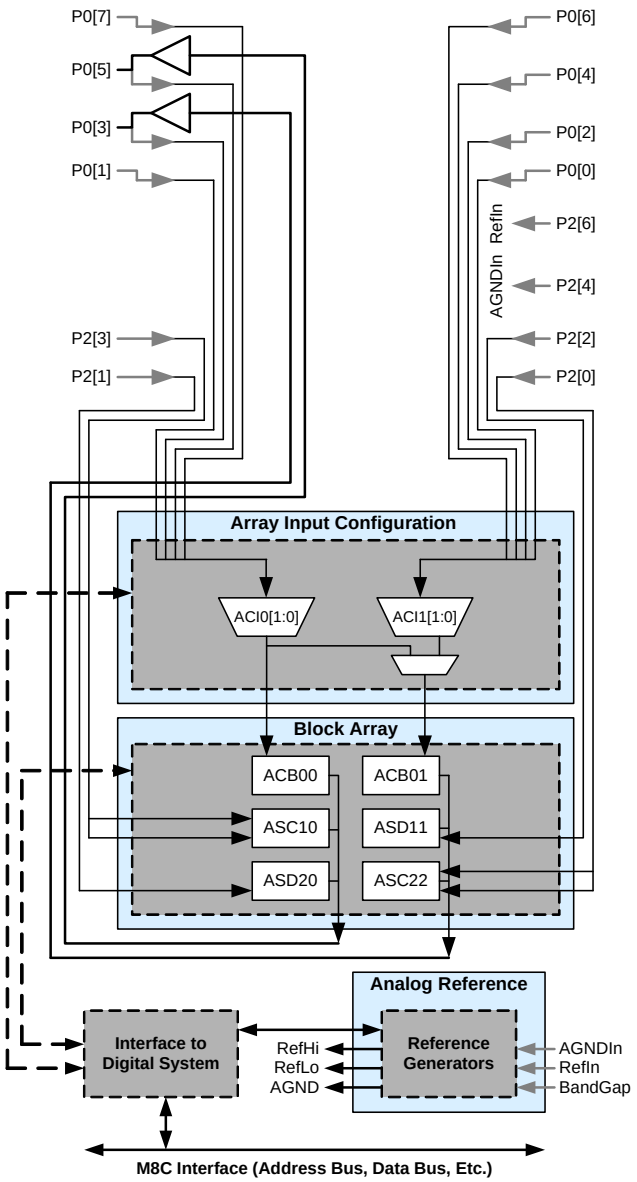
Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta-Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain up to 48x)
- Instrumentation amplifiers (one with selectable gain up to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful for complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in Table 1.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[2]	up to 64	4	16	12	4	4	12	2K	32K
CY8C27x43	up to 44	2	8	12	4	4	12	256 Bytes	16K
CY8C24x94	64	1	4	48	2	2	6	1K	16K
CY8C24x23A[2]	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C23x33	up to	1	4	12	2	2	4	256 Bytes	8K
CY8C21x34[2]	up to 28	1	4	28	0	2	4[3]	512 Bytes	8K
CY8C21x23	16	1	4	8	0	2	4[3]	256 Bytes	4K
CY8C20x34	up to 28	0	0	28	0	0	3[3, 4]	512 Bytes	8K

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Programmable System-on-Chip Technical Reference Manual for CY8C24x23A PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Notes
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense™ block.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC On-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 7 on page 12 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are decimal.

Pinouts

The automotive CY8C24x23A PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

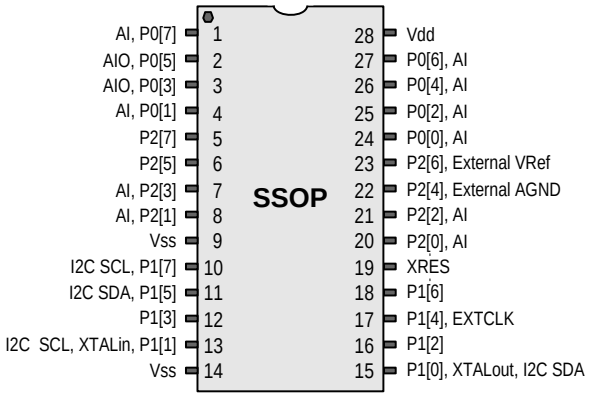
28-Pin Part Pinout

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		Vss	Ground connection
10	I/O		P1[7]	I^2C Serial Clock (SCL)
11	I/O		P1[5]	I^2C Serial Data (SDA)
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal Input (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[5]
14	Power		Vss	Ground connection
15	I/O		P1[0]	Crystal Output (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[5]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK)
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External Analog Ground (AGND)
23	I/O		P2[6]	External Voltage Reference (VRef)
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		Vdd	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C24423A 28-Pin PSoC Device



Note
5. These are the ISSP pins, which are not High Z when coming out of POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.

Registers

Register Conventions

This section lists the registers of the automotive CY8C24x23A PSoC device. For detailed register information, reference the *PSoC Technical Reference Manual*.

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C24x23A PSoC devices. For the latest electrical specifications, visit http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Refer to Table 22 on page 22 for the electrical specifications on the IMO using SLIMO mode.

Figure 4. Voltage versus CPU Frequency

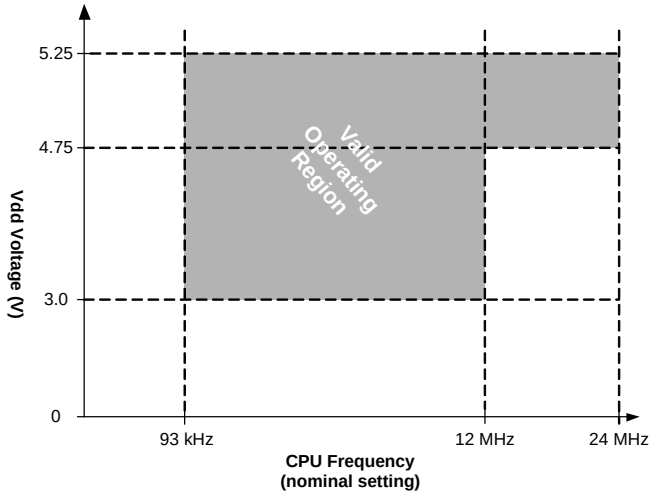
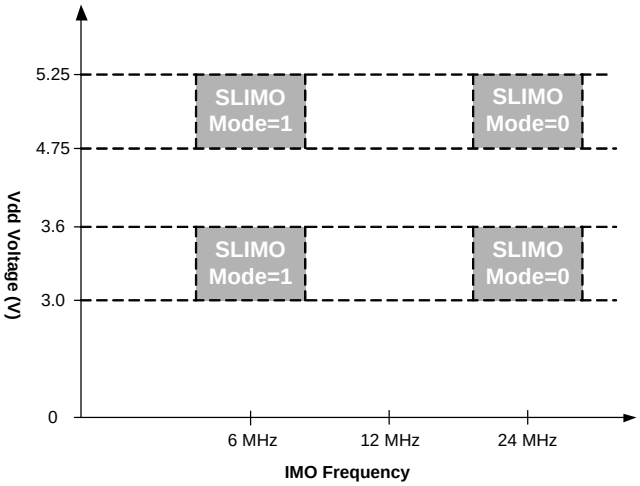


Figure 5. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 7. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µVrms	microvolts root-mean-square
dB	decibels	µW	microwatts
fF	femto farad	mA	milli-ampere
Hz	hertz	ms	milli-second
KB	1024 bytes	mV	milli-volts
Kbit	1024 bits	nA	nanoampere
kHz	kilohertz	ns	nanosecond
kΩ	kilohm	nV	nanovolts
Mbaud	megabaud	Ω	ohm
Mbps	megabits per second	pA	picoampere
MHz	megahertz	pF	picofarad
MΩ	megaohm	pp	peak-to-peak
µA	microampere	ppm	parts per million
µF	microfarad	ps	picosecond
µH	microhenry	sps	samples per second
µs	microsecond	σ	sigma: one standard deviation
µV	microvolts	V	volts

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch Up Current	–	–	200	mA	

Operating Temperature

Table 9. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 34 on page 32. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 10. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 20 on page 20.
I_{DD}	Supply Current	–	5	8	mA	Conditions are Vdd = 5.0V, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{DD3}	Supply Current	–	3.3	6.0	mA	Conditions are Vdd = 3.3V, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[6]	–	3	6.5	µA	Conditions are with internal low speed oscillator active, Vdd = 3.3V, -40°C ≤ T_A ≤ 55°C, Analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at High Temperature.[6]	–	4	25	µA	Conditions are with internal low speed oscillator active, Vdd = 3.3V, 55°C < T_A ≤ 85°C, Analog power = off.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and External Crystal.[6]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40°C ≤ T_A ≤ 55°C, Analog power = off.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and External Crystal at High Temperature.[6]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3 V, 55°C < T_A ≤ 85°C, Analog power = off.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate Vdd. Vdd ≥ 3.0V

Note
6. Standby current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC General Purpose I/O Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time (CT) PSoC blocks and the Analog Switched Capacitor (SC) PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time (CT) PSoC block.

Table 12. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 60 60 80	 – – –	 – – –	 dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = High Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	64	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd

Table 13. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5V Only	 – –	 1.65 1.32	 10 8	 mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 60 60 80	 – – –	 – – –	 dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – –	 150 300 600 1200 2400	 200 400 800 1600 3200	 µA µA µA µA µA	 Not allowed
$PSRR_{OA}$	Supply Voltage Rejection Ratio	64	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd

DC Low Power Comparator Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32Ω to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32Ω to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25).

Table 16. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25)

DC Analog Reference Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 17. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[7]	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[7]	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[7]	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[7]	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[7]	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[7]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap[8]	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap[8]	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)[8]	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)[8]	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2 P2[6] = 1.3V)[8]	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6] + 0.100	V
–	RefHi = 3.2 x BandGap[8]	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 - BandGap[8]	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V
–	RefLo = BandGap[8]	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)[8]	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)[8]	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4] - P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)[8]	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

Table 18. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2[7]	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[7]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)[7]	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[7]	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[7]	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[7]	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap[8]	Not Allowed			

Notes
7. This specification is only valid when CT Block Power = High. AGND tolerance includes the offsets of the local buffer in the PSoC block.
8. This specification is only valid when Ref Control Power = High.

Table 18. 3.3V DC Analog Reference Specifications (continued)

Symbol	Description	Min	Typ	Max	Units
–	RefHi = 3 x BandGap[8]		Not Allowed		
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)[8]		Not Allowed		
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)[8]		Not Allowed		
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)[8]	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap[8]		Not Allowed		
–	RefLo = Vdd/2 - BandGap[8]		Not Allowed		
–	RefLo = BandGap[8]		Not Allowed		
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)[8]		Not Allowed		
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)[8]		Not Allowed		
–	RefLo = P2[4] - P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)[8]	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

DC Analog PSoC Block Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 19. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

DC POR and LVD Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for more information on the VLT_CR register.

Table 20. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b		2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[9]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[10]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

Notes
9. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
10. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.

DC Programming Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 21. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	3.0	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	1,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[11]	36,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note

11. A maximum of 36 x 1,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 1,000 maximum cycles each, 36x2 blocks of 500 maximum cycles each, or 36x4 blocks of 250 maximum cycles each (to limit the total number of cycles to 36x1,000 and that no single block ever sees more than 1,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	22.8[13]	24	25.2[12,13]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 5 on page 12. SLIMO mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5[13]	6	6.5[12,13]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 5 on page 12. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (5V Vdd Nominal)	0.089[13]	24	25.2[12,13]	MHz	Minimum CPU frequency is 0.022 MHz when SLIMO mode = 1
F_{CPU2}	CPU Frequency (3.3V Vdd Nominal)	0.089[13]	12	12.6[13]	MHz	Minimum CPU frequency is 0.022 MHz when SLIMO mode = 1
F_{48M}	Digital PSoC Block Frequency	0	48	50.4[12,13,14]	MHz	Refer to the AC Digital Block Specifications.
F_{24M}	Digital PSoC Block Frequency	0	24	25.2[13,14]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed. During power up, the ILO is untrimmed and has a minimum frequency of 5 kHz.
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	Refer to Figure 9 on page 23.
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	Refer to Figure 6 on page 23.
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	Refer to Figure 7 on page 23.
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	Refer to Figure 8 on page 23.
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.25V, -40 °C ≤ T_A ≤ 85 °C.
Jitter32k	32 kHz Period Jitter	–	100	–	ns	Refer to Figure 10 on page 23.
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	45.6[13]	48.0	50.4[12, 13]	MHz	Trimmed. Using factory trim values.
Jitter24M1P	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300	–	ps	Refer to Figure 9 on page 23.
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	
F_{MAX}	Maximum Frequency of signal on row input or row output.	–	–	12.6[13]	MHz	
T_{RAMP}	Supply Ramp Time	20	–	–	µs	

Notes
12. 4.75V ≤ Vdd ≤ 5.25V.
13. Accuracy derived from Internal Main Oscillator (IMO) with appropriate trim for Vdd range.
14. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 6. PLL Lock Timing Diagram

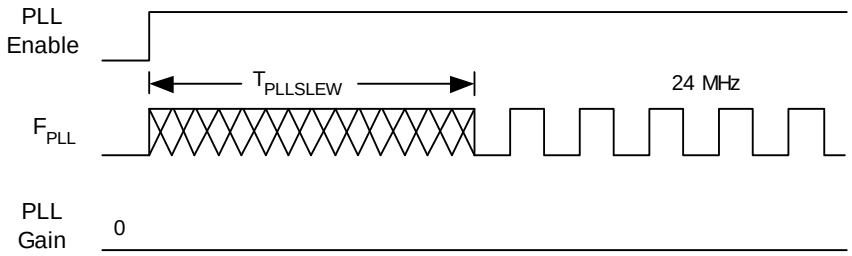


Figure 7. PLL Lock for Low Gain Setting Timing Diagram

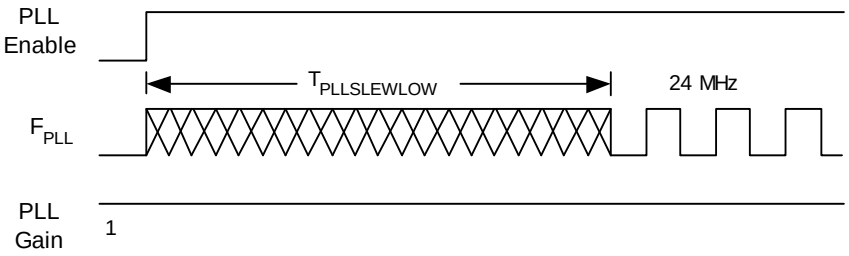


Figure 8. External Crystal Oscillator Startup Timing Diagram

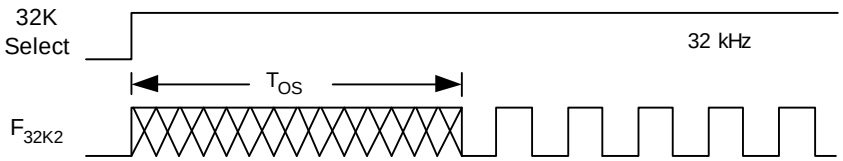


Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram

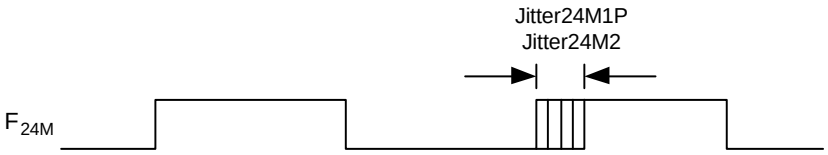
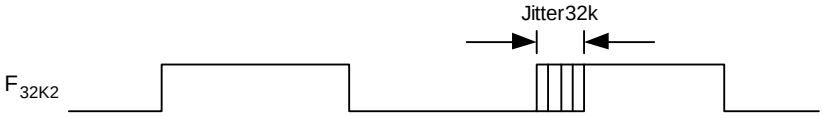


Figure 10. 32 kHz Period Jitter (ECO) Timing Diagram



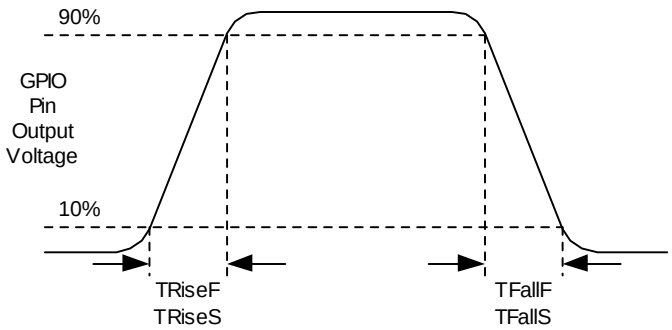
AC General Purpose I/O Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 23. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.6[13]	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 11. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 24. 5V AC Operational Amplifier Specifications

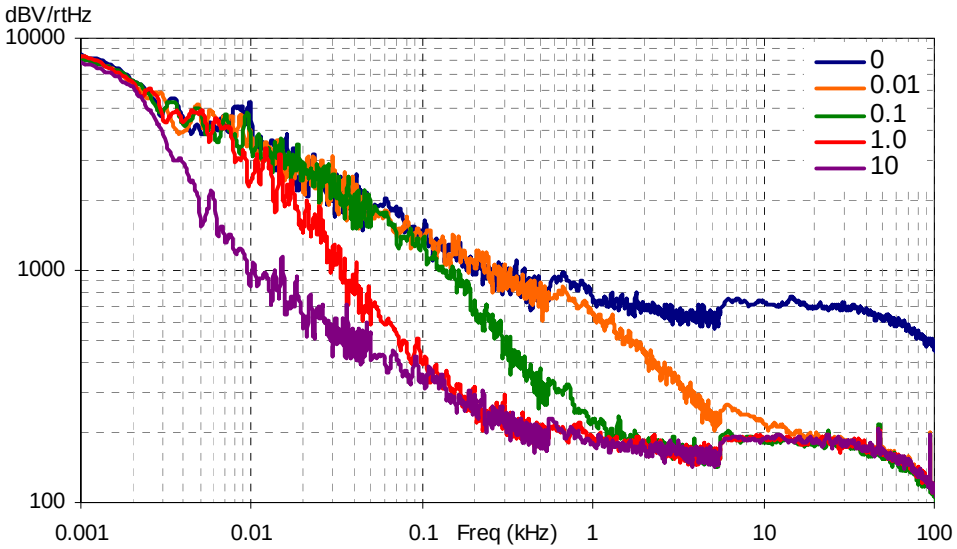
Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling Slew Rate (80% to 20%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 25. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling Slew Rate (80% to 20%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

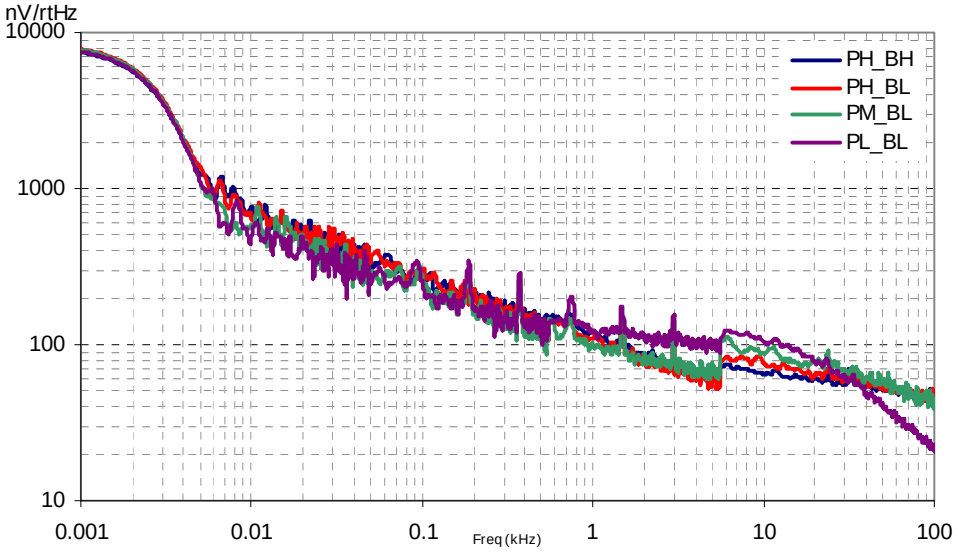
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 kΩ resistance and the external capacitor.

Figure 12. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 13. Typical Opamp Noise



AC Low Power Comparator Specifications

Table 26 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 26. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}

AC Digital Block Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 27. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[15]	–	–	ns	
	Maximum Frequency, No Capture	–	–	50.4[13]	MHz	4.75V ≤ Vdd ≤ 5.25V.
	Maximum Frequency, With Capture	–	–	25.2[13]	MHz	
Counter	Enable Pulse Width	50[15]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	50.4[13]	MHz	4.75V ≤ Vdd ≤ 5.25V.
	Maximum Frequency, Enable Input	–	–	25.2[13]	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[15]	–	–	ns	
	Disable Mode	50[15]	–	–	ns	
	Maximum Frequency	–	–	50.4[13]	MHz	4.75V ≤ Vdd ≤ 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	50.4[13]	MHz	4.75V ≤ Vdd ≤ 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	25.2[13]	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.4[13]	MHz	Maximum data rate is 4.2 Mbps due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.2[13]	MHz	
	Width of SS_ Negated Between Transmissions	50[15]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	25.2[13]	MHz	Maximum baud rate is 3.15 Mbaud due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	50.4[13]	MHz	Maximum baud rate is 6.3 Mbaud due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	25.2[13]	MHz	Maximum baud rate is 3.15 Mbaud due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	50.4[13]	MHz	Maximum baud rate is 6.3 Mbaud due to 8 x over clocking.

Note
15. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 28. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load				
	Power = Low	–	–	2.5	µs
	Power = High	–	–	2.5	µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load				
	Power = Low	–	–	2.2	µs
	Power = High	–	–	2.2	µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load				
	Power = Low	0.65	–	–	V/µs
	Power = High	0.65	–	–	V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load				
	Power = Low	0.65	–	–	V/µs
	Power = High	0.65	–	–	V/µs
BW_{OB}	Small Signal Bandwidth, 20 mV_{pp}, 3dB BW, 100 pF Load				
	Power = Low	0.8	–	–	MHz
	Power = High	0.8	–	–	MHz
BW_{OB}	Large Signal Bandwidth, 1 V_{pp}, 3dB BW, 100 pF Load				
	Power = Low	300	–	–	kHz
	Power = High	300	–	–	kHz

Table 29. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load				
	Power = Low	–	–	3.8	µs
	Power = High	–	–	3.8	µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load				
	Power = Low	–	–	2.6	µs
	Power = High	–	–	2.6	µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load				
	Power = Low	0.5	–	–	V/µs
	Power = High	0.5	–	–	V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load				
	Power = Low	0.5	–	–	V/µs
	Power = High	0.5	–	–	V/µs
BW_{OB}	Small Signal Bandwidth, 20 mV_{pp}, 3dB BW, 100 pF Load				
	Power = Low	0.7	–	–	MHz
	Power = High	0.7	–	–	MHz
BW_{OB}	Large Signal Bandwidth, 1 V_{pp}, 3dB BW, 100 pF Load				
	Power = Low	200	–	–	kHz
	Power = High	200	–	–	kHz

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 30. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

Table 31. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[16]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[17]	0.186	–	24.6	MHz
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

AC Programming Specifications

Table 32 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 32. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	20	–	ms	
T_{WRITE}	Flash Block Write Time	–	20	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6

Notes
16. Maximum CPU frequency is 12 MHz nominal at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
17. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

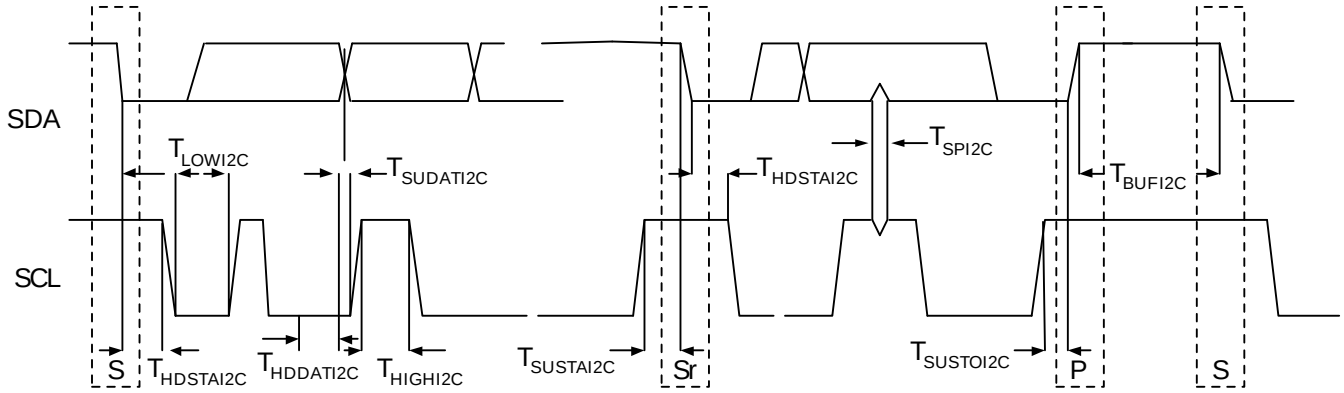
AC I²C Specifications

Table 33 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 33. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100[18]	0	400[18]	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[19]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

18. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
19. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

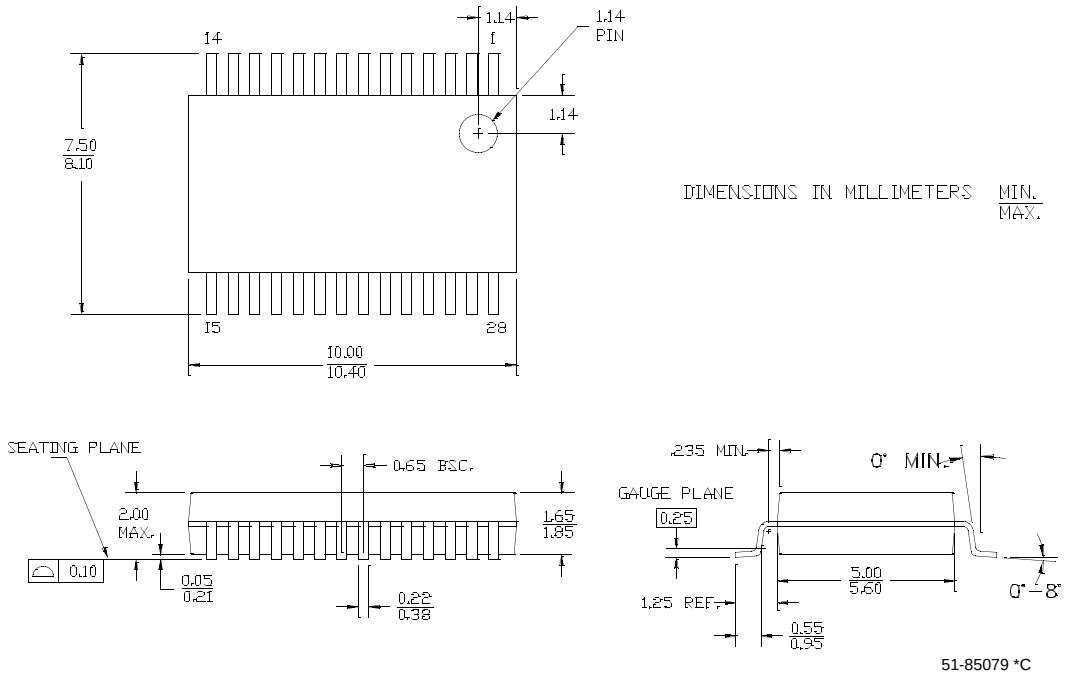
Packaging Information

This section illustrates the packaging specifications for the automotive CY8C24x23A PSoC device, along with the thermal impedances for the package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the drawings at http://www.cypress.com/design/MR10161.

Packaging Dimensions

Figure 15. 28-Pin (210-Mil) SSOP



Thermal Impedances

Table 34. Thermal Impedances per Package

Package	Typical θ_{JA} [20]
28 SSOP	101°C/W

Capacitance on Crystal Pins

Table 35. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 SSOP	2.8 pF

Solder Reflow Peak Temperature

The following table lists the minimum solder reflow peak temperatures to achieve good solderability.

Table 36. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[21]	Maximum Peak Temperature
28 SSOP	240°C	260°C

Notes
20. $T_J = T_A + POWER \times \theta_{JA}$
21. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for the CY8C24x23A family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store (www.cypress.com/shop) also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube Unit
- 28-Pin PDIP Emulation Pod for CY8C29466-24PXI
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Samples (two)
- PSoC Designer Software CD
- ISSP Cable
- MiniEval Socket Programming and Evaluation board
- Backward Compatibility Cable (for connecting to legacy Pods)
- Universal 110/220 Power Supply (12V)
- European Plug Adapter
- USB 2.0 Cable
- Getting Started Guide
- Development Kit Registration form

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store (www.cypress.com/shop) also has the most up to date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-24X23 Evaluation Pod (EvalPod)

PSoC EvalPods are pods that connect to the ICE In-Circuit Emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-24X23 provides evaluation of the CY8C24x23A PSoC device family.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 37. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit[22]	Foot Kit[23]	Adapter[24]
CY8C24423A-24PVXA	28 SSOP	CY3250-24X23A	CY3250-28SSOP-FK	Adapters can be found at http://www.emulation.com.

Third Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Design Resources > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com.

Notes
22. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
23. Foot kit includes surface mount feet that can be soldered to the target PCB.
24. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the automotive CY8C24x23A PSoC device group's key package features and ordering codes.

Table 38. CY8C24423A Automotive PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs[1]	Analog Outputs	XRES Pin
28 Pin (210 Mil) SSOP	CY8C24423A-24PVXA	4K	256	-40°C to +85°C	4	6	24	12	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423A-24PVXAT	4K	256	-40°C to +85°C	4	6	24	12	2	Yes

Ordering Code Definitions

CY 8 C 24 xxx-SPxx

Package Type:
- PX = PDIP Pb-Free
- SX = SOIC Pb-Free
- PVX = SSOP Pb-Free
- LFX/LKX = QFN Pb-Free
- AX = TQFP Pb-Free

Thermal Rating:
- C = Commercial
- I = Industrial
- E = Automotive Extended -40°C to +125°C
- A = Automotive -40°C to +85°C

CPU Speed: 24 MHz

Part Number

Family Code

Technology Code: C = CMOS

Marketing Code: 8 = PSoC

Company ID: CY = Cypress

Document History Page

Document Title: CY8C24423A Automotive PSoC® Programmable System-on-Chip Document Number: 001-52469				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2678061	VIVG/PYRS	03/24/09	New data sheet for Automotive A-Grade
*A	2685606	SHEA	04/08/09	Minor ECN to correct the spec number in Document History.
*B	2702925	BTK	05/06/2009	Post to external web
*C	2742354	BTK/PYRS	07/22/09	Changed title. Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of the Register Reference section to "Registers". Added clarifying comments to some electrical specifications. Updated some figures. Changed T_{RAMP} specification per MASJ input. Fixed all AC specifications to conform to a ±5% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Added a footnote to clarify that 8 of the 12 analog inputs are regular and the other 4 are direct SC block connections. Updated Development Tool Selection section.

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