Timers, Counters, and Display Drivers

Counters, Timers and Display Drivers

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7207 ICM7207A	Frequency counter timebase.	14-Pin DIP 14-Pin DIP	6.5536 MHz 5.2488 MHz	0.01, 0.1, or 1-second count window plus store, reset and MUX.
ICM7208	7-digit unit counter. With addition of 7207 the circuit becomes a complete timer-frequency counter.	28-Pin DIP	—	LED display drive
ICM7211 ICM7212	Four-digit display decoder drivers; ICM7211 is LCD; ICM7212 is LED; Non-multiplexed for low noise, BCD input, decoded display drive output.	40-Pin DIP (plastic)	—	Four-digit, seven-segment direct display drive; LED or LCD
ICM7216 ICM7226	Eight-digit universal counter measures frequency, period, frequency ratio, time interval, units; on-board time base.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	1 or 10 MHz	Eight-digit-common anode or common cathode direct LED drive; BCD output
ICM7217 ICM7227	Four-digit CMOS up/down counter; presettable start/count and compare register; for hard-wired or microprocessor control applications; cascadable.	28-Pin Cerdip or plastic	—	Four-digit, seven-segment common anode or common cathode direct LED display drive; equal, zero, carry/borrow
ICM7218A/D ICM7218E	LED display driver system with 8x8 memory; numeric or dot (1 of 64) decoding; microprocessor compatible.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	—	Eight-digit, seven-segment plus decimal point; common cathode or common anode
ICM7224 ICM7225	4½-digit high speed counter/decoder/driver; 25 MHz typ; ICM7224 is LCD, ICM7225 is LED; direct display drive, cascadable.	40-Pin DIP (plastic)	—	4½-digit seven-segment direct display driver; LED or LCD
ICM7231	8-digit CMOS multiplexed LCD driver. Parallel input.	40-Pin DIP (plastic)	—	Eight-digit, seven-segment plus two flags per digit
ICM7232	10½-digit CMOS multiplexed LCD driver. Serial input.	40-Pin DIP (plastic)	—	10½-digit, seven-segment plus two flags per digit
ICM7233	4-character CMOS multiplexed LCD driver. Parallel alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Four-character, 16-segment plus colon
ICM7234	5-character CMOS multiplexed LCD driver. Serial alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Five-character, 16-segment plus colon
ICM7235/A	4-digit CMOS decoder/driver for direct drive vacuum fluorescent displays. BCD input.	40-Pin DIP (plastic)	—	Four-digit, seven-segment, vacuum fluorescent display drive; either HEX or CODE B
ICM7235M/AM	Same as above but microprocessor compatible.			
ICM7236	4½-digit high speed CMOS counter/decoder/driver for vacuum fluorescent displays; 25 MHz typ. counting speed.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7236A	Same as above but counting to 15959.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7240 ICM7250 ICM7260	Programmable CMOS counter/timers using external RC time base. Programmable from μs to years.	16-Pin DIP	External	Timed output
ICM7242	Fixed CMOS counter/timer. Uses external RC time base; sequence timing from μs to minutes.	8-Pin DIP	External	Timed output
ICM7243	8-character multiplexed LED display driver with alphanumeric (6-bit ASCII) input.	40-Pin Cerdip	—	Eight-character, 14/16-segment common cathode alphanumeric LED display drive
ICM7281	LCD Dot Matrix Column Driver	40-Pin DIP	—	Up to 256 x 256 dots
ICM7555 ICM7556	Single or dual CMOS version of industry-standard 555 timer; 80 μA typ. supply current; 500 kHz guaranteed; 2-18V power supply.	8-Pin DIP 14-Pin DIP	—	

ICM7207/A CMOS Oscillator Controller

FEATURES

- Stable HF oscillator
- Low power dissipation ≤ 5mW with 5 volt supply
- Counter chain has outputs at $\div 2^{12}$ and $\div 2^n$ or $\div (2^n \times 10)$; n = 17 for 7207, and 20 for 7207A
- Low impedance output drivers ≤100 ohms
- Count windows of 10/100ms (7207 with 6.5536MHz crystal) or 0.1/1 sec. (7207A with 5.24288MHz crystal)

APPLICATIONS

- System timebases
- Oscilloscope calibration generators
- Marker generator strobes
- Frequency counter controllers

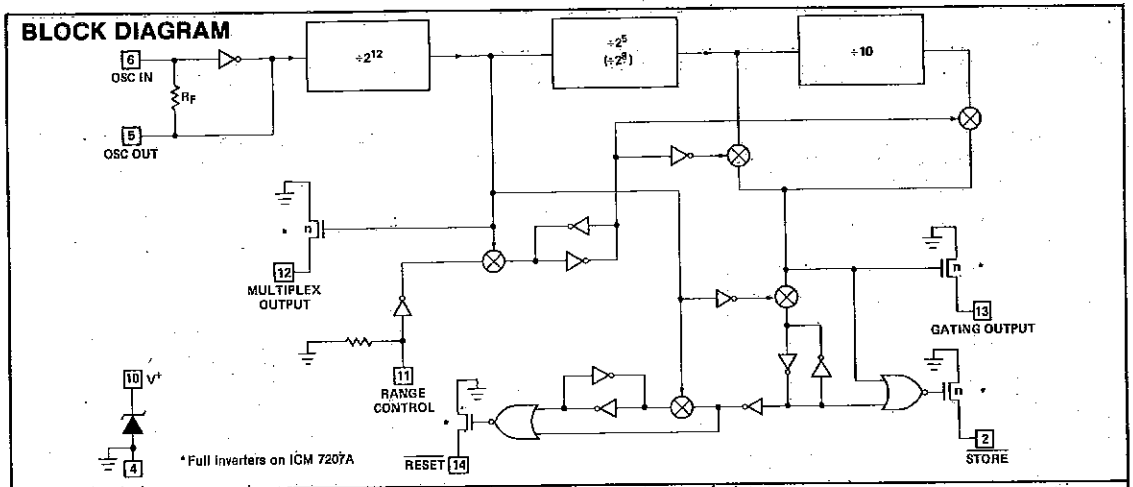
DESCRIPTION

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts at which the typical dissipation is less than 2mW using an oscillator frequency of 6.5536MHz (5.24288MHz).

In the 7207/A the GATING output, $\overline{\text{RESET}}$, and the MULTIPLEX output provide both pull up and pull down, eliminating the need for 3 external resistors; although, buffering must be provided if interfacing with T^2L is required.

BLOCK DIAGRAM



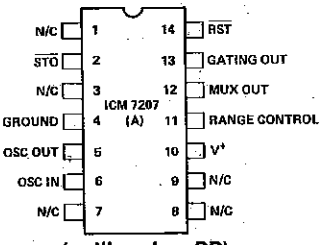
ORDERING INFORMATION

PART	PACKAGE	ORDER NUMBER
ICM7207	14-Pin DIP	ICM7207IPD
	DICE	ICM7207/D
	EV/Kit*	ICM7207EV/Kit
ICM7207A	14-Pin DIP	ICM7207AIPD
	DICE	ICM7207A/D
	EV/Kit*	ICM7207AEV/Kit

Temperature Range on packaged parts is −20°C to +85°C

*These EV/Kits contain just the IC and the corresponding crystal. The ICM7207A is also used in the 4½-Digit Counter/Driver kits, the ICM7224 EV/Kit, ICM7225 EV/Kit, and ICM7236 EV/Kit, which include several ICs, a crystal, PC board, and some passive components.

PIN CONFIGURATION



(outline dwg PD)

6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.0V
Input Voltages ..... Equal to or less than supply voltage
Output Voltages (7207) .... Not more positive than +6V with respect to GROUND
(7207A) ..... V^+ to V^-
Output Currents 25mA
Power Dissipation @ 25°C Note 1 ..... 200mW
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

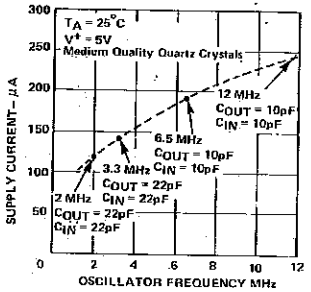
TEST CONDITIONS: f_{OSC} = 6.5536MHz(7207), 5.24288MHz(7207A), V^+ = 5V, T_A = 25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V^+	-20°C to +85°C	4		5.5	V
Supply Current	I^+	All outputs open circuit		260	1000	μA
Output on Resistances	$r_{ds(on)}$	Output current = 5mA All outputs		50	120	Ω
Output Leakage Currents	I_{OLK}	All outputs (STORE only)			50	μA
(Output Resistance Terminals 12,13,14)	(R_{OUT})	Output current = 50μA, 7207A only			33K	Ω
Input Pulldown Current	I_{pd}	Terminal 11 connected to V^+		50	200	μA
Input Noise Immunity			25			% supply voltage
Oscillator Frequency Range	f_{osc}	Note 2	2		10	MHz
Oscillator Stability	f_{STAB}	$C_{IN} = C_{OUT}$ = 22pF		0.2	1.0	ppm/V
Oscillator Feedback Resistance	r_{OSC}	Quartz crystal open circuit Note 3	3			MΩ

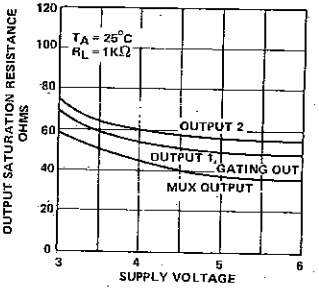
NOTE 2: Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.

NOTE 3: The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

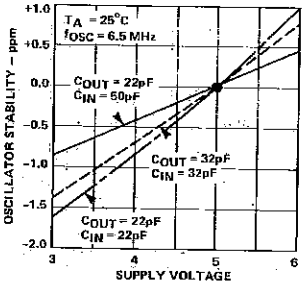
SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



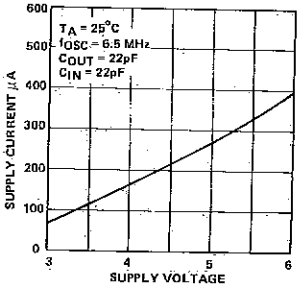
OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

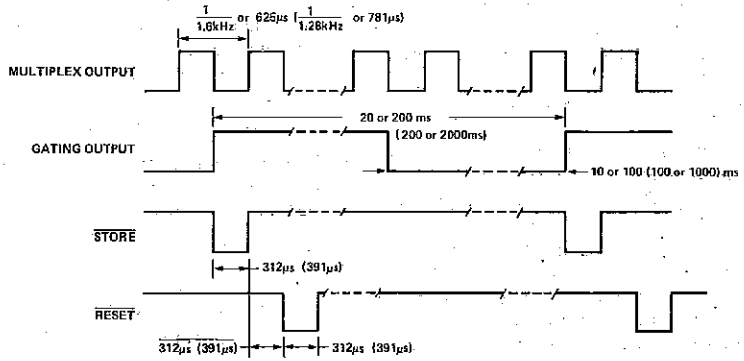


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



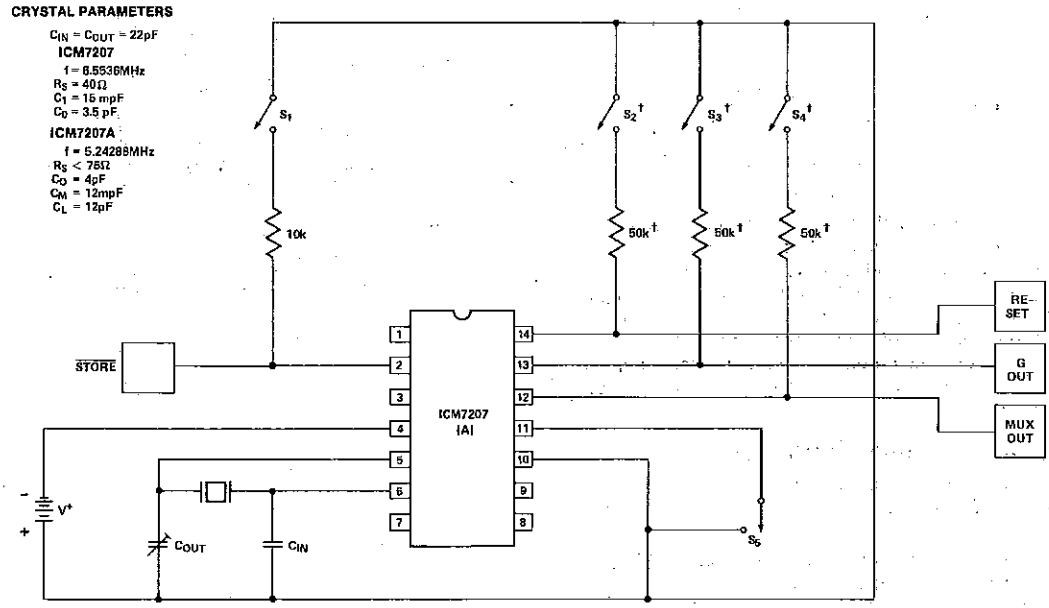
OUTPUT TIMING WAVEFORMS 7207 (7207A)

Crystal Frequency = 6.5536 (5.24288) MHz



Referring to the test circuit, the crystal oscillator frequency is divided by 2^{12} to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to V^+ or GROUND (open circuit).

TEST CIRCUIT



SWITCHES S_1, S_2, S_3, S_4 OPEN CIRCUIT FOR SUPPLY CURRENT MEASUREMENT.
SWITCH S_5 OPEN CIRCUIT FOR SLOW GATING PERIOD.

† SWITCHES S_2, S_3, S_4 and 50k RESISTORS ARE NOT NEEDED WHEN USING THE ICM7207A.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

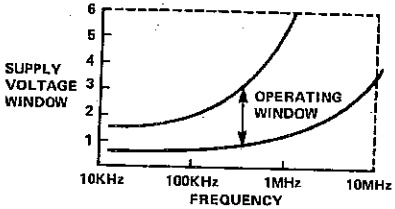
It is recommended that the crystal load capacitance (C_L) be no greater than 15pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10 ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05 ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.



For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet.

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet, and app note A015. Other frequency counters using the ICM7207/A can be constructed using the ICM7224, ICM7225, and ICM7236, for LCD, LED and VF displays. The latter are available as EV/Kits also.

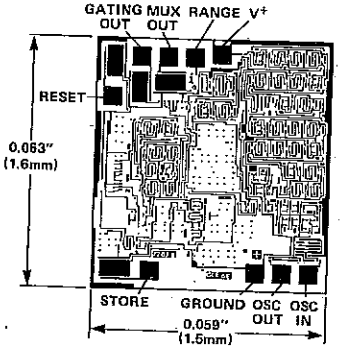
The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

QUARTZ CRYSTAL MANUFACTURERS

The following list of possible suppliers is intended to be of assistance in putting a design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Intersil.

a) CTS Knights, Sandwich, Illinois, (815) 786-8411
b) Motorola Inc., Franklin Park, Illinois (312) 451-1000
c) Sentry Manufacturing Co., Chickasaw, Oklahoma (405) 224-6780
d) Tyco Filters Division, Phoenix, Arizona (602) 272-7945
e) M-Tron Inds., Yankton, South Dakota (605) 665-9321
f) Saronix, Palo Alto, California (415) 856-6900

CHIP TOPOGRAPHY



Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

ICM7208
CMOS
7 Decade Counter

FEATURES
- Low operating power dissipation < 10mW
- Low quiescent power dissipation < 5mW
- Counts and displays 7 decades
- Wide operating supply voltage range
  $2V \leq V^{+} \leq 6V$
- Drives directly 7 decade multiplexed common cathode LED display
- Internal store capability
- Internal inhibit to counter input
- Test speedup point
- All terminals protected against static discharge

DESCRIPTION
The ICM7208 is a fully integrated seven decade counter-decoder-driver and is manufactured using Intersil's low voltage metal gate C-MOS process.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

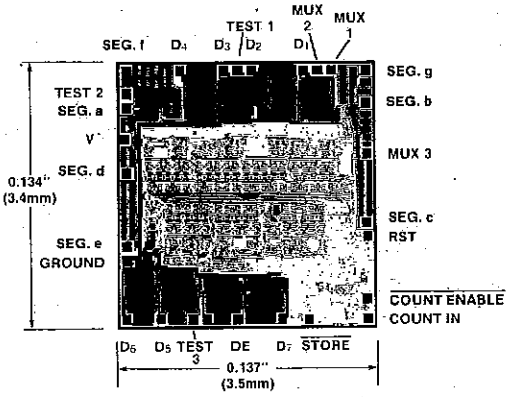
The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signal gating.

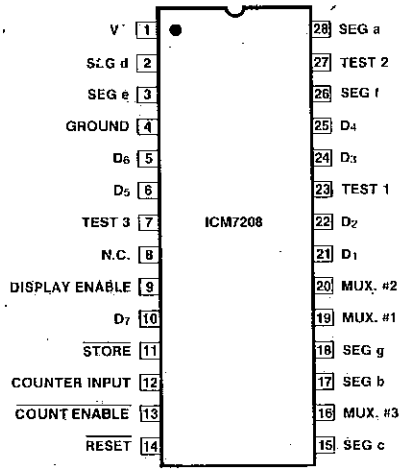
ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	28 LEAD PACKAGE
ICM7208IPI	-20°C to +85°C	PLASTIC
ORDER DICE BY FOLLOWING PART NUMBER: ICM7208D		

CHIP TOPOGRAPHY



PIN CONFIGURATION (OUTLINE DRAWING PI)



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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 1 W
Supply voltage (Note 2) 6V
Output digit drive current (Note 3) 150mA
Output segment drive current ..... 30 mA
Input voltage range (any input terminal) (Note 2) ... Not to exceed the supply voltage
Operating temperature range ..... -20°C to +85°C
Storage temperature range ..... -55°C to +125°C
Lead temperature (soldering, 10 seconds) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATION CHARACTERISTICS

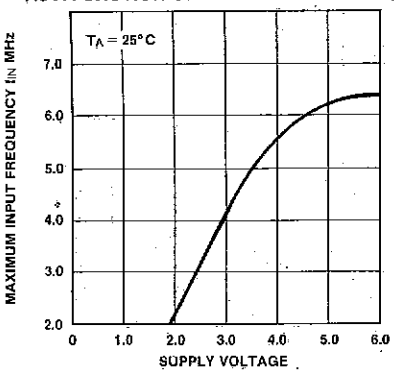
TEST CONDITIONS: (V^+ = 5V, T_A = 25°C, TEST CIRCUIT, display off, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I_Q	All controls plus terminal 19 connected to V^+ No multiplex oscillator		30	300	μA
Quiescent Current	I_Q	All control inputs plus terminal 19 connected to V^+ except STORE which is connected to GROUND		70	350	
Operating Supply Current	I^+	All inputs connected to V^+, RC multiplexer osc operating $f_{in} \leq 25KHz$		210	500	
Operating Supply Current	I^+	$f_{in} = 2MHz$			700	
Supply Voltage Range	V^+	$f_{in} \leq 2MHz$	3.5		5.5	V
Digit Driver On Resistance	r_{DIG}			4	12	Ω
Digit Driver Leakage Current	I_{DIG}				500	μA
Segment Driver On Resistance	r_{SEG}			40		Ω
Segment Driver Leakage Current	I_{SLK}				500	μA
Pullup Resistance of RESET or STORE Inputs	R_p		100	400		kΩ
COUNTER INPUT Resistance	R_{IN}	Terminal 12 either at V^+ or GROUND			100	
COUNTER INPUT Hysteresis Voltage	V_{HIN}			25	50	mV

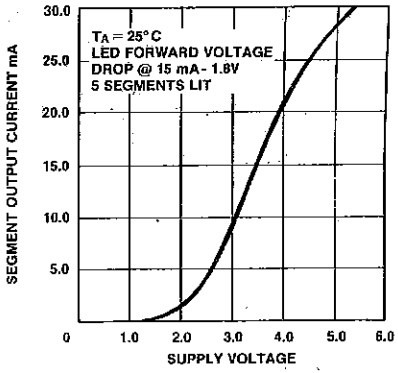
NOTE 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
NOTE 2: The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.
NOTE 3: The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

TYPICAL PERFORMANCE CHARACTERISTICS

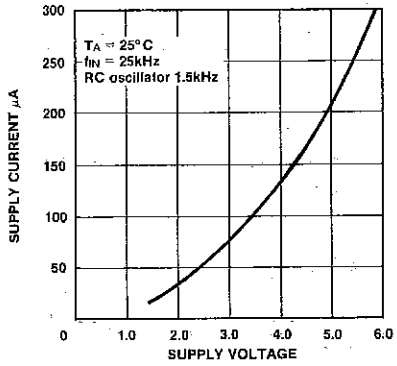
MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



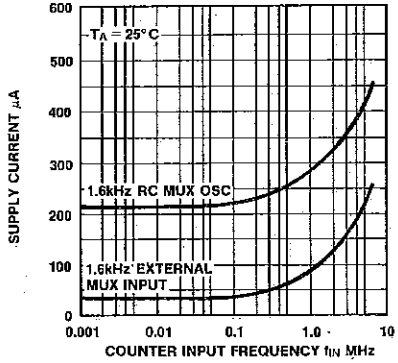
SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY



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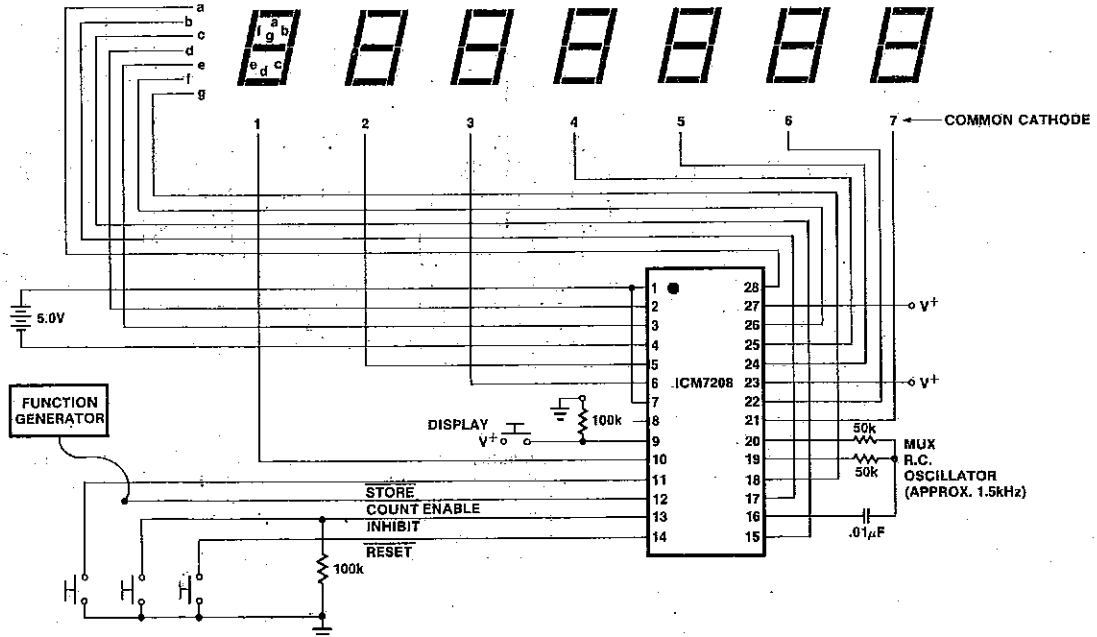
TEST CIRCUIT



TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

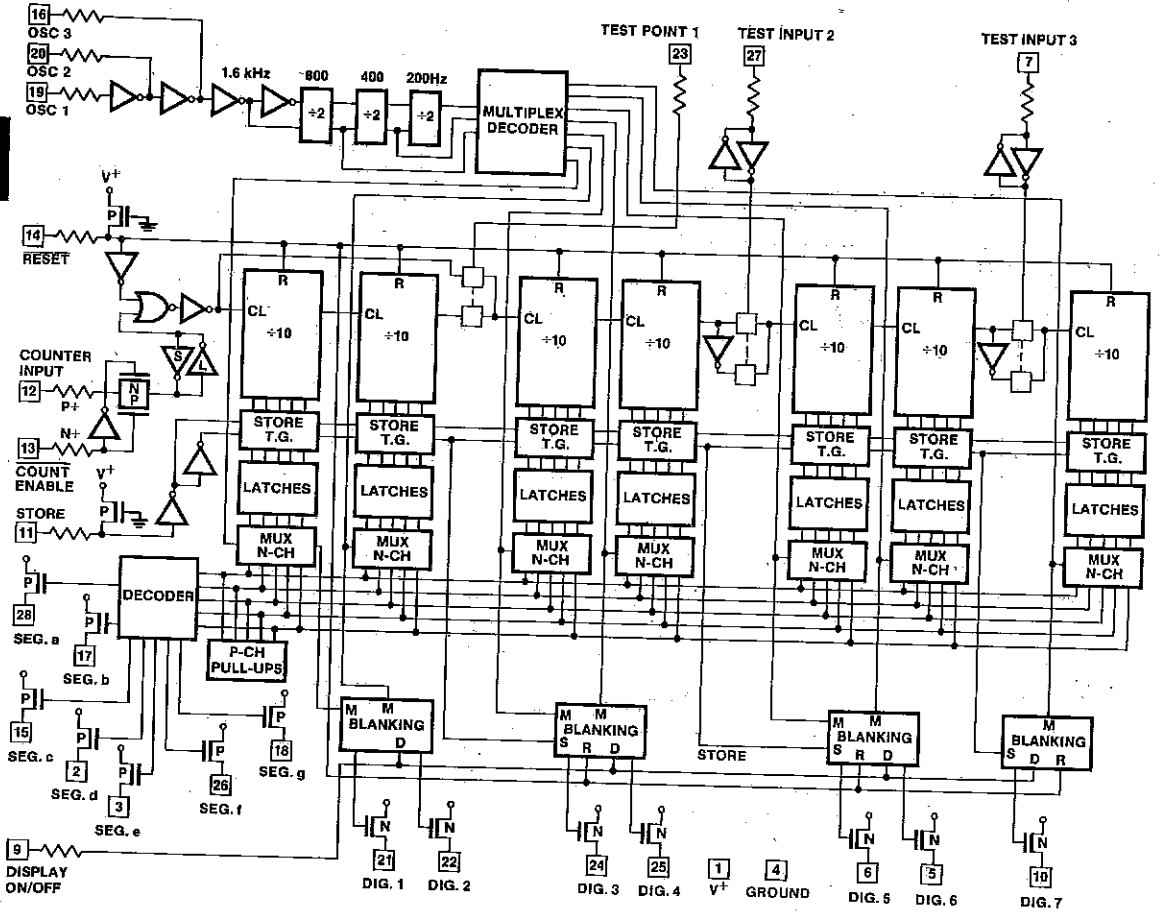
CONTROL INPUT DEFINITIONS

INPUT	TERMINAL	VOLTAGE	FUNCTION
1. DISPLAY	9	V^+	Display On
		Ground	Display Off
2. STORE	11	V^+	Counter Information Latched
		Ground	Counter Information Transferring
3. ENABLE	13	V^+	Input to Counter Blocked
		Ground	Normal Operation
4. RESET	14	V^+	Normal Operation
		Ground	Counters Reset

COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

BLOCK DIAGRAM



APPLICATION NOTES

1. Format of Signal to be Counted

The noise immunity of the COUNTER INPUT Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply. **NOTE: The amplitude of the input signal should not exceed the supply; otherwise, damage may be done to the circuit.**

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately 10-4V/μsec at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

When driving the input of the ICM7208 from TTL, a 1k-5k ohm pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

2. Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit current exceed 150 mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with 500μA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

3. Display Multiplex Rate

The ICM7208 has approximately 0.5μs overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input.

4. Unit Counter

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.

For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

Figure 1 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4 x 1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

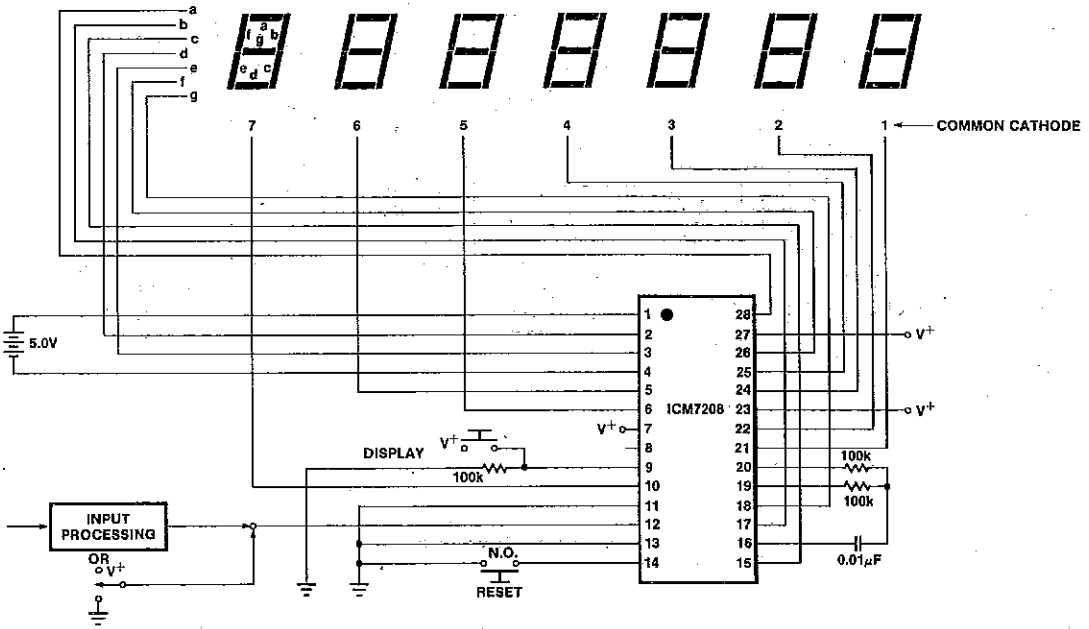


Figure 1: Schematic Unit Counter

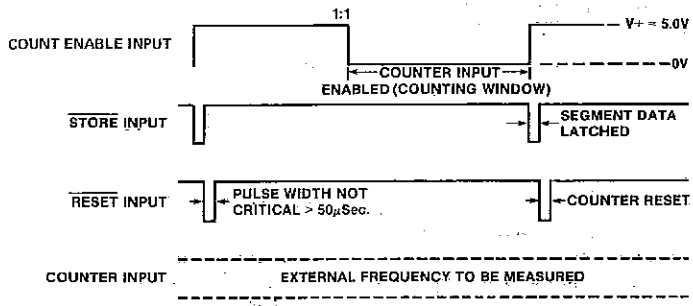


Figure 3: Frequency Counter Input Waveforms

6. Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure 5 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 4.

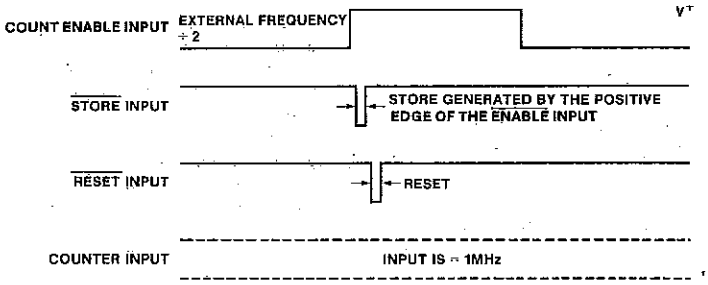


Figure 4: Period Counter Input Waveforms

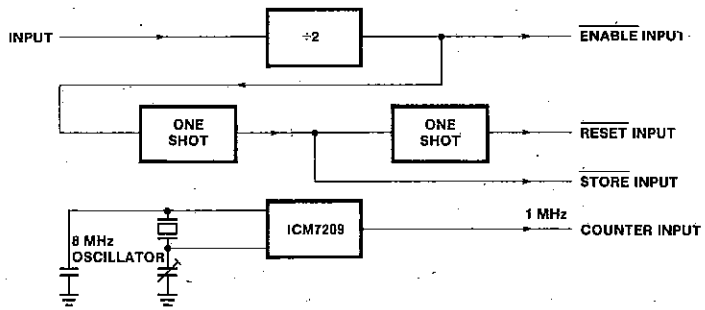


Figure 5: Period Counter Input Generator

ICM7211 (LCD)
ICM7212 (LED)
Four Digit CMOS Display Decoder/Drivers

ICM7211 (LCD) FEATURES

- **Four digit non-multiplexed 7 segment LCD display outputs with backplane driver**
- **Complete onboard RC oscillator to generate backplane frequency**
- **Backplane input/output allows simple synchronization of slave-device segment outputs to a master backplane signal**
- **ICM7211 devices provide separate Digit Select inputs to accept multiplexed BCD input (Pinout and functionally compatible with Siliconix DF411)**
- **ICM7211M devices provide data and digit select code input latches controlled by $\overline{\text{Chip Select}}$ inputs to provide a direct high speed processor interface**
- **ICM7211 decodes binary hexadecimal; ICM7211A decodes binary to Code B (0-9, dash, E, H, L, P, blank)**

ICM7212 (LED) FEATURES

- **28 current-limited segment outputs provide 4-digit non-multiplexed direct LED drive at > 5mA per segment.**
- **Brightness input allows direct control of LED segment current with a single potentiometer. Can function digitally as a display enable.**
- **ICM7212M and ICM7212A devices provide same input configuration and output decoding options as the ICM7211.**

DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs. These outputs provide the zero d.c. component signals necessary for long display life.

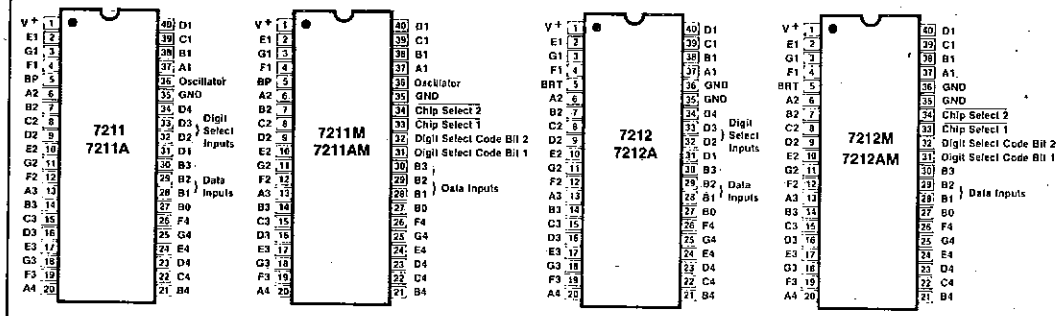
The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled low leakage open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with two input configurations. The basic devices provide four data-Bit inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL71C03. The microprocessor interface (suffix M) devices provide data input latches and Digit Select code latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

PIN CONFIGURATIONS (OUTLINE DRAWING PL)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 70°C
Supply Voltage 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, GROUND −0.3V
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.
NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

TEST CONDITIONS: All parameters measured with $V^+ = 5V$ unless otherwise specified.

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{op}	Test circuit, Display blank		10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36		±2	±10	
Segment Rise/Fall Time	t_{rfs}	C_L = 200pF		0.5		µs
Backplane Rise/Fall Time	t_{rfb}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{osc}	Pin 36 Floating		19		kHz
Backplane Frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

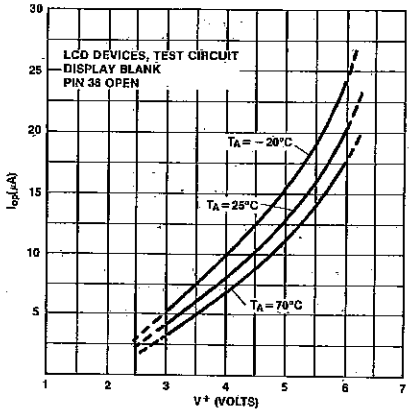
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{op}	Pin 5 (Brightness), Pins 27-34 - GROUND		10	50	µA
Operating Current	I_{op}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment On Current	I_{SEG}	Segment On, V_O = +3V	5	8		mA

INPUT CHARACTERISTICS

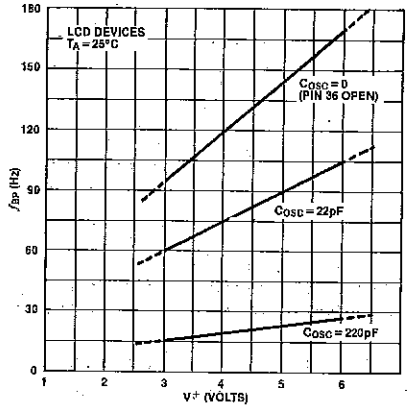
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				2	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	µA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	µA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			
Inter-Digit Select Time	t_{ids}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
$\overline{\text{Chip Select}}$ Active Pulse Width	t_{csa}	other $\overline{\text{Chip Select}}$ either held active, or both driven together	200			ns
Data Setup Time	t_{ds}		100			
Data Hold Time	t_{dh}		10	0		
Inter-$\overline{\text{Chip Select}}$ Time	t_{ics}		2			µs

TYPICAL CHARACTERISTICS

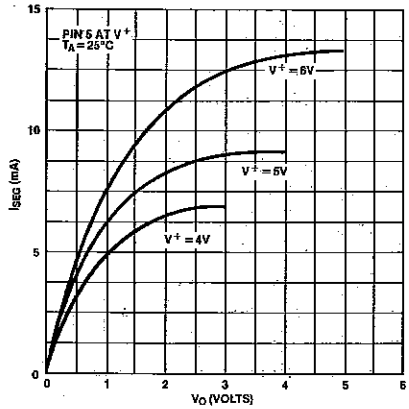
ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



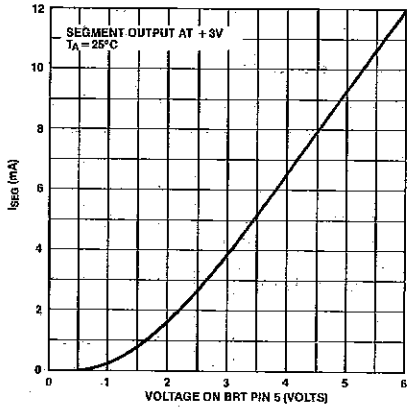
ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



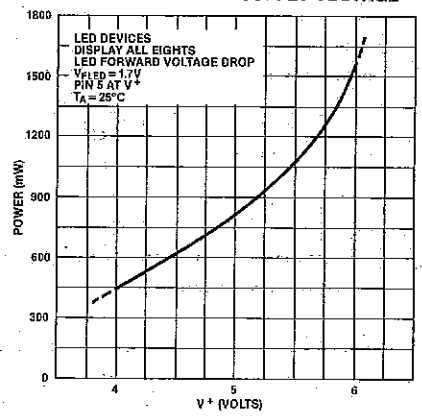
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



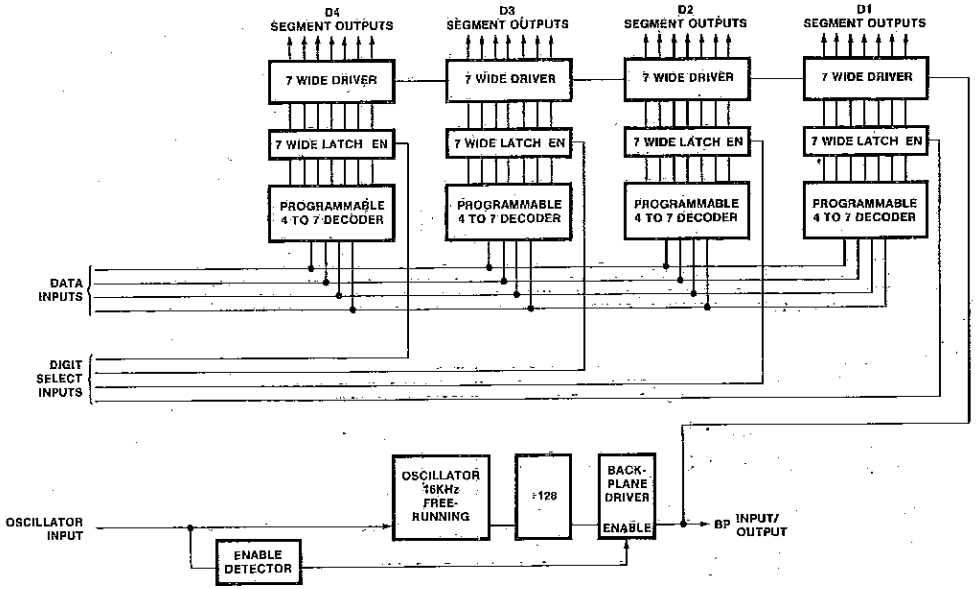
ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



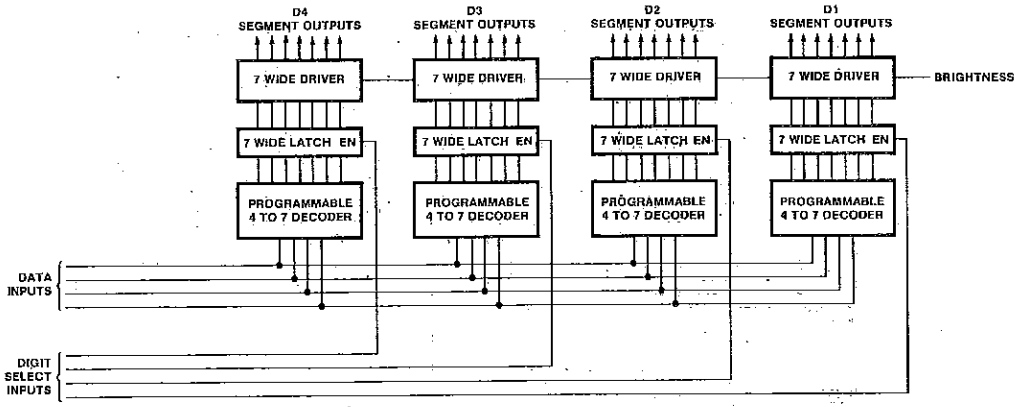
6

BLOCK DIAGRAMS

ICM7211 (A)



ICM7212 (A)



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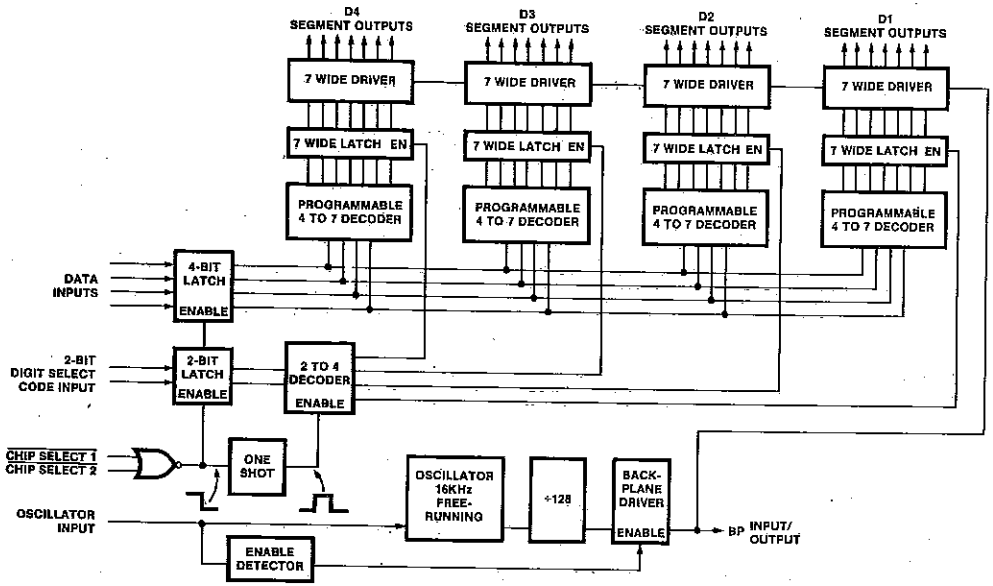
ICM7211(A)M



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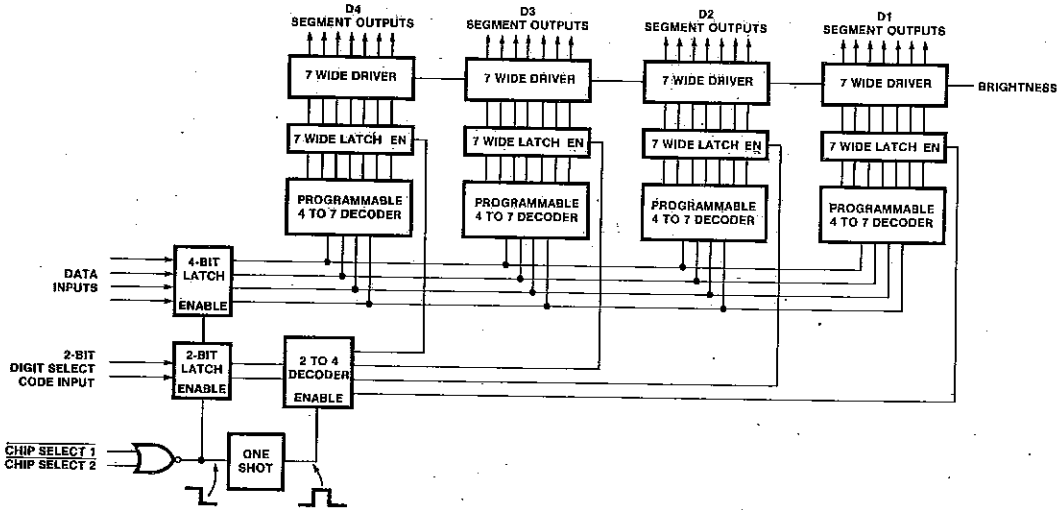
ICM7212(A)M



INPUT DEFINITIONS

In this table, V^+ and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One GND = Logical Zero	Twos	
B2	29	V^+ = Logical One GND = Logical Zero	Fours	
B3	30	V^+ = Logical One GND = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V^+ GROUND	Oscillator input Disables BP output devices, allowing segments to be synced to an external signal input at the BP terminal (Pin 5)	

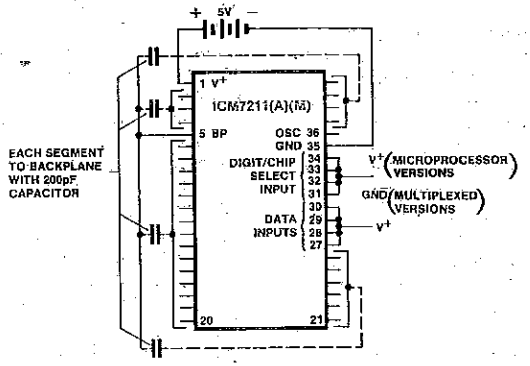
ICM7211/ICM7212
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active GND = Inactive	D1 (Least significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most significant) Digit Select

ICM7211M/ICM7212M
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One GND = Logical Zero	DS1 & DS2 serve as a two bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V^+ = Inactive GND = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

TEST CIRCUIT



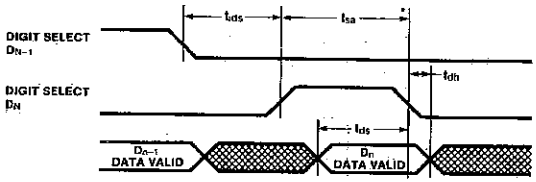


Figure 1: Multiplexed Input Timing Diagram

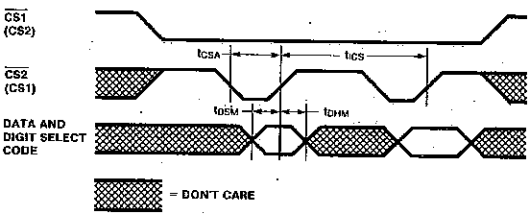


Figure 2: Microprocessor Interface Input Timing Diagram

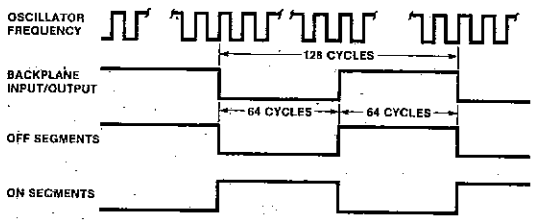
DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit by seven-segment LCD displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to GrouND. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment), thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits; and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters (rise and fall times not exceeding 5μs. ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very



Display Waveforms

large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V^+.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above GrouND). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit by seven-segment common-anode LED displays, including 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100KΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED devices have two connections for GrouND; both of these pins should be connected. The

double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (–15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})\ (I_{SEG})\ (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRIghTness input to keep power dissipation within the limits described above.

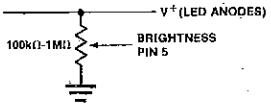


Figure 3: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211M, ICM7212, and ICM7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AM decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E. H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Fig (1) and under Operating Characteristics for data setup, hold, and inter-digit select times must be met to ensure correct output.

The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit select code latches.

A select code of 00 writes into D4, DS2 = 0, DS1 = 1 writes into D3, DS2 = 1, DS1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Fig (2), and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

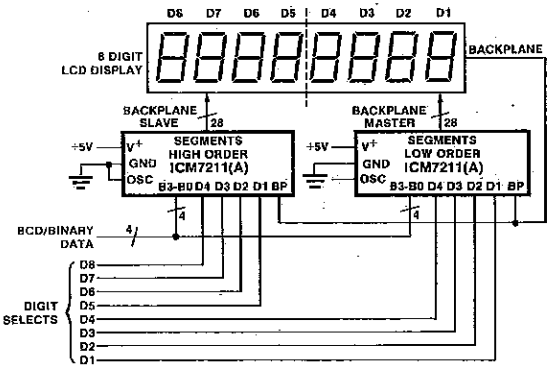
Table 1: Output Codes

BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

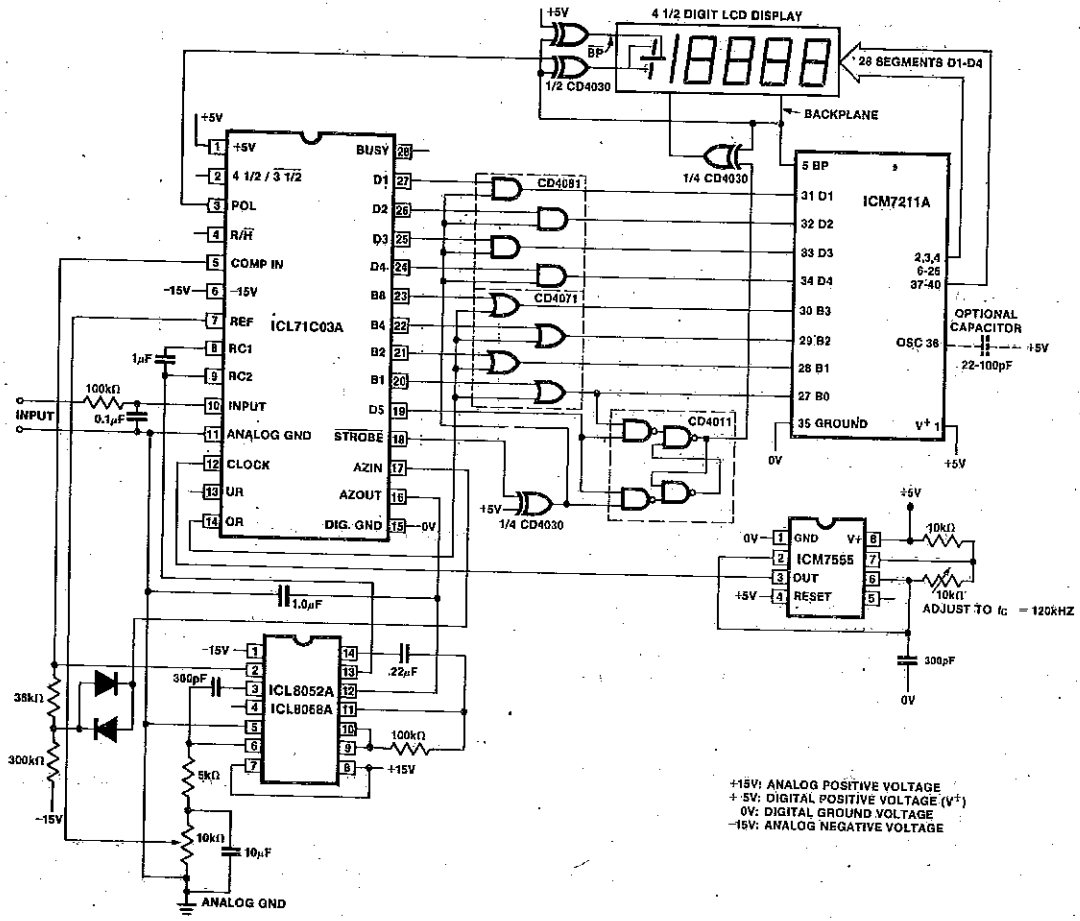
SEGMENT ASSIGNMENT

APPLICATIONS

1. Ganged ICM7211's Driving 8-Digit LCD Display.

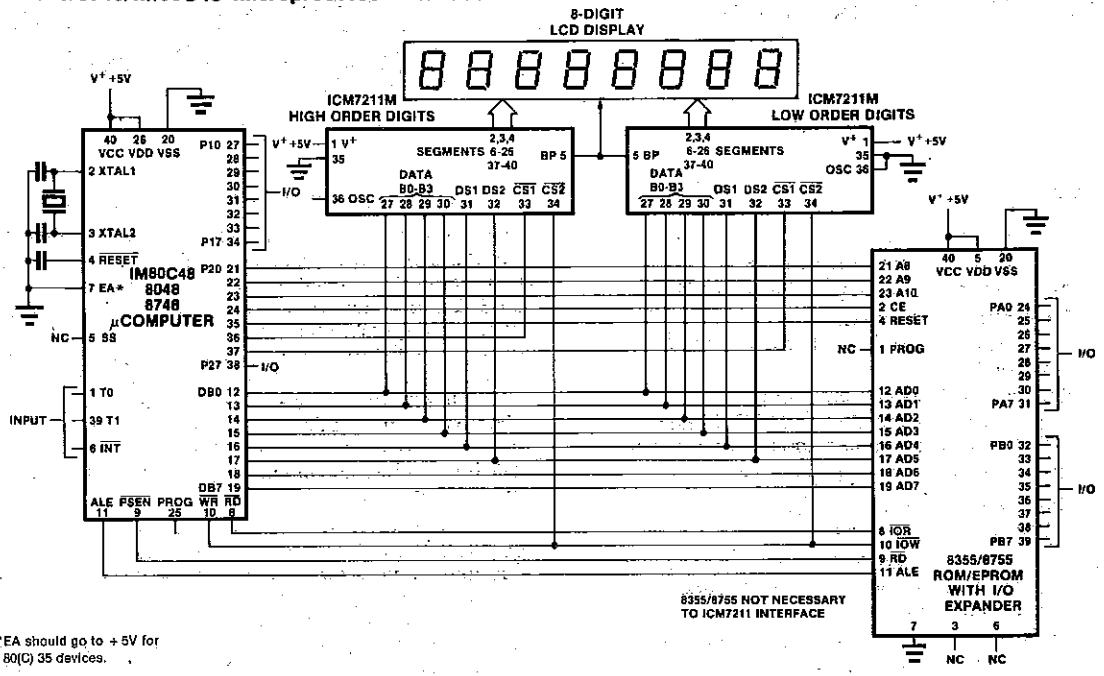


2. 4 1/2 Digit LCD DPM with Digit Blanking on Overrange.



NOTE: See also ICL8052/ICL8068/ICL71C03 and ICL7135 Data Sheets for similar circuits with fewer features.

3. 8048/8748/IM80C48 Microprocessor Interface.



*EA should go to + 5V for 80(C) 35 devices.

ORDERING INFORMATION

ORDER PART NUMBER		OUTPUT CODE	INPUT CONFIGURATIONS
LCD DISPLAY	ICM7211 IPL ICM7211A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT
	ICM7211M IPL ICM7211AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE
LED DISPLAY	ICM7212 IPL ICM7212A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT
	ICM7212M IPL ICM7212AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE

Evaluation Kits are also available. Order ICM7211 EV/Kit or ICM7212 EV/Kit.

ICM7216A/B/C/D 10 MHz Universal/ Frequency Counters

FEATURES

ALL VERSIONS:

- **Functions as a frequency counter. Measures frequencies from DC to 10 MHz**
- **Four internal gate times: 0.01 sec, 0.1 sec, 1 sec, 10 sec in frequency counter mode**
- **Output directly drives digits and segments of large multiplexed LED displays. Common anode and common cathode versions**
- **Single nominal 5V supply required**
- **Stable high frequency oscillator, uses either 1 MHz or 10 MHz crystal**
- **Internally generated decimal points, interdigit blanking, leading zero blanking and overflow indication**
- **Display Off mode turns off display and puts chip into low power mode**
- **Hold and Reset inputs for additional flexibility**

ICM7216A AND B

- **Functions also as a period counter, unit counter, frequency ratio counter or time interval counter**
- **1 cycle, 10 cycles, 100 cycles, 1000 cycles in period, frequency ratio and time interval modes**
- **Measures period from 0.5μs to 10s**

ICM7216C AND D

- **Decimal point and leading zero blanking may be externally selected**

6

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Universal Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1 Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in μsec. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

ORDERING INFORMATION

Universal Counter; Common Anode LED	**ICM 7216 A**	**IJI**
Universal Counter; Common Cathode LED	**ICM 7216 B**	**IPI**
Frequency Counter; Common Anode LED	**ICM 7216 C**	**IJI**
Frequency Counter; Common Cathode LED	**ICM 7216 D**	**IPI**

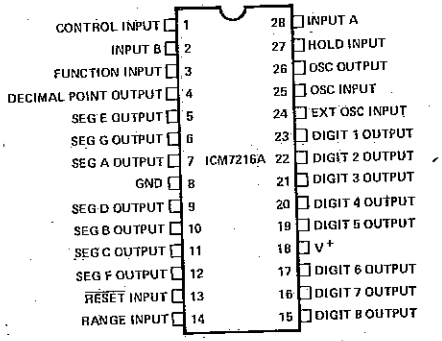
Evaluation Kit:
Use ICM7226 EV/Kit

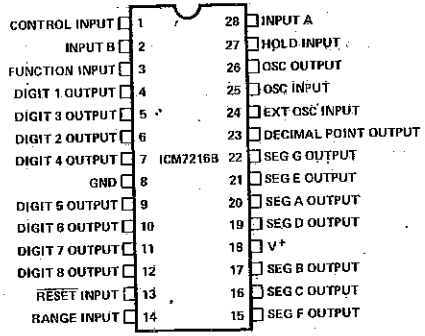
ICM 7216 D IPI

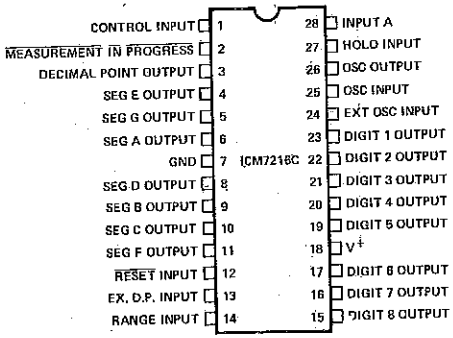
- **ICM 7216 D** — Type
- **IPI** — Package: JI — 28 pin CERDIP; PI — 28 pin PLASTIC DIP
- **IPI** — Temperature Range -20°C to +85°C

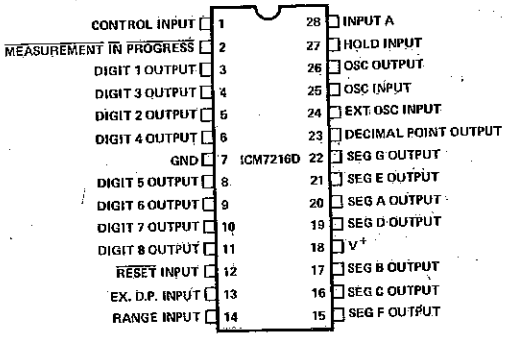
ICM7216

PIN CONFIGURATIONS (outline dwgs JI, PI)









EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIJL (Common Anode LED Display), a 10MHz quartz crystal, eight 7 segment 0.3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or Output Terminal[1] ..... $V^+ + 0.3V$ to $-0.3V$
Maximum Power Dissipation at 70°C ..... 1.0 W (ICM7216A & C) 0.5W (ICM7216B & D)
Lead Temperature (Soldering, 10 sec) ..... 300°C
Maximum Operating Temperature Range ..... −20°C to +85°C
Maximum Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ to GND by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216A/B						
Operating Supply Current	I^+	Display Off, Unused Inputs to GND		2	5	mA
Supply Voltage Range	V^+	$-20°C < T_A < +85°C$, INPUT A, INPUT B Frequency at f_{max}	4.75		6.0	V
Maximum Frequency INPUT A, Pin 28	$f_{A(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$, Figure 1, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5			 MHz MHz
Maximum Frequency INPUT B, Pin 2	$f_{B(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$, Figure 2	2.5			MHz
Minimum Separation INPUT A to INPUT B Time Interval Function		$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$, Figure 3	250			ns
Maximum Osc. Freq. and Ext. Osc. Frequency	f_{osc}	$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$	10			MHz
Minimum Ext. Osc. Freq.	f_{osc}				100	kHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$, $T_A = +85°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		ms
Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage	 V_{INL} V_{INH}	$-20°C < T_A < +85°C$	 3.5		 1.0	 V V
Input Resistance to V^+ Pins 13,24	R_{IN}	$V_{IN} = V^+ - 1.0V$	100	400		kΩ
Input Leakage Pin 27,28,2	I_{ILK}				20	μA
Minimum Input Rate of Change	dV_{IN}/dt	Supplies Well Bypassed		15		mV/μs
ICM7216A						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	 I_{OH} I_{OL}	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = +1.0V$	 -140	 -180 +0.3		 mA mA
SEGment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = +1.5V$ $V_{OUT} = V^+ - 2.5V$	 20	 35 -100		 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to GROUND	 V_{INL} V_{INH} R_{IN}	 $V_{IN} = +1.0V$	 2.0 50	 100	 0.8	 V V kΩ
ICM7216B						
Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = +1.3V$ $V_{OUT} = V^+ - 2.5V$	 50	 75 -100		 mA μA
SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	 I_{OH} I_{SLK}	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	 -10		 10	 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V^+	 V_{INL} V_{INH} R_{IN}	 $V_{IN} = V^+ - 1.0V$	 $V^+ - 0.8$ 200	 360	 $V^+ - 2.0$	 V V kΩ

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP	MAX.	UNITS
ICM7216C/D						
Operating Supply Current	I^+	Display Off, Unused Inputs to GND		2	5	mA
Supply Voltage Range		$-20°C < T_A < +85°C$, INPUT A Frequency at f_{max}	4.75		6.0	V
Maximum Frequency INPUT A, Pin 28	$f_{A(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ < 6.0V$, Figure 1	10			MHz
Maximum Osc. Freq and Ext. Osc. Frequency	f_{osc}	$-20°C < T_A < +85°C$ $4.75 < V^+ < 6.0V$	10			MHz
Minimum Ext. Osc. Freq.	f_{osc}				100	kHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$, $T_A = +85°C$	2000			µmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		ms
Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage	V_{INL} V_{INH}	$-20°C < T_A < +85°C$	 3.5		1.0	V V
Input Resistance to V^+ Pins 12,24	R_{IN}	$V_{IN} = V^+ - 1.0V$	100	400		kΩ
Input Leakage Pin 27, Pin 28	I_{ILK}				20	µA
Output Current Pin 2	I_{OL}	$V_{OL} = +.4V$	0.36			mA
	I_{OH}	$V_{OH} = V^+ - .8V$	265			µA
Minimum Input Rate of Change	dV_{IN}/dt	Supplies Well Bypassed		15		mV/µs
ICM7216C						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	I_{OH} I_{OL}	$V_{OUT} = V^+ - 2.0V$ $V_{OUT} = 1.0V$	-140	-180 0.3		mA mA
SEGment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	I_{OL} I_{OH}	$V_{OUT} = +1.5V$ $V_{OUT} = V^+ - 2.5V$	20	30 -100		mA µA
Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to GROUND	V_{INL} V_{INH} R_{IN}	$V_{IN} = +1.0V$	 2.0 50	 100	0.8	V V kΩ
ICM7216D						
Digit Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	I_{OL} I_{OH}	$V_{OUT} = +1.3V$ $V_{OUT} = V^+ - 2.5V$	50	75 100		mA µA
SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	I_{OH} I_{SLK}	$V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	10	15	 10	mA µA
Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V^+	V_{INL} V_{INH} R_{IN}	$V_{IN} = V^+ - 1.0V$	 $V^+ - 0.8$ 200	 360	$V^+ - 2.0$	V V kΩ

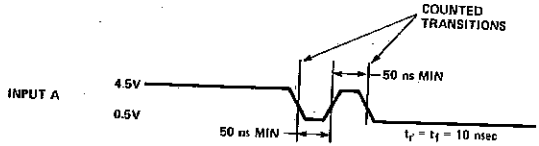


FIGURE 1. Waveform for Guaranteed Minimum $f_{A(max)}$ Function = Frequency, Frequency Ratio, Unit Counter.

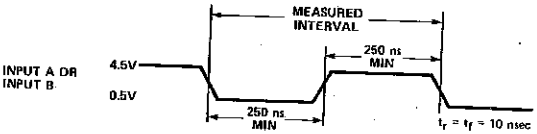


FIGURE 2. Waveform for Guaranteed Minimum $f_{B(max)}$ and $f_{A(max)}$ for Function = Period and Time Interval.

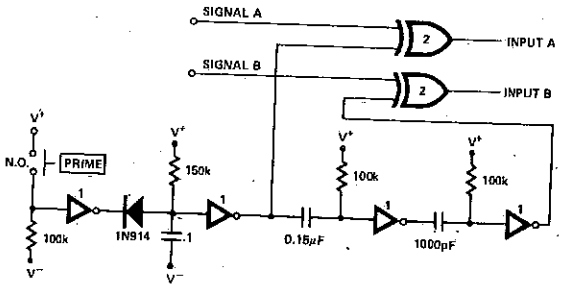
TIME INTERVAL MEASUREMENT

The ICM7216A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7216A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can be easily accomplished with the following circuit: (Figure 3b).



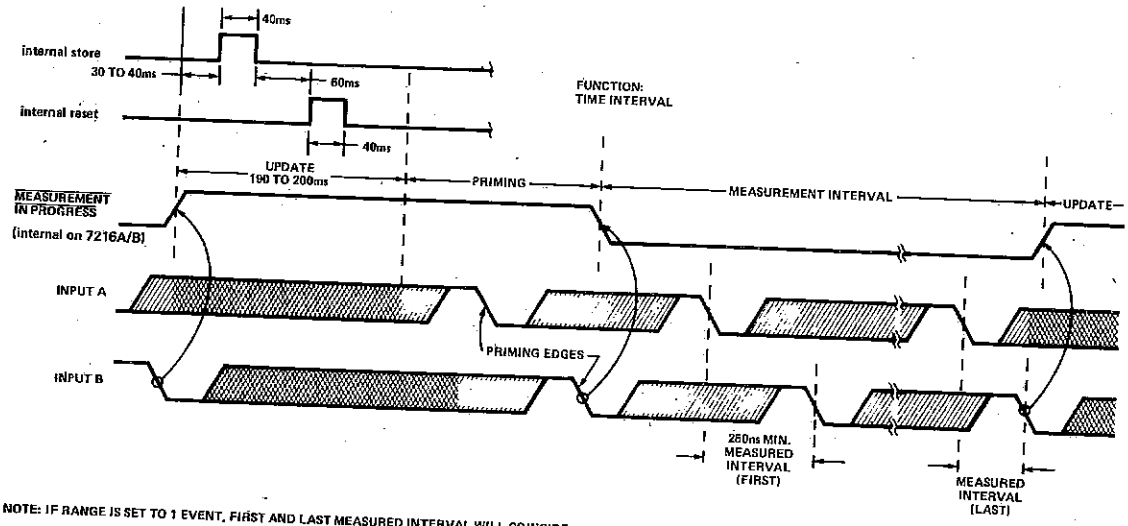
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3b. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A/B as the first alternating signal states automatically prime the device. See Figure 3b.

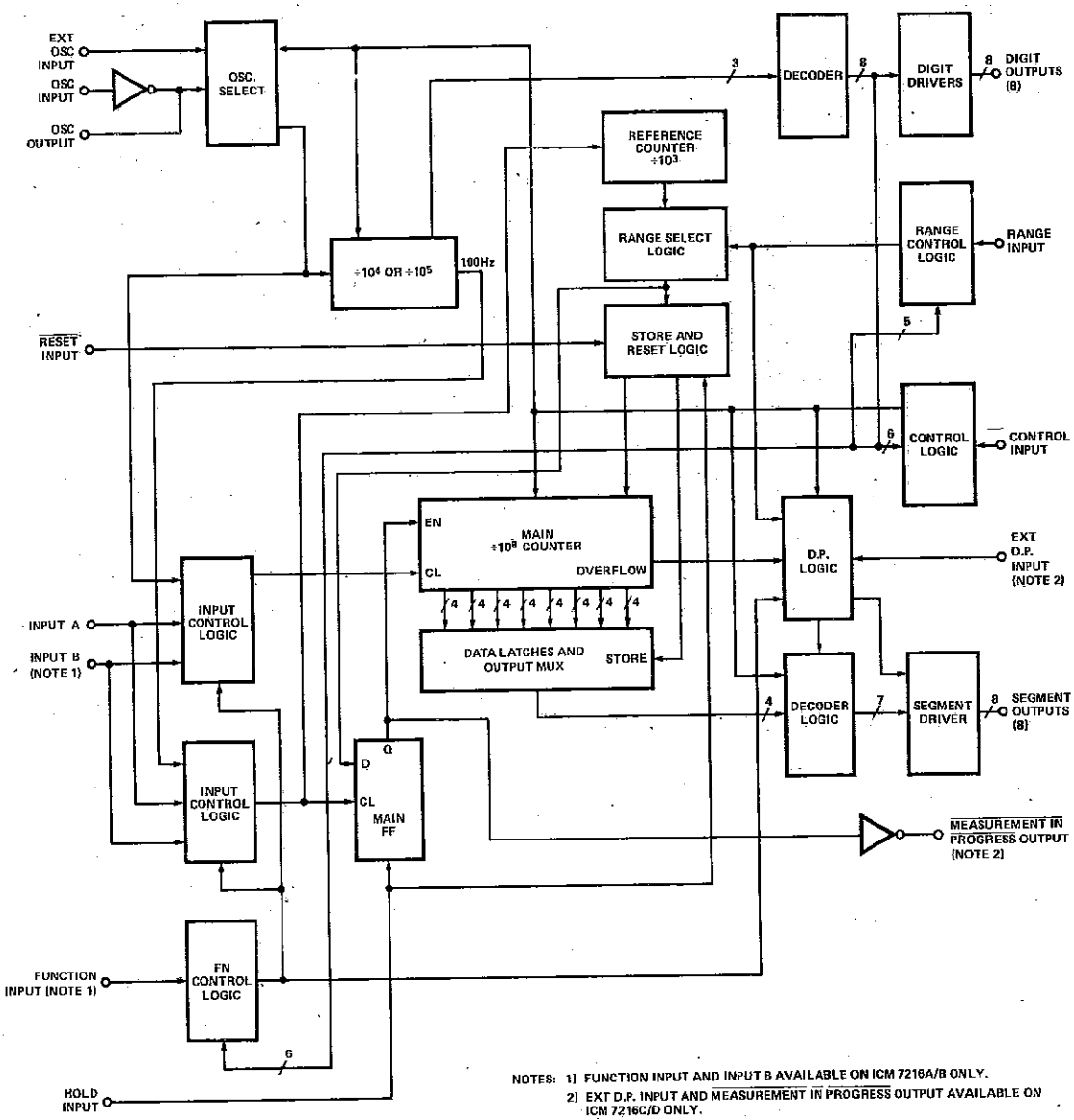
During any time interval measurement cycle, the ICM7216A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

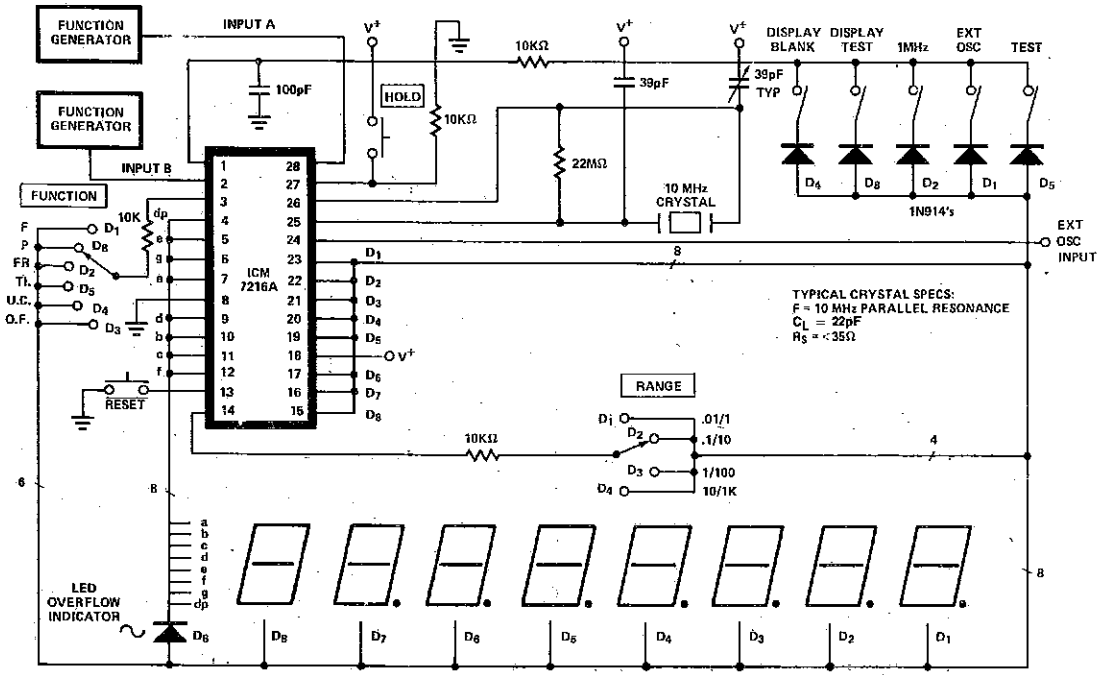
FIGURE 3a. Waveforms for Time Interval Measurement (others are similar, but without priming phase).

BLOCK DIAGRAM

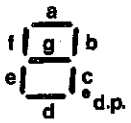


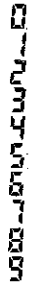
NOTES: 1) FUNCTION INPUT AND INPUT B AVAILABLE ON ICM 7216A/B ONLY.
2) EXT D.P. INPUT AND MEASUREMENT IN PROGRESS OUTPUT AVAILABLE ON ICM 7216C/D ONLY.

TEST CIRCUIT (7216A shown; others similar)



SEGMENT IDENTIFICATION AND DISPLAY FONT





Overflow will be indicated on the decimal point output of digit 8.

A separate LED overflow indicator can be connected as follows:

	CATHODE	ANODE
ICM7216A/C	DEC. PT.	D_8
ICM7216B/D	D_8	DEC. PT.

APPLICATION NOTES

GENERAL

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from T2L logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A/B).

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

CONTROL INPUT Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Blank Display is selected at the same time.

Blank Display — To disable the drivers, it is necessary to tie D_4 to the CONTROL INPUT and have the HOLD input at V^+. The chip will remain in this "Display Off" mode until HOLD is switched back to GND. While in the "Display Off" mode, the segment and digit driver outputs are open, the oscillator continues to run with a typical supply current of 1.5mA with a 10 MHz crystal, and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to GND. Segment and Digit Drive outputs may thus be bussed to drive a common display (up to 6 circuits).

1 MHz Select — The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable — In this mode the EXTERNAL OSCILLATOR INPUT is used instead of the on-chip oscillator for Timebase Input and Main Counter input in **period** and **time interval modes.** The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 kHz or the chip will reset itself to enable the on-chip oscillator. OSCillator INPUT (pin 25) must also be connected to EXT. OSC. input when using EXT. OSC. input.

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to EXTERNAL DECIMAL POINT input is active. Leading Zero Blanking will be disabled for all digits following the decimal point (7216C/D only).

Test Mode — This is a special mode for testing purposes only. Contact factory for details.

TABLE 1. Multiplexed Input Functions

	FUNCTION	DIGIT
FUNCTION INPUT Pin 3 (ICM7216A & B Only)	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT Pin 14	.01 sec/1 Cycle	D_1
	.1 sec/10 Cycles	D_2
	1 sec/100 Cycles	D_3
	10 sec/1K Cycles	D_4
CONTROL INPUT Pin 1	Blank Display	D_4 and Hold
	Display Test	D_8
	1 MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	(Test	D_5)
EXT. D.P. INPUT Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

RANGE INPUT

The RANGE INPUT selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except **unit counter** a change in the RANGE INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

FUNCTION INPUT

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.** This Input is available on the ICM7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the Reference Counter, as shown in Table 2. In all cases, only 1→0 transitions are counted or timed. In **time interval**, a flip-flop is toggled first by a 1→0 transition of INPUT A and then by a 1→0 transition of INPUT B. The oscillator is gated into the Main Counter from the time INPUT A toggles the flip-flop until INPUT B toggles it. In **unit counter** mode, the main counter contents are continuously displayed. A change in the FUNCTION INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed.

TABLE 2. 7216A/B Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A → B)	Oscillator (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

6

EXTernal DECimal Point INput

When the **external decimal point** is selected this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

HOLD Input — Except in **unit counter** mode, when the HOLD input is at V^+ any measurement in progress (before the "store time", see Figure 3a) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When HOLD is changed to GND a new measurement is immediately initiated. In **unit counter** mode, the counter is not reset; the count is frozen but will continue if HOLD goes low again.

$\overline{\text{RESET}}$ Input — The RESET input is the same as an inverted HOLD input, except the latches for the Main Counter are enabled, resulting in an output of all zeros, and the pin has a pull-up.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking assume right hand decimal point displays, and zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows. Overflow is indicated by the decimal point on digit 7 turning on.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8$ V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with $V_F = 1.8$V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4,5,6 and 7 show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

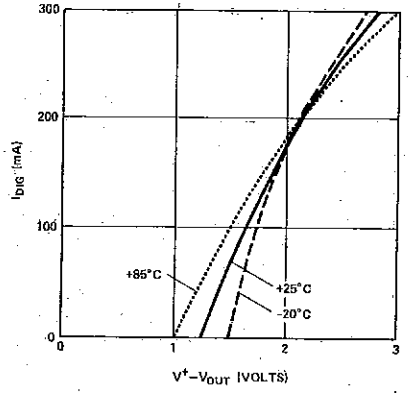


FIGURE 4. ICM7216A & C Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \le V^+ \le 6.0V$

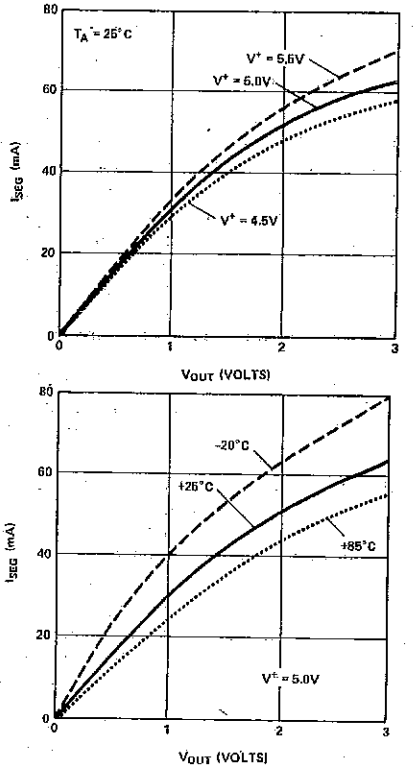
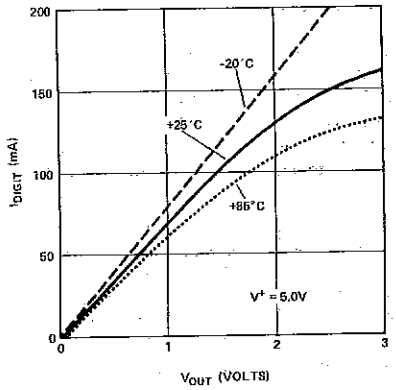
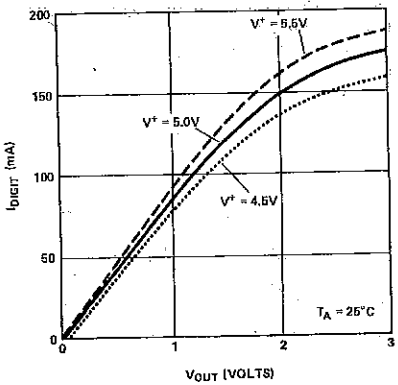


FIGURE 5. ICM7216A & C Typical I_{SEG} vs. V_{OUT}



(a)



(b)

FIGURE 6. ICM7216B & D Typical I_{DIGIT} vs. V_{OUT}

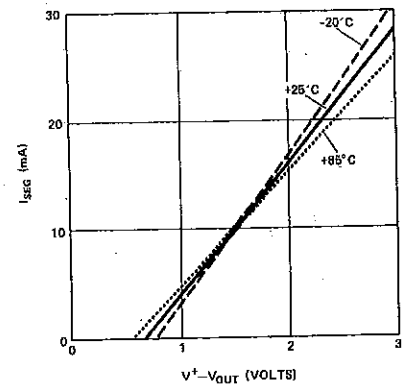


FIGURE 7. ICM7216B & D Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

ACCURACY

In a Universal Counter crystal drift and quantization effects cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 8, the least accuracy will be obtained at 10 kHz. In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 9. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 10.

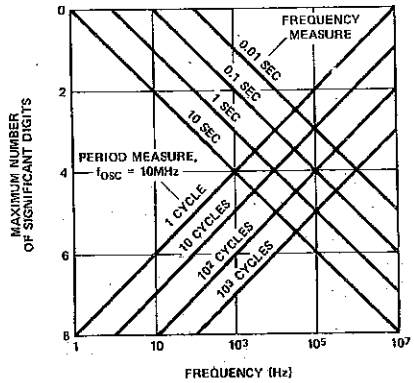


FIGURE 8. Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

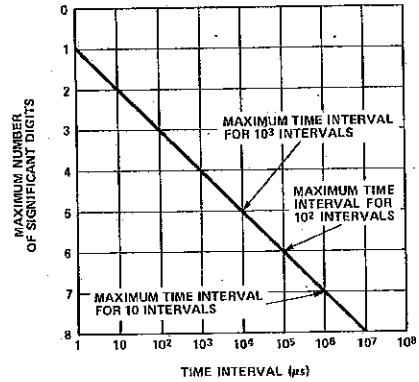


FIGURE 9. Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

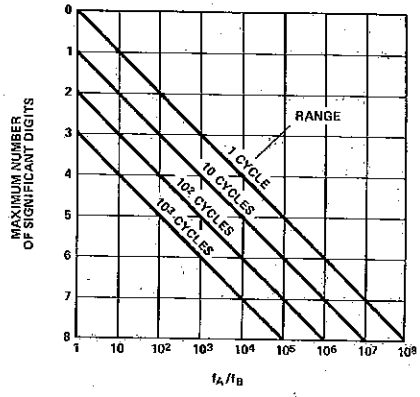


FIGURE 10. Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 11. This circuit can use input frequencies up to 10 MHz at INPUT A and 2 MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ns in duration.

To measure frequencies up to 40 MHz the circuit of Figure 12 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 ms and the display multiplex rate is decreased to 125 Hz.

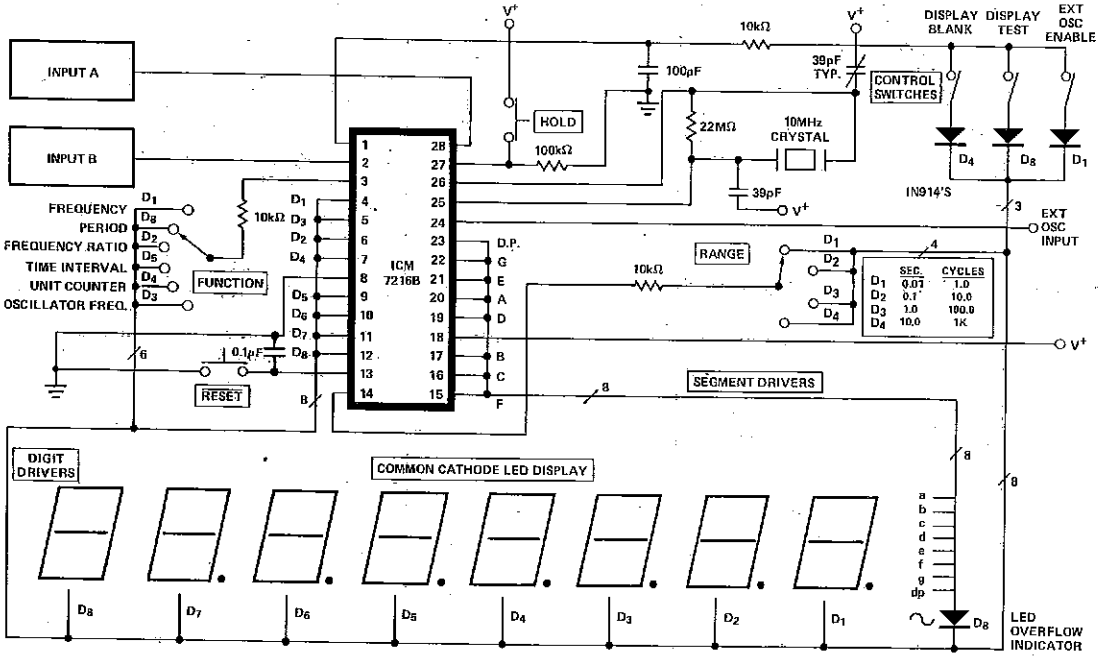


FIGURE 11. 10MHz Universal Counter

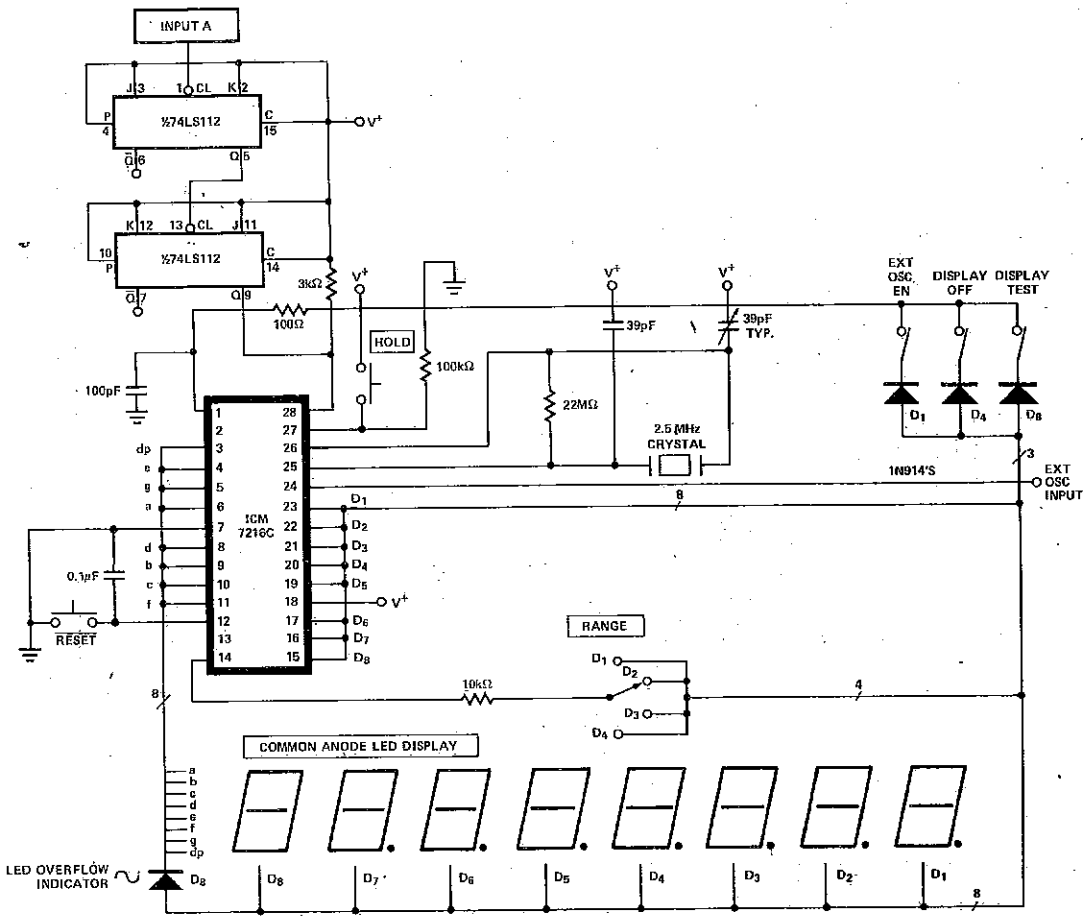


FIGURE 12. 40MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 MHz, but the decimal point must be moved one digit to the right. Figure 13 shows a frequency counter with a ÷10 prescaler and an ICM7216C. Since there is no external decimal point control with the ICM7216A or B, the decimal point may be controlled externally with additional drivers as shown in Figure 14. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 15 additional logic has been added to count the input directly in **period** mode for maximum accuracy. In Figures 13 through 15, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

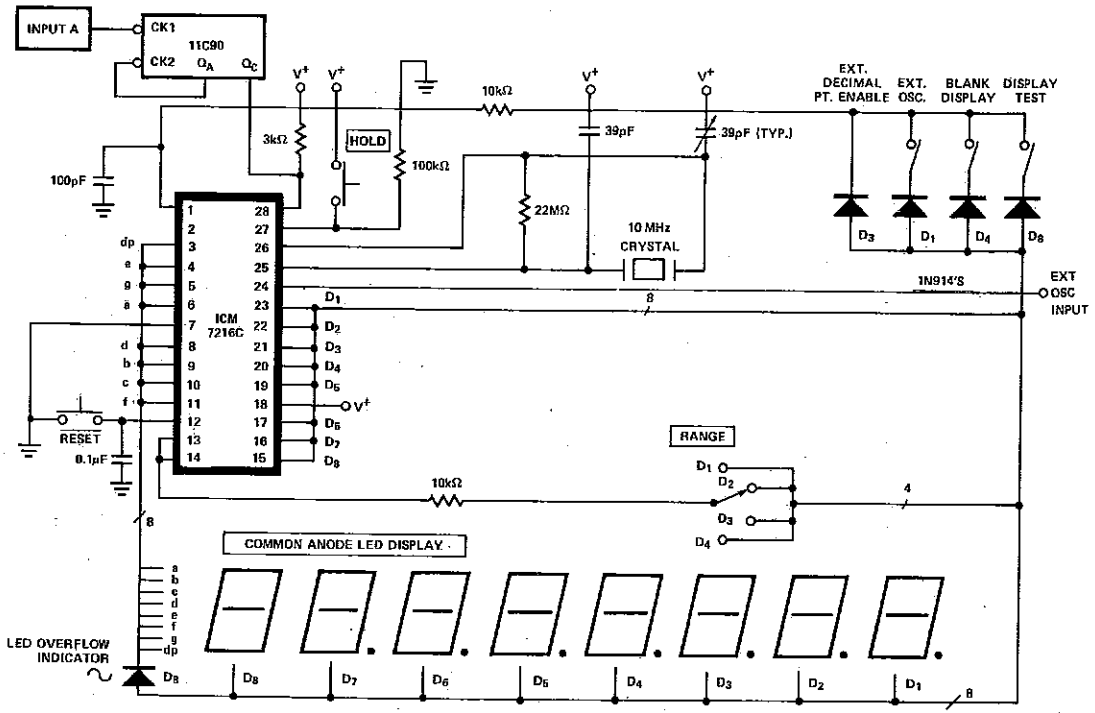


FIGURE 13. 100MHz Frequency Counter

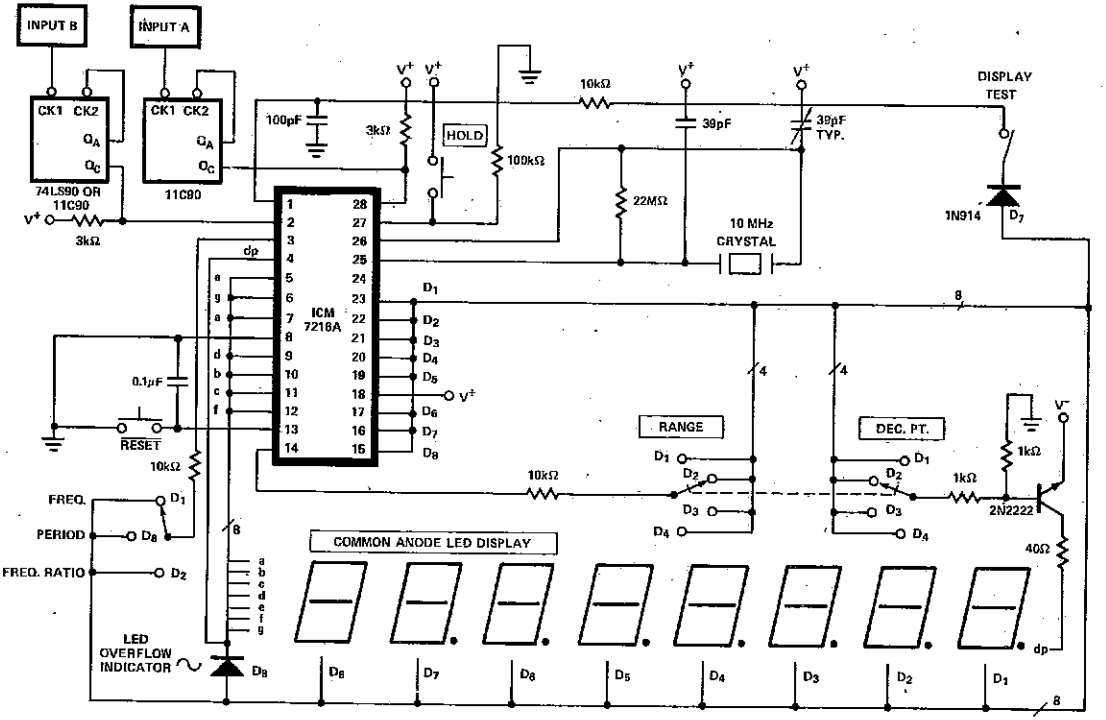


FIGURE 14. 100MHz Multifunction Counter

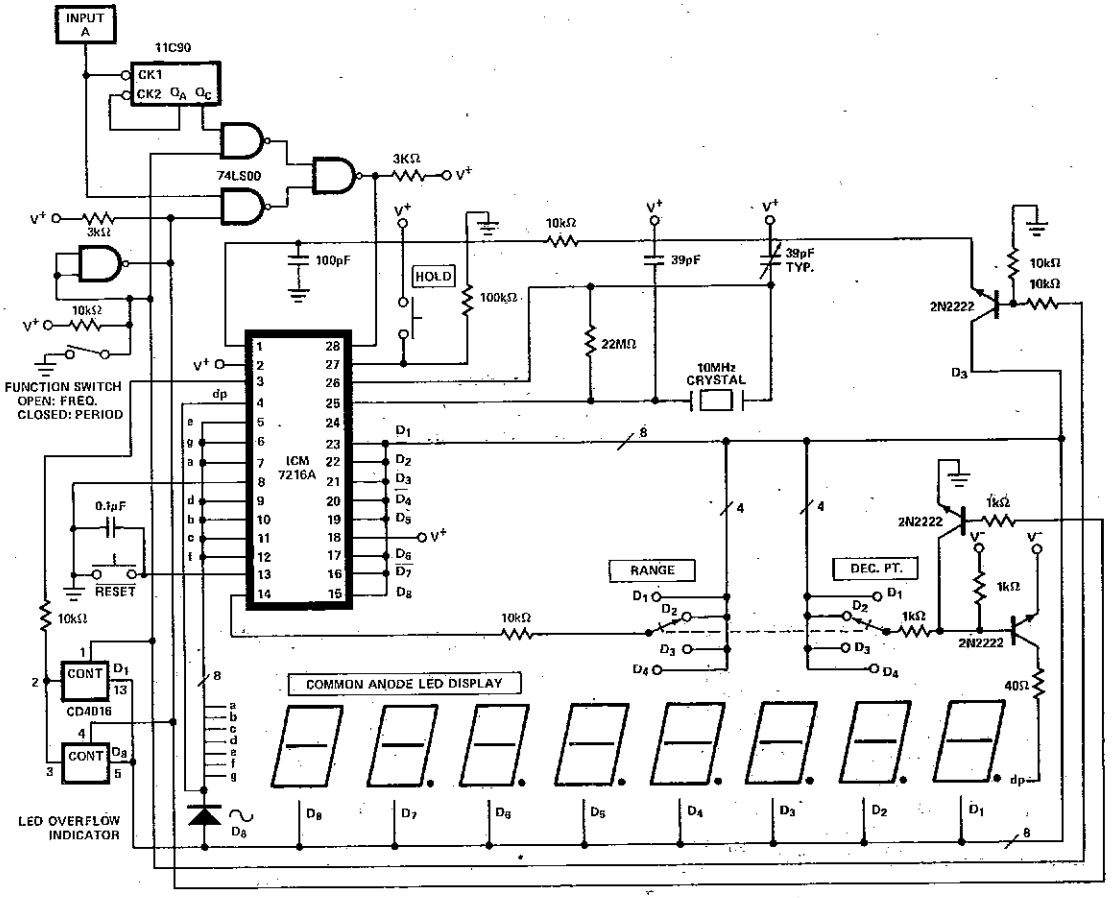


FIGURE 15. 100MHz Frequency, 2MHz Period Counter

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{In} C_{out} R_S \left(1+\frac{C_O}{C_L}\right)^2$$

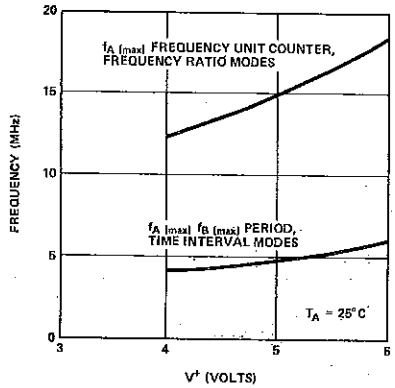
where $C_L = \left(\frac{C_{In}C_{out}}{C_{in}+C_{out}}\right)$

C_O = Crystal Static Capacitance
R_S = Crystal Series Resistance
C_{In} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2\times10^4}$ for 10 MHz mode and $f_{mux} = \frac{f_{osc}}{2\times10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1 MHz mode.

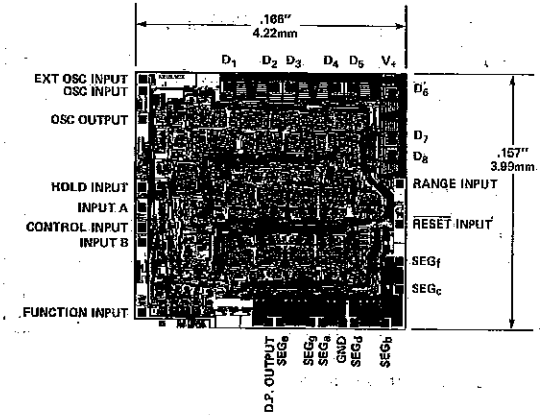
The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.



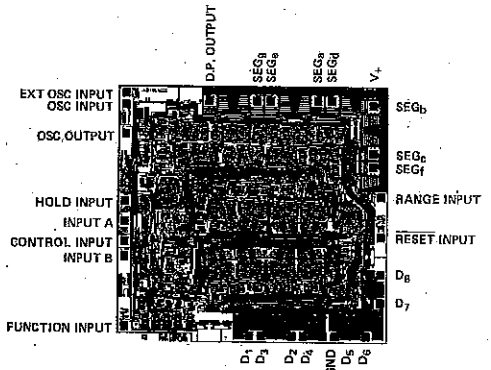
$f_{A(max)}$, $f_{B(max)}$ as a Function of V+

FIGURE 16. Typical Operating Characteristics

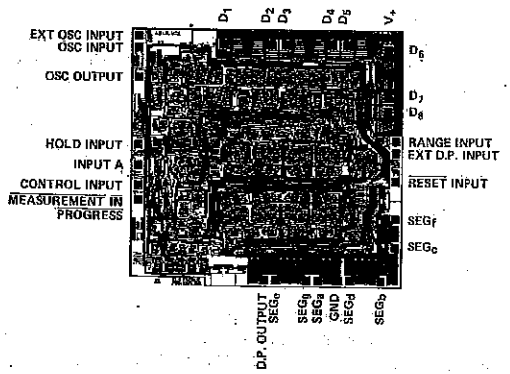
CHIP TOPOGRAPHIES



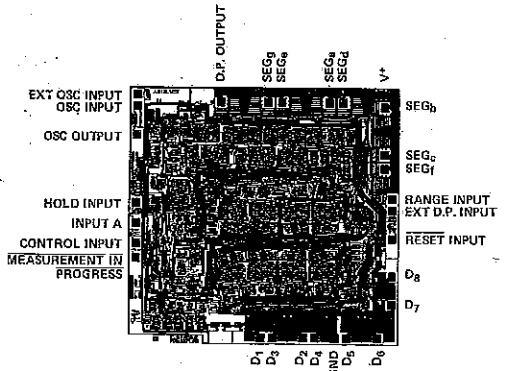
ICM7216A



ICM7216B



ICM7216C



ICM7216D

ICM7217 Series
ICM7227 Series
4-Digit CMOS Up/Down Counter/ Display Driver

FEATURES

- **Four decade, presettable up-down counter with parallel zero detect**
- **Settable register with contents continuously compared to counter**
- **Directly drives multiplexed 7 segment common anode or common cathode LED displays**
- **On-board multiplex scan oscillator**
- **Schmitt trigger on count input**
- **TTL compatible BCD I/O port, carry/borrow, equal, and zero outputs**
- **Display blank control for lower power operation; quiescent power dissipation < 5mW**
- **All terminals fully protected against static discharge**
- **Single 5V supply operation**

DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to .8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

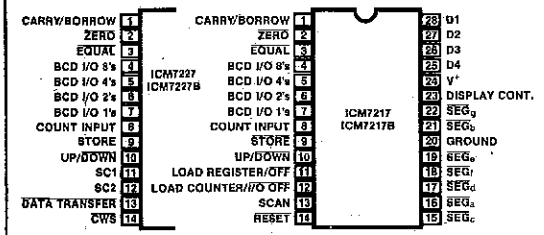
The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

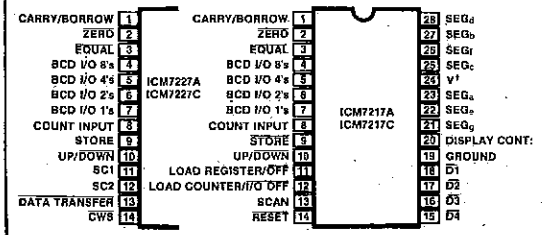
To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2 MHz, although the device will typically run with f_{in} as high as 5 MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750 kHz maximum.

PIN CONFIGURATIONS (outline dwgs JI, PI)



COMMON ANODE



COMMON CATHODE

ORDERING INFORMATION

Display Option	Count Option Max Count	28-LEAD Package	Order Part Number
Common Anode	Decade/9999	CERDIP	ICM7217IJI
Common Cathode	Decade/9999	PLASTIC	ICM7217AIPI
Common Anode	Timer/5959	CERDIP	ICM7217BIJI
Common Cathode	Timer/5959	PLASTIC	ICM7217CIPI
Common Anode	Decade/9999	CERDIP	ICM7227IJI
Common Cathode	Decade/9999	PLASTIC	ICM7227AIPI
Common Anode	Timer/5959	CERDIP	ICM7227BIJI
Common Cathode	Timer/5959	PLASTIC	ICM7227CIPI

6

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (common anode/Cerdip) ..... 1W Note 1
Power Dissipation (common cathode/Plastic) ...0.5W Note 1
Supply Voltage $V^+ - V^-$ 6V
Input Voltage
(any terminal)..... V^+ +0.3V, Ground -0.3V Note 2
Operating temperature range.....-20°C to +85°C
Storage temperature range..... -55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures..

OPERATING CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $T_A = 25°C$, Test Circuit, Display Diode Drop 1.7V, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply current (Lowest power mode)	I^+ (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 3)		350	500	μA
Supply current (Lowest power mode)	I^+ (7227)	Display off (Note 3)		300	500	μA
Supply current OPERATING	I_{OP}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver output current	I_{DIG}	Common anode, $V_{OUT} = V^+ -2.0V$	140	200		mA peak
SEGment driver output current	I_{SEG}	Common anode, $V_{OUT} = +1.3V$	-25	-40		mA peak
Digit Driver output current	I_{DIG}	Common cathode, $V_{OUT} = +1.3V$	-75	-100		mA peak
SEGment driver output current	I_{SEG}	Common cathode $V_{OUT} = V^+ -2V$	10	12.5		mA peak
$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	I_P	$V_{OUT} = V^+ -2V$ (See Note 3)	5	25		μA
3 level input impedance	Z_{IN}			100		kΩ
BCD I/O input high voltage	V_{BIH}	ICM7217 common anode (Note 4) ($V^+ = 5.0V$)	1.3			V
		ICM7217 common cathode (Note 4)	$V^+ -0.8$			V
		ICM7227 with 50pF effective load	3			V
BCD I/O input low voltage	V_{BIL}	ICM7217 common anode (Note 4) ($V^+ = 5.0V$)			0.8	V
		ICM7217 common cathode (Note 4)			$V^+ -1.8$	V
		ICM7227 with 50pF effective load			1.5	V
BCD I/O input pullup current	I_{BPU}	ICM7217 common cathode $V_{IN} = V^+ -2V$ (Note 3)	5	25		μA
BCD I/O input pulldown current	I_{BPD}	ICM7217 common anode $V_{IN} = +1.3V$ (Note 3)	5	25		μA
BCD I/O, CARRY/BORROW, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high current	I_{BOH}	$V_{OH} = V^+ -1.5V$	100			μA
BCD I/O, CARRY/BORROW, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low current	I_{BOL}	$V_{OL} = +0.4V$	-2			mA
Count input frequency (Guaranteed)	f_{in}	$V^+ = 5V \pm 10\%$, $-20°C < T_A < +70°C$	0	5	2	MHz
Count input threshold	V_{TH}	$V^+ = 5V$		2		V
Count input hysteresis	V_{HYS}	$V^+ = 5V$		0.5		V
Display scan oscillator frequency	f_{ds}	Free-running (SCAN terminal open circuit)		2.5		kHz
Operating Temperature Range	T_A	Industrial temperature range	-20		+85	°C

NOTE 1 These limits refer to the package and will not be obtained during normal operation.

NOTE 2 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

NOTE 3 In the ICM7217 the UP/$\overline{DOWN}$, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.

NOTE 4 These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common cathode versions.

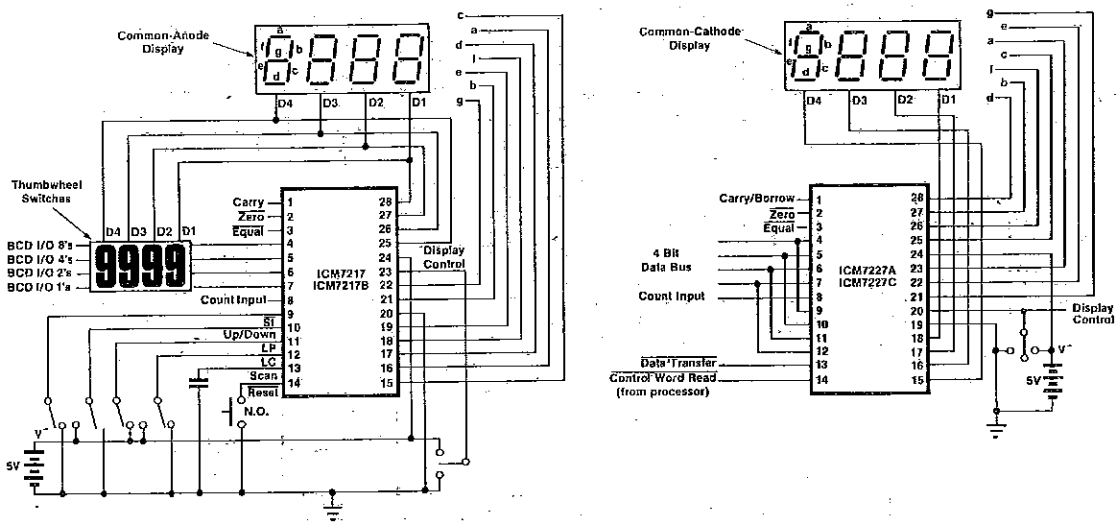


Figure 1: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

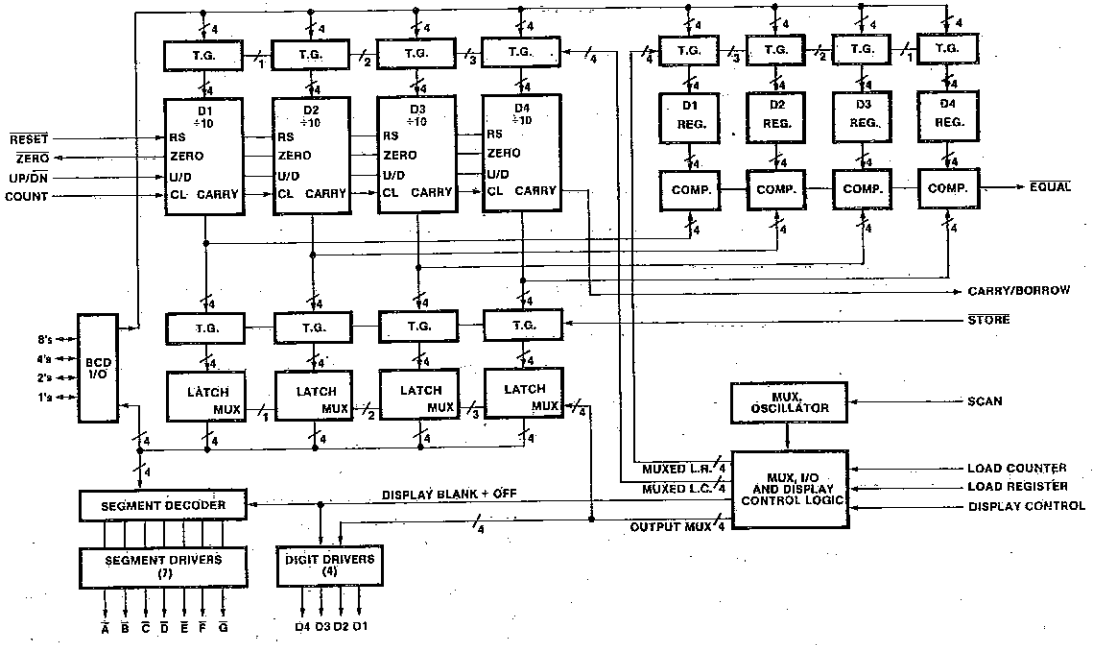


Figure 2: ICM7217 Functional Block Diagram

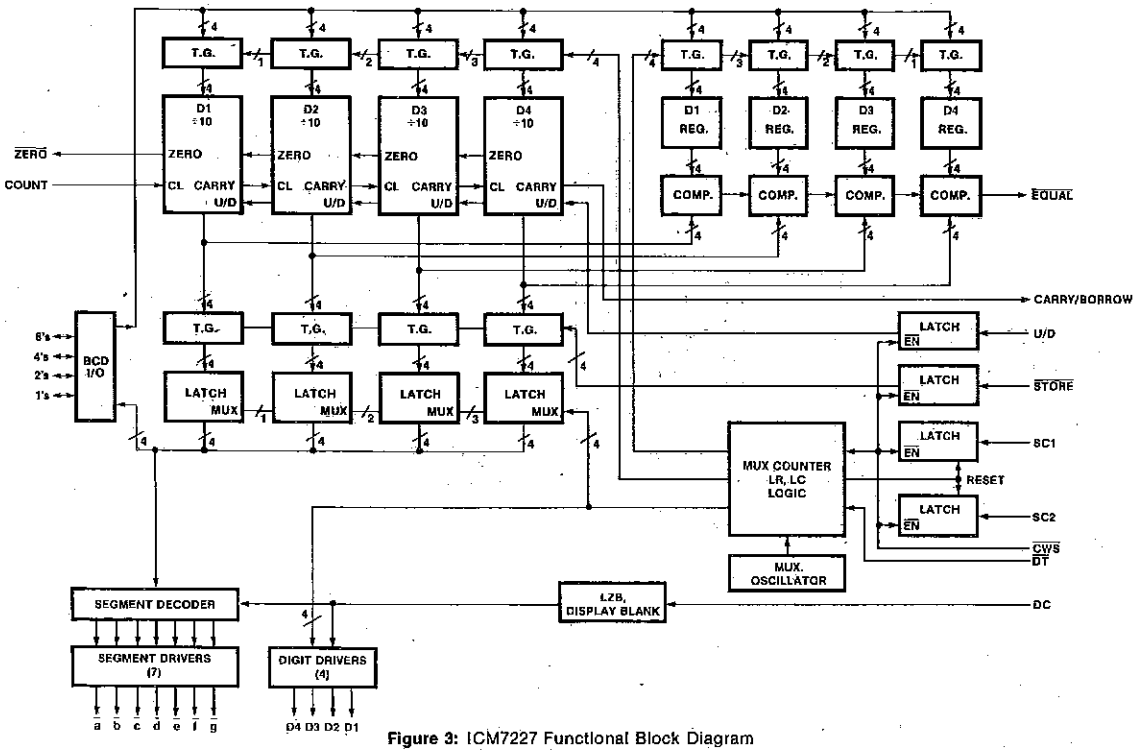


Figure 3: ICM7227 Functional Block Diagram

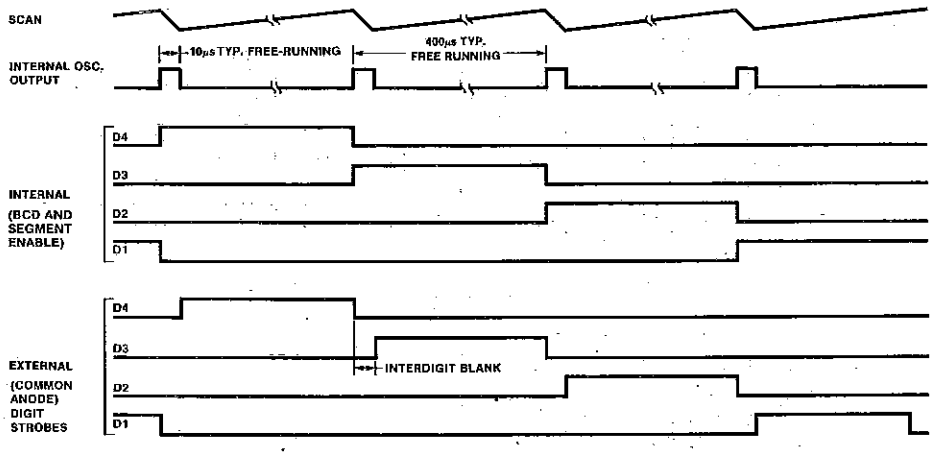


Figure 4: Multiplex Timing

DESCRIPTION OF OPERATION

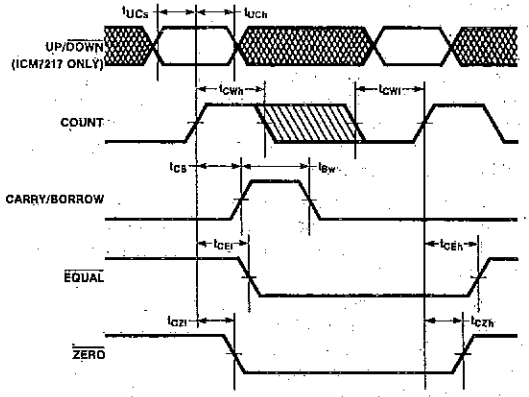
OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 2mA @ 0.4V (on resistance 200 ohms), and for a logic one, the outputs will source >60μA. A 10kΩ pull-up resistor to V+ on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.



SYMBOL	DESCRIPTION	MUX	TYP	MAX	UNITS
t_{UCs}	UP/$\overline{DOWN}$ setup time (min)		300		
t_{UCh}	UP/$\overline{DOWN}$ hold time (min)		0		
t_{CUh}	COUNT pulse high (min)		100	250	ns
t_{CUl}	COUNT pulse low (min)		100	250	
t_{CB}	COUNT to CARRY/ BORROW delay		750		
t_{Bw}	CARRY/BORROW pulse width		100		
t_{CEl}	COUNT to $\overline{EQUAL}$ delay		500		
t_{CZl}	COUNT to $\overline{ZERO}$ delay		300		

Figure 5: ICM7217/27 COUNT and Output Timing

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 4 shows the multiplex timing, while Figure 5 shows the Output Timing. Figures 6 through 9 show the output characteristics of the Digit and SEGment drivers. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V^+); this corresponds to normal operation. When this pin is connected to V^+, the segments are inhibited, and when connected to V^-, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 1.

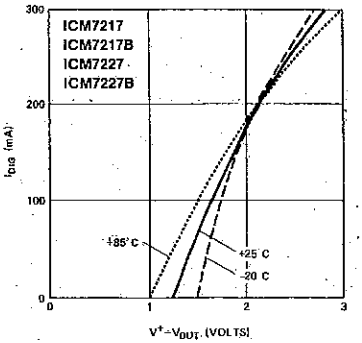


Figure 6: Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \le V^+ \le 6.0V$

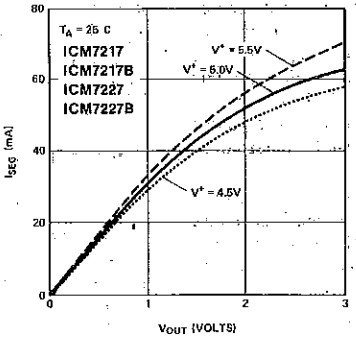
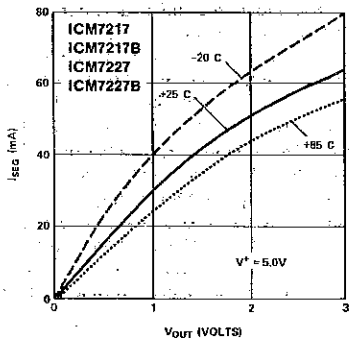


Figure 7: Typical I_{SEG} vs. V_{OUT}



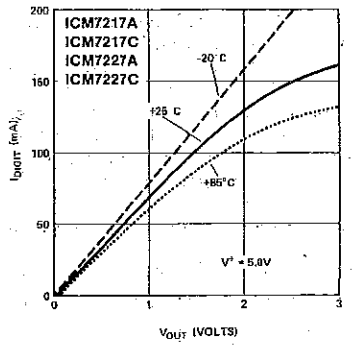
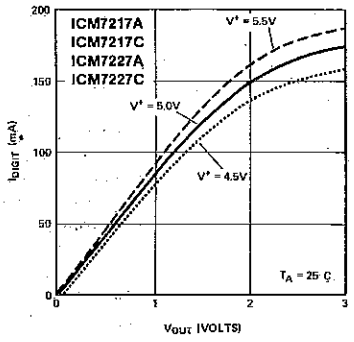


Figure 8: Typical I_{DIGIT} vs. V_{OUT}



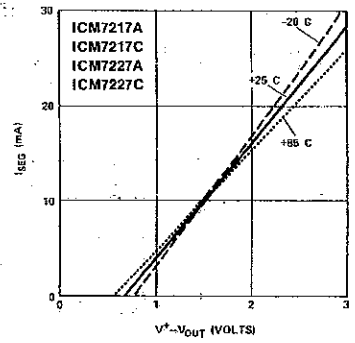


Figure 9: Typical I_{SEG} vs. $V^+ - V_{OUT}$,

CONTROL OF ICM7217

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for ICM7217 versions) are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplex Rate Control

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time (4 digits)
None	2.5 kHz	625 Hz	1.6 ms
20 pF	1.25 kHz	300 Hz	3.2 ms
90 pF	600 Hz	150 Hz	8 ms

During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 10 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

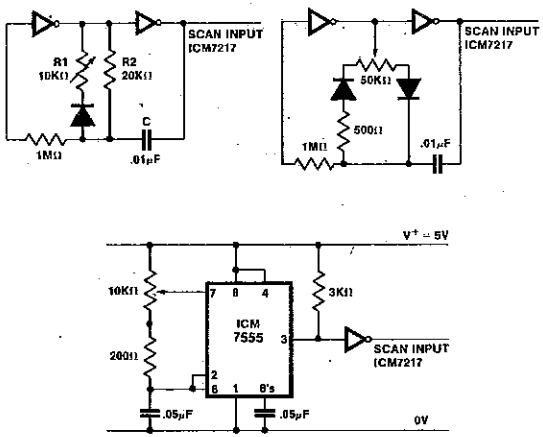


Figure 10: Brightness Control Circuits

Counting Control

As shown in Figure 5, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pullup resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately 1/2 V^+ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V^+, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V^+, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V^+, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 11). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD

I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 12). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Fig. 12. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

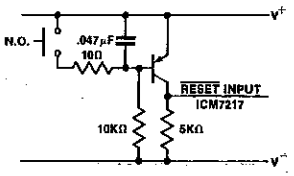
Output and Input Restrictions

The CARRY/BORROW output is not valid during load counter and reset operations.

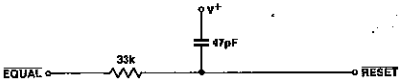
The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below.



When using the circuit as a programmable divider(÷ by n with equal outputs) a short time delay (about 1μs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration.



When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

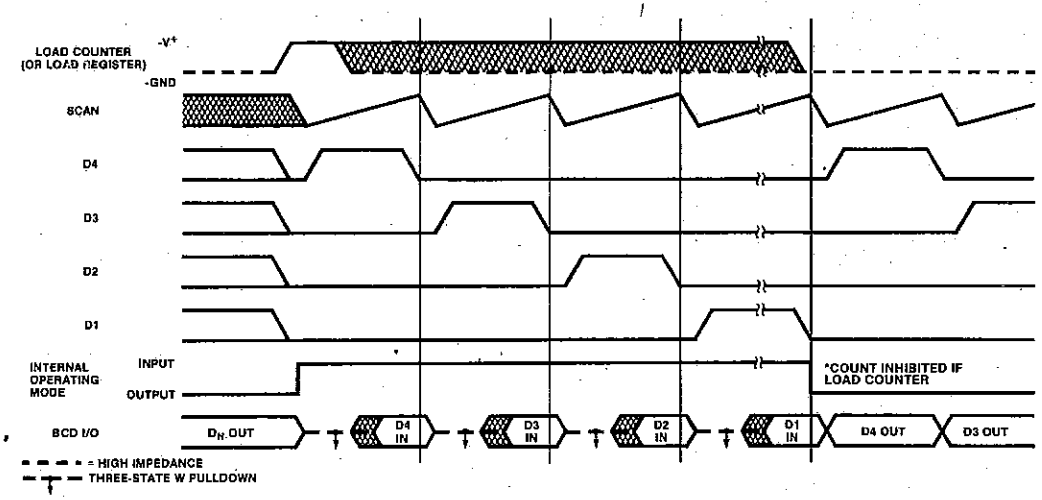
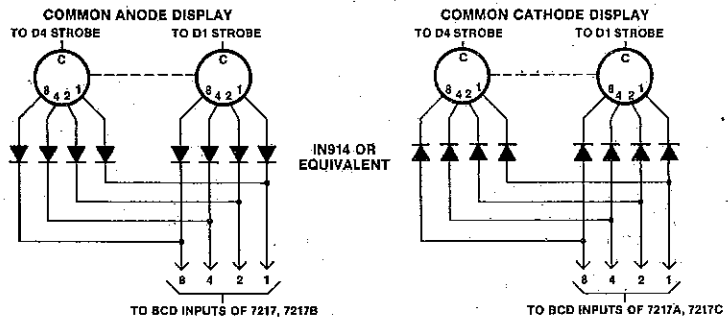


Figure 11: ICM7217 BCD I/O and LOADING TIMING



Note: If the BCD pins are to be used for outputs a 10kΩ resistor should be placed in series with each digit line to avoid loading problems through the switches.

Figure 12: Thumbwheel switch/diode connections

Table 2: Control Input Definitions ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{STORE}}$	9	V^+ (or floating) Ground	Output latches not updated Output latches updated
UP/$\overline{\text{DOWN}}$	10	V^+ (or floating) Ground	Counter counts up Counter counts down
$\overline{\text{RESET}}$	14	V^+ (or floating) Ground	Normal Operation Counter Reset
LOAD COUNTER/ $\overline{\text{I/O OFF}}$	12	Unconnected V^+ Ground	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ $\overline{\text{OFF}}$	11	Unconnected V^+ Ground	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ Ground	Normal operation Segment drivers disabled Leading zero blanking inhibited

Table 3: Control Input Definitions ICM7227

INPUT		TERMINAL	VOLTAGE	FUNCTION
	$\overline{\text{DATA TRANSFER}}$	13	V^+ Ground	Normal Operation Causes transfer of data as directed by select code
Control Word Port	STORE	9	V^+ (During $\overline{\text{CWS}}$ Pulse) Ground	Output latches updated Output latches not updated
"	UP/$\overline{\text{DOWN}}$	10	V^+ (During $\overline{\text{CWS}}$ Pulse) Ground	Counter counts up Counter counts down
" "	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V^+ = "1" Ground = "0"	SC1, SC2 control:– 00 Change store and up/$\overline{\text{down}}$ latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	$\overline{\text{Control Word Strobe}}$ ($\overline{\text{CWS}}$)	14	V^+ Ground	Normal operation Causes control word to be written into control latches
	DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ Ground	Normal operation Display drivers disabled Leading zero blanking inhibited

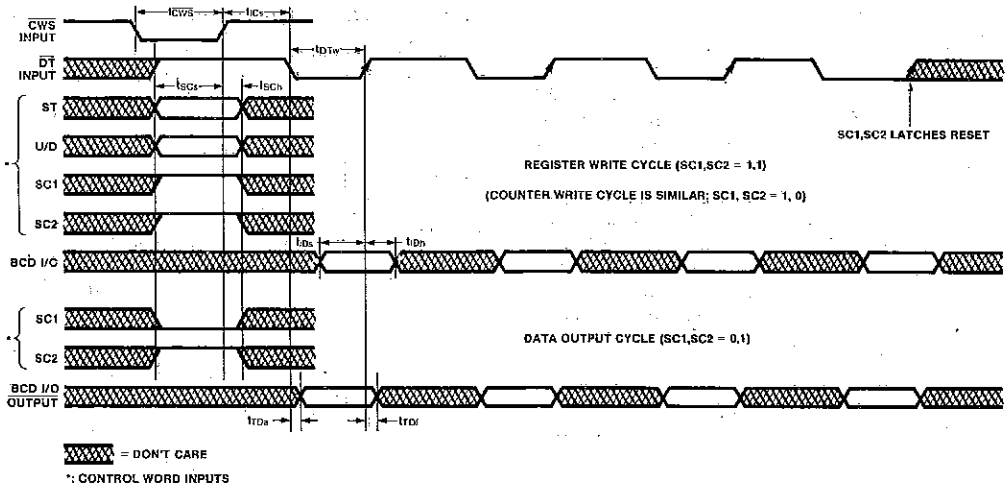


Figure 13: ICM7227 I/O Timing (see Table 4)

CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/$\overline{\text{DOWN}}$, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a **data transfer** operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DATA TRANSFER}}$ pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Fig. 13 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{\overline{CWS}}$	Control Word Strobe Width (min)		275		ns
t_{ICS}	Internal Control Set-up (min)		2.5	3	μs
$t_{\overline{DT}W}$	DATA TRANSFER pulse width (min)		300		ns
t_{SCS}	Control to Strobe setup (min)		300		ns
t_{SCH}	Control to Strobe hold (min)		300		ns
t_{IDS}	Input Data setup (min)		300		ns
t_{IDH}	Input Data hold (min)		300		ns
t_{TDacc}	Output Data access		300		ns
t_{TDf}	Output Transfer to Data float		300		ns

APPLICATIONS

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V^+.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Figure 9 for a similarly operating multi-digit connection.

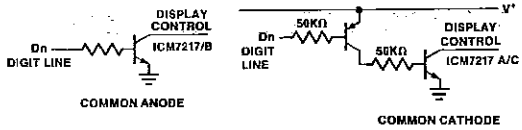


Figure 14: Forcing Leading Zero Display

DRIVING LARGER DISPLAYS

For displays requiring more current than the ICL7217/7227 can provide, the circuits of Figure 15 can be used.

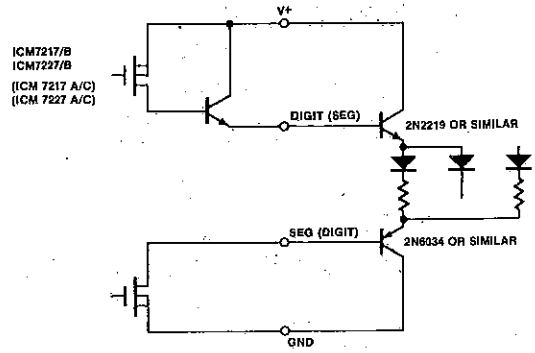


Figure 15: Driving High Current Displays

LCD DISPLAY INTERFACE (Figure 16)

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10—20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

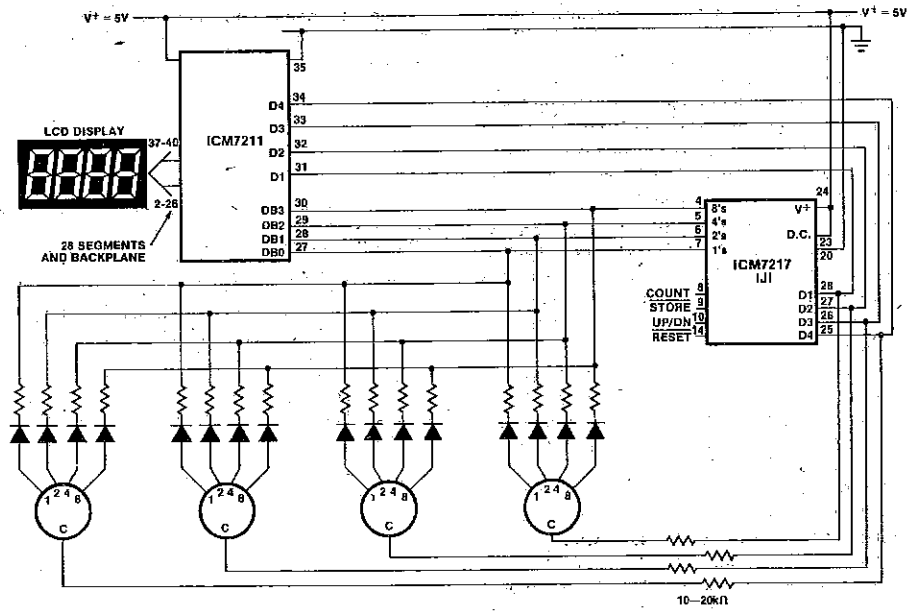


Figure 16: LCD Display Interface (with Thumbwheel Switches)

UNIT COUNTER WITH BCD OUTPUT (Figure 17)

The simplest application of the ICM7217 is a 4 digit unit counter. All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A and a common-cathode calculator-type display, results in the least expensive digital counter/display system available.

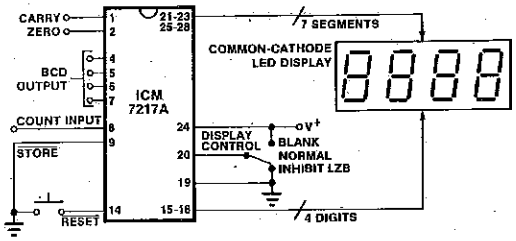
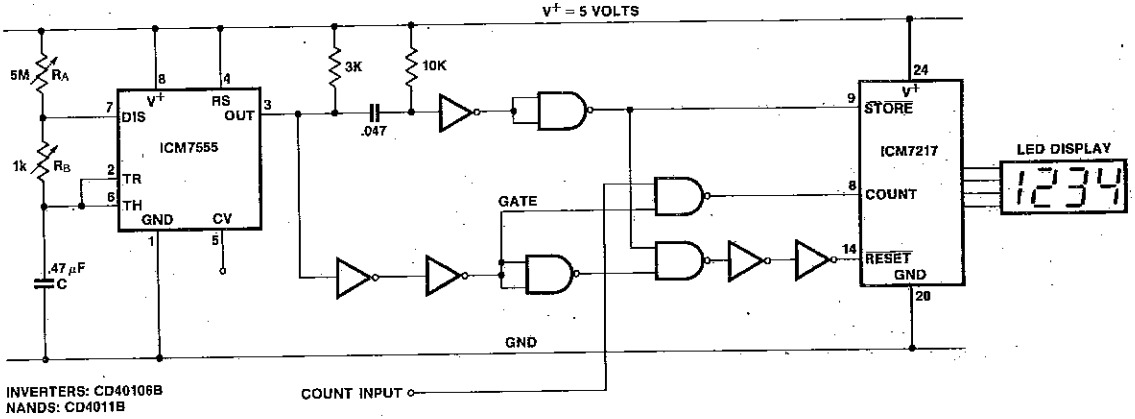


Figure 17: Unit Counter

INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER (Figure 18)

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300-500μs. The positive waveform time is given by $t_{wp} = 0.693 (R_A + R_B) C$, while the negative waveform is given by $t_{wn} = 0.693 R_B C$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1k potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.



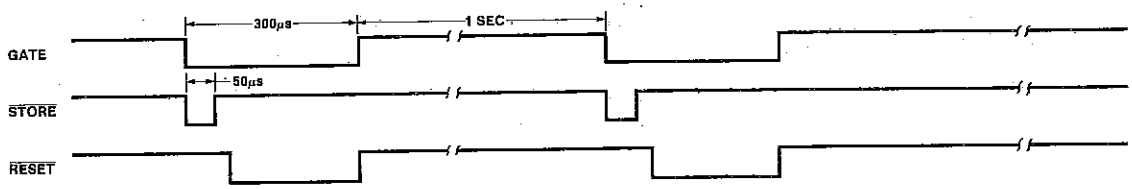


Figure 18: Inexpensive Frequency Counter

TAPE RECORDER POSITION INDICATOR/ CONTROLLER (Figure 19)

This circuit shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047 μF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

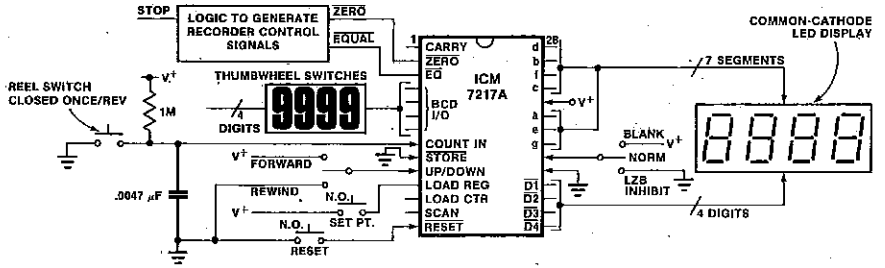


Figure 19: Recorder Indicator

PRECISION ELAPSED TIME/COUNTDOWN TIMER (Figure 20)

This circuit uses an ICM7213 precision one minute/one second timebase generator using a 4.1943 MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used. This technique may be used on any 3-level input. The 100k pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 18 to generate a 1Hz reference.

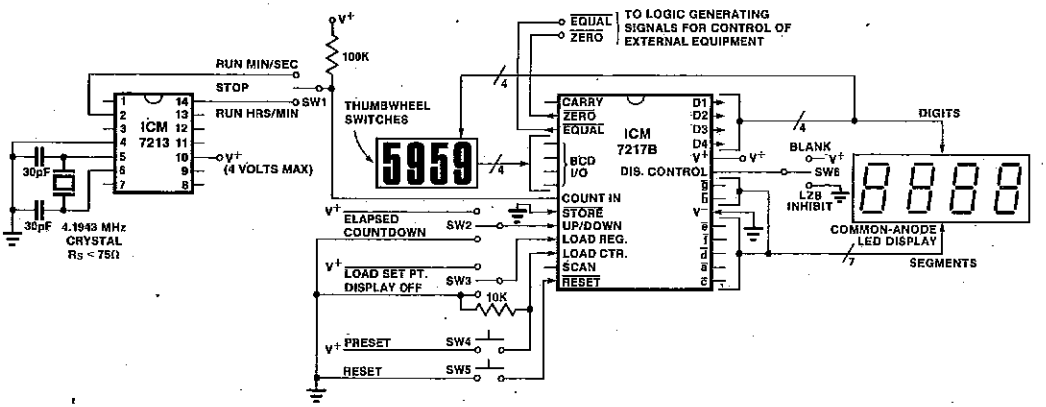


Figure 20: Precision Timer

MICROPROCESSOR INTERFACE-ICM7227
(Figure 21)

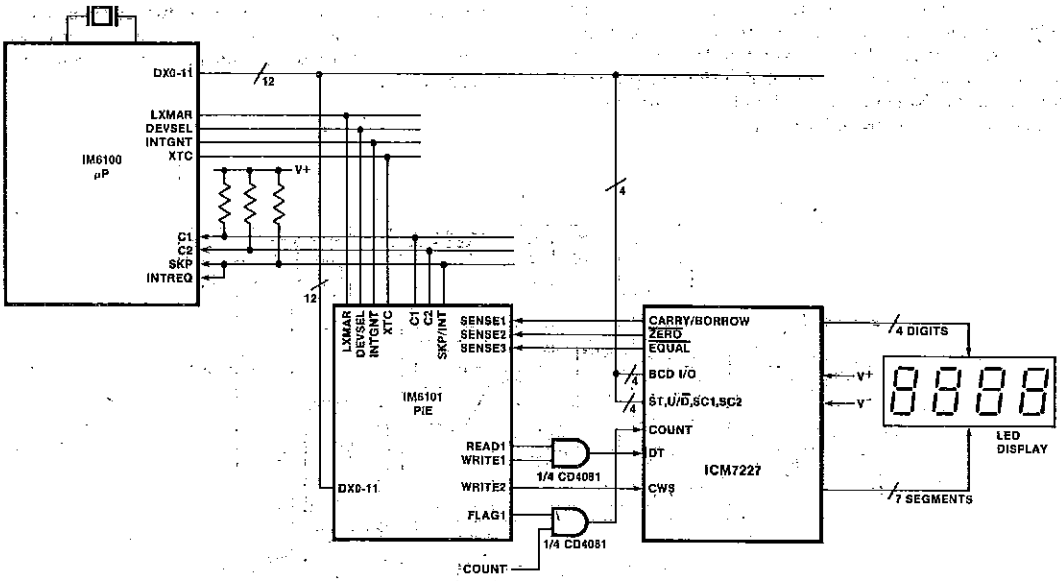


Figure 21: IM6100

This circuit shows the hardware necessary to interface the ICM7227 to an Intersil IM6100 CMOS microprocessor. Using an IM6101 Parallel Interface Element (PIE) allows the addition of one or more ICM7227 devices as generalized peripherals to any IM6100 system, using a minimum of external components.

A similar configuration may be used with the MC6800 using the corresponding PIE, while an 8255 can be used to interface 8080 based systems.

The ICM7227 can perform many "accessory" functions that are inefficient or impossible for the processor to perform. For example, by adding a timebase such as an ICM7213, and using an ICM7227C or D, an inexpensive real-time clock/display, directly accessible by the processor, can be constructed.

8-DIGIT UP/DOWN COUNTER (Figure 22)

This circuit shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

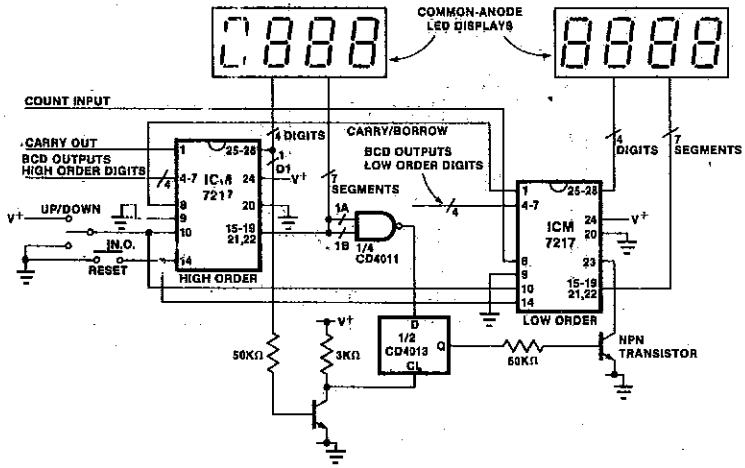
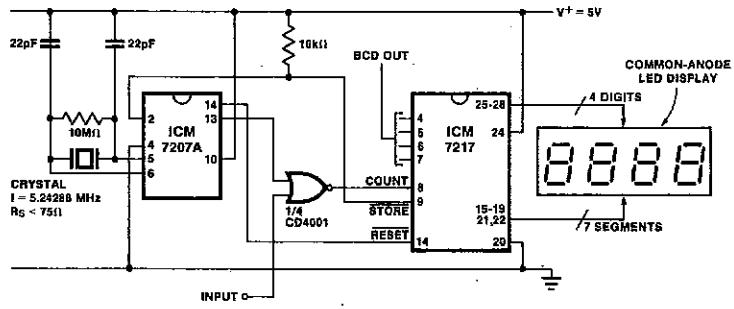


Figure 22: 8 Digit Up/Down Counter



PRECISION FREQUENCY COUNTER/ TACHOMETER (Figure 23)

This circuit is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V^+, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536 MHz crystal), giving a 0.01 second gating with Pin 11 connected to V^+, and a 0.1 second gating with Pin 11 open.

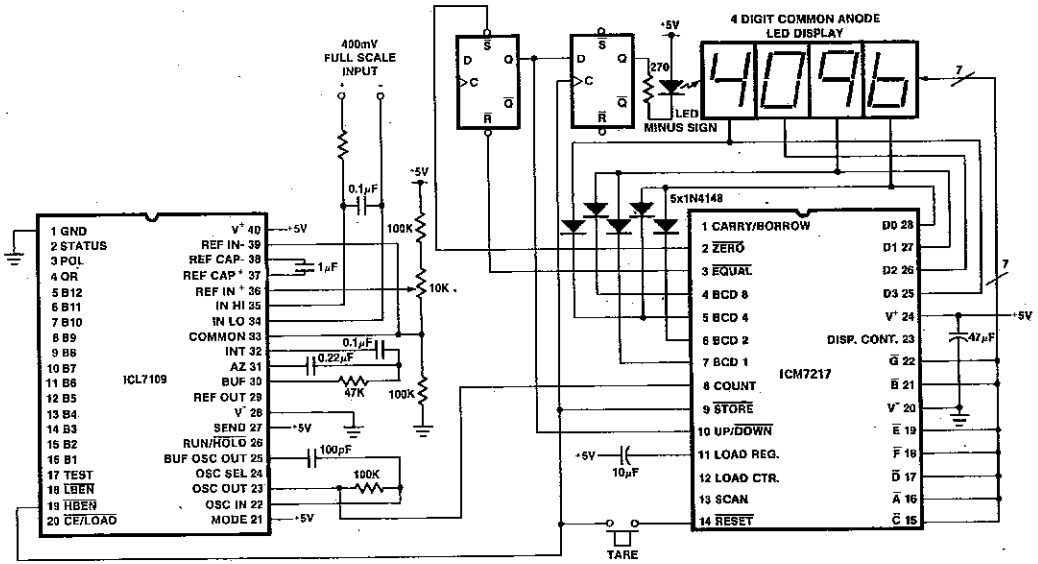
To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs, to count in SYNC with an ICL7109 A/D Converter. By $\overline{\text{RESET}}$ing the ICM7217 on a "tare" value conversion, and $\overline{\text{STORE}}$-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7019 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.



TAPE RECORDER POSITION INDICATOR/ CONTROLLER (Figure 19)

This circuit shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047 μF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

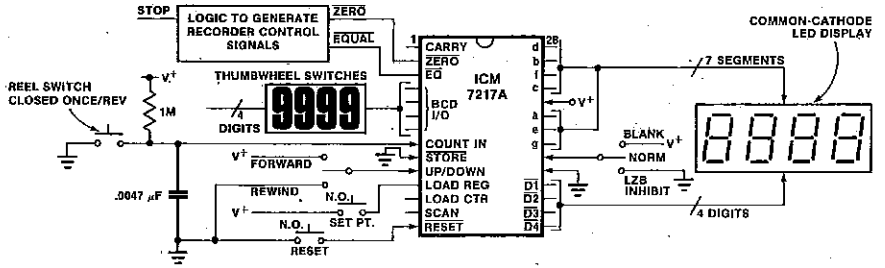


Figure 19: Recorder Indicator

PRECISION ELAPSED TIME/COUNTDOWN TIMER (Figure 20)

This circuit uses an ICM7213 precision one minute/one second timebase generator using a 4.1943 MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used. This technique may be used on any 3-level input. The 100k pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 18 to generate a 1Hz reference.

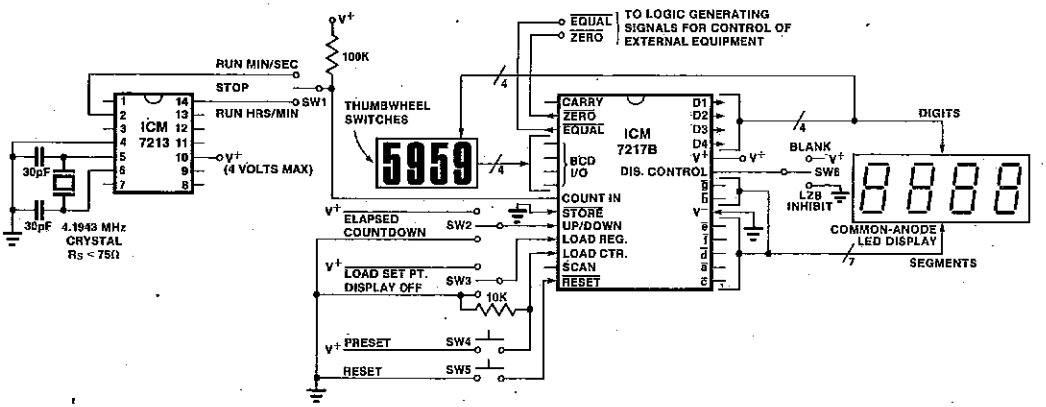
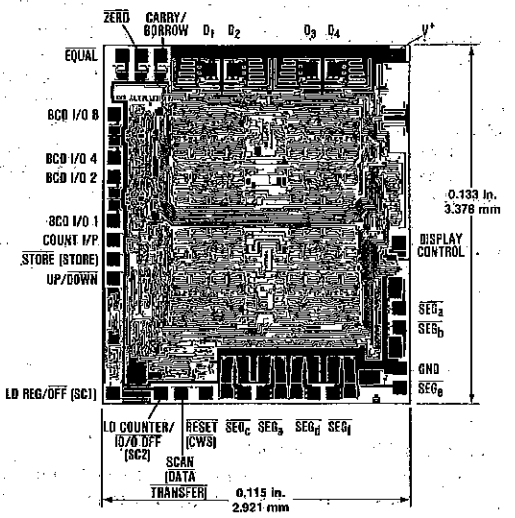
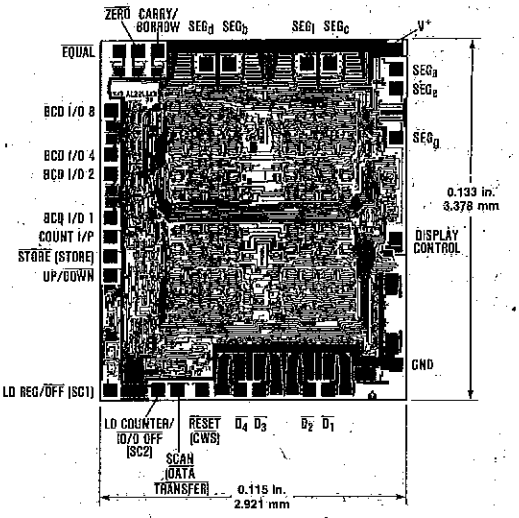


Figure 20: Precision Timer

CHIP TOPOGRAPHY



ICM7217/B (ICM7227/B)



ICM7217A/C (ICM7227A/C)

6

ICM7218 Series
CMOS Universal 8 Digit LED Driver System

FEATURES

- **Total circuit integration on chip includes:**
  - **a) Digit and segment drivers**
  - **b) All multiplex scan circuitry**
  - **c) 8X8 static memory**
  - **d) 7 segment Hexadecimal and Code B decoders**
- **Output drive suitable for large LED displays**
- **Both common anode and common cathode LED drive versions**
- **Single 5 volt supply required**
- **Data retention to 2 volts supply**
- **Shutdown feature - turns off display and puts chip into very low power dissipation mode**
- **Pin selectable choice of 2 seven segment decoders - Hexa or Code B - or no decode**
- **Microprocessor compatible**
- **Serial and random access versions**
- **Decimal point drive on each digit**

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems and an LED display. Included on chip is an 8x8 static memory array providing storage for the displayed information, 2 types of 7 segment decoders, all the multiplex scan circuitry and the high power digit and segment drivers.

The ICM7218A and ICM7218B are intended to be used primarily in microprocessor systems. Data is read directly from the I/O bus line from the microprocessor. 2 Control lines ($\overline{\text{Write}}$, and Mode) define chip select, which reads either 4 bits of control information (Data Coming, $\overline{\text{Shutdown}}$, Decode, Hexa or Code B Decoding) or 8 bits of Display Input Data. Display Input Data (8 words, 8 bits each) is automatically sequenced into the memory on successive positive going $\overline{\text{Write}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218A drives a common anode display while the ICM7218B drives a common cathode display. (See Block Diagram 1)

The ICM7218C and ICM7218D feature 2 lines for control information ($\overline{\text{Write}}$, Three Level Input; Hexa, Code B, $\overline{\text{Shutdown}}$), 4 lines for Input Data and 3 lines for Data Addressing of each of eight data memory locations.

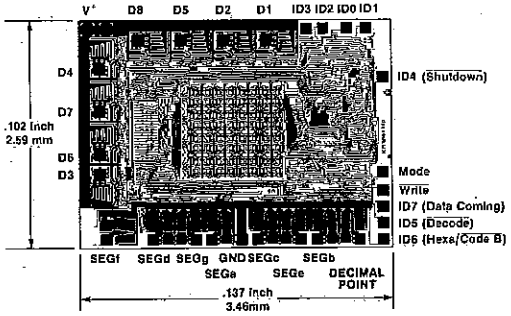
Data is written into memory by setting up a Data Address memory location, defining 4 lines of Input Data and then strobe the $\overline{\text{Write}}$ line low. The Three Level Control Input is independent of the $\overline{\text{Write}}$ instruction. Only Hexadecimal and Code B decoding are available for the Display Outputs. The ICM7218C drives a common anode display, the ICM7218D a common cathode display. (See Block Diagram 2)

The ICM7218E provides 4 separate lines for control information ($\overline{\text{Write}}$, Hexa-Code B, Decode, $\overline{\text{Shutdown}}$), 8 lines for input data, and 3 lines for digit address. Data is written into the memory by setting up a Data Address memory location, defining 8 lines of Input Data, and then strobe the $\overline{\text{Write}}$ line low. Control information is on separate lines and is independent of the $\overline{\text{Write}}$ instruction. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218E drives a common anode display. (See Block Diagram 3)

ORDERING INFORMATION

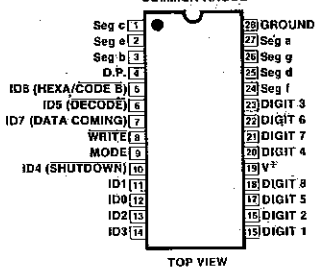
Typical App.	Order Part Number	Display Option	Package
Serial Access	ICM7218A IJI	Common Anode	28 Lead CERDIP
	ICM7218B IPI	Common Cathode	28 Lead Plastic
Random Access	ICM7218C IJI	Common Anode	28 Lead CERDIP
	ICM7218D IPI	Common Cathode	28 Lead Plastic
	ICM7218E IDL	Common Anode	40 Lead Ceramic

CHIP TOPOGRAPHY ICM7218A



PIN CONFIGURATION (OUTLINE DRAWING JI)

ICM7218A



Note: Pins 5, 6, 7, 10 are under control of Mode pin 9. See page 6-60.

See page 6-57 for other device configurations.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V
Digit Output Current	300mA
Segment Output Current	50mA
Input Voltage (any terminal)	V^+ +0.3V to V^- −0.3V NOTE 1
Power Dissipation (28 Pin CERDIP)	1 W NOTE 2
Power Dissipation (28 Pin Plastic)	0.5 W NOTE 2
Power Dissipation (40 Pin Ceramic)	1 W NOTE 2
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	−55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

SYSTEM ELECTRICAL CHARACTERISTICS

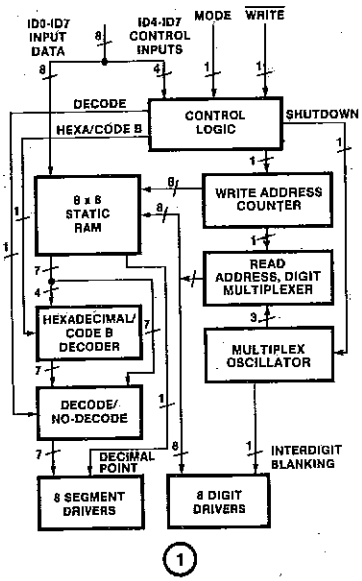
$V^+ = 5V \pm 10\%$; $T_A = 25°C$, Test Circuit, Display Diode Drop 1.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+		4		6	V
		Power Down Mode	2		6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	μA
Operating Supply Current	I_{OP}	Decoder On, Outputs Open Ckt	250		950	μA
		No Decode, Outputs Open Ckt	200		450	μA
Digit Drive Current	I_{DIG}	Common Anode Vout = V^+ −2.0	−170			mA
		Common Cathode Vout = V^- +1V	50			mA
Digit Leakage Current	I_{DLK}				100	μA
Peak Segment Drive Current	I_{SEG}	Common Anode Vout = V^- +1.5V	20	25		mA
		Common Cathode Vout = V^+ −2.0V	−10			mA
Segment Leakage Current	I_{SLK}				50	μA
Display Scan Rate	f_{MUX}	Per Digit		250		Hz
Three Level Input						
Logical "1" Input Voltage	V_{INH}	Hexidecimal ICM7218C, D (Pin 9)	4.0			V
Floating Input	V_{INF}	Code B ICM7218C, D (Pin 9)	2.0		3.0	V
Logical "0" Input Voltage	V_{INL}	Shutdown ICM7218C, D (Pin 9)			1.75	V
Three Level Input Impedance	Z_{IN}	Note 3		100		kΩ
Logical "1" Input Voltage	V_{IH}		3.5			V
Logical "0" Input Voltage	V_{IL}				.8	V
Write Pulse Width (Negative)	t_W	7218A, B	550	400		ns
Write Pulse Width (Positive)	$t_{\overline{W}}$	7218A, B	550	400		ns
Write Pulse Width (Negative)	t_W	7218C, D, E	400	250		ns
Write Pulse Width (Positive)	$t_{\overline{W}}$	7218C, D, E	400	250		ns
Mode Hold Time	t_{mh}	7218A,B		150		ns
Mode Pulse Width	t_m	7218A, B	500			ns
Data Set Up Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		25			ns
Digit Address Set Up Time	t_{das}	ICM7218C, D, E	500			ns
Digit Address Hold Time	t_{dah}	ICM7218C, D, E	100			ns
Data Input Impedance	Z_{IN}	5-10 pF Gate Capacitance		10^{10}		Ohms

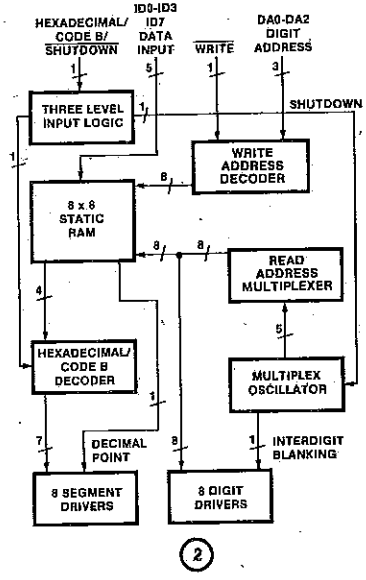
NOTE 3: In the ICM7218C and D (random access versions) the Hexa/Code B/$\overline{\text{Shutdown}}$ input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50μA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

BLOCK DIAGRAMS

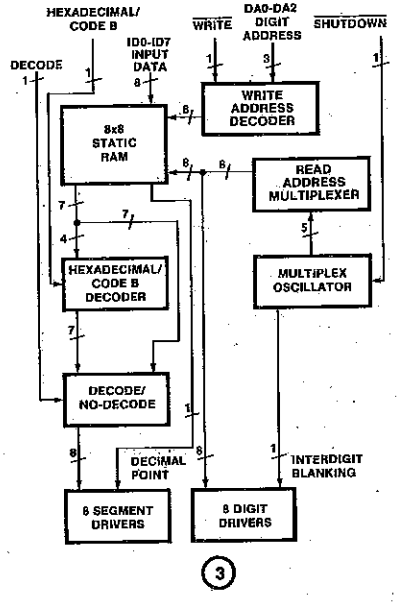
ICM7218A, ICM7218B



ICM7218C, ICM7218D

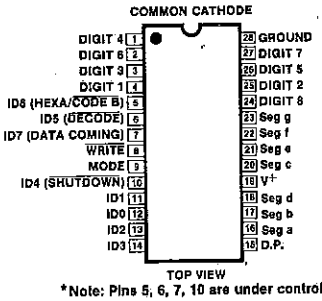


ICM7218E



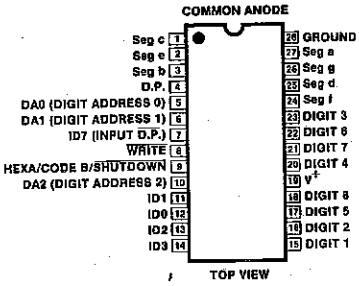
PIN CONFIGURATIONS (See page 6-65 for ICM7218A)

ICM7218B* (OUTLINE DRAWING PI)

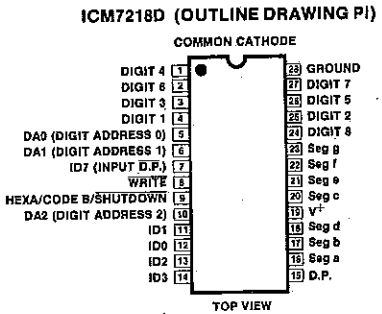


*Note: Pins 5, 6, 7, 10 are under control of Mode pin 9. See page 6-60.

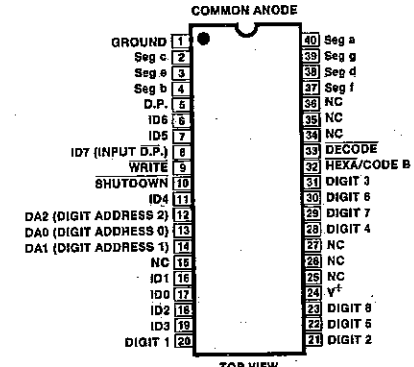
ICM7218C (OUTLINE DRAWING JI)



ICM7218D (OUTLINE DRAWING PI)



ICM7218E (OUTLINE DRAWING DL)



INPUT DEFINITIONS ICM7218A and B

INPUT		TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{WRITE}}$		8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
MODE		9	High Low	Load Control Word on Write Pulse Load Input Data on Write Pulse
ID4 $\overline{\text{SHUTDOWN}}$	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder, and Displays Disabled)
ID5 ($\overline{\text{DECODE}}$/No Decode)	MODE High	6	High Low	No Decode Decode
ID6 (HEXAdecimal/CODE B)	MODE High	5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING - Control Word)	MODE High	7	High Low	Data Coming No Data Coming } Control Word
Input Data ID0-ID7*	MODE Low	11,12,13, 14,5,6 10,7	High Low	Loads "One" (Note 2) Loads "Zero" (Note 2)

*ID0-ID3 = Don't care when writing control word
ID4-ID7 = Don't care when writing Hex/Code B
(The display blanks on ICM7218A/B versions when writing in Data)

INPUT DEFINITIONS ICM7218C and D

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{WRITE}}$	8	High Low	Inputs Not Loaded Into Memory Inputs Loaded Into Memory
Three Level Input (Note 1)	9	High Floating Low	Hexadecimal Decode Code B Decode Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address DA2 (MSB)-DA0 (LSB)	10,6,5	High Low	Loads "Ones" Loads "Zeros"
Input Data ID3 (MSB) - ID0 = Data ID7 = $\overline{\text{D.P.}}$	14,13,11,12 7	High Low	Loads "Ones" (Note 2) Loads "Zeros" (Note 2)

INPUT DEFINITIONS ICM7218E

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{WRITE}}$	9	High Low	Input Latches Not Updated Input Latches Updated
$\overline{\text{SHUTDOWN}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address (0,1,2) DA0-DA2	13,14,12	High Low	Loads "Ones" Loads "Zeros"
$\overline{\text{DECODE}}$/No Decode	33	High Low	No Decode Decode
$\overline{\text{HEX}}$Adecimal/CODE B	32	High Low	Code B Decoding Hexadecimal Decoding
Input Data ID0-ID7	16,17,18,19 6 7,11,8	High Low	Loads "Ones" (Note 2) Loads "Zeros" (Note 2)

NOTE 1 In the ICM7218C and ICM7218D versions, Hexadecimal, Code B and Shutdown are controlled with a three level input on Pin 9. Pulling Pin 9 high decodes Hexadecimal. Floating Pin 9 decodes Code B and pulling Pin 9 low puts the ICM7218 in a Shutdown mode.

NOTE 2 In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents "on" segments, (i.e. segments are positive true, decimal point is negative true).

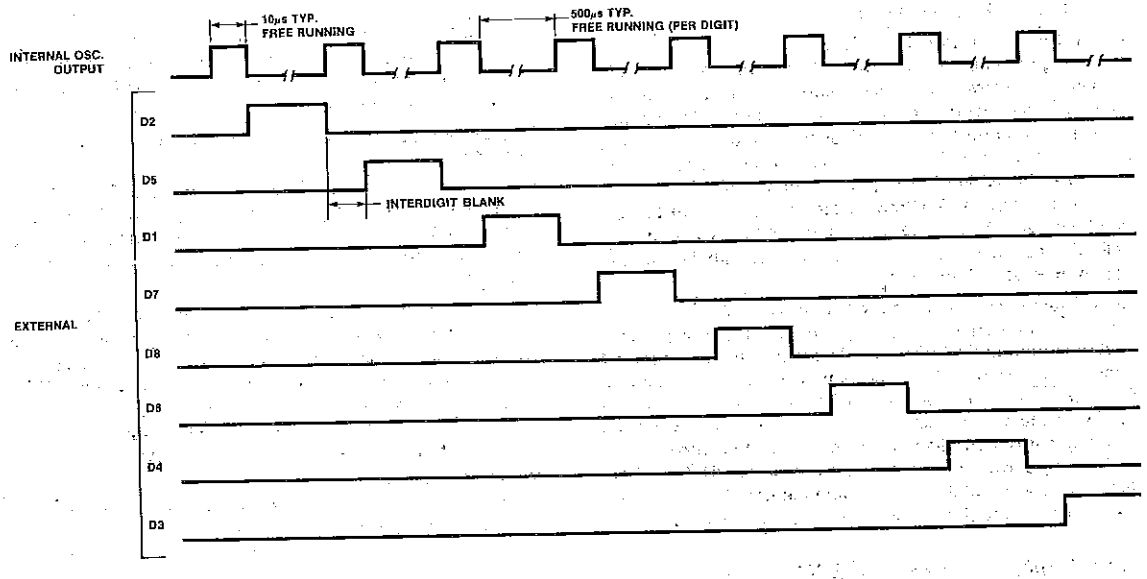


Figure 1: Multiplex Timing

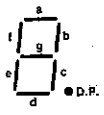


Figure 2: Segment Assignments

DECODE/No Decode

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or 2 Binary codes plus decimal point (5 bits per digit). The 7 segment decoder on chip may be disabled if direct segment information is inputted.

In the No Decode format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: D.P. a b c e g f d

In this format, "Ones" represents on segments for all inputs except for the Decimal Point, where "zero' represents on segments.

HEXAdecimal or CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (—), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Binary Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexa Code	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
Code B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(Blank)

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically 10μA at $V^+ = 5$), turns off both the digit and segment drivers, stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown - only the output and read sections of the device are disabled.

Powerdown

In a Shutdown Mode, the supply voltage may be reduced to 2 volts without data being lost in memory. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With 5 segments being driven, this is equal to about 40mA per segment peak drive or 5mA average drive. The common cathode drive is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes to ensure that segment information is correct before the next digit drive thereby avoiding ghosting.

Leading Zero Blanking

This may be programmed into chip memory in the no-decode operation (each segment programmed for a zero for the blanked digits) or by using the 16th state (binary 15) with the Code B decoder.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to parallel connect digit drives together. For example, by paralleling pairs of digit drives together to drive a 4 digit display 10 mA average segment drive can be obtained.

APPLICATIONS, continued

Power Dissipation Considerations
Assuming common anode drive at $V^+ = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will, therefore, be 640mW rising to about 900mW for all '8"s displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Serial Input Drive Considerations (ICM7218A/B)
The control instructions are read from the input bus lines if MODE is high and $\overline{\text{WRITE}}$ low. The instructions occur on 4 lines and are - Decode/no Decode, type of Decode (if desired), $\overline{\text{SHUTDOWN}}$/no Shutdown and DATA COMING/not Coming. After the control instructions have been read (with Data Coming instruction) display data can be written into memory with each following negative going pulse of $\overline{\text{WRITE}}$, MODE being low. After all 8 words or digit memory locations have been written, additional transitions of the state of $\overline{\text{WRITE}}$ are ignored. It is not possible to change one individual digit without refreshing the data for all the other digits. (This can, however, be achieved with the ICM7218C/D/E where the digits are individually addressed.)

Random Access Input Drive Considerations (ICM7218C/D/E)
Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{WRITE}}$ pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs (which define the digit where the data is to be written into the memory) and apply a negative going WRITE pulse. For example, it is possible to change only digit 7 without refreshing the data for all the other digits. (However, this cannot be achieved with the ICM7218A/B.)

Supply Capacitor
A 0.1μF capacitor is recommended between V^+ and GROUND to bypass multiplex noise.

SWITCHING WAVEFORMS ICM7218

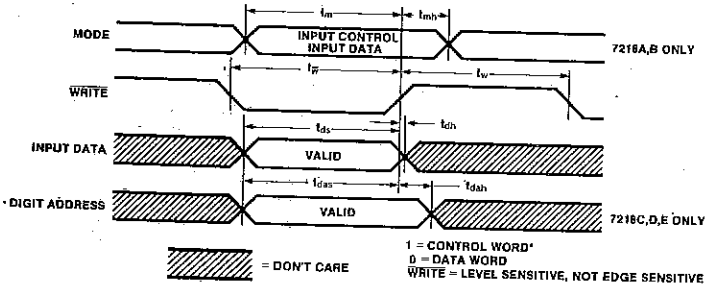


Figure 3

CHIP ADDRESS SEQUENCE ICM7218A and B

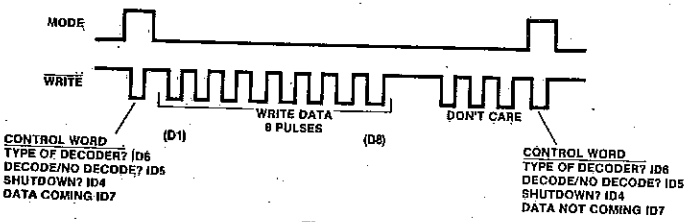


Figure 4

CHIP ADDRESS SEQUENCE EXAMPLE ICM7218C/D/E

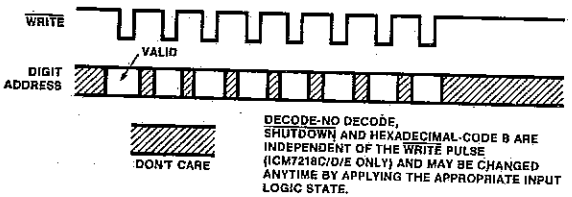
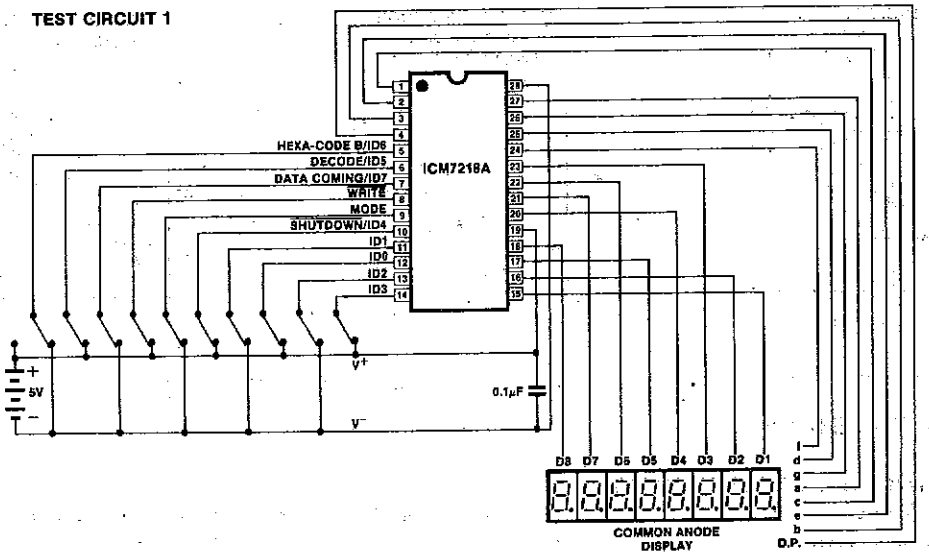


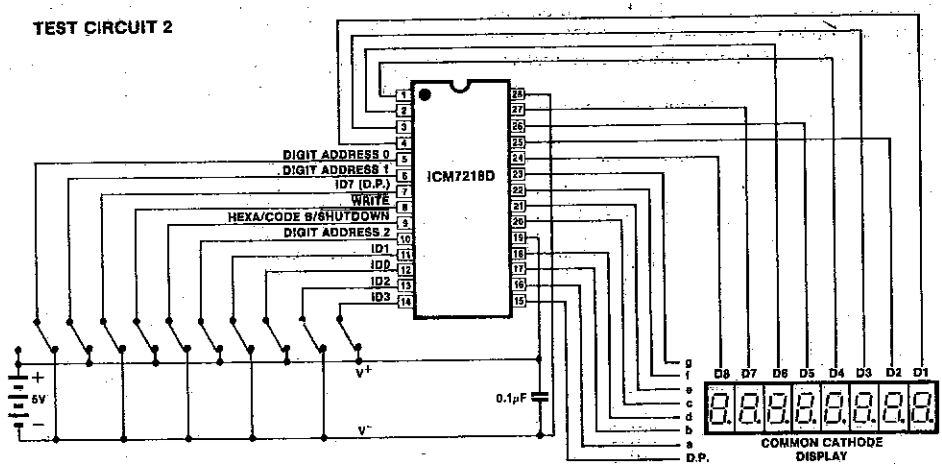
Figure 5

TEST CIRCUITS

TEST CIRCUIT 1

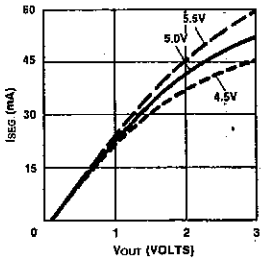


TEST CIRCUIT 2

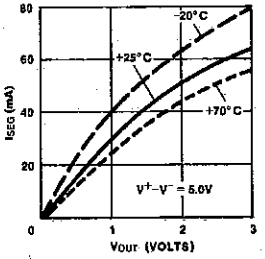


TYPICAL CHARACTERISTICS

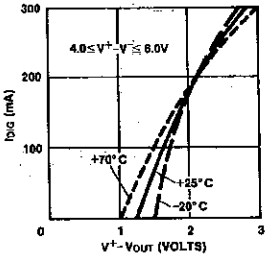
COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT} AT 25°C



COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT}

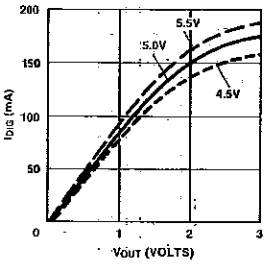


COMMON ANODE DIGIT DRIVER
I_{DIG} vs. $(V^+ - V_{OUT})$

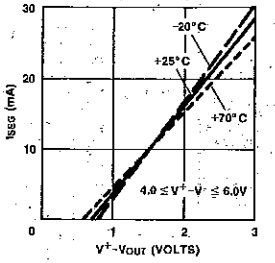


TYPICAL CHARACTERISTICS, CONTINUED

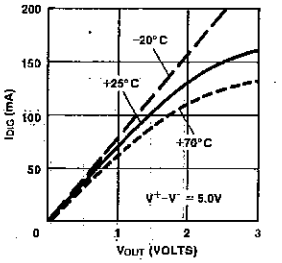
COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}
AT 25°C



COMMON CATHODE SEG. DRIVER
I_{SEG} vs. $(V^+ - V_{OUT})$



COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}



APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

The display interface (ICM7218) is shown with an MCS-48 family microprocessor. The 8 bit data bus DB0/DB7-ID0/ID7 transfers control and data information to the 7218 display interface on successive $\overline{WRITE}$ pulses. When MODE is high a control word is transferred. MODE low allows data transfer on a $\overline{WRITE}$ pulse. Eight memory address locations in the 8 x 8 static memory are automatically sequenced on each successive $\overline{WRITE}$ pulse. After eight $\overline{WRITE}$ pulses have occurred, further pulses are ignored and the display interface returns to normal display operation until a new control word is transferred. See Figure 4. This also allows writing to other peripheral devices without disturbing the ICM7218 A/B.

Decoding of the stored data in memory is defined by the control word and may be decoded in Hexadecimal, Code B, or No-Decode formats.

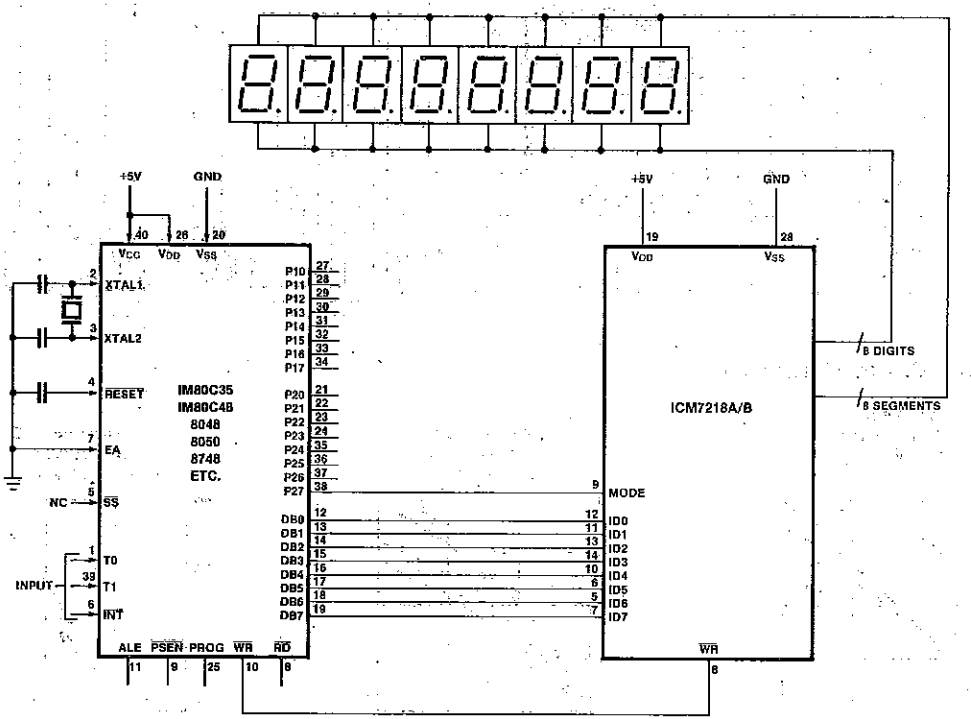


Figure 6: 8 Digit Microprocessor Display

16 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the MCS-48 I/O bus (DB7-DB0) is transferred to both ICM7218 (ID3-ID0) simultaneously, 4 bits + 4 bits on $\overline{\text{WRITE}}$ enable.

Display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded sequentially on a single 8 bit data bus, ie D0 D1, D2 D3, D4 D5, etc..

Decimal point information (from the processor, P26-P27) is supplied to the ICM7218 on bus lines ID7 to both devices.

Choice of decoding is available in either Hexadecimal or Code-B format by hardwiring or decoding to a Three Level format on Pin 9 of the ICM7218.

Multiplexing is asynchronous with respect to the microprocessor and is completely performed by the ICM7218.

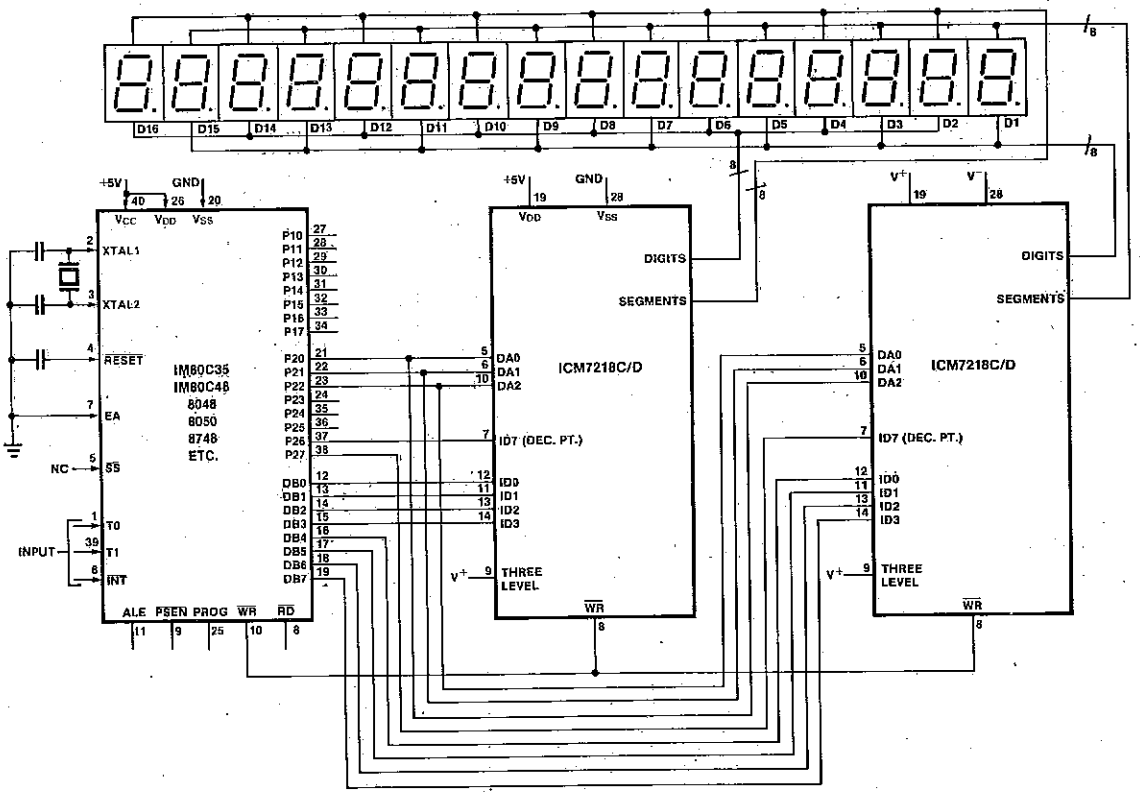


Figure 7: 16 Digit Display

NO DECODE APPLICATION

The ICM7218 can be used as a microprocessor based LED status panel driver. The microprocessor selected control word would include "No Decode" and "Data Coming". The computer then outputs word oriented "Ones" and "Zeroes" to indicate on-off states. This data is read into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 "segments" x 8 digits = 64 dots ÷ 2 per red or green = 32 channels). With red, yellow and green, 21 channels can be accommodated.

Additional ICM7218's may be bussed and addressed (see Figures 6 and 7) to expand the status panel capacity. Note per figure 4 that after the ICM7218A/B has been read in its data (8 $\overline{\text{WRITE}}$ pulses), it ignores additional information on the data lines. A new control word must be received before the next write sequence can be accommodated. Consequently, by address decoding and $\overline{\text{WRITE}}$ pulse enabling, numerous ICM7218's can be bussed together to allow a large number of indicator channels.

ICM7224 (LCD)
ICM7225 (LED)
4½-Digit Counter/ Decoder/Drivers

FEATURES

- High frequency counting—guaranteed 15MHz, typically 25MHz at 5V
- Low power operation—less than 100μW quiescent
- STORE and RESET inputs permit operation as frequency or period counter
- True COUNT INHIBIT disables first counter stage
- CARRY output for cascading four-digit blocks
- Schmitt-trigger on the COUNT input allows operation in noisy environments or with slowly changing inputs
- Leading Zero Blanking INput and OUTput for correct leading zero blanking with cascaded devices
- LCD devices provide complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal
- LED devices provide BRightness input which can function digitally as a display enable or with a single potentiometer as a continuous display brightness control

GENERAL DESCRIPTION

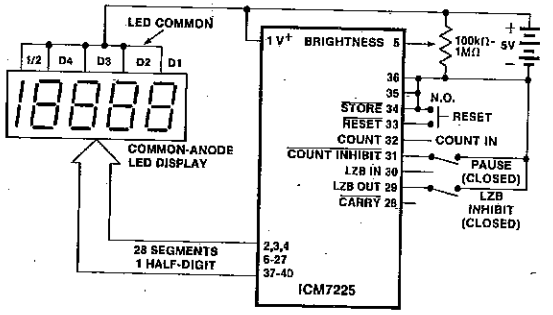
The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry, which allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In LED systems, the BRightness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic package.

TYPICAL APPLICATION (UNIT COUNTER)

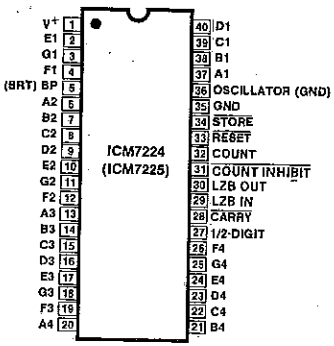


ORDERING INFORMATION

	ORDER PART NUMBER	COUNT OPTION
LCD DISPLAY	ICM7224 IPL	19999
	ICM7224A IPL	15959
LED DISPLAY	ICM7225 IPL	19999
	ICM7225A IPL	15959

Evaluation Kits, order ICM7224 EV/Kit or ICM7225 EV/Kit

PIN CONFIGURATION (outline dwg PL)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 70°C
Supply Voltage (V^+) 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, −0.3V
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.
NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

(All Parameters measured with $V^+ = 5V$ unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{DD}	Test circuit, Display blank		10	50	µA
Operating supply voltage range	V^+		3	5	6	V
OSCILLATOR input current	I_{OSCI}	Pin 36		±2	±10	µA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		µs
BackPlane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		µs
Oscillator frequency	f_{osc}	Pin 36 Floating		19		KHz
Backplane frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (BRighTness) at GROUND Pins 29, 31-34 at V^+		10	50	µA
Operating supply voltage range	V^+		4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment on current	I_{SEG}	Segment On, Vout = + 3V	5	8		mA
Half-digit on current	I_H	Half-digit on, Vout = + 3V	10	16		mA

FAMILY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 Vout = V^+ - 3V		10		µA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			1	V
$\overline{COUNT}$ Input Threshold	V_{CT}			2		V
$\overline{COUNT}$ Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = $V^+ - 3V$	350	500		µA
Output Low Current	I_{OL}	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = +3V	350	500		µA
Count Frequency	f_{count}	4.5V < V^+ < 6V	0	DC-25	15	MHz
$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width	t_S,t_R		3			µs

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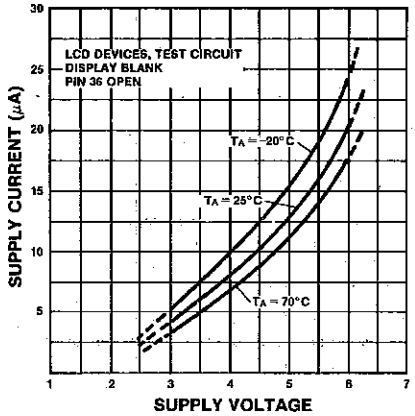
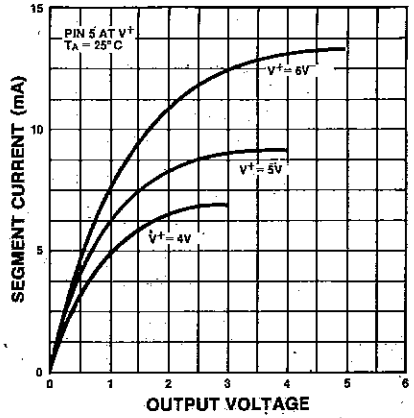
TYPICAL CHARACTERISTICS

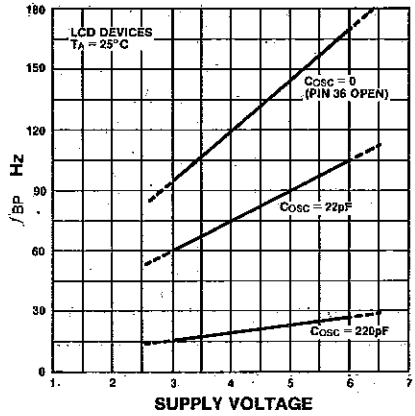
7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



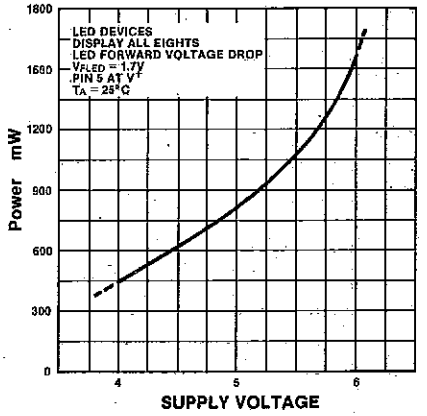
7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



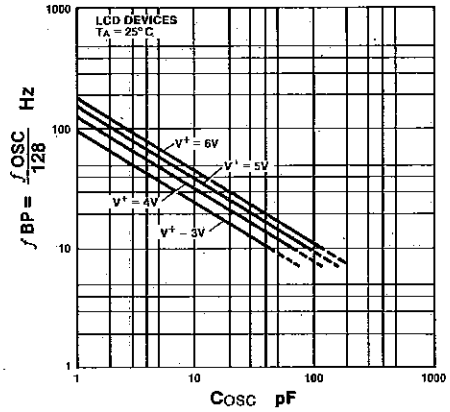
7224 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



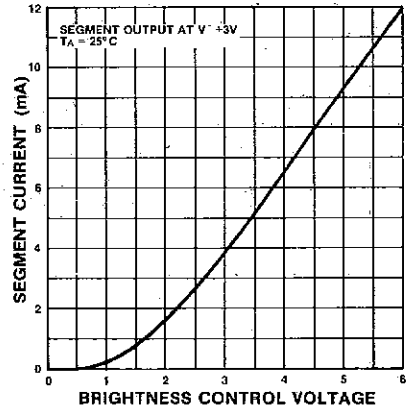
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



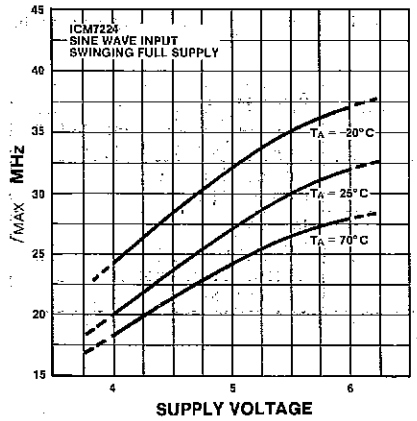
7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}



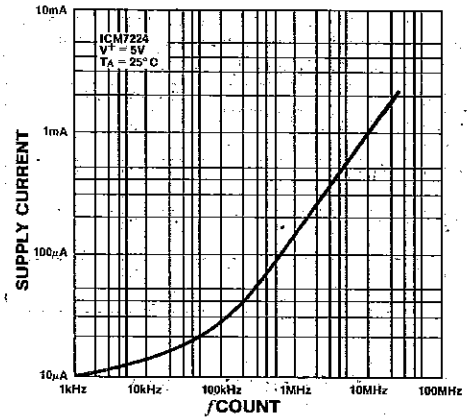
7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



MAXIMUM COUNT FREQUENCY (TYPICAL)
AS A FUNCTION OF SUPPLY VOLTAGE

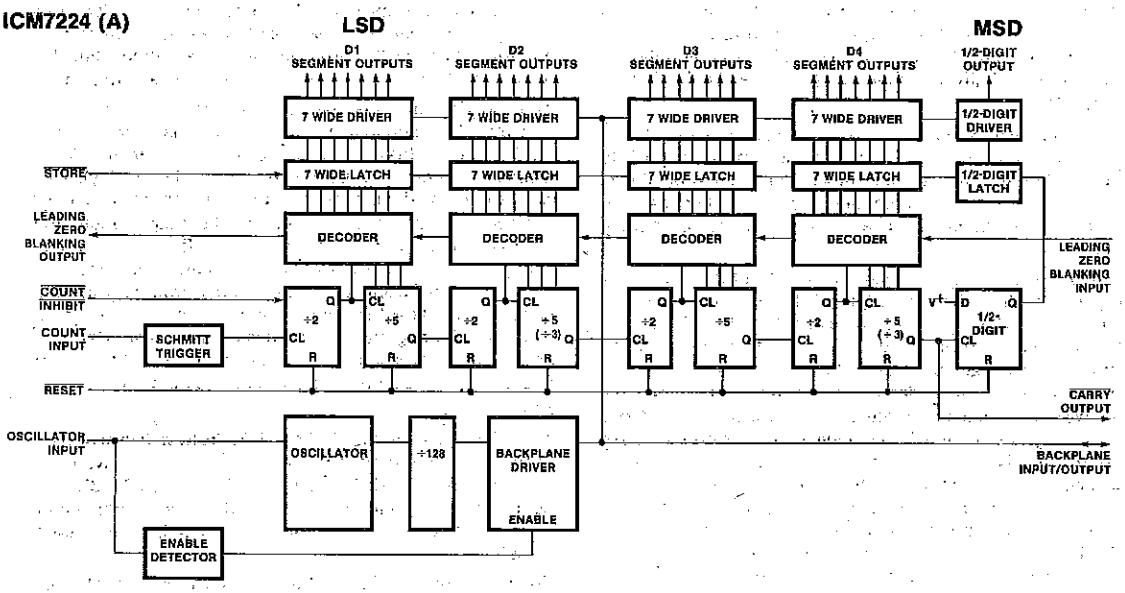


SUPPLY CURRENT AS A FUNCTION
OF COUNT FREQUENCY

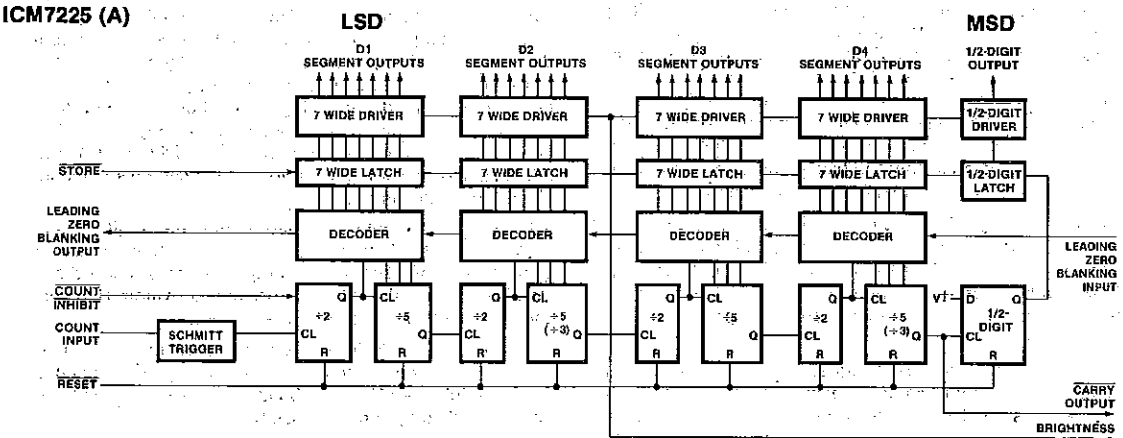


BLOCK DIAGRAMS

ICM7224 (A)



ICM7225 (A)



CONTROL INPUT DEFINITIONS

In this table, V^+ and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking INput	29	V^+ or Floating GROUND	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V^+ or Floating GROUND	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V^+ or Floating GROUND	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V^+ or Floating GROUND	Output Latches not Updated Output Latches Updated

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional 4½-digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

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The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to GROUND. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1–2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19KHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V^+; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving 4½-digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at ground, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for ground; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (–15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

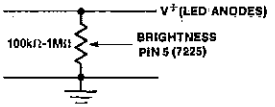


Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the $\overline{\text{CARRY}}$ signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, while the $\overline{\text{CARRY}}$ output provides a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

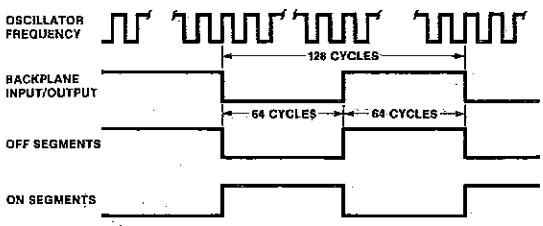
Each decade of counter drives directly into a four-to-seven decoder which develops the seven-segment output code. The output data is latched at the driver; when the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes; when low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

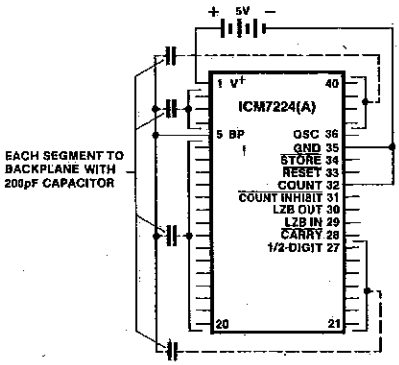
For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit device would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 or ICM7225 devices in four-digit blocks.

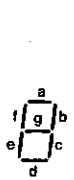
DISPLAY WAVEFORMS

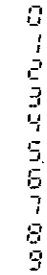


TEST CIRCUIT



SEGMENT ASSIGNMENT AND DISPLAY FONT

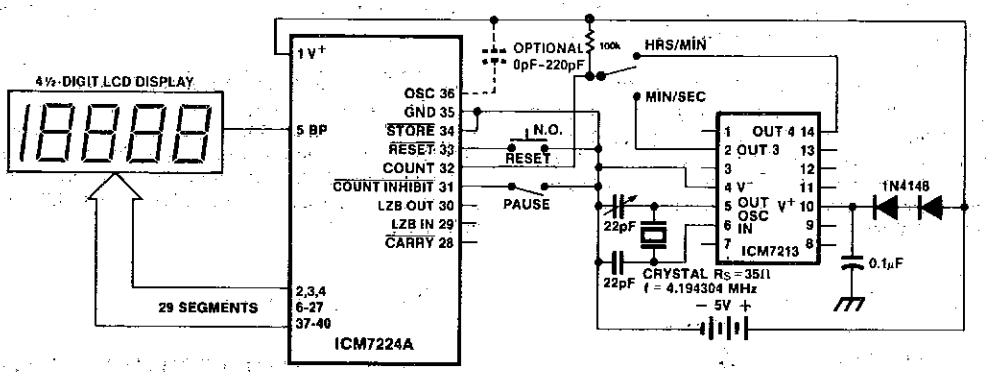




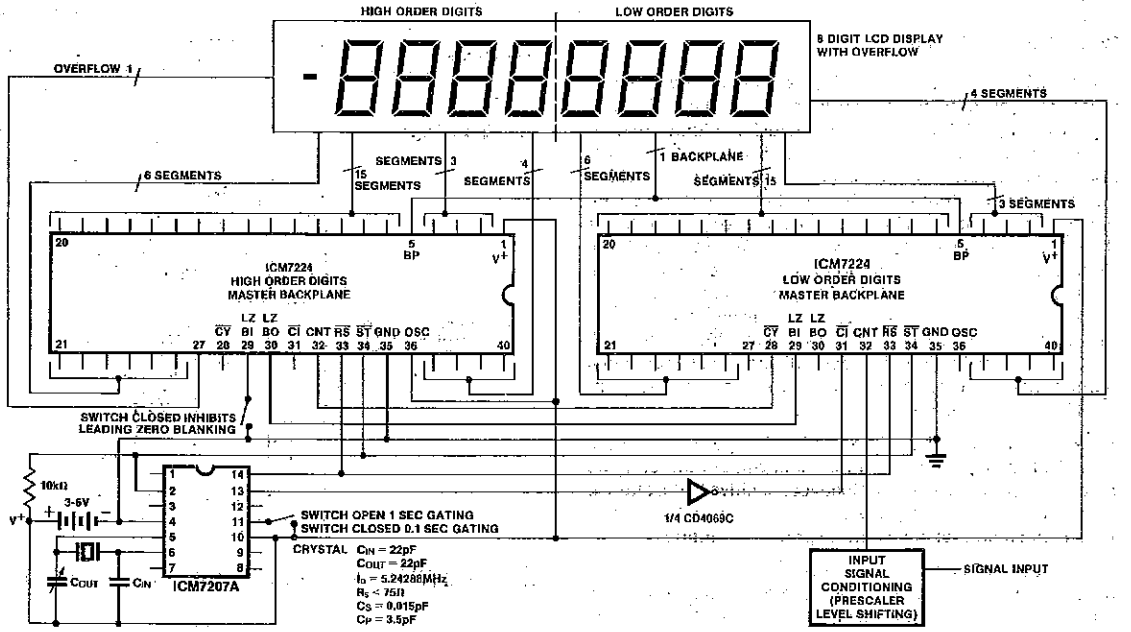
(BLANK)

APPLICATIONS

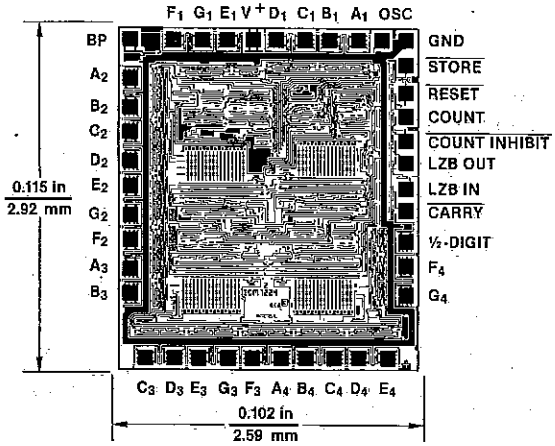
1. Two-Hour Precision Timer



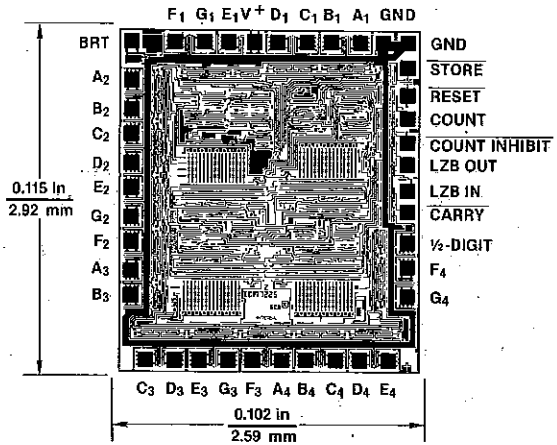
2. Eight-Digit Precision Frequency Counter



CHIP TOPOGRAPHIES



ICM7224



ICM7225

ICM7226A/B

10MHz Universal Counter System for LED Displays

FEATURES

- **CMOS design for very low power**
- **Output drivers directly drive both digits and segments of large 8 digit LED displays. Both common anode and common cathode versions are available**
- **Measures frequencies from DC to 10MHz; periods from 0.5μs to 10s**
- **Stable high frequency oscillator uses either 1MHz or 10MHz crystal**
- **Control signals available for external systems operation**
- **Multiplexed BCD outputs**

APPLICATIONS

- **Frequency Counter**
- **Period Counter**
- **Unit Counter**
- **Frequency Ratio Counter**
- **Time Interval Counter**

ORDERING INFORMATION

DISPLAY	DEVICE	PACKAGE	ORDER NUMBER
Common Anode	ICM7226A	CERDIP	ICM7226AIJL
		DICE	ICM7226A/D
Common Cathode	ICM7226B	Plastic	ICM7226BIPL
		DICE	ICM7226B/D

NOTE: An evaluation kit is available for these devices — order ICM7226AEV/KIT.

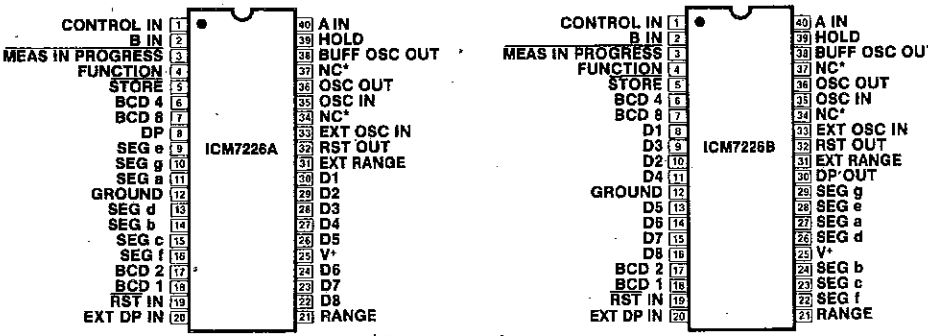
GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in **frequency** and **unit counter** modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval**, the 10MHz timebase gives a 0.1μsec resolution. In **period average** and **time interval average**, the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode display with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

PIN CONFIGURATION (outline dwgs JL, PL)



*For maximum frequency stability, connect to V^+ or GROUND

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
*Voltage on any Input or
Output Terminal (Note 1) ..... Not to exceed V^+ or GND by more than 0.3V
Maximum Power Dissipation at 70°C (Note 2)
ICM7226A 1.0W
ICM7226B 0.5W
Maximum Operating Temperature Range ..... −20°C to +85°C
Maximum Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Note 1: Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V^+ or GROUND by 0.3V.

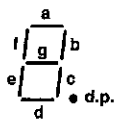
Note 2: Assumes all leads soldered or welded to PC board and free air flow.

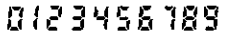
ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Supply Current	I^+_{OP}	Display Off Unused inputs to GROUND		2	5	mA
Supply Voltage Range	V_{SUPP}	−20°C < T_A < 85°C Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
Maximum Guaranteed Frequency Input A, Pin 40	$f_{A(max)}$	−20°C < T_A < 85°C 4.75V < V^+ < 6.0V Figure 1 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5	14		MHz
Maximum Frequency Input B, Pin 2	$f_{B(max)}$	−20°C < T_A < 85°C 4.75V < V^+ < 6.0V Figure 2	2.5			
Minimum Separation Input A to Input B Time Interval Function		−20°C < T_A < 85°C 4.75V < V^+ < 6.0V Figure 3	250			ns
Maximum osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	f_{OSC}	−20°C < T_A < 85°C 4.75V < V^+ < 6.0V	(0.1)	10		MHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$ $T_A = +85°C$	2000			μs
Multiplex Frequency	f_{mux}	f_{osc} = 10 MHz		500		Hz
Time Between Measurements		f_{osc} = 10 MHz		200		ms
Minimum Input Rate of Change	dV_{In}/dt	Inputs A, B		15		mV/μs

SEGMENT IDENTIFICATION AND DISPLAY FONT





LED overflow indicator connections:
Overflow will be indicated on the decimal point output of digit 8.

	CATHODE	ANODE
ICM7226A	d.p.	D_8
ICM7226B	D_8	d.p.

ELECTRICAL CHARACTERISTICS (Continued)

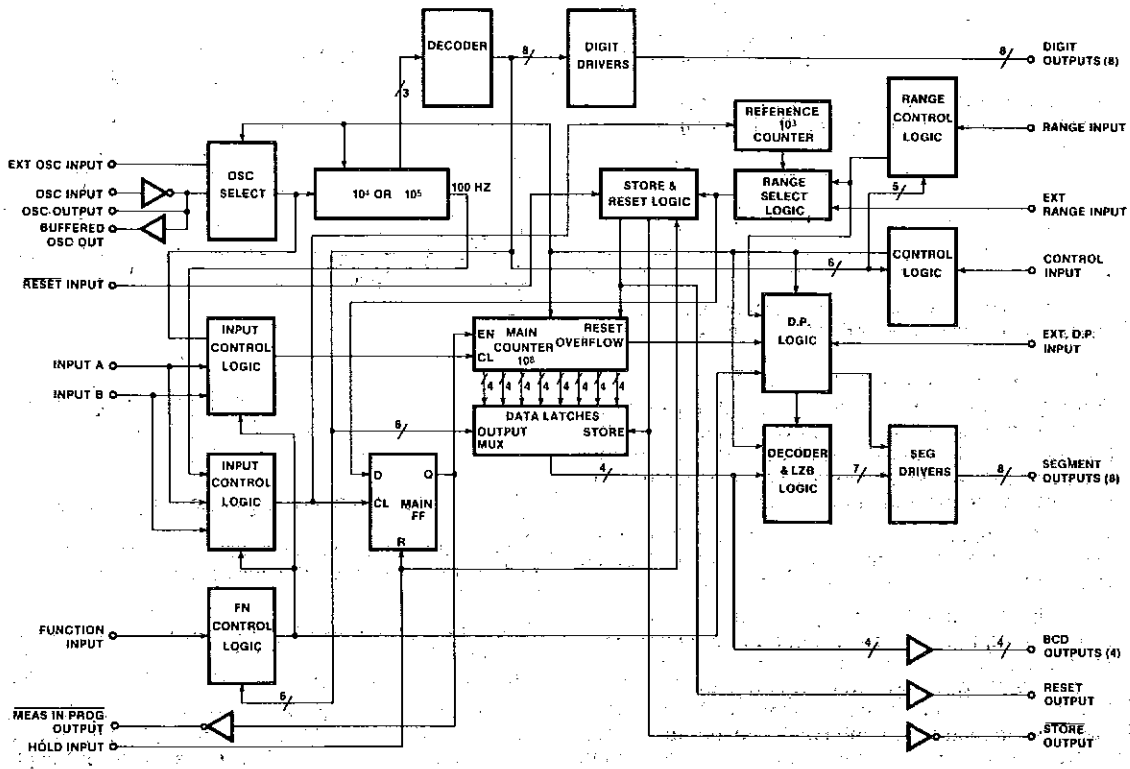
TEST CONDITIONS: $V^+ = 5.0V$, test circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT VOLTAGES PINS 2,19,33,39,40,35						
input low voltage	V_{IL}	$-20°C < T_A < +70°C$	1.0			V
input high voltage	V_{IH}				3.5	
PIN 2, 39, 40 INPUT LEAKAGE, A,B	I_{ILK}				20	µA
Input resistance to V^+ PINS 19,33	R_{IN}	$V_{IN} = V^+ -1.0V$.	100	400		kΩ
Input resistance to GROUND PIN 31	R_{IN}	$V_{IN} = +1.0V$	50	100		
Output Current PINS 3,5,6,7,17,18,32,38	I_{OL}	$V_{OL} = +0.4V$	400			µA
PINS 5,6,7,17,18,32	I_{OH}	$V_{OH} = +2.4V$	100			µA
PINS 3,38	I_{OH}	$V_{OH} = V^+ -0.8V$	265			
ICM7226A PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER						
high output current	I_{OH}	$V_O = V^+ -2.0V$	150	180		mA
low output current	I_{OL}	$V_O = +1.0V$		-0.3		
SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16						
low output current	I_{OL}	$V_O = +1.5V$	25	35		mA
high output current	I_{OH}	$V_O = V^+ -1.0V$		100		µA
MULTIPLEX INPUTS PINS 1,4,20,21						
input low voltage	V_{IL}				0.8	V
input high voltage	V_{IH}		2.0			
input resistance to GROUND	R_{IN}	$V_{IN} = +1.0V$	50	100		kΩ
ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16						
low output current	I_{OL}	$V_O = +1.0V$	50	75		mA
high output current	I_{OH}	$V_O = V^+ -2.5V$		100		µA
SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30						
high output current	I_{OH}	$V_O = V^+ -2.0V$	10	15		mA
leakage current	I_L	V_O = GROUND			10	µA
MULTIPLEX INPUTS PINS 1,4,20,21						
input low voltage	V_{IL}				$V^+ -2.0$	V
input high voltage	V_{IH}		$V^+ -0.8$			
input resistance to V^+	R_{IN}	$V_{IN} = V^+ -1.0V$	200	360		kΩ

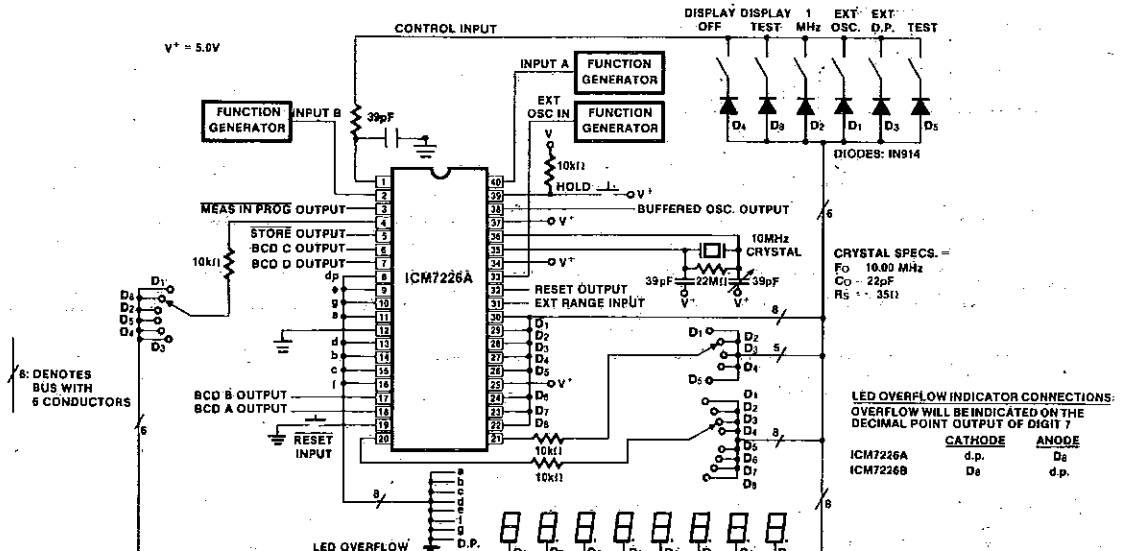
EVALUATION KIT

An evaluation kit is available for the ICM7226. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226. With the help of this kit, an engineer or technician can have the ICM7226 "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIJL, a 10MHz quartz crystal, eight each 7-segment 0.3" LEDs, PC board, resistors, capacitors, diodes, switches and IC socket. Order Number ICM7226AEV/Kit.

BLOCK DIAGRAM



TEST CIRCUIT



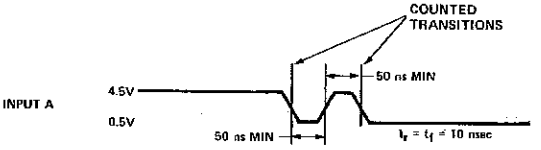


FIGURE 1. Waveform for Guaranteed Minimum $f_{A(max)}$ Function = Frequency, Frequency Ratio, Unit Counter.

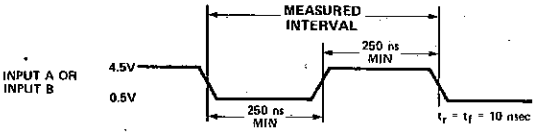


FIGURE 2. Waveform for Guaranteed Minimum $f_{B(max)}$ and $f_{A(max)}$ for Function = Period and Time Interval.

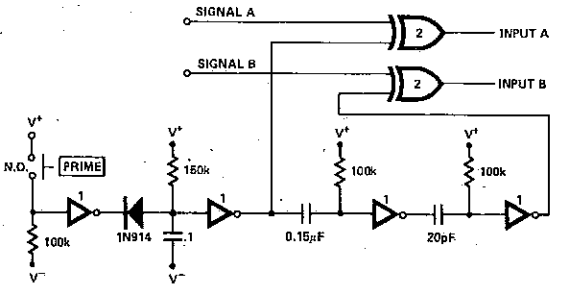
TIME INTERVAL MEASUREMENT

The ICM7226A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can be easily accomplished with the following circuit: (Figure 3b).



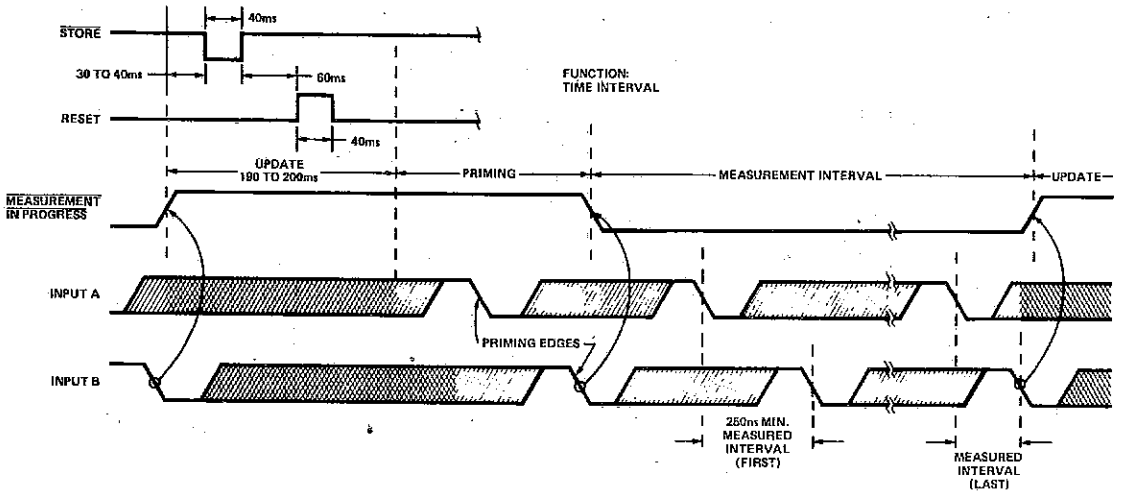
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3b. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A/B as the first alternating signal states automatically prime the device. See Figure 3a.

During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

FIGURE 3a. Waveforms for Time Interval Measurement (Others are similar, without priming phase)

APPLICATION NOTES

GENERAL

INPUTS A & B

The signal to be measured is applied to INPUT A in **frequency period, unit counter, frequency ratio** and **time interval** modes. The other input signal to be measured is applied to INPUT B in **frequency ratio** and **time interval**. f_A should be higher than f_B during **frequency ratio**.

Both inputs are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$ and input impedance of 250kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. Multiplexed Input Control

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	0.01 Sec/1 Cycle	D_1
	0.1 Sec/10 Cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1k Cycles	D_4
PIN 31	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Blank Display	D_4&Hold
	Display Test	D_8
	1MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	Test	D_5
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

CONTROL INPUTS

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be

Display Off - To enable the **display off** mode it is necessary to tie D_4 to the CONTROL input and have the HOLD input at V^+. The chip will remain in this mode until HOLD is switched low. While in the **display off** mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5mA with a 10MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter.)

1MHz Select - The **1MHz select** mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in **period** and **time interval**, since the least significant digit will be in 1μs increments rather than 0.1μs.

External Oscillator Enable - In this mode, the EXTernal OSCillator INput is used, rather than the on-chip oscillator, for the Timebase and Main Counter inputs in **period** and **time interval** modes. The on-chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to **both** OSC IN (pin 35) and EXT OSC IN (pin 33), or provide crystal for "default" oscillation, to avoid hang-up problems.

External Decimal Point Enable - When **external decimal point** is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode - This is a special mode used only in high speed production testing, and serves no other purpose.

RANGE INPUT

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter, or if the EXTernal RANGE INput determines the measurement time. In all functional modes except **unit counter**, a change in the RANGE input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

FUNCTION INPUT

Six functions can be selected. They are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.**

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In **time interval**, a flip flop is set first by a 1→0 transition at INPUT A and then reset by a 1→0 transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow

TABLE 2. Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Osc ON Gate	Osc OFF Gate
Unit Counter(Count A)	Input A	Not Applicable
Osc. Freq. (fosc)	Oscillator	100Hz (Osc ÷ 10^5 or 10^4)

EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input - Except in the **unit counter** mode, when the HOLD input is at V^+, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD Input is at V^+, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

$\overline{\text{RESET}}$ Input - The $\overline{\text{RESET}}$ Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTernal RANGE Input - The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure 4 shows the relationship between MEASurement IN $\overline{\text{PROGRESS}}$ and EXTernal RANGE Input.

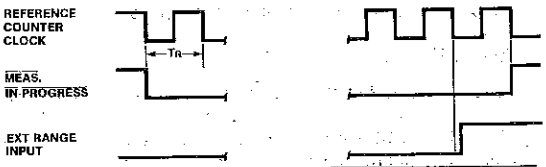


Figure 4: External Range Input to End of Measurement in Progress.

$\overline{\text{MEASUREMENT IN PROGRESS}}$, $\overline{\text{STORE}}$ AND RESET Outputs - These Outputs are provided to facilitate external interfacing. Figure 5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The $\overline{\text{MEASUREMENT IN PROGRESS}}$ output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.

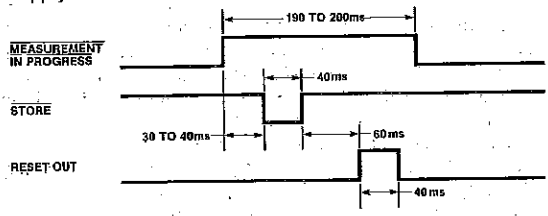


Figure 5: RESET OUT, $\overline{\text{STORE}}$, and $\overline{\text{MEASUREMENT IN}}$

BCD Outputs - The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A - Common Anode) or negative going (ICM7226B - Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load and when interfacing low power Schottky TTL latches, it is necessary to use 1kΩ pull down resistors on the TTL inputs for optimum results. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

TABLE 3 Truth Table BCD Outputs

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFFered OSCillator OUTput - The BUFFered OSCillator OUTput has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244μs, and an interdigit blanking time of 6μs to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the Main Counter overflows. The internal decimal point control displays frequency in kHz and time in μs.

The ICM7226A is designed to drive common anode LED displays at a peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 6, 7, 8 and 9 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

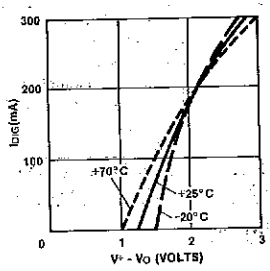


Figure 6: ICM7226A Typical I_{DIG} vs. V^+-V_O $4.5 \leq V^+ \leq 6.0V$

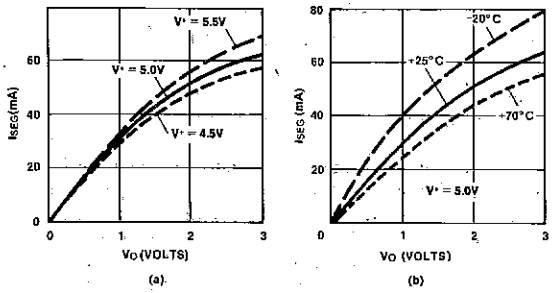


Figure 7: ICM7226A Typical I_{SEG} vs. V_O

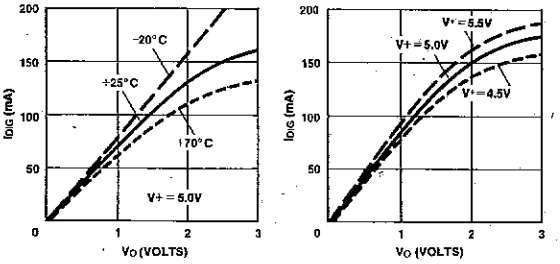


Figure 8: ICM7226B Typical I_{DIG} vs. V_O

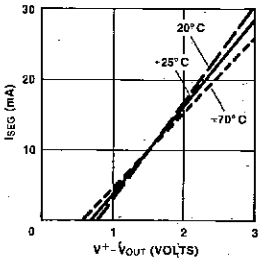


Figure 9: ICM7226B Typical I_{SEG} vs. $(V^+ - V_O)$ $4.5V \leq V^+ \leq 6.0V$

To increase the light output from the displays, V^+ may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

ACCURACY

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode, maximum accuracy is obtained with high frequency inputs, and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10, the least accuracy will be obtained at 10kHz. In **time interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 11. In **frequency ratio** measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 12.

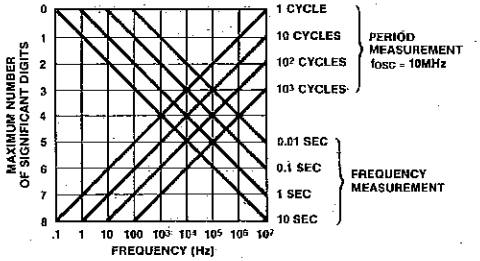


Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

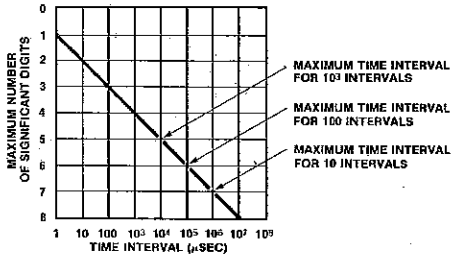


Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

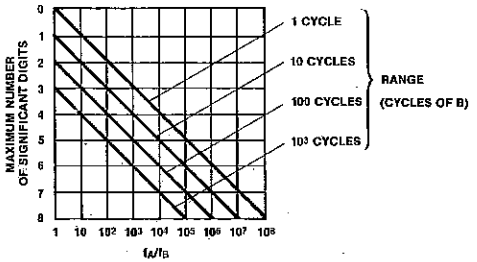


Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and

hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V+ should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in figure 13.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **frequency and period counter**. To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 15 shows use of a ÷10 prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy. Note that A IN comes from Q_C rather than Q_D, to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.

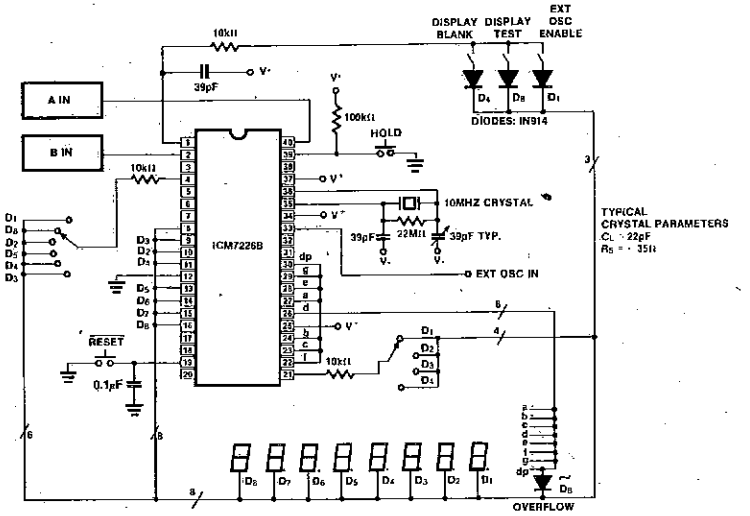
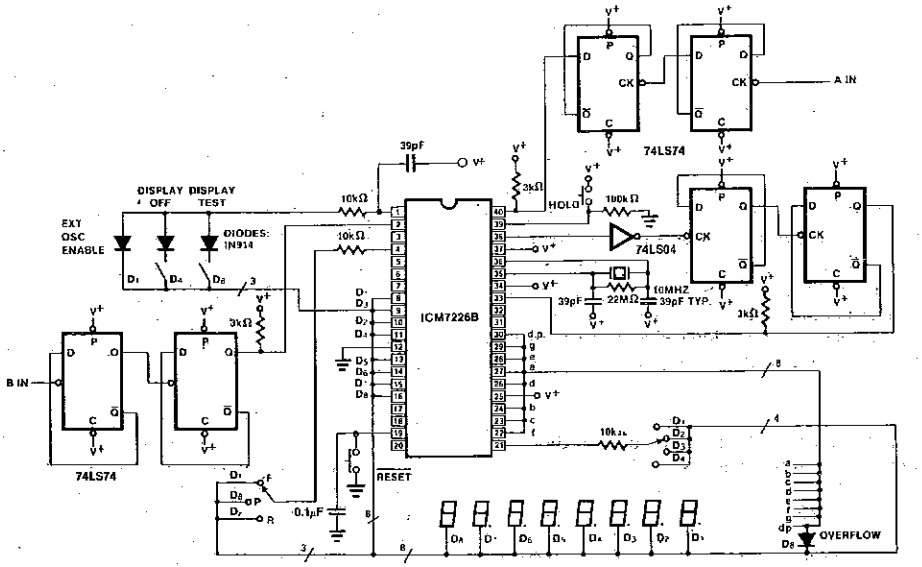


Figure 13: 10MHz Universal Counter



Notes: 1) If a 2.5MHz crystal is used, diode D1 and I.C.'s 1 and 2 can be eliminated.

Figure 14: 40MHz Frequency, Period Counter

Figure 16 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74153 or 74251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

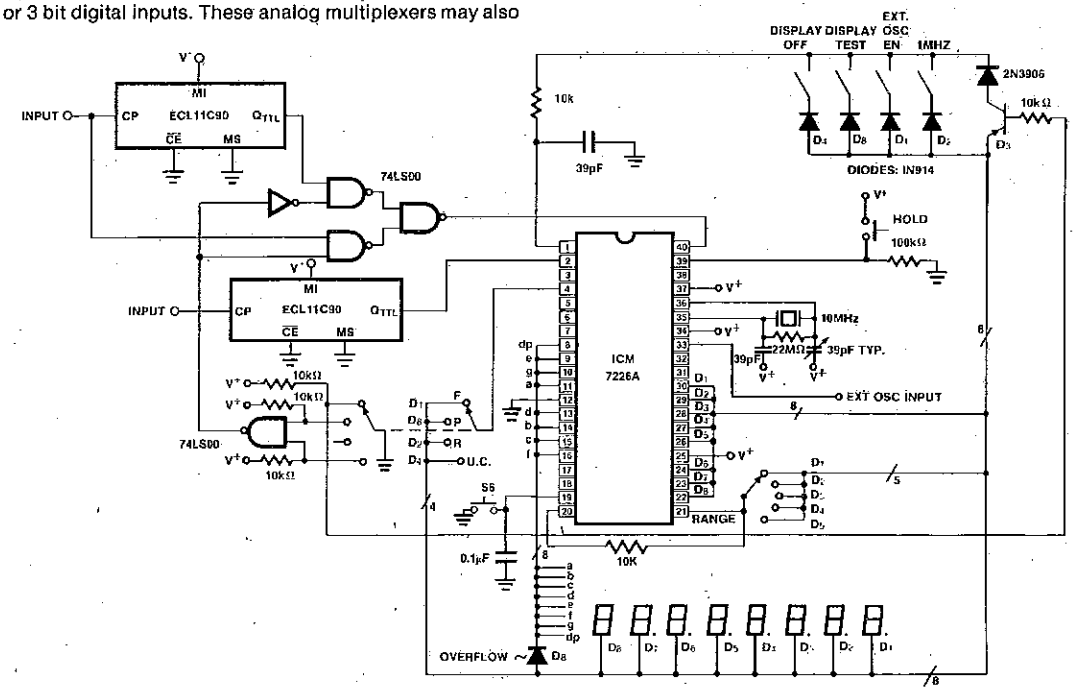


Figure 15: 100MHz Multi Function Counter

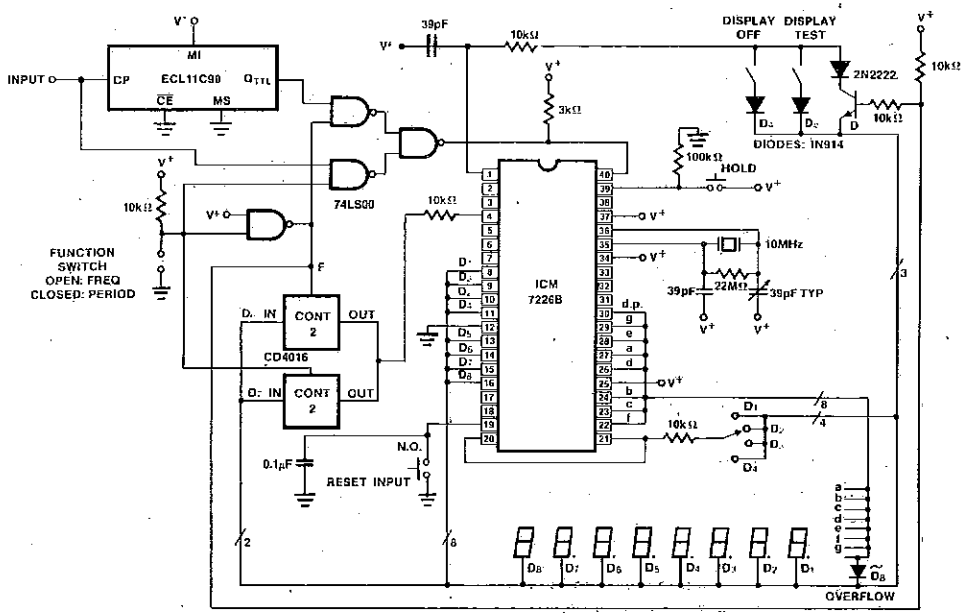
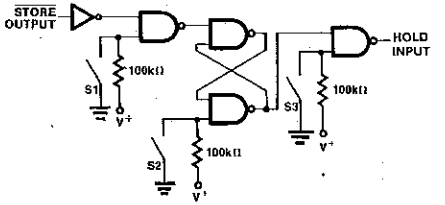


Figure 16: 100MHz Frequency Period Counter

The circuit shown in figure 17 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in figure 18 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 18 on the circuit shown in Figure 14 will reduce the time between measurements from 1600ms to 800ms.



SWITCH	FUNCTION
S1	OPEN = SINGLE MEAS MODE ENABLED
S2	CLOSED = INITIATE NEW MEASUREMENT
S3	CLOSED = HOLD INPUT

Figure 17: Single Measurement Circuit for Use With ICM7226

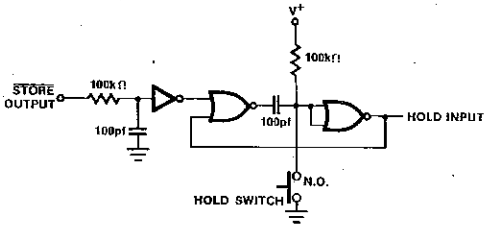


Figure 18: Circuit for Reducing Time Between Measurements

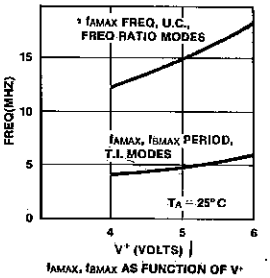


Figure 19: Typical Operating Characteristics

Figure 20 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive 2 ICM7211 display drivers. The ICM7226 EV/Kit may easily be interfaced to 2 ICM7211 EV/Kits in this way. A similar arrangement can be used for driving vacuum fluorescent displays with the ICM7235.

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a load capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{IN} C_{OUT} R_S \left(1+\frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{IN} C_{OUT}}{C_{IN}+C_{OUT}}\right)$

C_O = Crystal static capacitance
R_S = Crystal Series Resistance
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4pF to C_{IN} and C_{OUT}. For maximum frequency stability, C_{IN} and C_{OUT} should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10MHz nor 1MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate is $f_{mux}=\frac{f_{osc}}{2\times10^4}$ for 10MHz mode and $f_{mux}=\frac{f_{osc}}{2\times10^3}$ for the 1MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1MHz mode. The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to V^+.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFfered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator INput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V^+ or GROUND and these two signals should be kept away from the oscillator circuit.

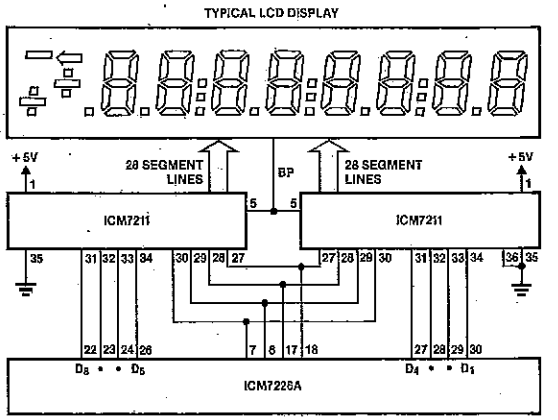
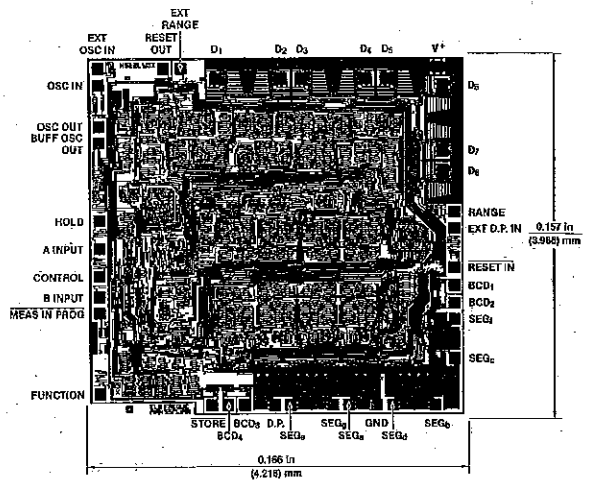
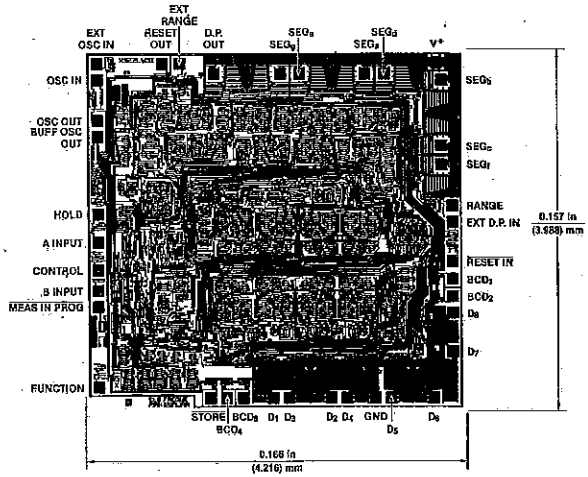


Figure 20: 10MHz Universal Counter System with LCD Display

CHIP TOPOGRAPHIES



ICM7226A



ICM7226B

ICM7231/32/33/34 Display Decoder/Drivers for Triplexed Liquid Crystal Displays

FEATURES

- **ICM7231: Drives 8 digits of 7 segments with two independent annunciators per digit. Address and data input in parallel format.**
- **ICM7232: Drives 10 digits of 7 segments with two independent annunciators per digit. Address and data input in serial format.**
- **ICM7233: Drives 4 characters of 18 segments. Address and data input in parallel format.**
- **ICM7234: Drives 5 characters of 18 segments. Address and data input in serial format.**
- **Chips provide all signals required to drive rows and columns of triplexed LCD display.**
- **Display voltage independent of power supply, allows user control of display operating voltage and temperature compensation if desired.**
- **On-chip oscillator provides all display timing.**
- **Total power consumption typically 200μW, maximum 500μW at 5V.**
- **Low-power shutdown mode retains data with 5μW typical power consumption at 5V, 1μW at 2V.**
- **Direct interfacing to high-speed microprocessors and microcomputers.**

6

GENERAL DESCRIPTION

The ICM7231/7234 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry and contain a mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

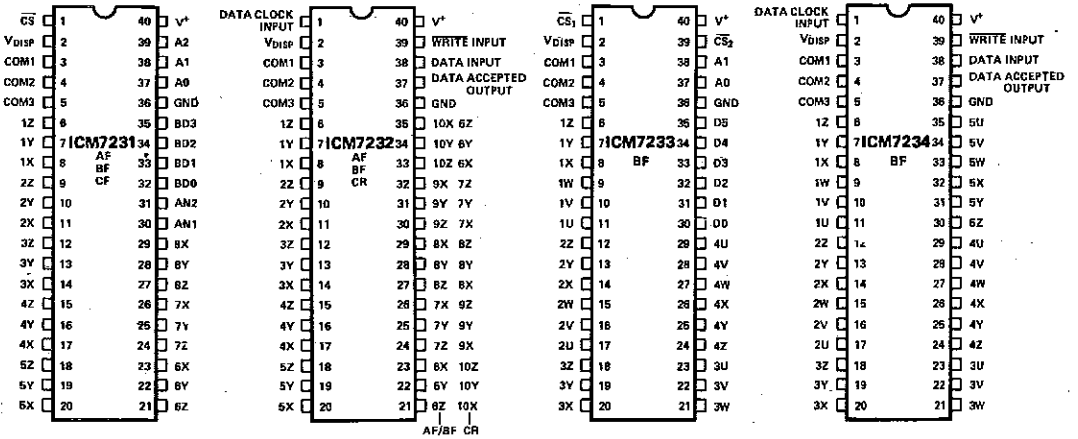
The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits. The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

The ICM7234 uses a serial input structure like that of the ICM7232, and drives five 18-segment characters. Again, the input bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static discharge. Devices are packaged in a 40 pin plastic DIP.

PIN CONFIGURATIONS (outline dwg PL)



OPTION TABLE AND ORDERING INFORMATION

ORDER PART* NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231AFIPL	Hexadecimal	Both Annunciators on COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
ICM7231BFIPL	Code B			
ICM7231CFIPL	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7232AFIPL	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data 2 bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
ICM7232BFIPL	Code B			
ICM7232CRIPL	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7233AFIPL	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7233BFIPL	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Four Characters
ICM7234AFIPL	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Five Characters
ICM7234BFIPL	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

*Dice versions also available (ICM7231AF/D, ICM7233AF/D, etc.) Introductory parts may be available only in CERDIP package. Change suffix to IJL if necessary.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] ..... 0.5 W @ 70°C
Supply Voltage (V^+) ..... 6.5 V
Input Voltage[2] ..... $-0.3 \le V_{IN} \le 6.5$
Display Voltage[2] ..... $-0.3 \le V_{DISP} \le +0.3$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. This limit refers to that of the package and will not be obtained during normal operation.
2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V^+ but not more than 6.5 volts above GND.

6

ELECTRICAL CHARACTERISTICS $V^+ = 5V \pm 10\%$, $T_A = -20°C$ to $+85°C$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Power Supply Voltage	V^+		4.5	>4	5.5	V
Data Retention Supply Voltage	V^+	Guaranteed Retention at 2V	2	1.6		V
Logic Supply Current,	I^+	Current from V^+ to Ground excluding Display. $V_{DISP} = 2V$		30	100	µA
Shutdown Total Current	I_S	V_{DISP} Pin 2 Open		1	10	µA
Display Voltage Range	V_{DISP}	Ground $\le V_{DISP} \le V^+$	0		V^+	V
Display Voltage Setup Current	I_{DISP}	$V_{DISP} = 2V$ Current from V^+ to V_{DISP} On-Chip		15	25	µA
Display Voltage Setup Resistor Value	R_{DISP}	One of Three Identical Resistors in String	40	75		kΩ
DC Component of Display Signals		(Sample Test only)		1/4	1	% (V^+ - V_{DISP})
Display Frame Rate	f_{DISP}	See Figure 2	60	90	120	Hz
Input Low Level	V_{IL}	ICM7231, ICM7233 Pins 30-35, 37-39, 1			0.8	V
Input High Level	V_{IH}		2.0			V
Input Leakage	I_{ILK}	ICM7232, ICM7234 Pins 1, 38, 39		0.1	1	µA
Input Capacitance	C_{IN}			5		pF
Output Low Level	V_{OL}	Pin 37, ICM7232, ICM7234, $I_{OL} = 1mA$,			0.4	V
Output High Level	V_{OH}	$V^+ = 4.5V$, $I_{OH} = -500\mu A$	4.1			V
Operating Temperature Range	T_{OP}	Industrial Range	-20		+85	°C

AC CHARACTERISTICS $V^+ = 5V \pm 10\%, -20°C \leq T_A \leq +85°C$

PARALLEL INPUT (ICM7231, ICM7233) See Figure 12

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
$\overline{\text{Chip Select}}$ Pulse Width	t_{cs}		500	350		ns
Address/Data Setup Time	t_{ds}		200			ns
Address/Data Hold Time	t_{dh}		0	-20		ns
Inter-Chip Select Time	t_{ics}		3			µs

SERIAL INPUT (ICM7232, ICM7234) See Figures 15, 16, 17

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Data Clock Low Time	$t_{\overline{cl}}$		350			ns
Data Clock High Time	t_{cl}		350			ns
Data Setup Time	t_{ds}		200			ns
Data Hold Time	t_{dh}		0	-20		ns
$\overline{\text{Write}}$ Pulse Width	t_{wp}		500	350		ns
$\overline{\text{Write}}$ Pulse to Clock at Initialization	t_{wll}		1.5			µs
Data Accepted Low Output Delay	t_{odl}			200	400	ns
Data Accepted High Output Delay	t_{odh}			1.5	3	µs
Write Delay After Last Clock	t_{cws}		350			ns

6

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF	See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant 4 Bit Binary Data Inputs	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant 3 Bit Digit Address Inputs	Input Address (See Table 2)	
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	

Note:

3. $\overline{CS}$ has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

ICM7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
D0	30	Least Significant ┐	Input Data	HIGH = Logical One (1)
D1	31	├ 6 Bit (ASCII) Data Inputs	See Table 4	LOW = Logical Zero (0)
D2	32			
D3	33			
D4	34			
D5	35	Most Significant ┘		
A0	37	Least Significant ┐ Address Inputs	Input Add. See Table 5	
A1	38	Most Significant ┘		
$\overline{CS1}$	39	Chip Select Inputs (Note 3)	Both inputs LOW load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.	
CS2	1			

Note:
3. $\overline{CS1}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided either by pulling it high when inactive, or ensuring frequent activity.

ICM7232 and ICM7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic. ICM7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits ICM7234 9 bits

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V^+) chip is shutdown; oscillator stops, all display pins to V^+.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On ICM7231/33) (On ICM7232/34)	Drive display segments, or columns.
V^+	40	Chip Positive Supply	
GND	36	Chip Ground	

TRIPLEXING (1/3 MULTIPLEXING) LIQUID CRYSTAL DISPLAYS

Figure 1 shows the connection diagram for a typical 7-segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 2 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 2 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunicator) acts as a capacitance from segment line to common line, shown schematically in Figure 3. Figure 4 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments in Figure 2.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 4 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always 1.92 $V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 5 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7234 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V^+ and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V^+ - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below ground. This can cause device latchup and destruction of the chip.

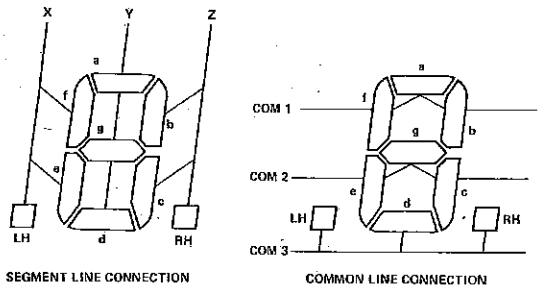
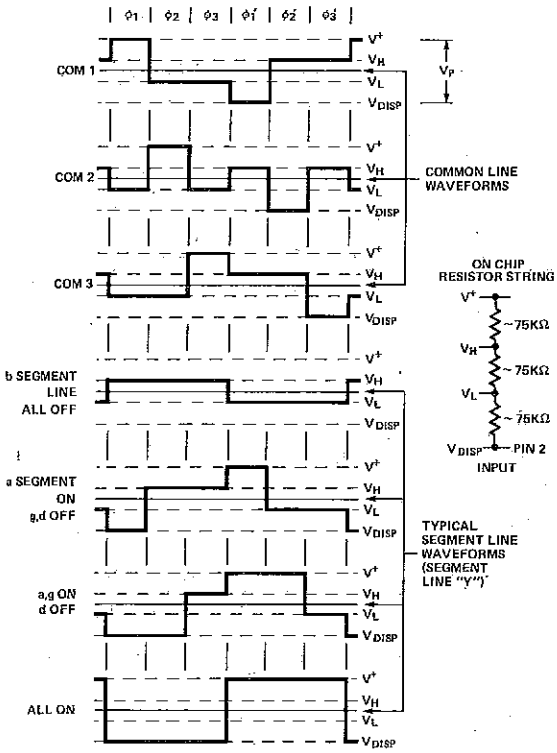


Figure 1. Connection Diagrams for Typical 7-Segment Displays



NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.
$\phi_1', \phi_2', \phi_3'$ – COMMON LOW WITH RESPECT TO SEGMENT.
COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'
COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'
COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

Figure 2. Display Voltage Waveforms

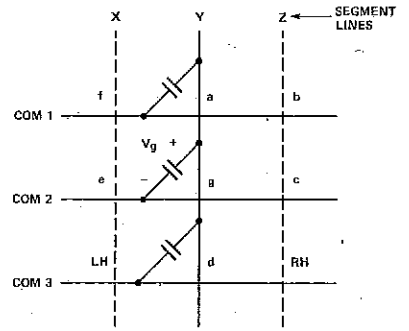


Figure 3. Display Schematic

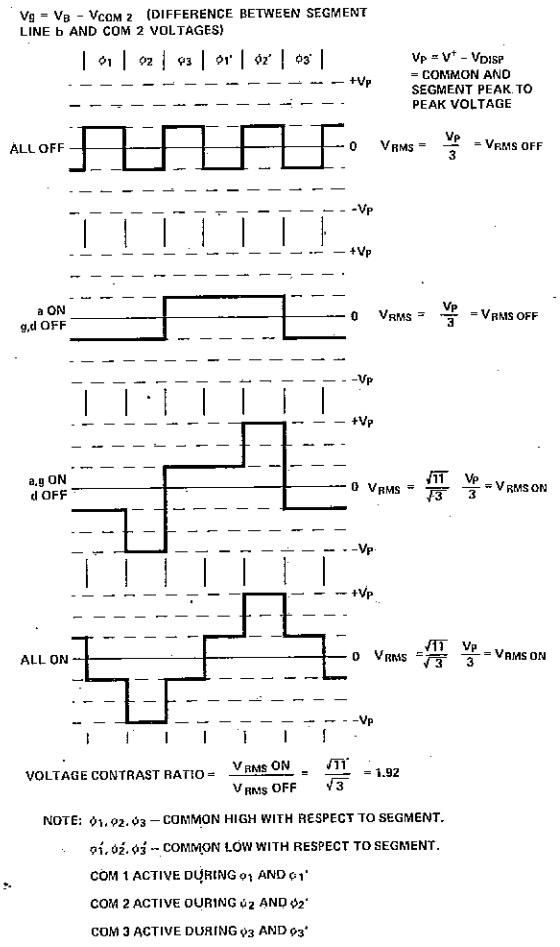


Figure 4. Voltage Waveforms on Segment g (V_g)

TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change to a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal

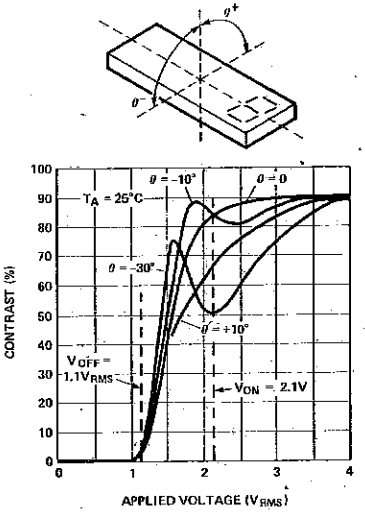


Figure 5. Contrast vs. Applied RMS Voltage

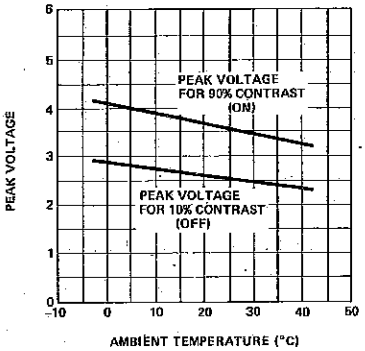


Figure 6. Temperature Dependence of LC Threshold

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 6 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 5.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to GND as shown in Figure 7. A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

Figure 8(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 5 and 6. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of -2 mV/°C; five in series gives -10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 8(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about -2 mV/°C) is also multiplied. The transistor should have a beta of at least 100 with a collector current of 10 μA. The inexpensive 2N2222 shown in the figure is a suitable device.

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to GND. The inputs of the chip are designed such that they may be driven above V^+ without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663, as shown in Figure 9. This circuit allows independent adjustment of both voltage and temperature compensation.

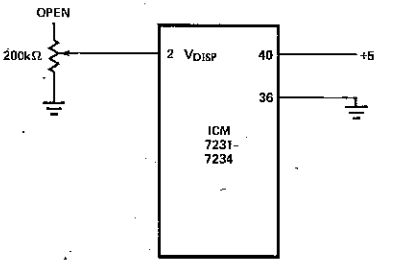


Figure 7 Simple Display Voltage Adjustment

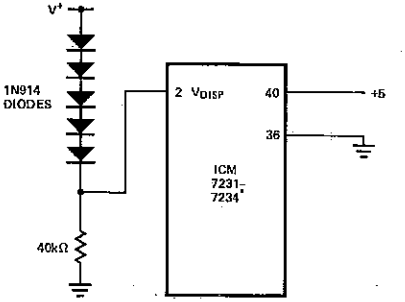


Figure 8(a) String of Diodes

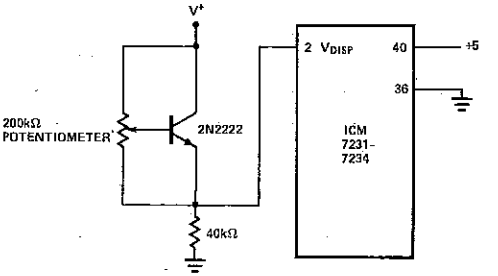


Figure 8(b) Transistor-Multiplier

Figure 8 Diode-based Temperature Compensation

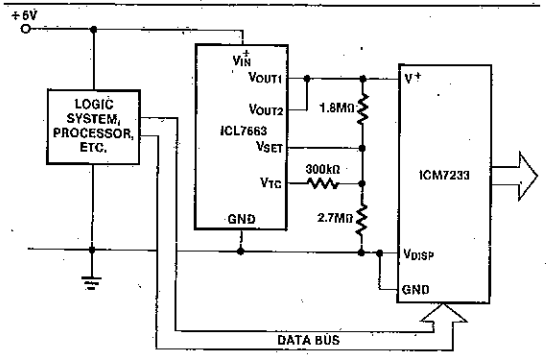


Figure 9 Flexible Temperature Compensation

DESCRIPTION OF OPERATION

PARALLEL INPUT OF DATA AND ADDRESS (ICM7231, ICM7233)

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, see block diagrams Figures 10 and 11. In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input. In the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input devices are shown in Figure 12, with the values for setup, hold, and pulse width times shown in AC Characteristics on page 3. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

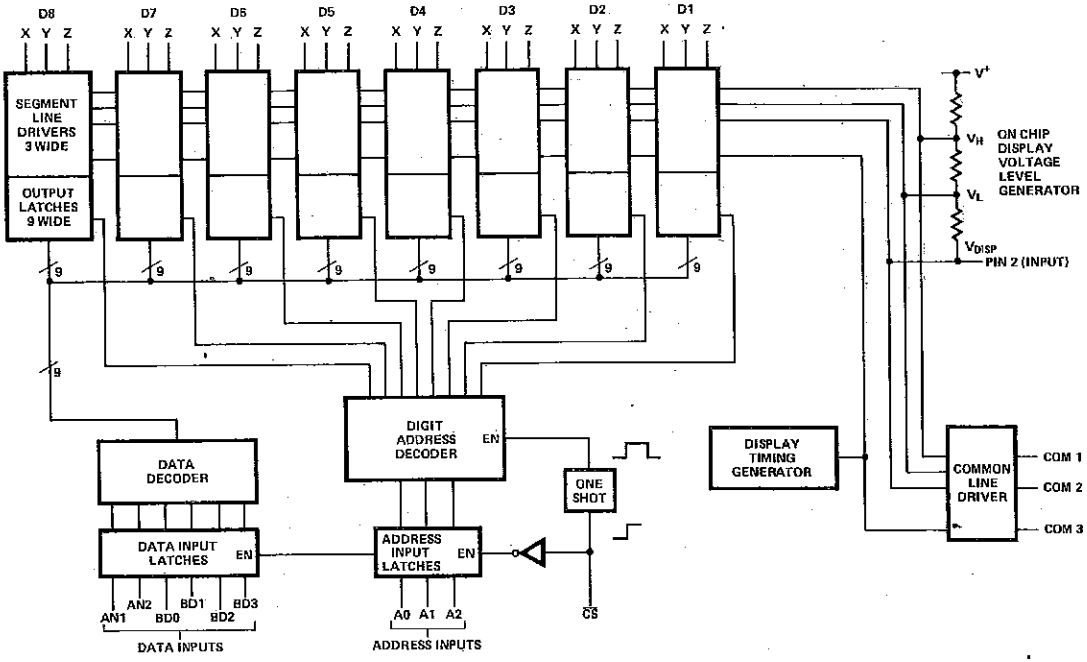


Figure 10. ICM7231 Block Diagram

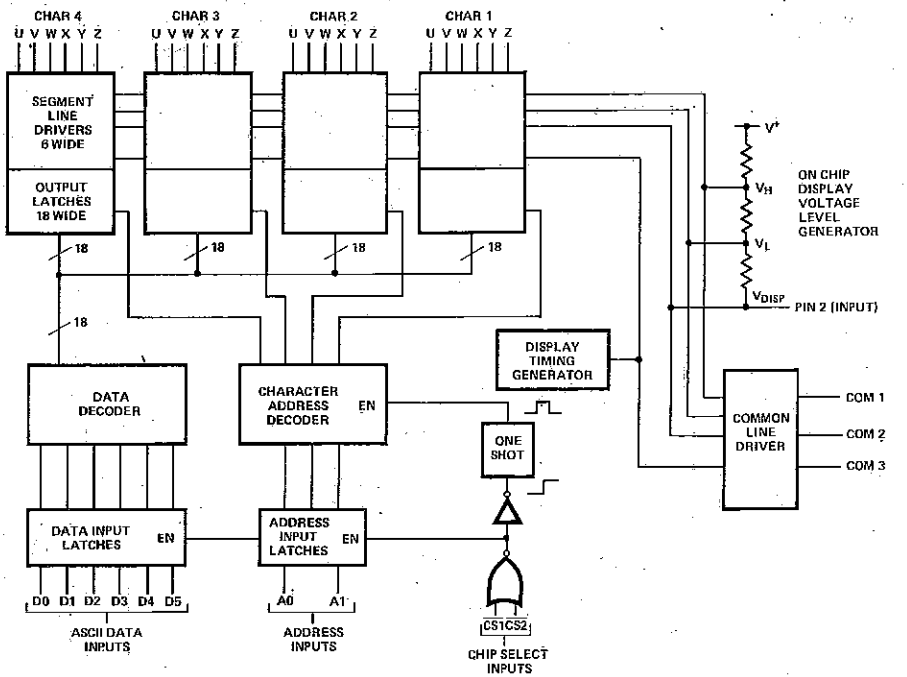
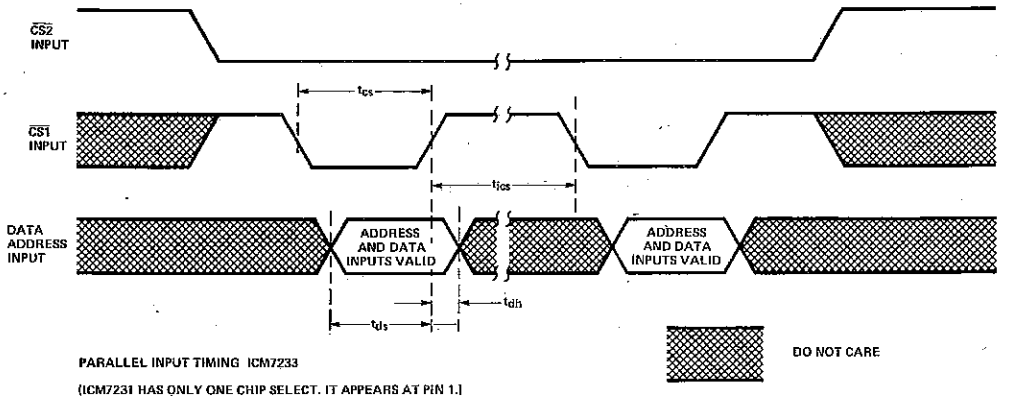


Figure 11. ICM7233 Block Diagram



PARALLEL INPUT TIMING ICM7233

(ICM7231 HAS ONLY ONE CHIP SELECT. IT APPEARS AT PIN 1.)

Figure 12. Parallel Input Timing

SERIAL INPUT OF DATA AND ADDRESS (ICM7232, ICM7234)

The ICM7232 and ICM7234 trade six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits (ICM7232) or one more 18-segment character (ICM7234). This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to block diagrams, Figures 13 and 14 and timing diagrams, Figures 15, 16, and 17. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232, 9 in the ICM7234), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the $\overline{\text{WRITE}}$ input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

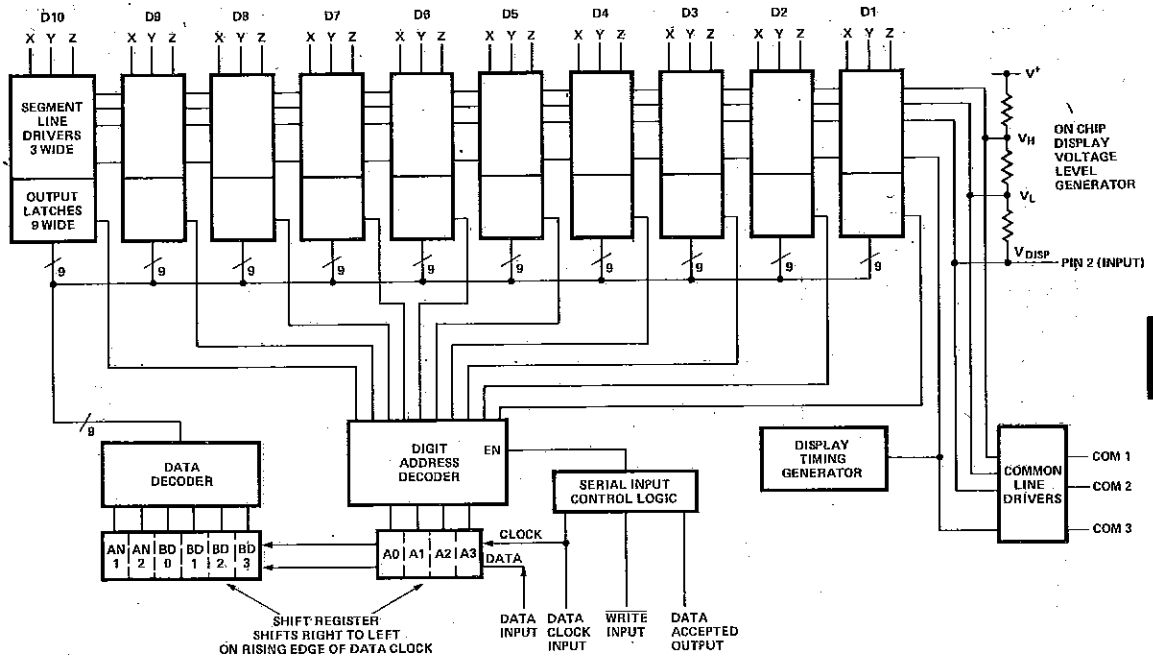


Figure 13. ICM7232 Block Diagram

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic, while in the ICM7234 it is the tenth.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 15. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunicators off, as shown in Figure 16.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

In the ICM7234, nine bits are always required; the control logic is similar, but allows only a $\overline{\text{WRITE}}$ (DATA ACCEPTED Low) with nine bits entered in the shift register, as shown in Figure 17.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

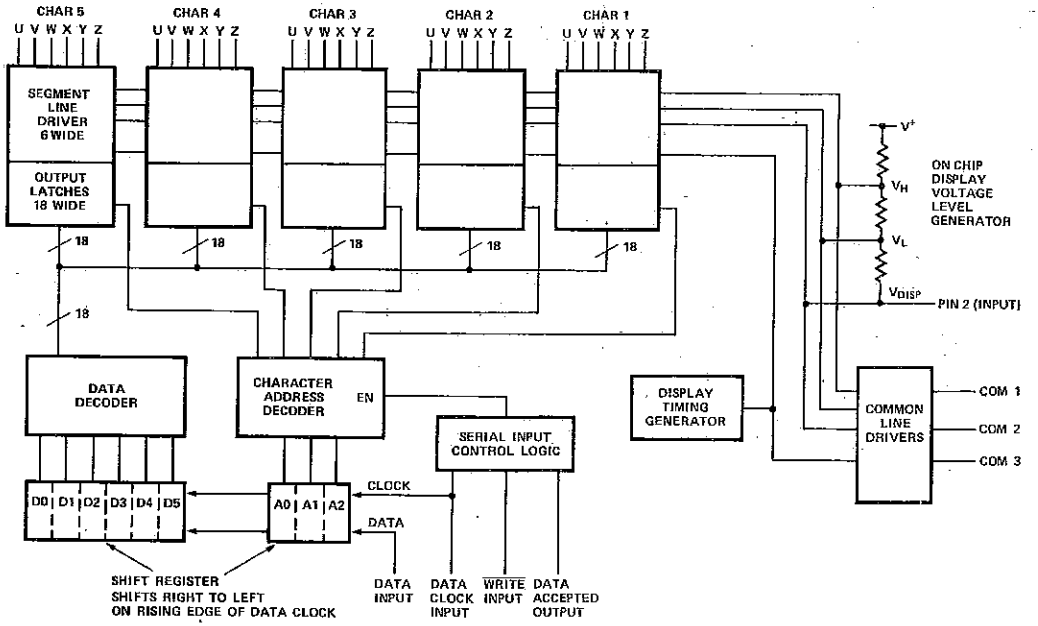


Figure 14. ICM7234 Block Diagram

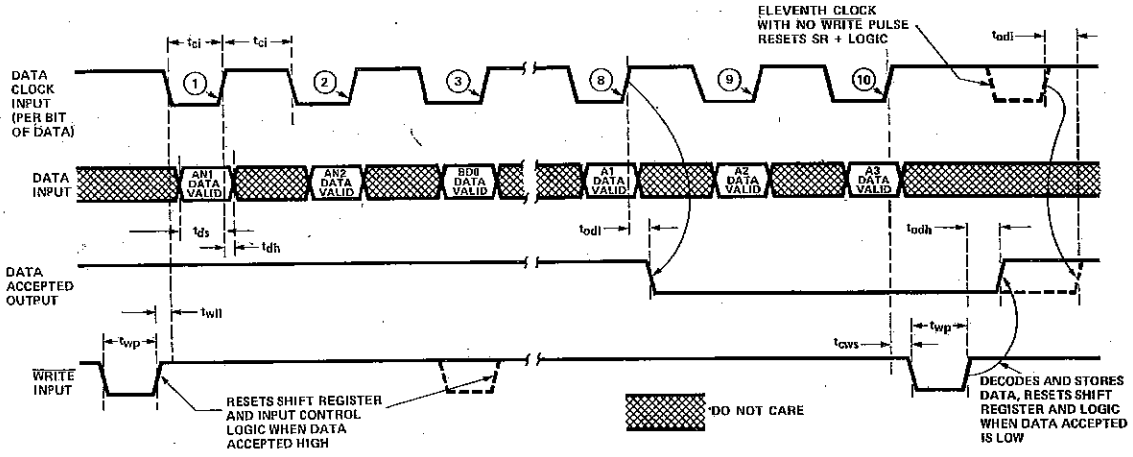


Figure 15. ICM7232 One Digit Input Timing Diagram, Writing Both Annunicators

AN1 ENTER FIRST	AN2	BD0	BD1	BD2	BD3	A_0	A_1	A_2	A_3 ENTER LAST

ICM7232 WRITE ORDER

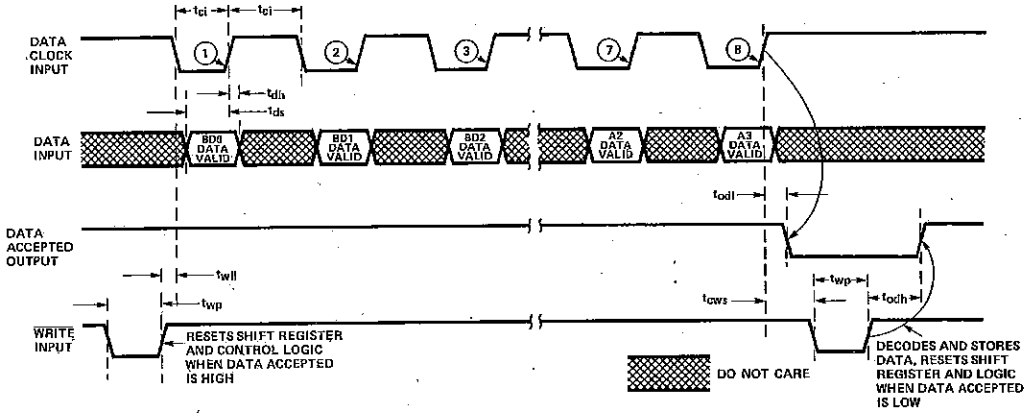


Figure 16. ICM7232 Input Timing Diagram, Leaving Both Annunciators OFF

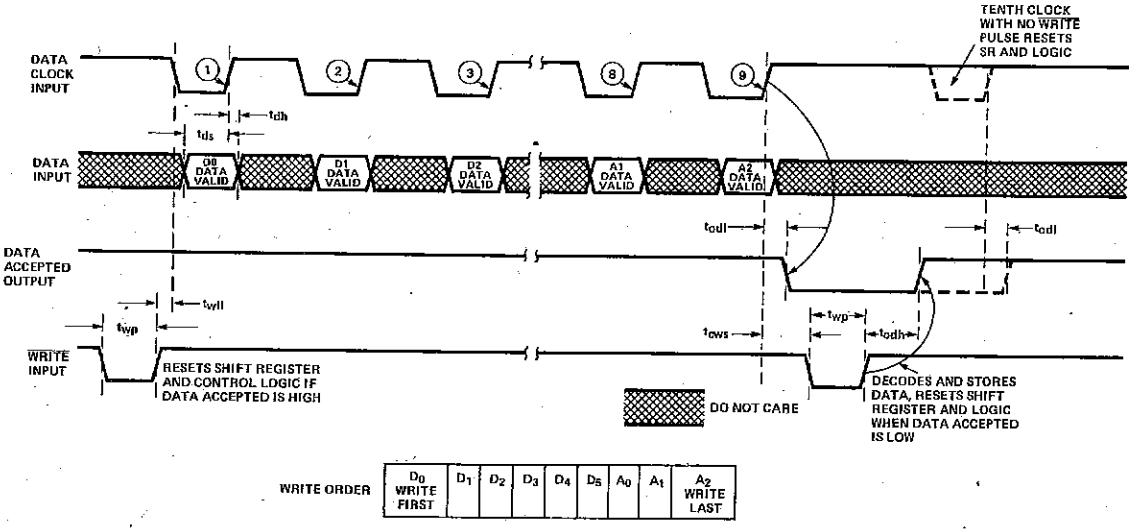


Figure 17. ICM7234 One Character Input Timing Diagram

DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 18. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1) (see Figure 19). The "C" devices provide only a "Code B" output for the 7-segments.

The ICM7233 and ICM7234 are supplied in "A" and "B" versions. Both versions decode an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and two "dots". The "A" devices have numbers which are half width and the "B" devices have full width numbers. The layout for a single character is shown in Figure 20 with output decoding shown in Table 4.

The data decoder is a mask programmable ROM. For large quantity orders custom decoder programs can be arranged. Contact the factory for details.

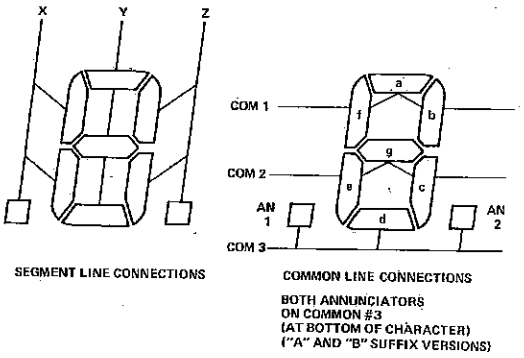


Figure 18. ICM7231 and ICM7232 Display Fonts ("A" and "B" Suffix Versions)

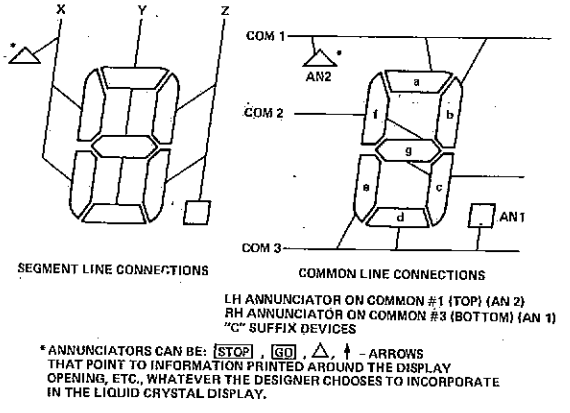


Figure 19. ICM7231 and ICM7232 Display Fonts ("C" Suffix Versions)

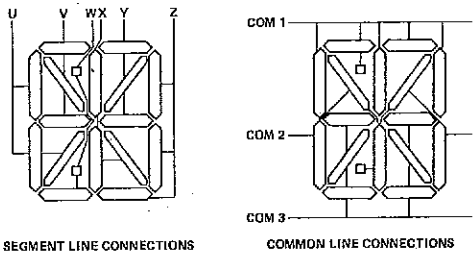


Figure 20. ICM7233 and ICM7234 Display Font (18-Segment Alphanumeric)

Table 1

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	B	E
1	1	0	0	C	H
1	1	0	1	D	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

BINARY DATA DECODING (ICM7231/32)

Table 2

CODE INPUT				DISPLAY OUTPUT
ICM 7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

ADDRESS DECODING (ICM7231/32)

Table 3

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0		
0	1		
1	0		
1	1		

ANNUNCIATOR DECODING

EVALUATION KITS

After purchasing a sample of the ICM7231/32/33/34, the majority of users will want to build a sample display. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering kits which contain all the necessary components to build 8 character or 8 digit displays. With the help of such a kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICM7231EV/KIT and the ICM7233 EV/KIT. Both contain the appropriate ICs, a circuit board, a Multiplexed LCD display (7/9 segment for 7231EV/KIT, 16/18 segment for ICM7233EV/KIT), passive components, and miscellaneous hardware.

COMPATIBLE DISPLAYS

Compatible displays are manufactured by:

G.E. Displays Inc., Beechwood, Ohio
(216) 831-8100 (#356E3R99HJ)

Epson America Inc., Torrance, CA
(Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA
(Custom Displays)

Table 4

CODE INPUT				DISPLAY OUTPUT				
							D5, D4	A B
D3	D2	D1	D0	0, 0	0, 1	1, 0	1, 1	
0	0	0	0					
0	0	0	1			!		
0	0	1	0			"		
0	0	1	1			#		
0	1	0	0			$		
0	1	0	1			%		
0	1	1	0			&		
0	1	1	1			'		
1	0	0	0			(		
1	0	0	1			)		
1	0	1	0			*		
1	0	1	1			+		
1	1	0	0			,		
1	1	0	1			-		
1	1	1	0			.		
1	1	1	1			/		

DATA DECODING
6 - BIT ASCII → 18 SEGMENT
(ICM7233/34)

Table 5

CODE INPUT			DIGIT SELECTED
ICM 7234 ONLY			
A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

ADDRESS
DECODING
(ICM7233/34)

TYPICAL APPLICATIONS

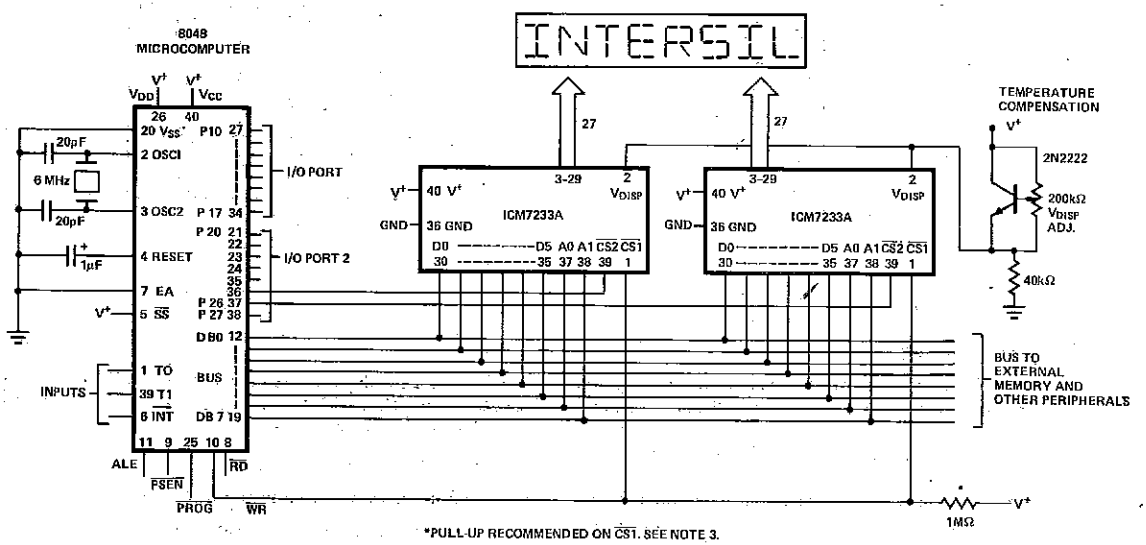


Figure 21. 8048/IM80C48 Microcomputer with 8 Character 16 Segment ASCII Triplex Liquid Crystal Display. The two bit character address is merged with the data and written to the display driver under the control of the $\overline{WR}$ line. Port lines are used to either select the target driver, or deselect all of them for other bus operations.

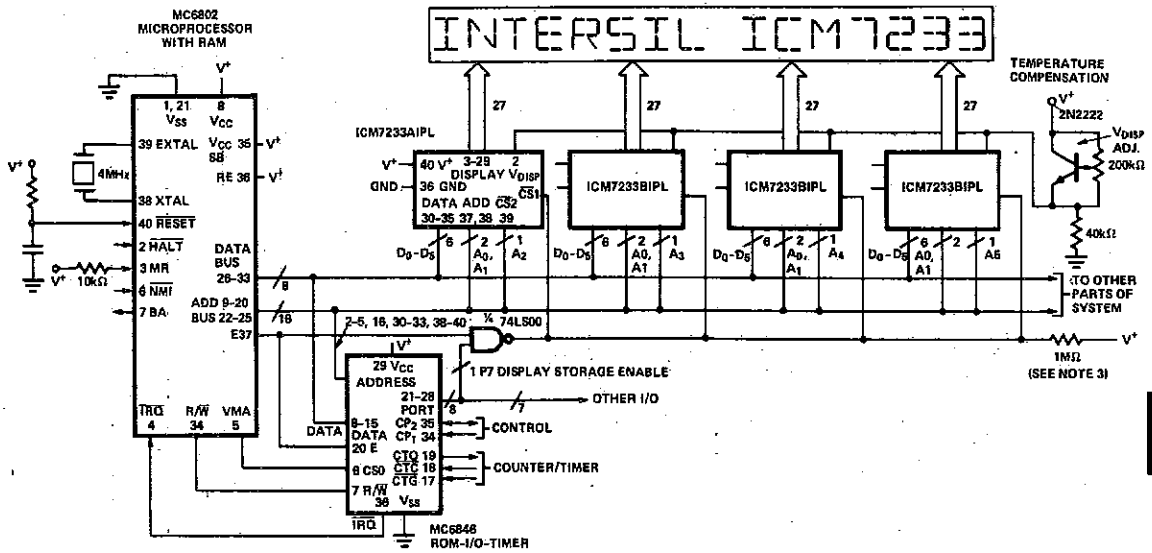


Figure 22. MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display. The peripheral device provides ROM and Timer functions in addition to port line control of the display bank. Individual character locations are addressed via the address bus. Note that VMA is not decoded on these lines, which could cause problems with the TST instruction.

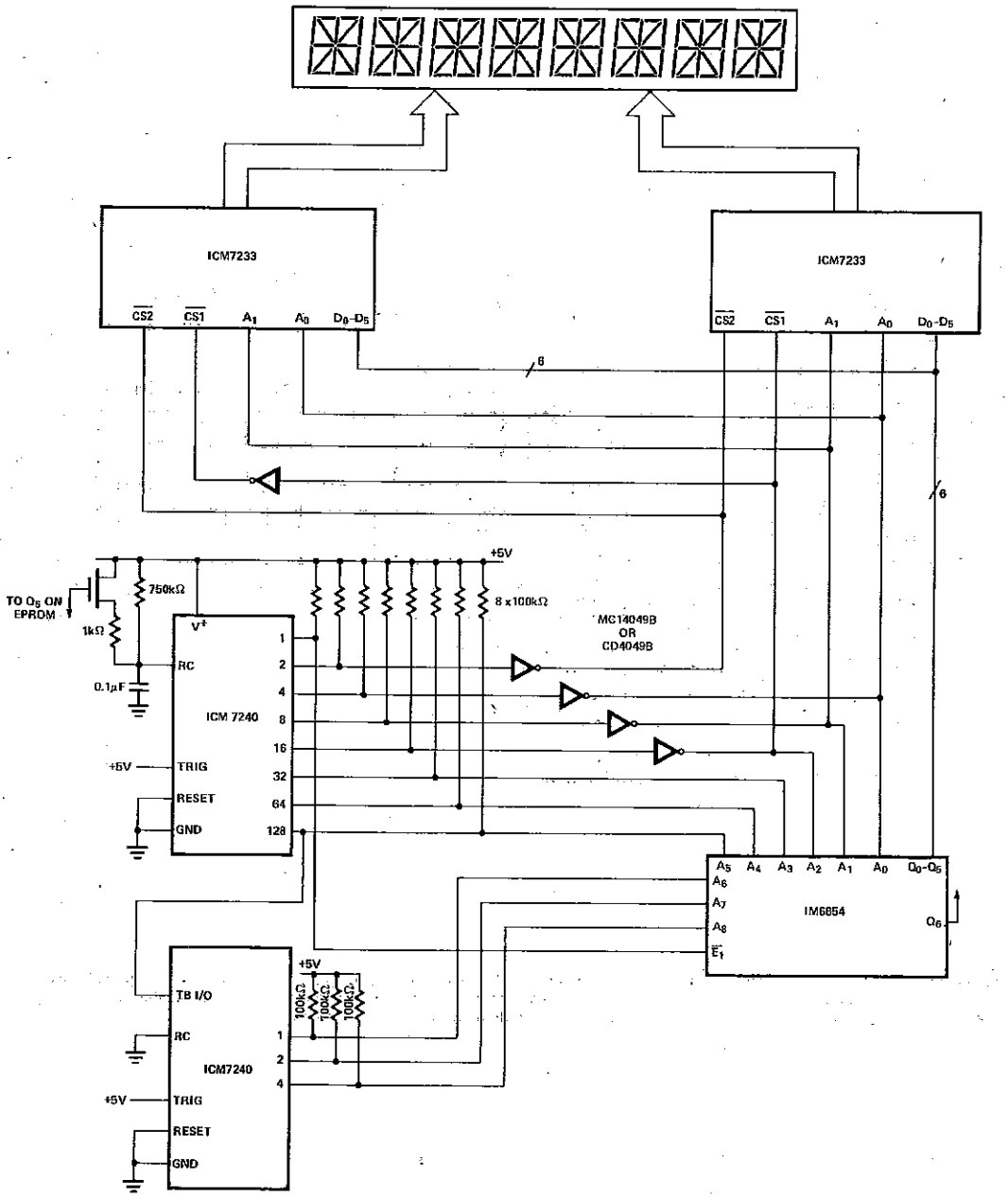


Figure 23. EPROM-Coded Message System. This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

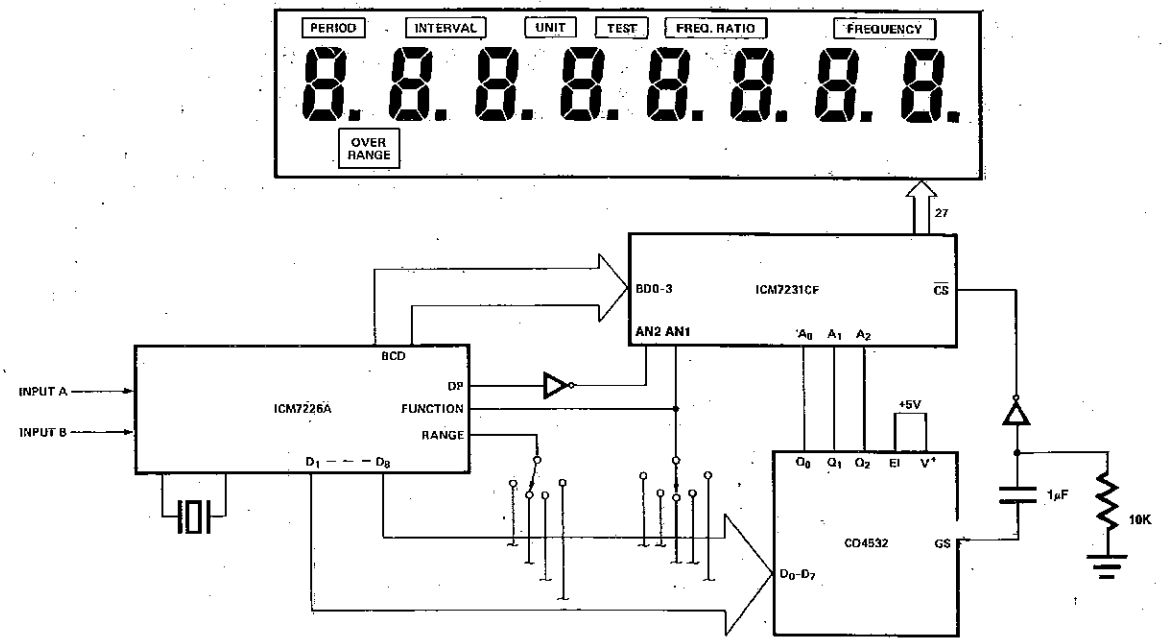


Figure 24. 10 MHz Frequency/Period Pointer with LCD Display. The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.

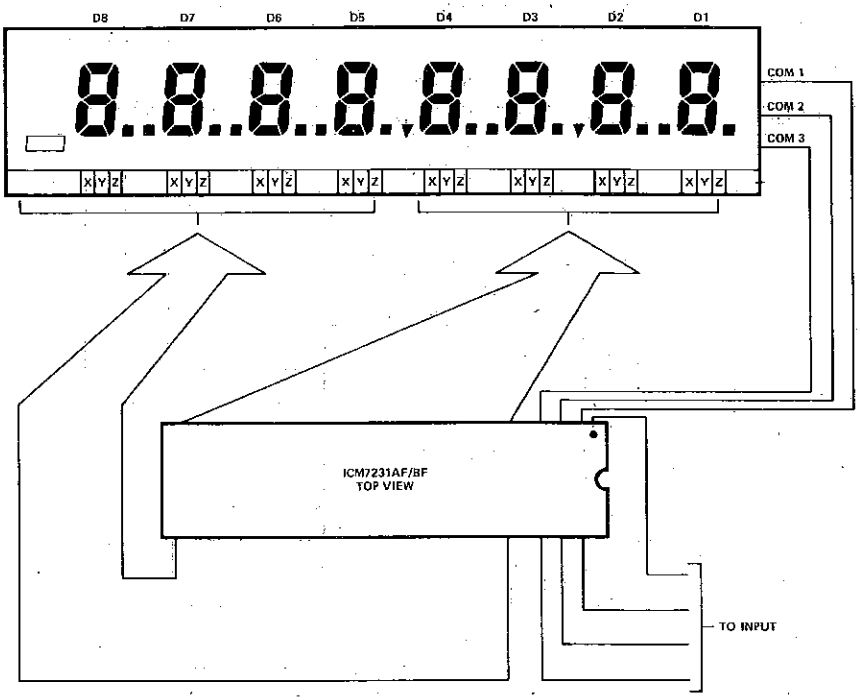


Figure 25. "Forward" Pin Orientation and Display Connections.

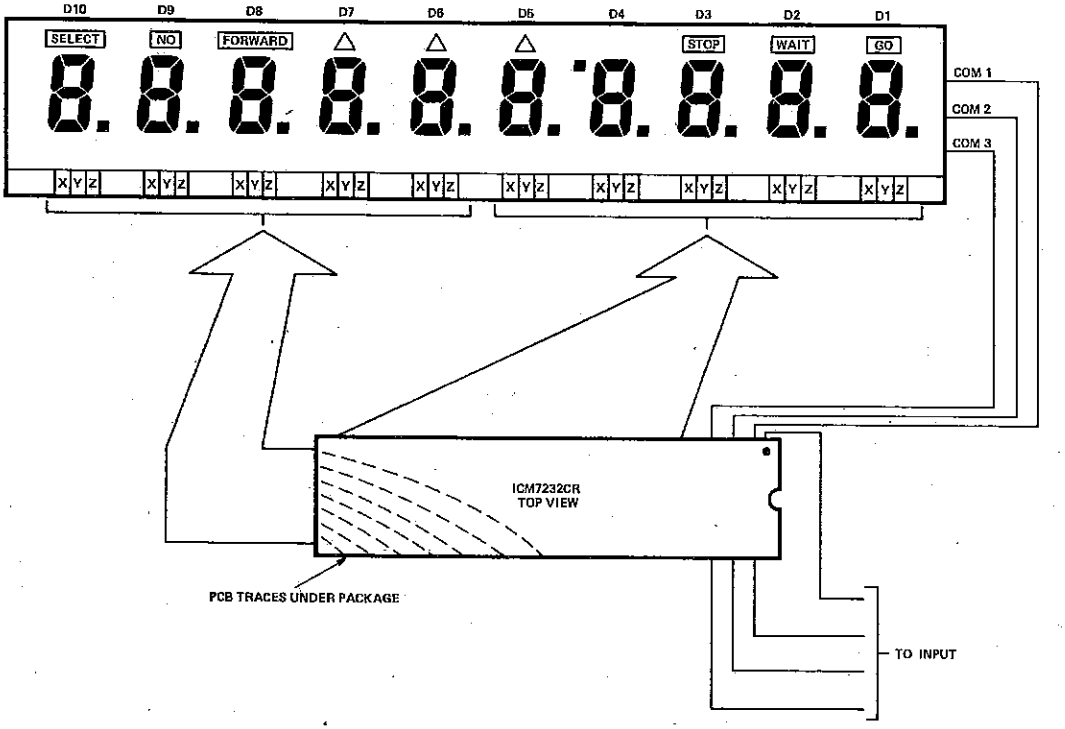


Figure 26. "Reverse" Pin Orientation and Display Connections

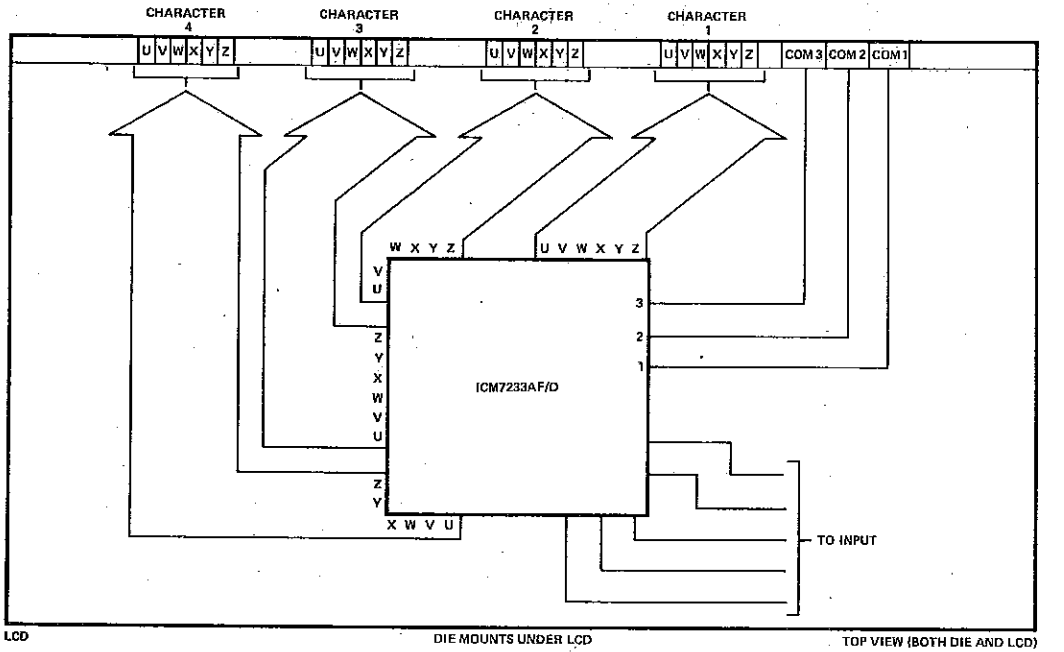
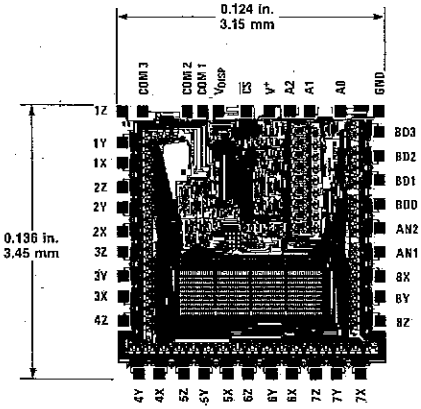
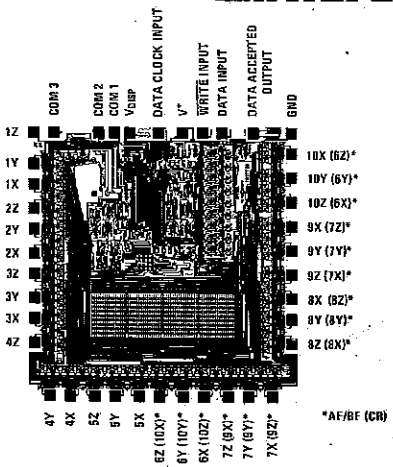


Figure 27. "Forward" Die Pad Orientation and Typical Triplex Alphanumeric Display Connections

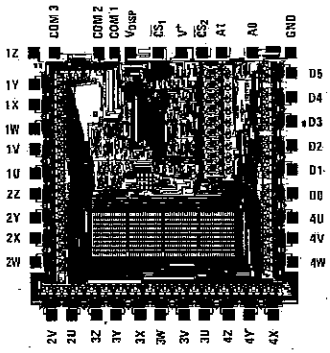
CHIP TOPOGRAPHY



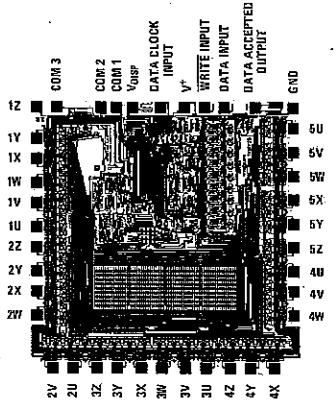
ICM7231



ICM7232



ICM7233



ICM7234

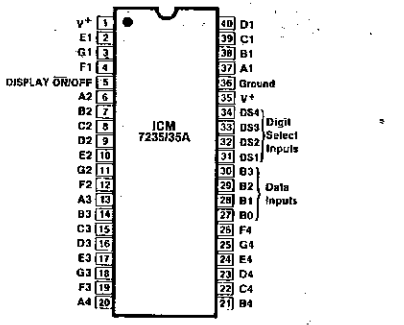
ICM7235

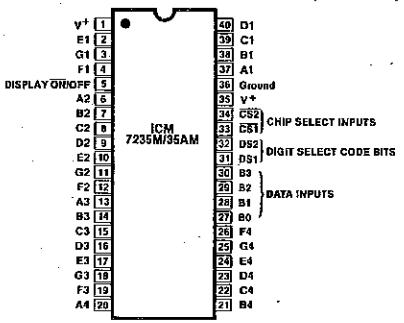
Four Digit Non-Multiplexed Vacuum Fluorescent Display Decoder/Drivers

FEATURES

- 28 high voltage segment drivers provide four 7-segment digits
- Multiplexed BCD input (7235)
- High speed processor interface (7235M)
- 7-segment hex (0-9, A-F) or Code-B (0-9, dash, E, H, L, P, blank) output versions available
- Display blanking input
- All devices fabricated using high density MAX-CMOS™ LSI technology for very low-power, high-performance operation
- All inputs fully protected against static discharge

PIN CONFIGURATIONS (outline dwg PL)





DESCRIPTION

The ICM7235 family of display driver circuits provides the user with a single chip interface between digital logic or microprocessors to non-multiplexed 7-segment vacuum fluorescent displays.

The chips provide 28 high voltage open drain P-channel transistor outputs organized as four 7-segment digits.

The devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the Intersil ICM7217, ICM7226 and ICL7135. The microprocessor interface devices (suffix M) provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output (0-9, A-F). The "A" versions provide the same output code as the ICM7218 Code "B" (0-9, dash, E, H, L, P, blank). Either device will correctly decode true BCD to seven-segment decimal outputs.

All devices in the ICM7235 family are packaged in a standard 40-pin plastic dual-in-line package.

The ordering information shows the four standard devices of the ICM7235 family and their markings, which serve as part numbers for ordering purposes.

ORDERING INFORMATION

Order Part Number	Output Code	Input Configuration
ICM7235 IPL	Hexadecimal	Multiplexed 4-Bit
ICM7235A IPL	Code B	Multiplexed 4-Bit
ICM7235M IPL	Hexadecimal	Microprocessor Interface
ICM7235AM IPL	Code B	Microprocessor Interface

An Evaluation Kit is available for this part.
Order number ICM7235 EV/Kit.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ +70°C
Supply Voltage (V^+ -Ground) ..... 6.5 Volts
Input Voltage (Note 2) ..... V^+ +0.3V, Ground −0.3V
Output Voltage (Note 3) ..... V^+ −35V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

All parameters measured with $V^+ = 5V$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Supply Current	I^+	Measured V^+ to Ground Test circuit; display blank or OFF		10	50	μA
Supply Current	I^+	Measured V^+ to Display			100	mA
Segment OFF Output Voltage	V_{SEG}	$I_{SLK} = 10\mu A$	30			V
Segment OFF Leakage Current	I_{LS}	$V_{SEG} = V^+ - 30V$		0.1	10	μA
Segment ON Current	I_{SEG}	$V_{SEG} = V^+ - 2V$	1.5	2.5		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}	Referred to Ground	3			V
Logical "0" Input Voltage	V_{IL}	Referred to Ground			1.5	V
Input Leakage Current	I_{ILK}	Pins 27-34		±0.1	±1	μA
Input Capacitance	C_{IN}	Pins 27-34		5		pF
$\overline{ON}$/OFF Input Leakage	$I_{ILK(\overline{ON}/OFF)}$	All Devices		±0.1	±1	μA
$\overline{ON}$/OFF Input Capacitance	$C_{IN(\overline{ON}/OFF)}$	All Devices		200		pF
AC CHARACTERISTICS — MULTIPLEXERD INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			ns
Inter-Digit Select Time	t_{ids}		2			μs
AC CHARACTERISTICS — MICROPROCESSOR INTERFACE						
$\overline{Chip}$ $\overline{Select}$ Active Pulse Width	t_{csa}	Other $\overline{Chip}$ $\overline{Select}$ either held active, or both driven together	200			ns
Data Setup Time	t_{dsm}		100			ns
Data Hold Time	t_{dhm}		10	0		ns
Inter-$\overline{Chip}$ $\overline{Select}$ Time	t_{ics}		2			μs

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any input terminal to a voltage in excess of V^+ or ground may cause destructive device latch-up. For this reason, it is recommended that inputs from external sources operating on a different power supply be applied only after the device's own power supply has been established, and that on multiple supply systems the supply to the ICM7235 be turned on first.

NOTE 3: This value refers to the display outputs only.

CIRCUIT DESCRIPTION

Each device in the ICM7235 family provides signals for directly driving the anode terminals of a four-digit, 7-segment non-multiplexed vacuum fluorescent display. The outputs are taken from the drains of high-voltage, low-leakage P-channel FETs, each capable of withstanding > −35V with respect to V^+. In addition, the inclusion of an ON/OFF input allows the user to disable all segments by connecting pin 5 to V^+; this same input may also be used as a brightness control by applying a signal swinging between V^+ and ground and varying its duty cycle.

The ICM7235 may also be used to drive non-multiplexed common cathode LED displays by connecting each segment output to its corresponding display input, and tying the common cathode to ground. Using a power supply of 5V and an LED with a forward drop of 1.7V results in an "ON" segment current of about 3mA, enough to provide sufficient brightness for displays of up to 0.3" character height.

Note that these devices have two V^+ terminals; each should be connected to the positive supply voltage. This double connection is necessary to minimize the effects of bond wire resistance, which could be a problem due to the high display currents.

Input Configurations and Output Codes

The standard devices in the ICM7235 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 through 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7235 and ICM7235M decode this binary input into a 7-segment alphanumeric hexadecimal output, while the ICM7235A and ICM7235AM decode the binary input into the same 7-segment output as the ICM7218 "Code B," i.e., 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a 7-segment decimal output.

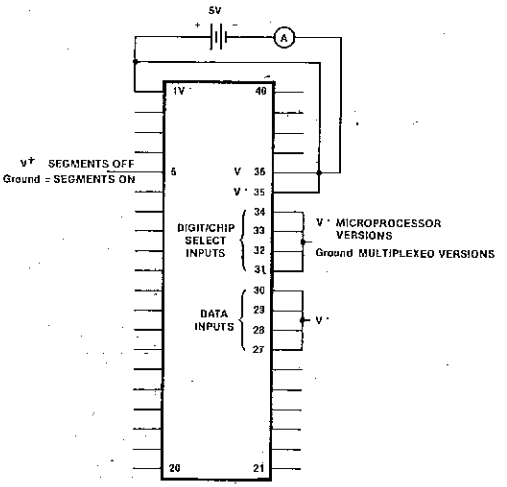
These devices are actually mask-programmable to provide any 16 combinations of the 7-segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact your Intersil Sales Office for details.

The ICM7235 and ICM7235A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate Digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one Digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Figure 2 and under Operating Characteristics for data setup, hold, and inter-digit select times must be met to ensure correct output.

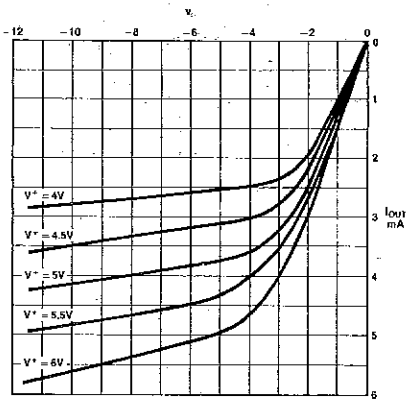
The ICM7235M and AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the 2-bit Digit Select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both Chip Select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken to ground. On the rising edge of either Chip Select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches. A select code of 00 writes into D4, 01 writes into D3, 10 writes into D2 and 11 writes into D1. The timing relationships for inputting data are shown in Figure 3, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS



INPUT DEFINITIONS

In this table, V^+ and ground are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One Ground = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One Ground = Logical Zero	Twos	
B2	29	V^+ = Logical One Ground = Logical Zero	Fours	
B3	30	V^+ = Logical One Ground = Logical Zero	Eights (Most Significant)	
$\overline{ON}$/OFF	5	V^+ = OFF, Ground = ON		Display $\overline{ON}$/OFF Input

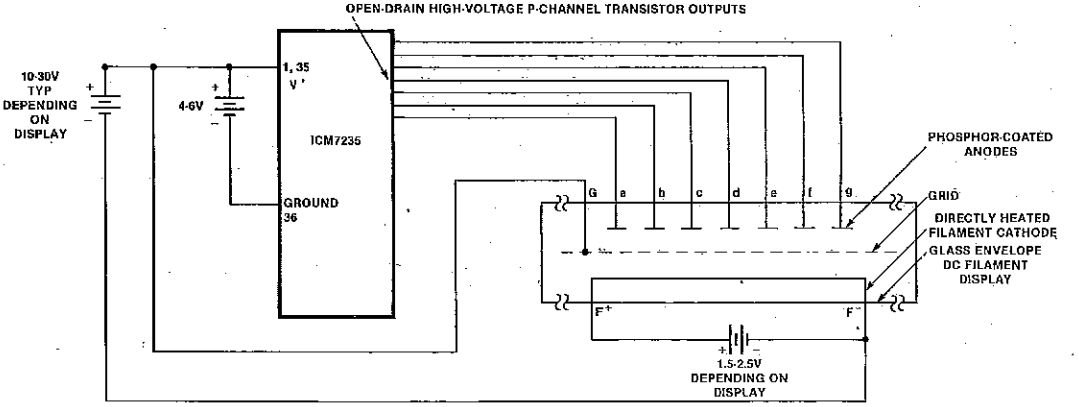
ICM7235, ICM7235A
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active Ground = Inactive	D1 (Least Significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most Significant) Digit Select

ICM7235M, ICM7235AM
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One Ground = Logical Zero	DS2 & DS1 serve as a two-bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V^+ = Inactive Ground = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken to ground, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

ICM7235 TYPICAL DC VACUUM FLUORESCENT DISPLAY CONNECTION



VACUUM FLUORESCENT DISPLAYS (4 DIGIT)
N.E.C. Electronics, Inc.
Models FIP4F8S and FIP5F8S

ICM7236
4½-Digit Counter With Vacuum Fluorescent Static Display Drivers

FEATURES

- High frequency counting—guaranteed 15MHz, typically 25MHz at 5V
- Low power operation—less than 100μW quiescent
- Direct 4½-digit seven-segment display drive for non-multiplexed Vacuum Fluorescent displays
- $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ inputs permit operation as frequency or period counter
- True $\overline{\text{COUNT INHIBIT}}$ disables first counter stage
- $\overline{\text{CARRY}}$ output for cascading four-digit blocks
- Schmitt-trigger on COUNT input allows operation in noisy environments or with slowly changing inputs
- Leading Zero Blanking INput and OUTput for correct leading zero blanking with cascaded devices
- All inputs fully protected against static discharge—no special handling precautions necessary
- Devices fabricated using MAXCMOS™ process for high-performance, low power operation

DESCRIPTION

The ICM7236 and ICM7236A devices are high-performance CMOS 4½-digit counters, including decoders, output latches, count inhibit, reset, and leading zero blanking circuitry, and twenty-nine high-voltage open drain P-channel transistor outputs suitable for driving non-multiplexed (static) vacuum fluorescent displays.

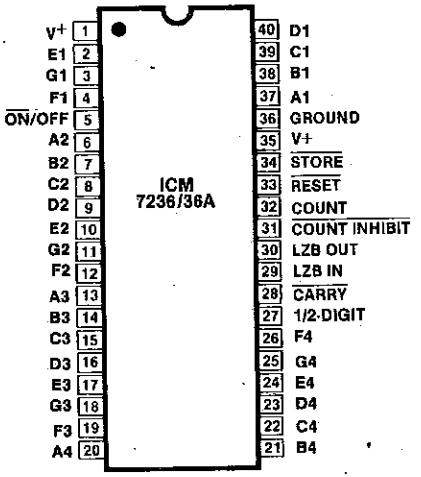
The ICM7236 is a decade counter, providing a maximum count of 19999, while the ICM7236A is intended for timing purposes, providing a maximum count of 15959.

The counter section of the two devices in the ICM7236 family provides direct static counting from DC to 15MHz guaranteed (with a 5V ±10% supply) over the operating temperature range. At normal room temperatures, the device will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allows a direct interface with the ICM7207 devices to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate features intended to simplify cascading in four-digit blocks. The $\overline{\text{CARRY}}$ output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allow correct leading zero blanking between four-decade blocks.

The ICM7236 and ICM7236A are packaged in a standard 40-pin dual-in-line plastic package.

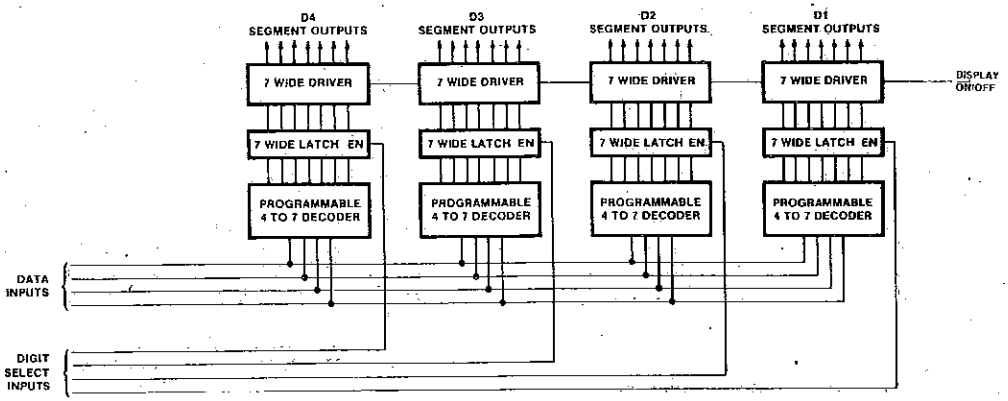
PIN CONFIGURATION (outline dwg PL)



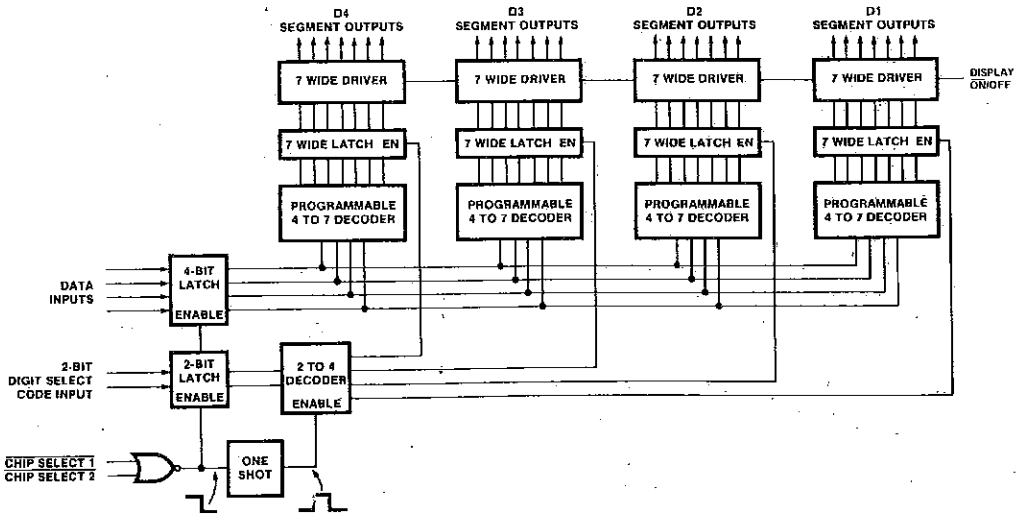
ORDERING INFORMATION

ORDER PART NUMBER	COUNT OPTION
ICM7236IPL	19999
ICM7236AIPL	15959
ICM7236 EV/KIT	(Evaluation Kit)

ICM7235/35A

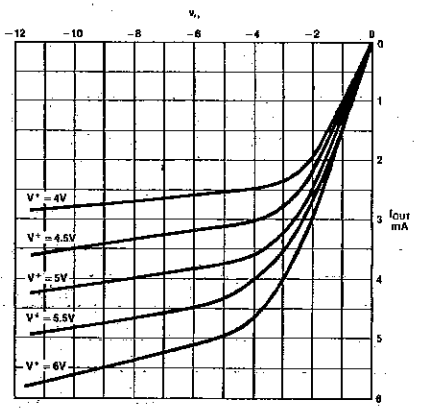


ICM7235M/35AM

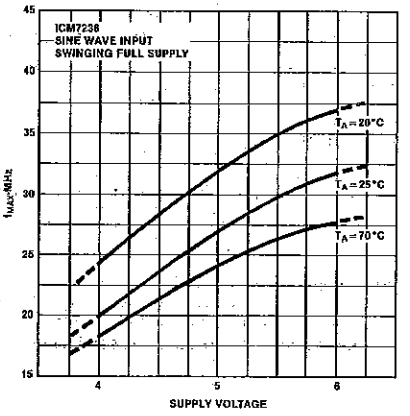


TYPICAL CHARACTERISTICS

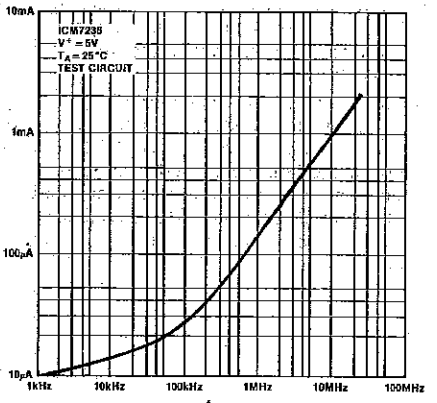
Output Characteristics



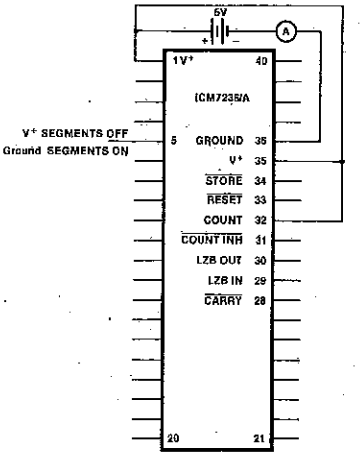
Maximum Count Frequency (Typical) as a Function of Supply Voltage



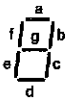
Supply Current as a Function of Count Frequency



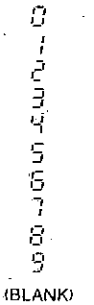
TEST CIRCUIT



SEGMENT ASSIGNMENT



DISPLAY FONT



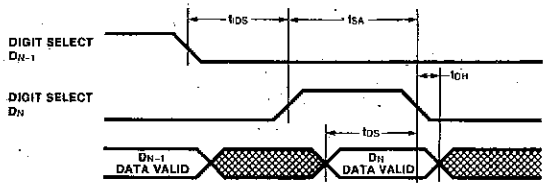


Figure 2. Multiplexed Input Timing Diagram

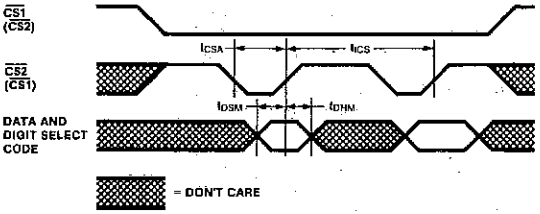


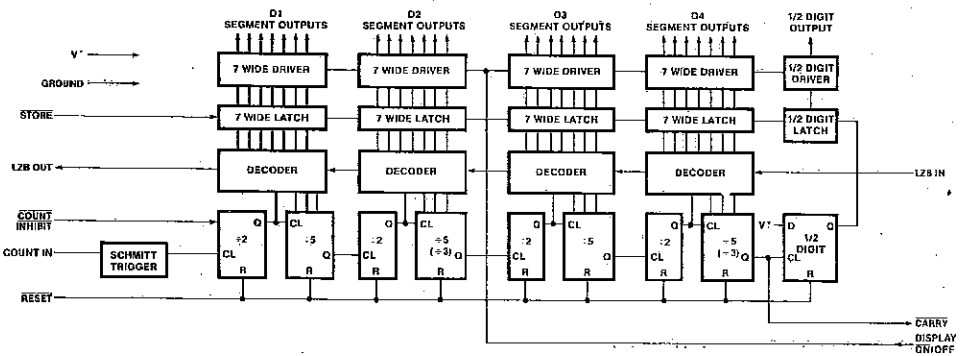
Figure 3. Microprocessor Interface Input Timing Diagram

Table 1: Output Codes

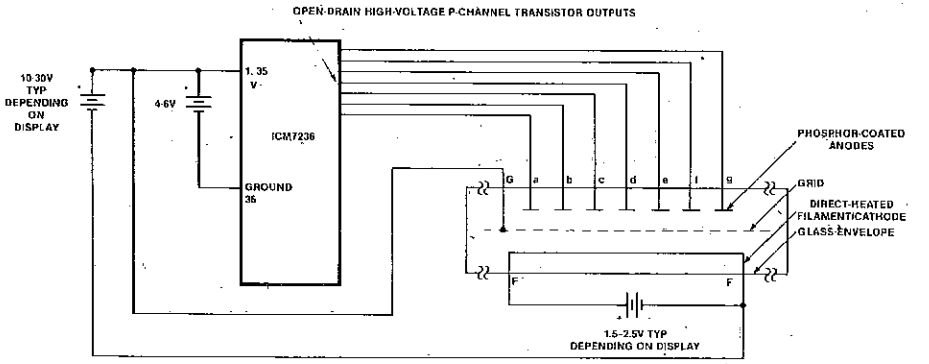
BINARY				HEXADECIMAL ICM7235 ICM7235M	CODE B ICM7235A ICM7235AM
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT

BLOCK DIAGRAM



TYPICAL DC VACUUM FLUORESCENT DISPLAY CONNECTION



VACUUM FLUORESCENT DISPLAYS (4½-DIGIT):

N.E.C. Electronics, Inc.
Model FIP5F8S

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ +70°C
Supply Voltage (V^+) ..... 6.5 V
Display Voltage (Note 3) ..... V^+ −35V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

(All parameters measured with $V^+ = 5V$ unless otherwise indicated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}	V^+	3	5	6	V
Operating Current	I_{OP}	Test circuit, Display blank		10	50	μA
Display Voltage	V_{DISP}				30	V
Display Output Leakage	I_{DLK}	Output OFF, $V = V^+ - 30V$		0.1	10	μA
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 $V = V^+ - 3V$		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			2	V
COUNT Input Threshold	V_{CT}			2		V
COUNT Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	$\overline{CARRY}$ (Pin 28), LZB OUT (Pin 30) $V_{OUT} = V^+ - 3V$.	350	500		μA
Output Low Current	I_{OL}	$\overline{CARRY}$ (Pin 28), LZB OUT (Pin 30) $V_{OUT} = +3V$.	350	500		μA
Count Frequency	f_{count}	$4.5V < V^+ < 6V$	0	25	15	MHz
$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width	t_S, t_W		3			μs

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.
NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than ground may cause destructive device latch-up. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7236/7236A be turned on first.
NOTE 3: This limit refers to the display output terminals only.

DESCRIPTION OF OPERATION

All of the chips in the ICM7236 family provide twenty-nine outputs suitable for directly driving the anode terminals of 4½ digit seven-segment non-multiplexed (static) vacuum-fluorescent displays. Each display output is the drain of a high-voltage low-leakage P-channel transistor, capable of withstanding typically greater than −35 volts with respect to V^+. The output characteristics are shown graphically under "Typical Characteristics."

These chips also provide a dislay $\overline{ON}$/OFF input which may be used to disable all the segment outputs and thus blank the display. This input may also be used to control the display brightness by varying the duty cycle of a signal at the input swinging between V^+ and ground.

NOTE that these circuits have two terminals for V^+; both of these pins should be connected to the power supply positive terminal. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

These chips may also be used to directly drive non-multiplexed common-cathode LED displays, where each segment of the display is driven by one ICM7236 output, and the common cathode is connected to ground. With a 5V power supply and a 1.7V LED diode forward voltage drop, the current in an "ON" segment will be typically 3mA. This should provide sufficient brightness in displays up to about 0.3" character height.

ICM7240/50/60 CMOS Programmable Timers/Counters

FEATURES

- **Replaces 8240/50/60, 2240 in most applications**
- **Timing from microseconds to days**
- **May be used as fixed or programmable counter**
- **Programmable with standard thumbwheel switches**
- **Select output count from**
  1RC to 255RC (ICM7240)
  1RC to 99RC (ICM7250)
  1RC to 59RC (ICM7260)
- **Monostable or astable operation**
- **Low supply current: 115μA @ 5 volts**
- **Wide supply voltage range: 2-16 volts**
- **Cascadeable**

GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICL 8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

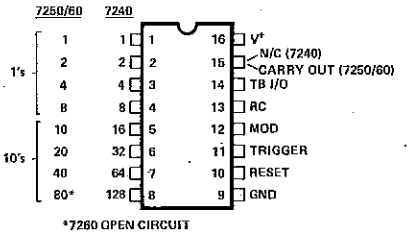
6

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240/D		Dice Only
ICM7250/D		Dice Only
ICM7260/D		Dice Only

PIN CONFIGURATION (OUTLINE DRAWING JE)

ICM7240, 7250, 7260



*7260 OPEN CIRCUIT

COUNTER SECTION

The devices in the ICM7236 family implement a four-digit ripple-carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the carry signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, and the $\overline{\text{CARRY}}$ output will provide a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ disables the first divide-by-two in the counter chain without affecting its clock. This provides a true **count** inhibit which is not sensitive to the state of the COUNT input, preventing false counts which can result from using a normal logic gate forcing the state of the clock to prevent counting.

Each decade drives directly into a four-to-seven decoder which derives the seven-segment output code. Each decoder output corresponds to the one-segment terminal of the device. The output data is latched at the driver; when the $\overline{\text{STORE}}$ pin is at a negative level, these latches are updated, and when the pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating, or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the Leading Zero Blanking INput is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, which can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, on an eight-decade counter with overflow using two ICM7236 devices, the Leading Zero Blanking OUTput of the high-order digit device would be connected to the Leading Zero Blanking INput of the low-order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7236 devices in four-digit blocks.

CONTROL INPUT DEFINITIONS

In this table, V^+ and ground are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

OPERATING CHARACTERISTICS

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking Input (LZB IN)	29	V^+ or Floating Ground	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V^+ or Floating Ground	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V^+ or Floating Ground	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V^+ or Floating Ground	Output Latches Not Updated Output Latches Updated
Display $\overline{\text{ON}}$/OFF	5	V^+ Ground	Display Outputs Disabled Display Outputs Enabled

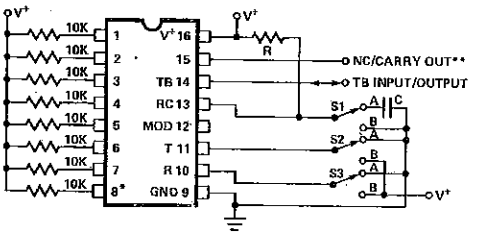
ELECTRICAL CHARACTERISTICS

Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, R = 10KΩ, C = 0.1μF		300	700	μA
		Operating, R = 1MΩ, C = 0.1μF		120	500	μA
		TB Inhibited, RC Connected to GND		125		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 1 mA	3.5	4.2		V
		I_{SINK} = 3.2 mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level	V_{MOD}	$V^+ = 5V$		3.5		V
		$V^+ = 15V$		11.0		V
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Max Count Toggle Rate 7240	f_t	$V^+ = 2V$ ┐		1		MHz
		$V^+ = 5V$ ├ Counter/Divider Mode	2	6		MHz
		$V^+ = 15V$ ┘		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Max Counter Toggle Rate 7250, 7260	f_t	$V^+ = 5V$ (Counter/Divider Mode)	1.5	5		MHz
Max Count Toggle Rate 7240, 7250, 7260	f_t	Programmed Timer — Divider Mode			100	KHz
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, I_{OUT} = 3.2 mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	$V^+ = 5V$, per Output			1	μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$	1K		22M	Ω
		$V^+ \leq 16V$	1K		22M	Ω

TEST CIRCUIT



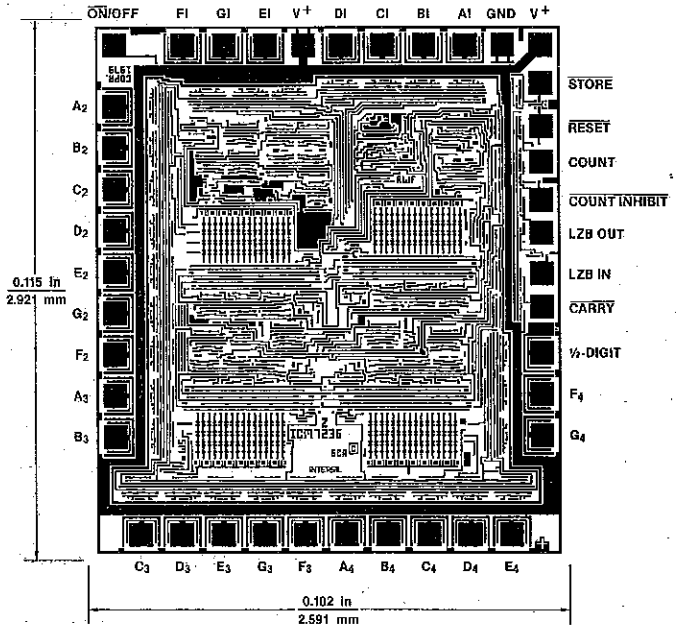
S1–A = RC RUN
B = T. B. INPUT RUN

S2–A = INACTIVE
B = TRIGGER

S3–A = INACTIVE
B = RESET

NOTE: S1–B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.
** TERMINAL 15 IS CARRY OUTPUT FOR 7250/60 DEVICES.
* TERMINAL 8 IS OPEN CIRCUIT FOR 7260.

CHIP TOPOGRAPHY



ICM7240/50/60 CMOS Programmable Timers/Counters

FEATURES

- **Replaces 8240/50/60, 2240 in most applications**
- **Timing from microseconds to days**
- **May be used as fixed or programmable counter**
- **Programmable with standard thumbwheel switches**
- **Select output count from**
  1RC to 255RC (ICM7240)
  1RC to 99RC (ICM7250)
  1RC to 59RC (ICM7260)
- **Monostable or astable operation**
- **Low supply current: 115μA @ 5 volts**
- **Wide supply voltage range: 2-16 volts**
- **Cascadeable**

GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICL 8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

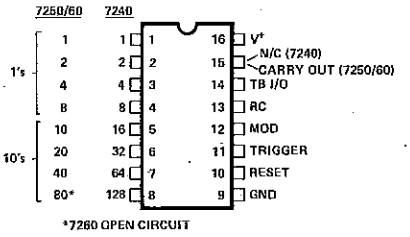
6

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240/D		Dice Only
ICM7250/D		Dice Only
ICM7260/D		Dice Only

PIN CONFIGURATION (OUTLINE DRAWING JE)

ICM7240, 7250, 7260



*7260 OPEN CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage[1]
Terminals 10,11,12,13,14 ..... GND -0.3V to $V^+ + 0.3V$

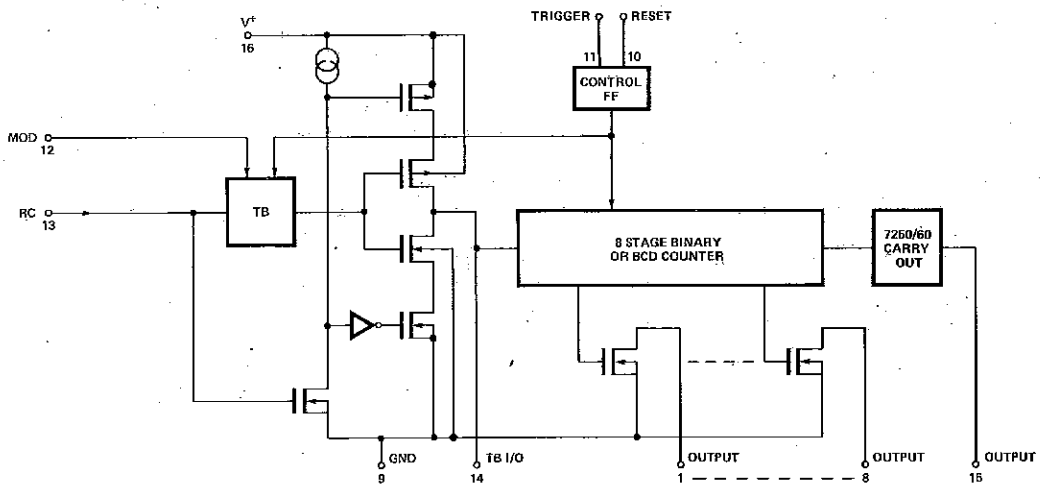
Maximum continuous output current (each output) ..... 50 mA
Power Dissipation[2] ..... 200 mW
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50/60 be turned on first.
2. Derate at -2 mW/°C above 25°C.

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM

ICM7240/50/60



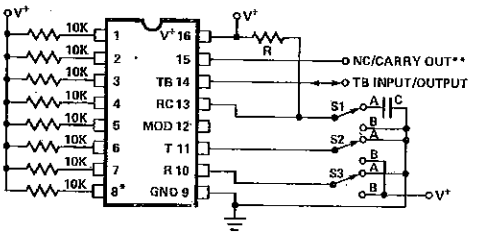
ELECTRICAL CHARACTERISTICS

Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, R = 10KΩ, C = 0.1μF		300	700	μA
		Operating, R = 1MΩ, C = 0.1μF		120	500	μA
		TB Inhibited, RC Connected to GND		125		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 1 mA	3.5	4.2		V
		I_{SINK} = 3.2 mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level	V_{MOD}	$V^+ = 5V$		3.5		V
		$V^+ = 15V$		11.0		V
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Max Count Toggle Rate 7240	f_t	$V^+ = 2V$ ┐		1		MHz
		$V^+ = 5V$ ├ Counter/Divider Mode	2	6		MHz
		$V^+ = 15V$ ┘		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Max Counter Toggle Rate 7250, 7260	f_t	$V^+ = 5V$ (Counter/Divider Mode)	1.5	5		MHz
Max Count Toggle Rate 7240, 7250, 7260	f_t	Programmed Timer — Divider Mode			100	KHz
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, I_{OUT} = 3.2 mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	$V^+ = 5V$, per Output			1	μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$	1K		22M	Ω
		$V^+ \leq 16V$	1K		22M	Ω

TEST CIRCUIT



S1–A = RC RUN
B = T. B. INPUT RUN

S2–A = INACTIVE
B = TRIGGER

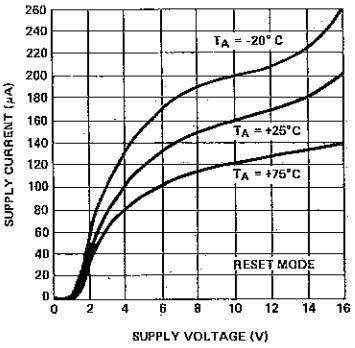
S3–A = INACTIVE
B = RESET

NOTE: S1–B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.
** TERMINAL 15 IS CARRY OUTPUT FOR 7250/60 DEVICES.
* TERMINAL 8 IS OPEN CIRCUIT FOR 7260.

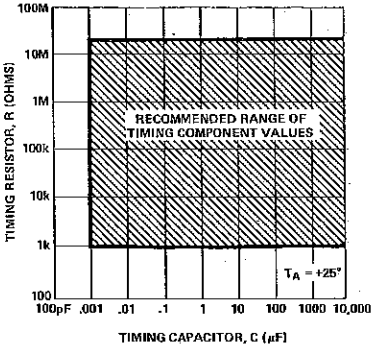
INTERSIL

TYPICAL PERFORMANCE CHARACTERISTICS

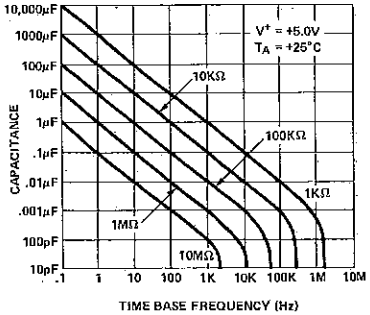
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



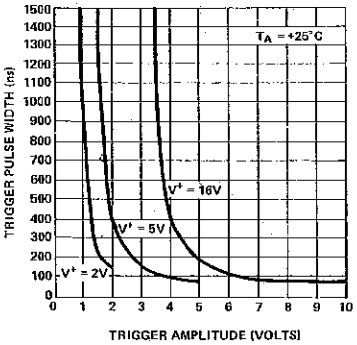
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



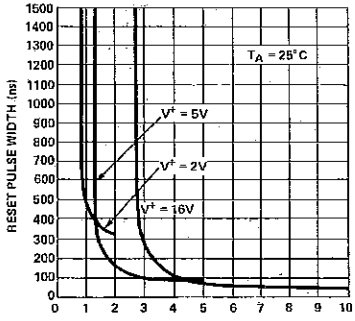
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



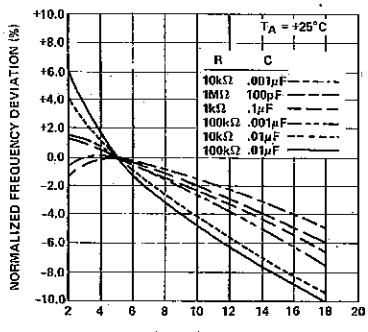
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



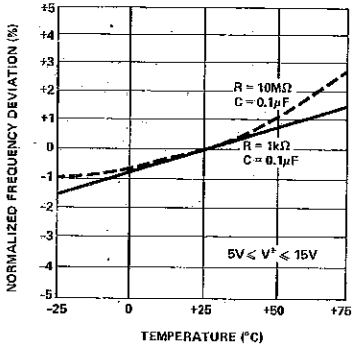
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



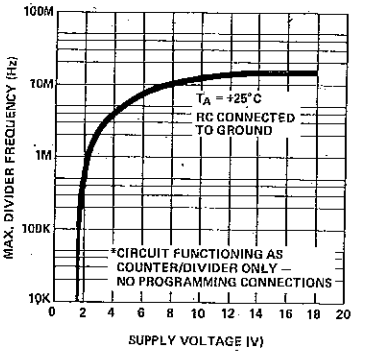
6

TYPICAL PERFORMANCE CHARACTERISTICS

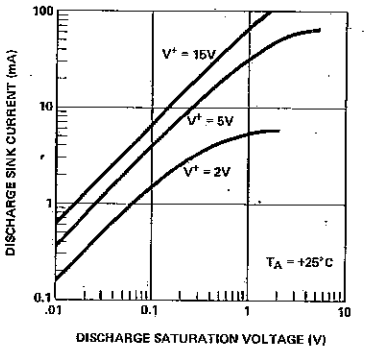
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



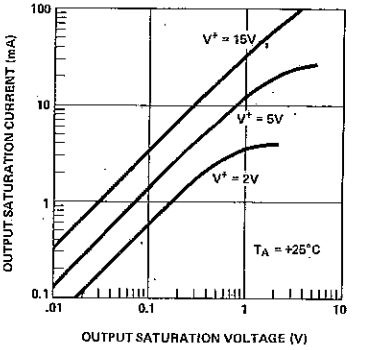
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE*



DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



DESCRIPTION OF PIN FUNCTIONS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 1). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.

GROUND (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by positive going control pulses applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

MODULATION AND SYNC INPUT (PIN 12)

The period t of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12

TIMEBASE INPUT/OUTPUT PIN (TERMINAL 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input terminal if terminal 13 (RC) is connected to GND.

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50/60 is used to replace an 8240/50/60 or 2240.

CARRY OUTPUT (TERMINAL 15, ICM7250/60 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 or 7260 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50/60 are shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. See Figure 3.

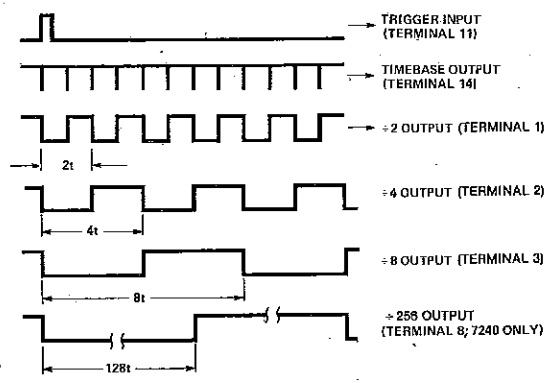


Figure 1. Timing Diagram for ICM7240/50/60

CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state, and starts the time base oscillator. Then, external C is charged through external R from 20% to 70% of V^+, generating a timing waveform with period t, equal to 1_{RC}. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250/60. The timing cycle terminates when a positive-going reset pulse is applied to pin 10. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carrry-out is also HIGH.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal; the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit operates in its astable, or free-running mode, after initial triggering.

PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain N-channel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as **any one** of the outputs is low. Each output is capable of sinking ≈5 mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) t_o would be 32t for a 7240 and 20t for a 7250/60. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $t_o = (1 + 16 + 32)t$ for the 7240 or $(1 + 10 + 20)t$ for the 7250/60. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

$1t \leq t_o \leq 255t$ (7240)
$1t \leq t_o \leq 99t$ (7250)
$1t \leq t_o \leq 59t$ (7260)

Note that for the 7250 and 7260, invalid count states (BCD values ≥ 10) will not be recognized and the counter will not stop.

The 7240/50/60 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see figure 2. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 2, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 1, which shows the phase relations between the counter outputs. Figure 3 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 and ICM7260 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of 1_{RC} to 99_{RC}. Cascading two ICM7250's (using the carry out gate) would expand selection to 9999_{RC}. For a ICM7260, there are standard BCD thumbwheel switches for the 0 through 5 digit (twelve position 0 to 5 repeated).

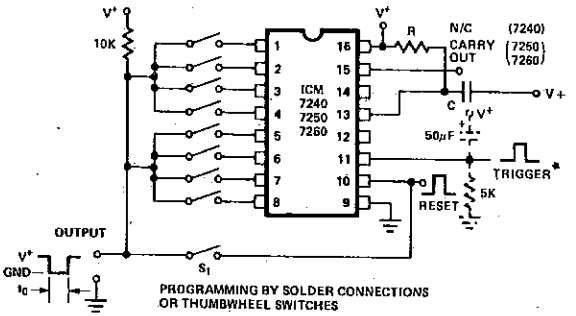


Figure 2. Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

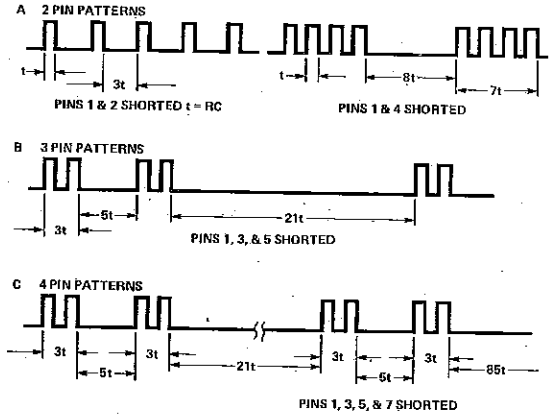


Figure 3. Pulse Patterns Obtained by Shorting Various Counter Outputs

NOTES ON THE COUNTER SECTION

Used as a straight binary counter (ICM7240), as a ÷100 (ICM7250), or ÷60 (ICM7260) all devices are significantly faster than their bipolar equivalents. However, when using these devices as *programmable* counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), 100 (ICM7250), or 60 (ICM7260) the maximum input frequency must be limited to approximately 100 KHz or less (with V+ equal to +5 volts). The reason for this is two-fold:

a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter (8 counters for the ICM7240/50 and 7 for the ICM7260). Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the Reset/Trigger signal.

b. There must be a delay of the positive going output to the Reset terminal, (pin 10) and the Trigger terminal (pin 11). The Reset signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The trigger overrides Reset.

The delay between Trigger and Reset is generated by the signal RC network consisting of the 56kΩ resistor and the 330pF capacitor.

The delay caused by the counter Ripple delays can be as long as 2μs (5 volt supply), and the delay between Reset and Trigger should be at least 2 μs. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 4 and 5.

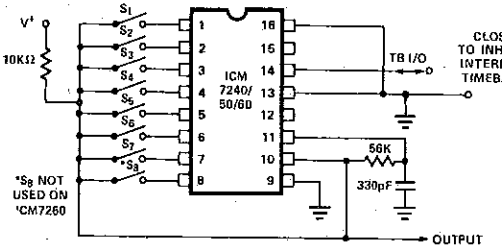


Figure 4. Programming the Counter Section of the ICM7240/50/60

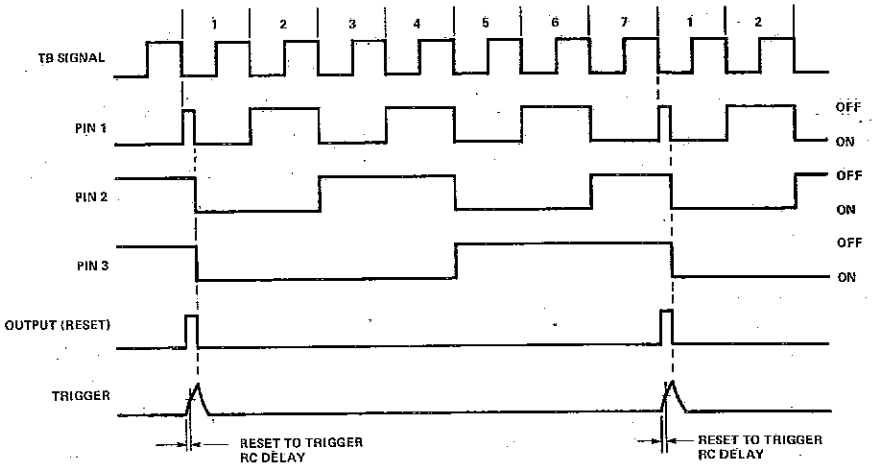


Figure 5. Waveforms for Programming the Counter Section for a Division Ratio of 7 (S_1, S_2, S_3 Closed)

APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V^+ may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200 KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time $\leq$ 1μs); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50/60.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C , a wide variety of sequence timing can be realized. A typical flow chart for a

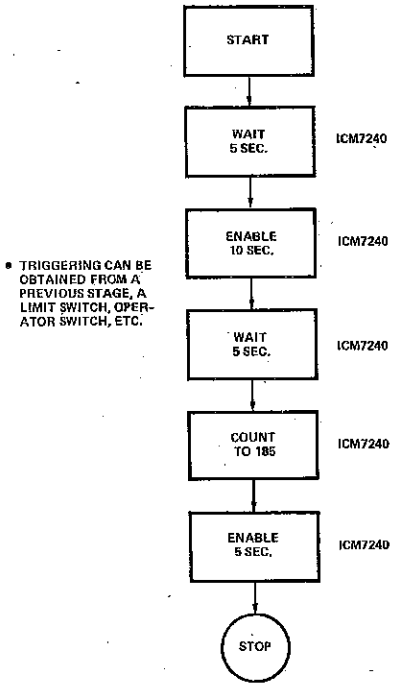


Figure 6.

CMOS PRECISION PROGRAMMABLE 0-99 SECONDS/MINUTES LABORATORY TIMER

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown, the timer can accurately measure preselected time intervals of 0-99 seconds or 0-99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0-99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the pre-programmed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.

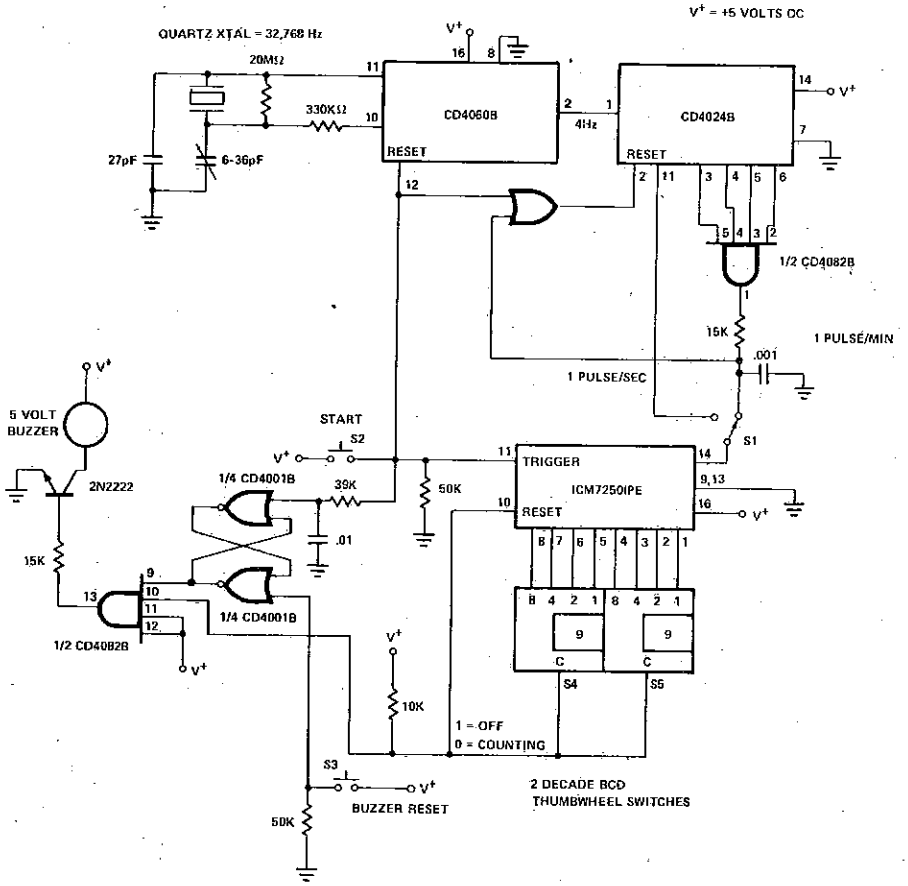


Figure 7.

LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four $\overline{\text{WRITE}}$ pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

With a resistor of approximately 10 MΩ and capacitor of 0.1 μF, the time base of the ICM7240 is one second. Thus, a time of 1-255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.

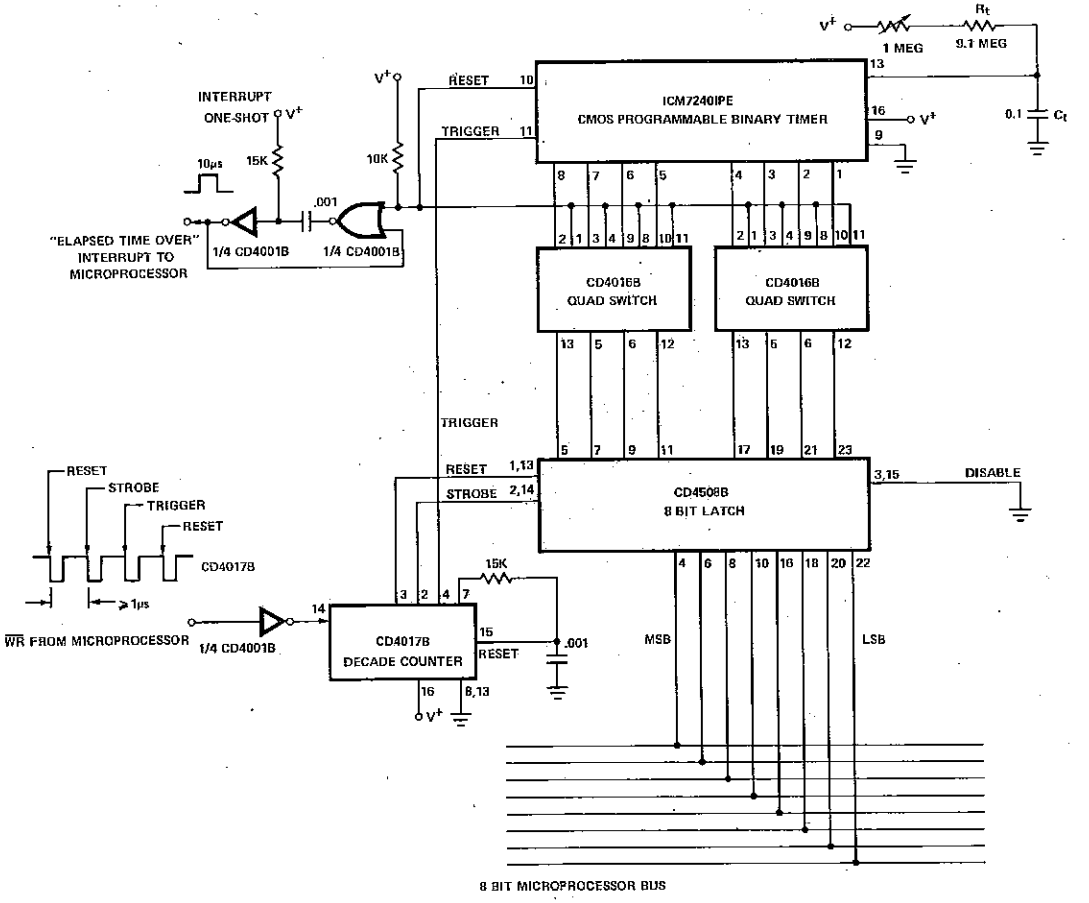
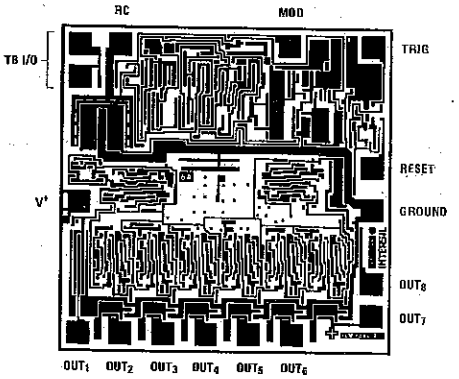


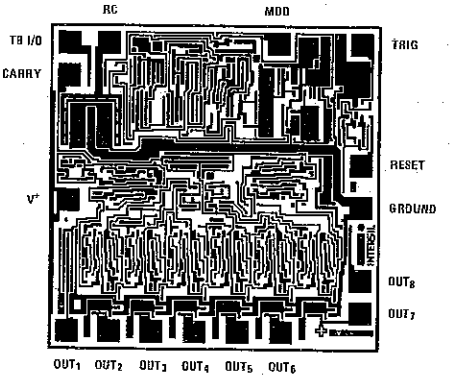
Figure 8.

ICM7240/50/60

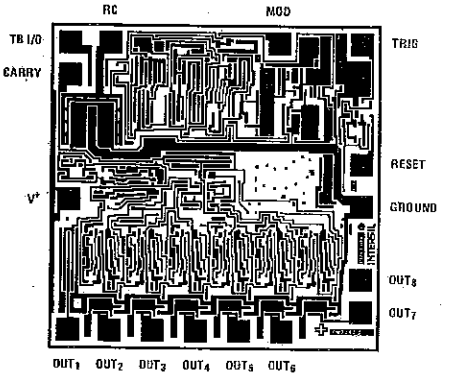
CHIP TOPOGRAPHY



ICM7240



ICM7250



ICM7260

ALL CHIPS 68 x 69 mils

ICM7242
Long Range
Fixed Timer/Counter

FEATURES

- **Replaces the 2242 in most applications**
- **Timing from microseconds to days**
- **Cascadeable**
- **Monostable or astable operation**
- **Wide supply voltage range: 2-16 volts**
- **Low supply current: 115μA @ 5 volts**
- **Extended temperature range: -20°C to +85°C**

GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in 95% of the applications, with a significant reduction in the number of external components.

Three outputs are provided. They are, the oscillator output, and buffered outputs from the first and eighth counters.

The ICM7242 is packaged in an 8-pin CERDIP.

ABSOLUTE MAXIMUM RATINGS

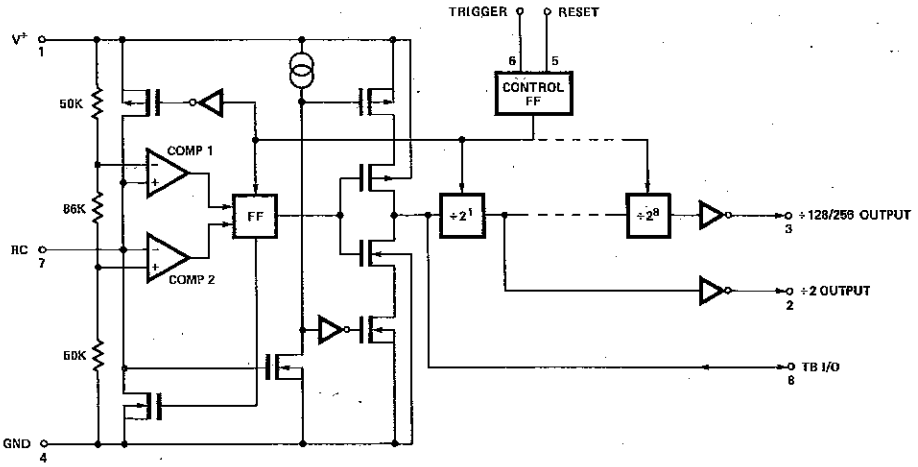
Supply Voltage 18V
Input Voltage[1]
Terminals (Pins 5, 6, 7, 8) ..... GND -0.3V to V^++ 0.3V
Maximum continuous output current (each output) ..... 50 mA
Power Dissipation[2] ..... 200 mW
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply by applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. Derate at -2 mW/°C above 25°C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

6

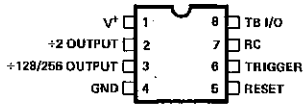
BLOCK DIAGRAM



ORDERING INFORMATION

Device:	ICM7242IJA
Dice:	ICM7242/D

PIN CONFIGURATION (OUTLINE DRAWING JA)

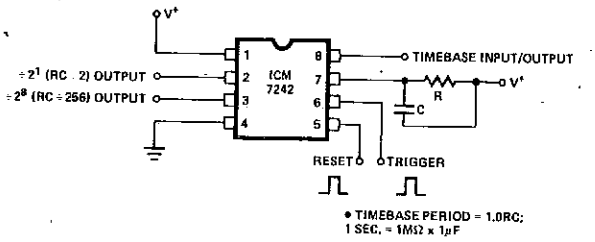


ELECTRICAL CHARACTERISTICS

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, $R = 10K\Omega$, $C = 0.1\mu F$		340	800	μA
		Operating, $R = 1M\Omega$, $C = 0.1\mu F$		220	600	μA
		TB Inhibited, RC Connected to GND		225		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	Independent of RC Components		250		ppm/°C
Time Base Output Voltage	V_{OTB}	$I_{SOURCE} = 1$ mA	3.5	4.2		V
		$I_{SINK} = 3.2$ mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Trigger/Reset Input Current	I_{TRIG}, I_{RST}			10		μA
Max Count Toggle Rate	f_t	$V^+ = 2V$		1		MHz
		$V^+ = 5V$ — Counter/Divider Mode	2	6		MHz
		$V^+ = 15V$		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, $I_{OUT} = 3.2$ mA		0.22	0.4	V
Output Sourcing Current 7242	I_{SOURCE}	$V^+ = 5V$ Terminals 2 & 3, $V_{OUT} = 1V$		300		μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ = 2 \cdot 16V$	1K		22M	Ω

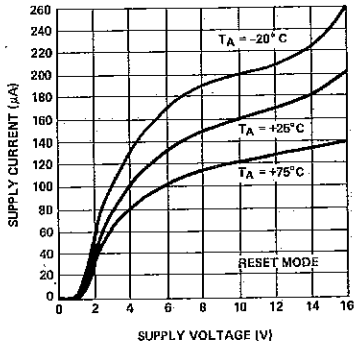
TEST CIRCUIT



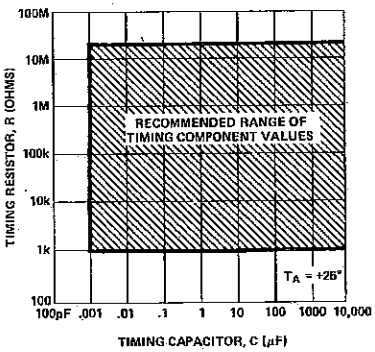
NOTE: OUTPUTS ÷2¹ AND ÷2⁸ ARE INVERTERS AND HAVE ACTIVE PULLUPS.

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

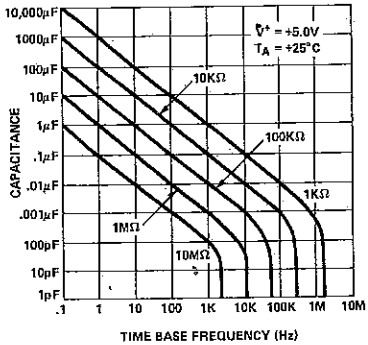


RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

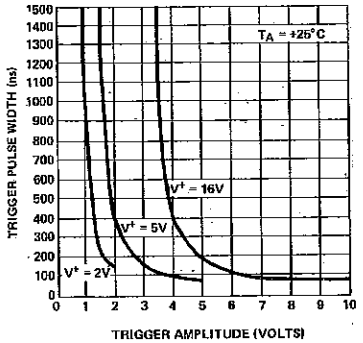


DIMENSIONS IN INCHES AND MILLIMETERS

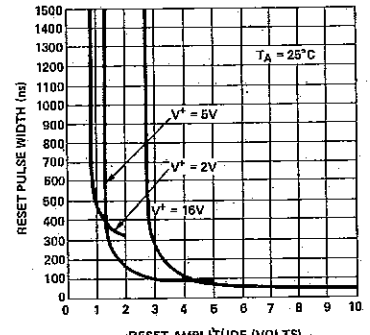
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



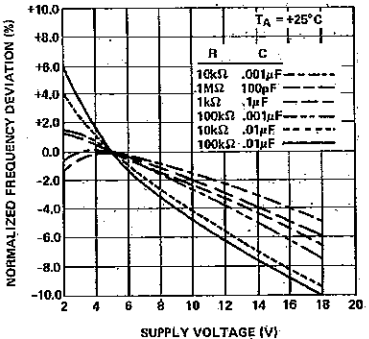
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



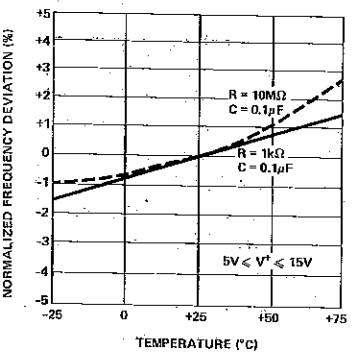
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



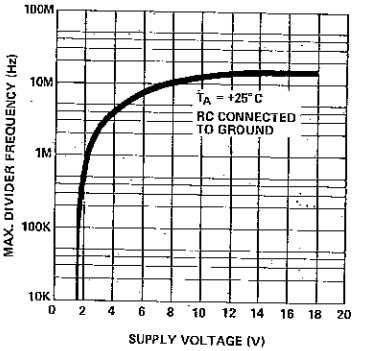
6

TYPICAL PERFORMANCE CHARACTERISTICS

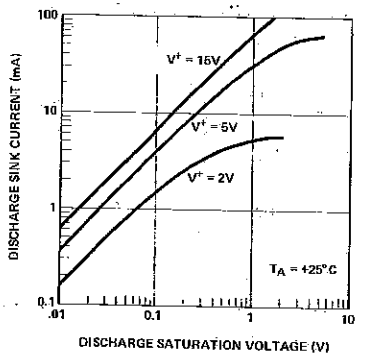
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



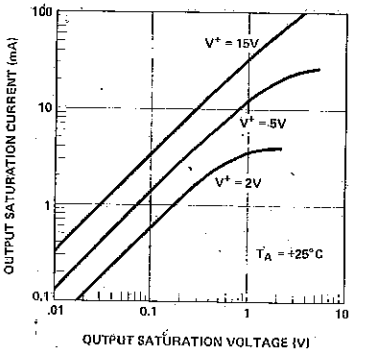
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V^+ may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

OPERATING LIMITS

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200 KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge

on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\div 2^8$ output returns to the high state.

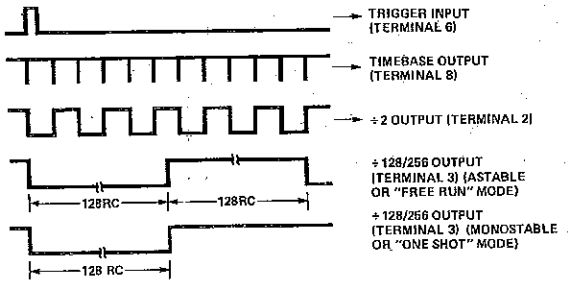


Figure 1. Timing Diagrams of Output Waveforms for the ICM7242. (Compare with Figure 5)

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.

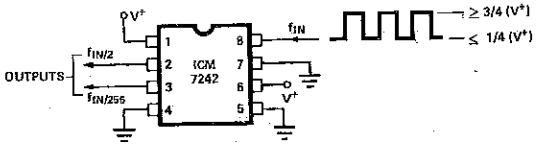


Figure 2. Using the ICM7242 as a Ripple Counter (Divider)

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 3).

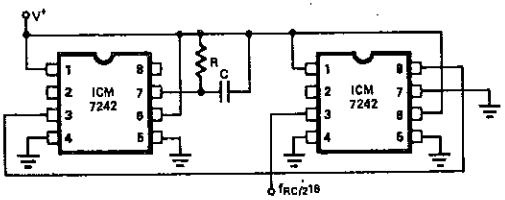


Figure 3. Low Frequency Reference (Oscillator)

For monostable operation the $\div 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p-resistors have been used on the ICM7242 to provide the comparator

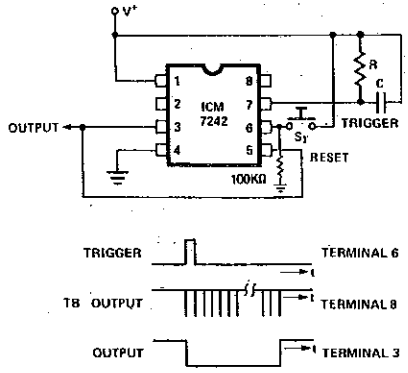


Figure 4. Monostable Operation

COMPARING THE ICM7242 WITH THE 2242

		ICM7242	2242
a.	Operating Voltage	2-16V	4-15V
b.	Commercial Temp. Range	-20°C to +75°C	0°C to +75°C
c.	Supply Current $V^+ = 5V$	0.7 mA Max.	7 mA Max.
d.	Pullup Resistors		
	TB Output	No	Yes
	÷2 Output	No	Yes
	÷256 Output	No	Yes
e.	Toggle Rate	3.0 MHz	0.5 MHz
f.	Resistor to Inhibit Oscillator	No	Yes
g.	Resistor in Series with Reset for Monostable Operation	No	Yes
h.	Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C , a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

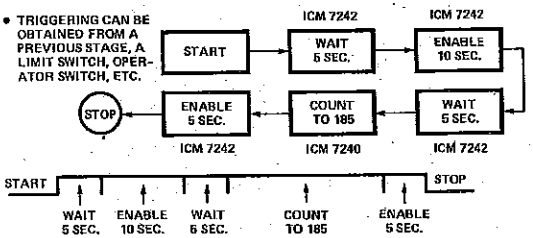


Figure 5.

By cascading devices, use of low cost CMOS AND/ OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

SEQUENCE TIMING

- Process Control
- Machine Automation
- Electro-pneumatic Drivers
- Multi-operation (Serial or Parallel controlling)

SEQUENCE TIMER:

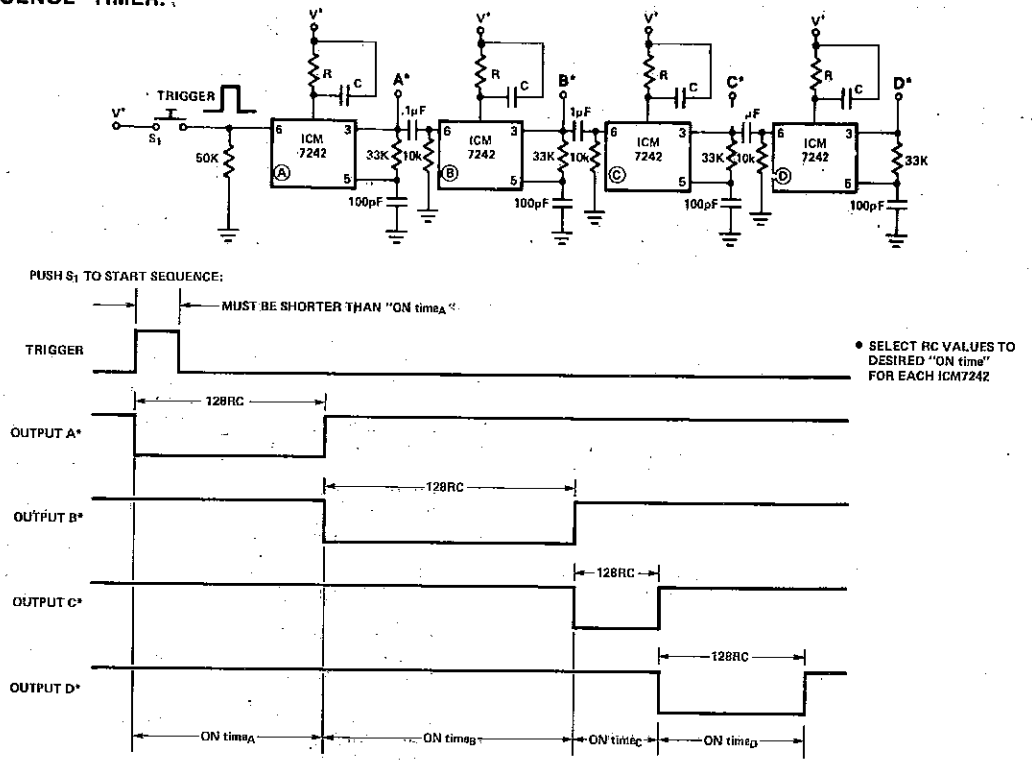
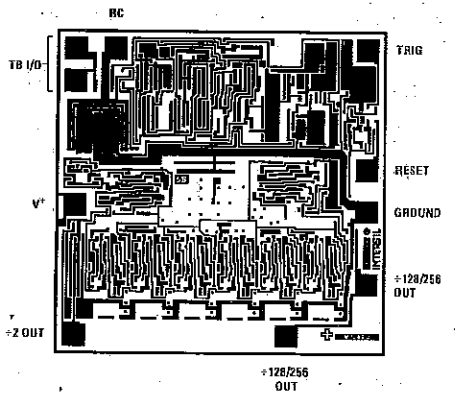


Figure 6.

CHIP TOPOGRAPHY (.068" × .069")



ICM7243

8-Character 14-/16-Segment Alphanumeric LED Display Driver

FEATURES

- **14- and 16-segment fonts with decimal point**
- **Mask programmable for other font-sets up to 64 characters**
- **Microprocessor compatible**
- **Directly drives small common cathode displays**
- **Cascadable without additional hardware**
- **Standby feature turns display off; puts chip in low power mode**
- **Serial entry or random entry of data into display**
- **Single + 5V operation**
- **Character and segment drivers, all MUX scan circuitry, 8 × 6 static memory and 64-character ASCII font generator included on-chip**

GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it offloads the processor and minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, an 8 × 6 memory, the high power character and segment drivers, and the multiplex scan circuitry.

Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Serial** (MODE = 1) or **Random** (MODE = 0). In the **Serial Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

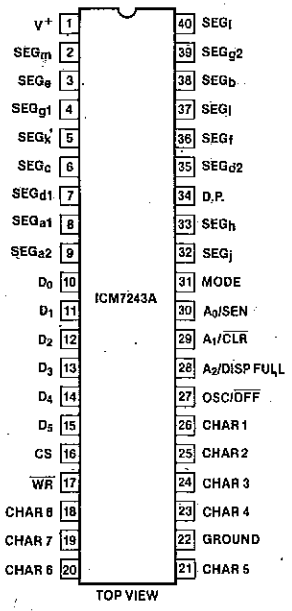
The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

ORDERING INFORMATION

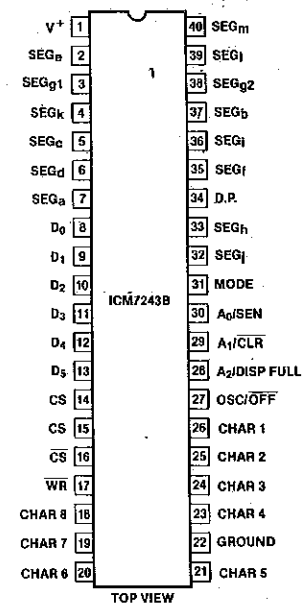
Part Number	Display Segments	Package	Order Number
ICM7243A	16 + d.p.	40 Pin CERDIP	ICM7243AIJL
ICM7243B	14 + d.p.	40 Pin CERDIP	ICM7243BIJL
ICM7243B EV/KIT	Kit with Display		ICM7243B EV/KIT

6

PIN CONFIGURATIONS



TOP VIEW



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
CHARacter Output Current 300mA
SEGment Output Current 30mA
Input Voltage (Any Terminal) ..... ($V^+ + 0.3V$) to $-0.3V$

Power Dissipation 1W
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Voltage	V^+		4.75	5.0	5.25	V
Operating Supply Current	I^+_{OP}	$V^+ = 5.25V$, 10 Segments ON, All 8 Characters		180		mA
Quiescent Supply Current	$I_Q{}^+$	$V^+ = 5.25V$, OSC/$\overline{OFF}$ Pin $< 1V$		30	250	µA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	$V^+ = 5.25V$, $V_{IH} = 5V$			+1	µA
		$V_{IL} = 0V$	−1			
CHARacter Drive Current	I_{CHAR}	$V^+ = 5V$, $V_{OUT} = 1V$	140	190		mA
CHARacter Leakage Current	I_{CHLK}					µA
SEGment Drive Current	I_{SEG}	$V^+ = 5V$, $V_{OUT} = 2.5V$	14	19		mA
SEGment Leakage Current	I_{SLK}			0.01		µA
DISPlay FULL Output Low	V_{OL}	$I_{OL} = 1.6mA$			0.4	V
DISPlay FULL Output High	V_{OH}	$I_{IH} = 100\mu A$	2.4			V
Display Scan Rate	f_{ds}			400		Hz

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AC CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V)

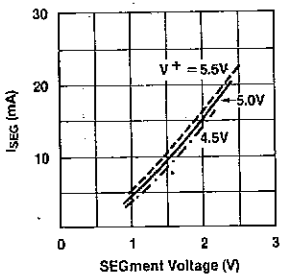
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low	t_{WPl}		250			ns
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High	t_{WPh}		250			
Data Hold Time	t_{Dh}		0	−20		
Data Setup Time	t_{Ds}		250	150		
Address, SEN, MODE Hold Time	t_{Ah}		125	80		
Address, SEN, MODE Setup Time	t_{As}		−20			
CS, $\overline{CS}$ Setup Time	t_{Cs}		0			
Pulse Transition Time	t_t				100	

CAPACITANCE

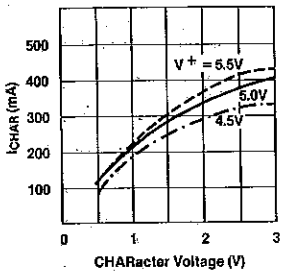
SYMBOL	TEST	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance				pF
C_O	Output Capacitance				pF

TYPICAL PERFORMANCE CURVES

SEGment Current vs Output Voltage

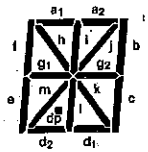


CHARacter Current vs Output Voltage



ICM7243A/B DISPLAY FONT, SEGMENT ASSIGNMENTS

Note: Some display manufacturers use different designations for some of the segments. Check data sheets carefully.



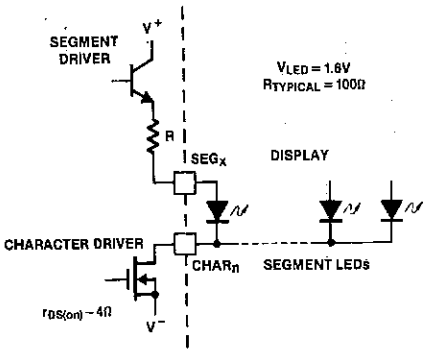
D5, D4	D3	D2	D1	D0	
00	0	0	0	0	
00	0	0	0	1	
00	0	0	1	0	
00	0	0	1	1	
00	0	1	0	0	
00	0	1	0	1	
00	0	1	1	0	
00	0	1	1	1	
00	1	0	0	0	
00	1	0	0	1	
00	1	0	1	0	
00	1	0	1	1	
00	1	1	0	0	
00	1	1	0	1	
00	1	1	1	0	
00	1	1	1	1	
01	0	0	0	0	
01	0	0	0	1	
01	0	0	1	0	
01	0	0	1	1	
01	0	1	0	0	
01	0	1	0	1	
01	0	1	1	0	
01	0	1	1	1	
01	1	0	0	0	
01	1	0	0	1	
01	1	0	1	0	
01	1	0	1	1	
01	1	1	0	0	
01	1	1	0	1	
01	1	1	1	0	
01	1	1	1	1	
10	0	0	0	0	
10	0	0	0	1	
10	0	0	1	0	
10	0	0	1	1	
10	0	1	0	0	
10	0	1	0	1	
10	0	1	1	0	
10	0	1	1	1	
10	1	0	0	0	
10	1	0	0	1	
10	1	0	1	0	
10	1	0	1	1	
10	1	1	0	0	
10	1	1	0	1	
10	1	1	1	0	
10	1	1	1	1	
11	0	0	0	0	
11	0	0	0	1	
11	0	0	1	0	
11	0	0	1	1	
11	0	1	0	0	
11	0	1	0	1	
11	0	1	1	0	
11	0	1	1	1	
11	1	0	0	0	
11	1	0	0	1	
11	1	0	1	0	
11	1	0	1	1	
11	1	1	0	0	
11	1	1	0	1	
11	1	1	1	0	
11	1	1	1	1	

ICM7243A
16-Segment Character Font with Decimal Point

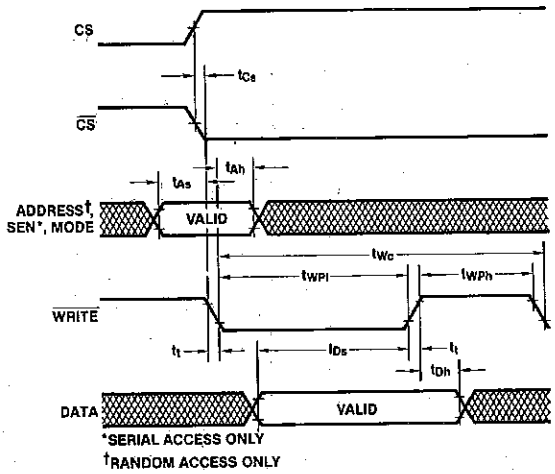
D5, D4	D3	D2	D1	D0	
00	0	0	0	0	
00	0	0	0	1	
00	0	0	1	0	
00	0	0	1	1	
00	0	1	0	0	
00	0	1	0	1	
00	0	1	1	0	
00	0	1	1	1	
00	1	0	0	0	
00	1	0	0	1	
00	1	0	1	0	
00	1	0	1	1	
00	1	1	0	0	
00	1	1	0	1	
00	1	1	1	0	
00	1	1	1	1	
01	0	0	0	0	
01	0	0	0	1	
01	0	0	1	0	
01	0	0	1	1	
01	0	1	0	0	
01	0	1	0	1	
01	0	1	1	0	
01	0	1	1	1	
01	1	0	0	0	
01	1	0	0	1	
01	1	0	1	0	
01	1	0	1	1	
01	1	1	0	0	
01	1	1	0	1	
01	1	1	1	0	
01	1	1	1	1	
10	0	0	0	0	
10	0	0	0	1	
10	0	0	1	0	
10	0	0	1	1	
10	0	1	0	0	
10	0	1	0	1	
10	0	1	1	0	
10	0	1	1	1	
10	1	0	0	0	
10	1	0	0	1	
10	1	0	1	0	
10	1	0	1	1	
10	1	1	0	0	
10	1	1	0	1	
10	1	1	1	0	
10	1	1	1	1	
11	0	0	0	0	
11	0	0	0	1	
11	0	0	1	0	
11	0	0	1	1	
11	0	1	0	0	
11	0	1	0	1	
11	0	1	1	0	
11	0	1	1	1	
11	1	0	0	0	
11	1	0	0	1	
11	1	0	1	0	
11	1	0	1	1	
11	1	1	0	0	
11	1	1	0	1	
11	1	1	1	0	
11	1	1	1	1	

NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

ICM7243B
14-Segment Character Font with Decimal Point



Segment and Character Drivers Output Circuit

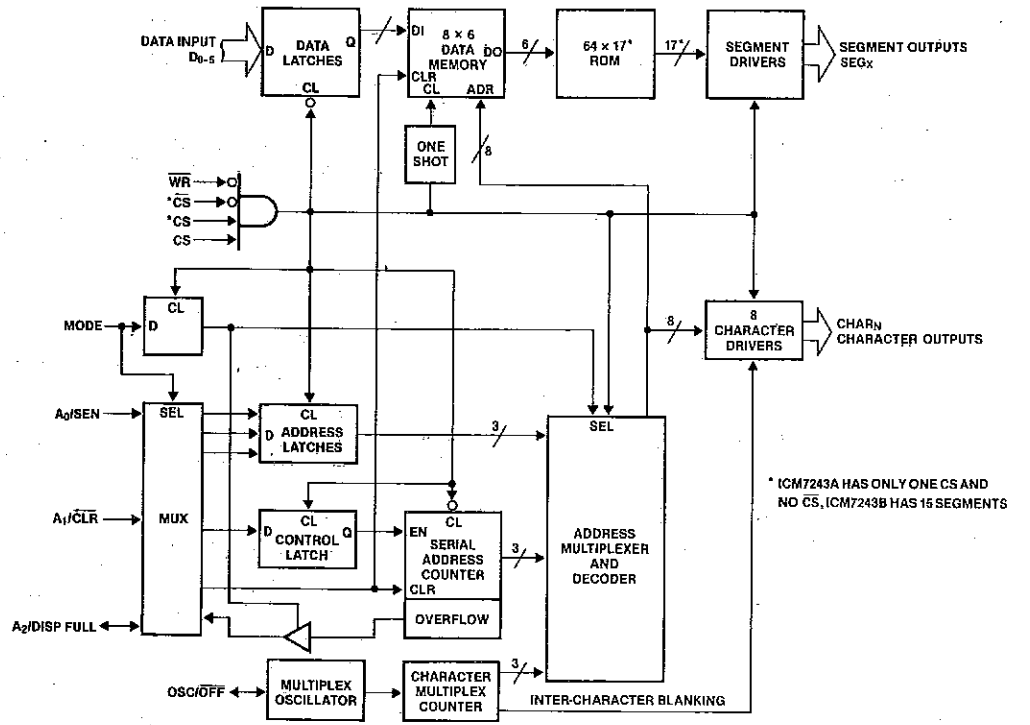


Data Entry Timing

PIN DESCRIPTIONS, ICM7243A *(B)*

SIGNAL	PIN	FUNCTION
D_0–D_5	10–15 *(8–13)*	Six-Bit ASCII Data input pins (active high).
CS, $\overline{CS}$	16 *(14–16)*	Chip Select for decoding from μP address bus, etc.
$\overline{WR}$	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and $\overline{WR}$ can be used as $\overline{CS}$.
MODE	31	Selects data entry MODE. High selects **Serial Access (SA)** mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the **Random Access (RA)** mode where data is displayed on the character addressed via A_0–A_2 Address pins.
A_0/SEN	30	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading display driver/controllers for displays of more than 8 characters (active high enables driver controller).
A_1/$\overline{CLeaR}$	29	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A_2/DISPlay FULL	28	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	27	OSCillator input pin. Adding capacitance to V^+ will lower the internal oscillator frequency. An external oscillator is also applied to this pin. A low puts the display controller/driver into a quiescent mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG_a–SEG_m, D.P.	2–9 *(7)*, 32–40	SEGment driver outputs.
CHARacter 1–8	18–21, 23–26	CHARacter driver outputs.

BLOCK DIAGRAM



DETAILED DESCRIPTION OF OPERATION

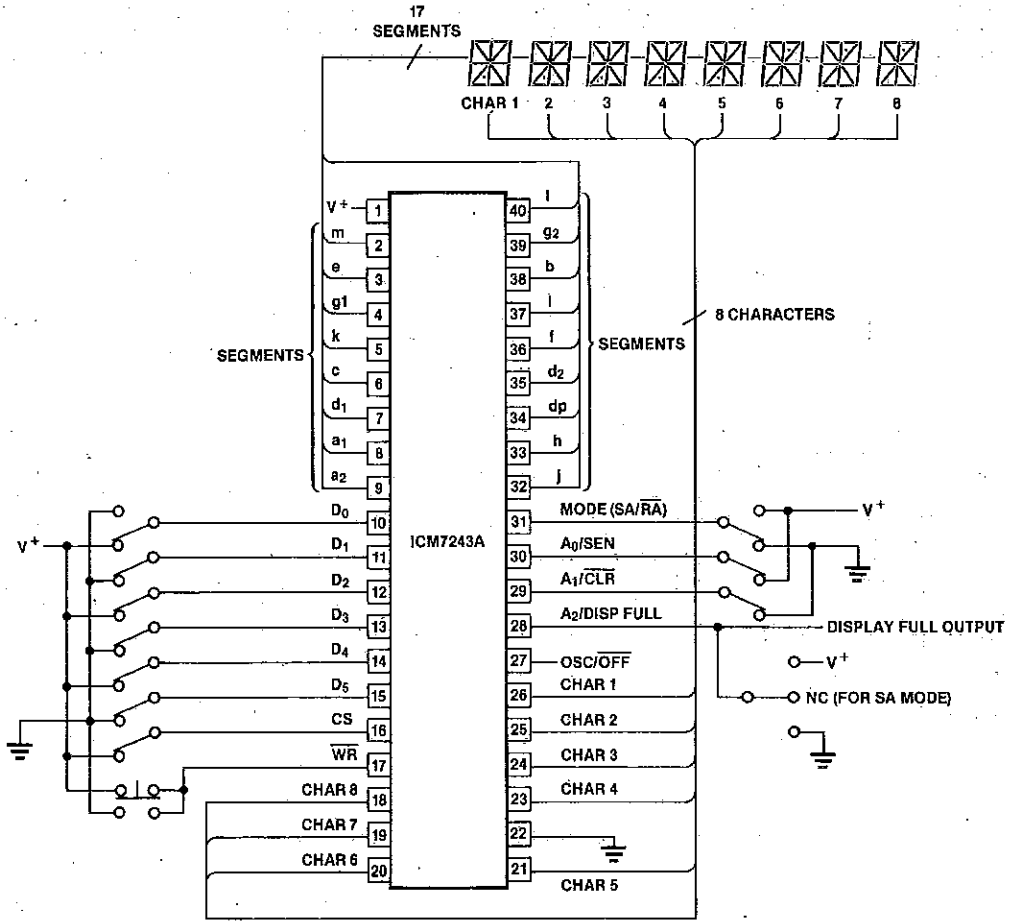
$\overline{WR}$, $\overline{CS}$, CS. These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS and $\overline{CS}$ enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5nsecs) greater than from $\overline{WR}$ or $\overline{CS}$ due to the additional inverter required on the former.

MODE. The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see above). The location in Data Memory where incoming data will be placed is determined either from the Address pins or the Serial Address Counter, under control of this latch, which also controls the function of A_0/SEN, $A_1/\overline{CLR}$, and A_2/DISPlay FULL.

Random Access Mode. When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A_0, A_1, and A_2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Serial Access Mode. If the internal latch is set for **Serial Access (SA)**, (MODE latched high), the Serial ENable input on SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Serial Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output is always active in **SA** mode also, and indicates the overflow status of the Serial Address Counter. If this output is low, and SEN is (latched as) high, the contents of the Counter will be used to establish the Data Memory location for the Data Input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur. This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Serial Access** mode.

TEST CIRCUIT (ICM7243A SHOWN)



Changing Modes. Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of $\overline{WR}$ (or its equivalent). When changing mode from **Serial Access to Random Access,** note that A_2/DISPlay FULL will be an output until $\overline{WR}$ has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Serial Access,** $A_1/\overline{CLR}$ should be high to avoid inadvertent clearing of the Data Memory and Serial Address Counter. DISPlay FULL will become active immediately after the falling edge of $\overline{WR}$.

Data Entry. The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/$\overline{OFF}$. The device includes a one-pin relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V+ at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter strobe lines (see **Display Output**). An inter-character blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Multiplex Counter. This puts the circuit in a low-power-dissipation passive condition in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output. The address output of the Multiplex Counter is multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in **Serial Access** mode, with SEN high and DISPlay FULL low), to control display operations. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5μsec). Each CHARacter output lasts nominally about 300μsec, and is repeated nominally every 2.5msec, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL low for **Serial Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

6 APPLICATIONS

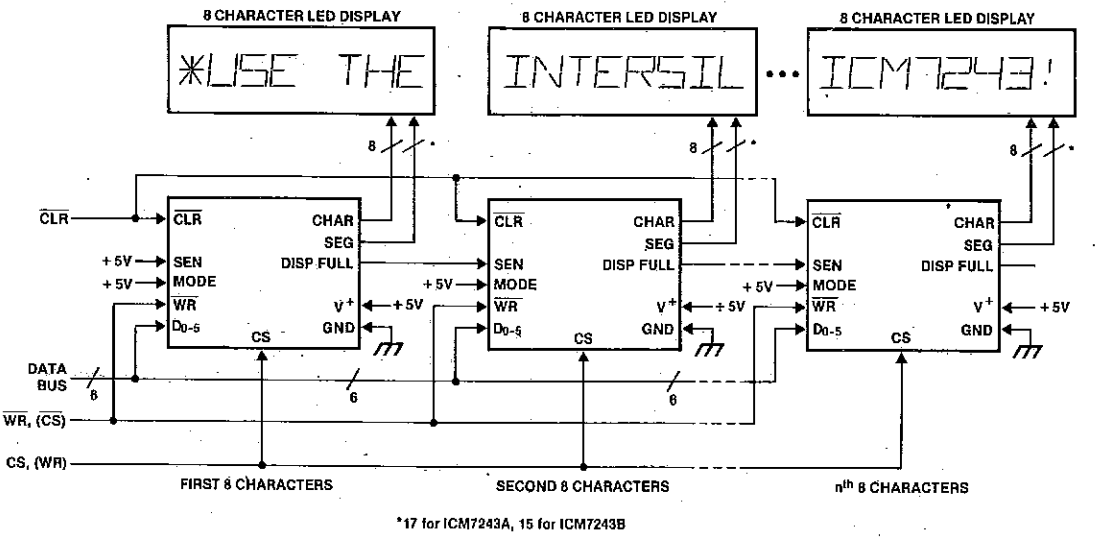


Figure 1. Multicharacter Display using Serial Access Mode

APPLICATIONS (Continued)

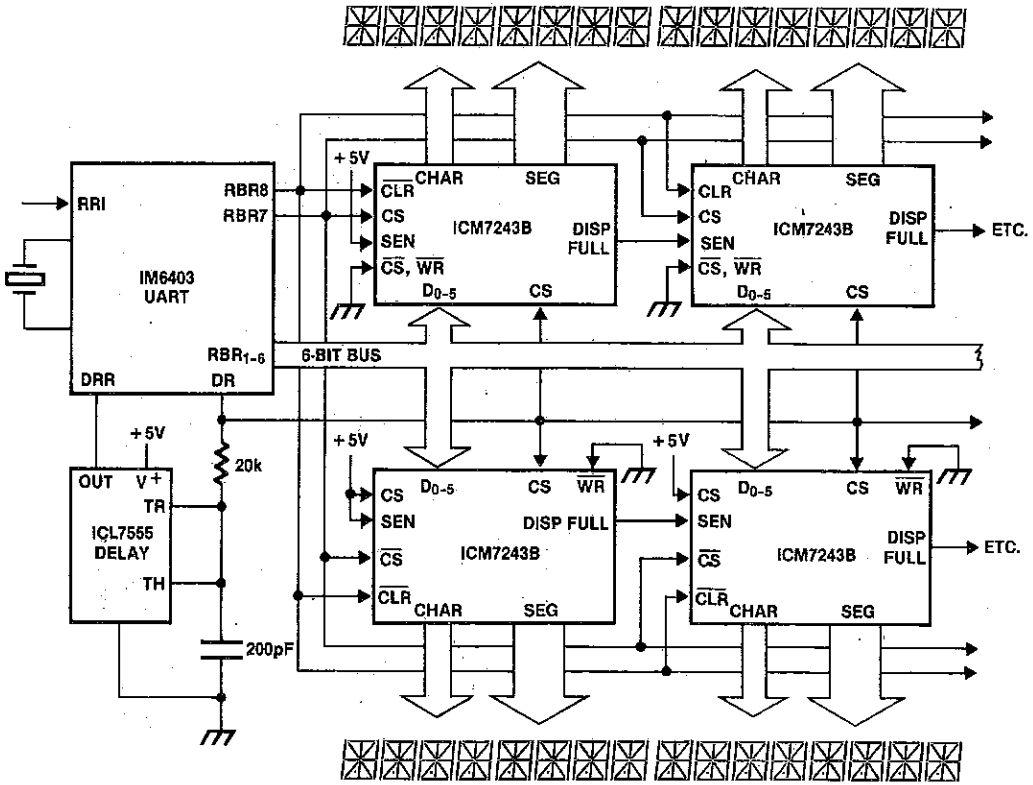


Figure 2. Driving Two Rows of Characters from a Serial Input. UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

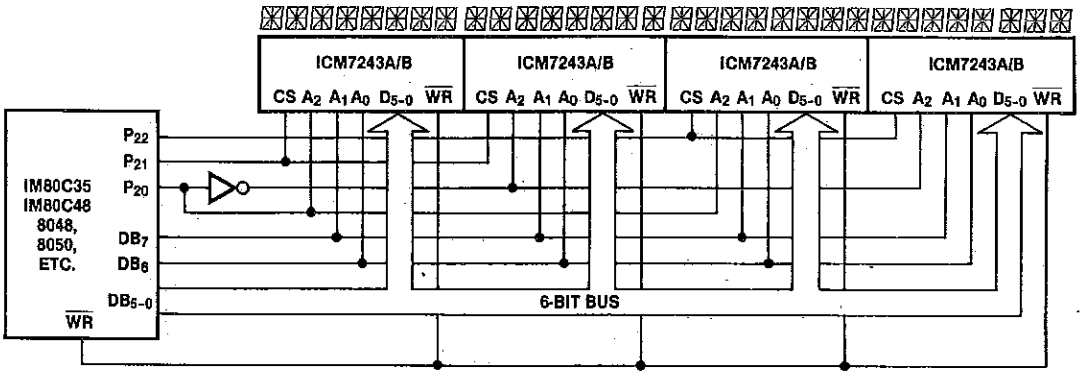


Figure 3. Random Access 32-Character Display in MCS-48 system. One port line controls A_2, other two are CS lines. 8-bit data bus drives 6 data and 2 address lines. MODE should be GrouNDed on each part.

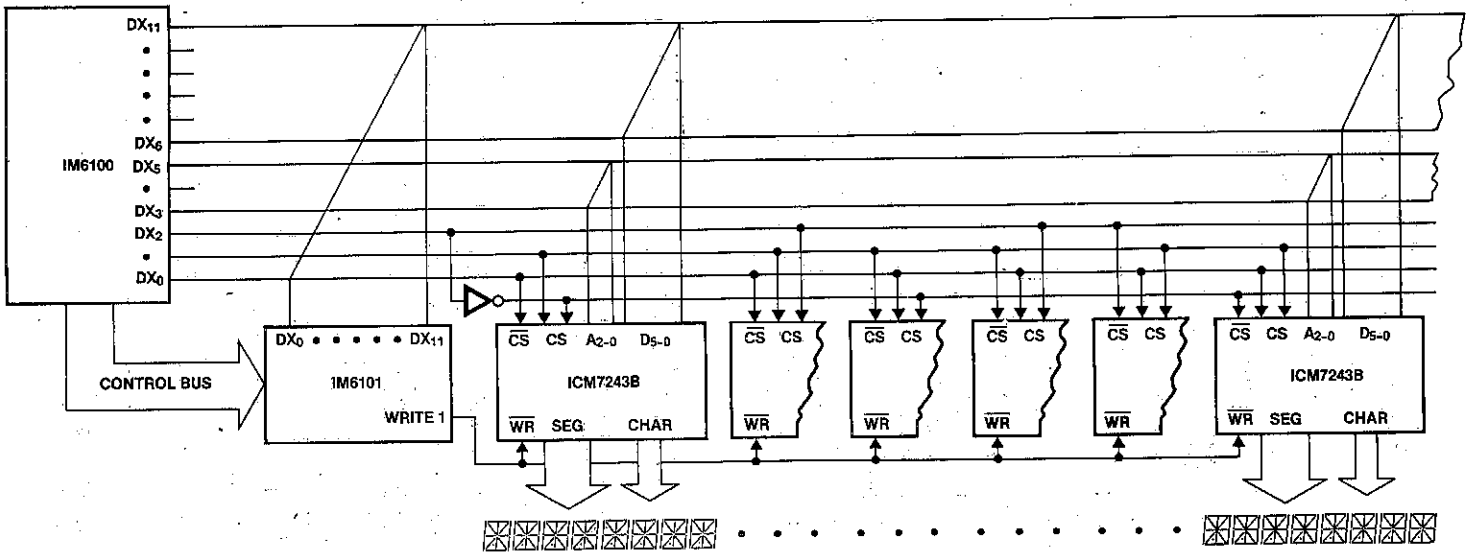


Figure 4. A 48-Character Random Access Display. 12-bit bus split into 6 bits data, 3 bits address within chip, and 3 bits chip address. Inverting one of these chip address lines allows selection of one of 6 chips without decode, using CS and $\overline{CS}$ lines on ICM7243B. Standard 1-of-8 decoder can select 64-character array using ICM7243A/B. WRITE 2 can be used for another row in either case.

APPLICATIONS (Continued)

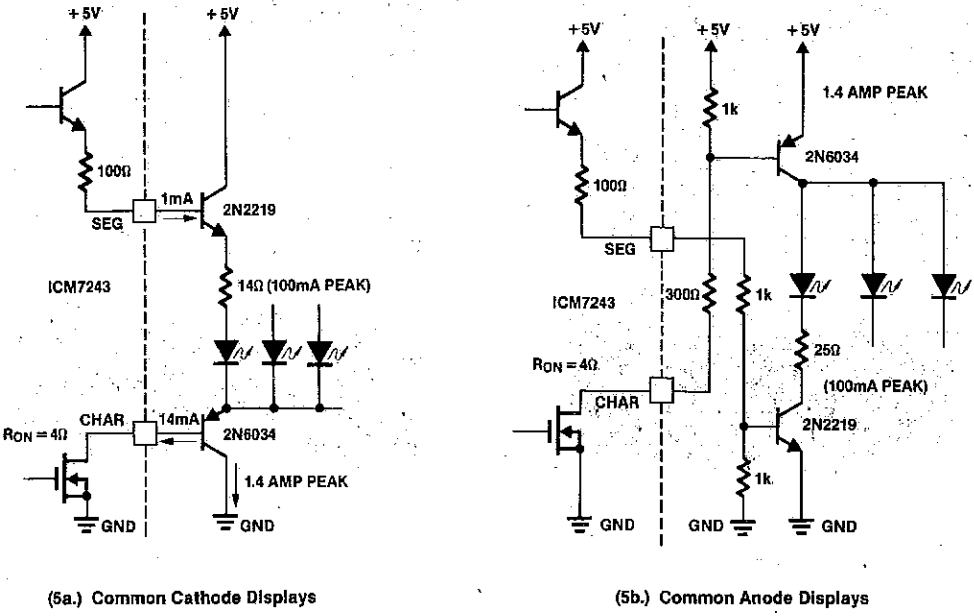


Figure 5. Driving Large Displays. The circuits of Figures 5a and 5b can be used to drive 0.5" or larger alphanumeric displays, either common cathode (5a) or common anode (5b).

COMPONENT SELECTION

Displays suitable for use with the ICM7243 may be obtained from the following manufacturers; among others:

Hewlett Packard Components, Palo Alto, California
(415) 857-6620 (part #HDSP6508, HDSP6300)

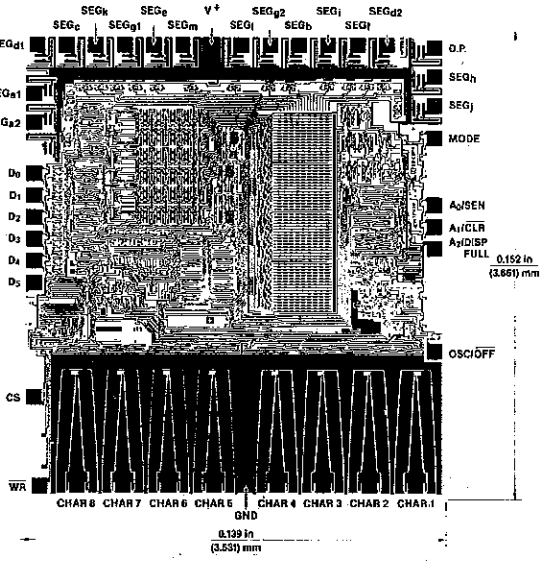
General Instruments Inc., Palo Alto, California
(415) 493-0400 (part #MAN2815)

Texas Instruments Inc., Dallas, Texas
(214) 995-6611 (part #HDSP6508)

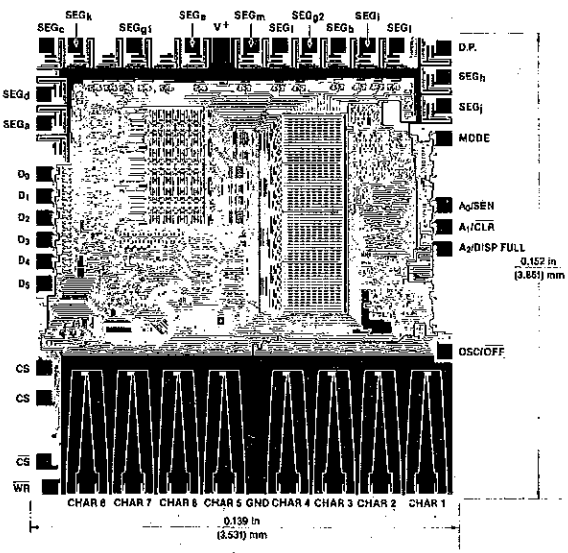
A.N.D., Burlingame, California
(415) 347-9916 (part #AND370R)

IEE Inc., Van Nuys, California
(213) 787-0311 (part #LR3784R)

CHIP TOPOGRAPHIES



ICM7243A



ICM7243B

ICM7281
LCD Column Driver

FEATURES

- LCD Dot Matrix Column Driver
- 40 High Voltage LCD Column Drive Outputs For Up to 8 5xN Characters per IC
- Easy Interface
  - —Serial Input Shift Register With parallel latch and carry outputs
- Directly Compatible with ICM7280 Row Driver
  - —Up to 10 ICM7281's can be driven by an ICM7280 with no external components
- Low Resistance Outputs
  - —Can drive both columns and rows of LCD graphics displays
- Will Drive 1.5V Threshold LCDs with Only Single 5V Supply
  - —Can drive up to 4.5V threshold LCDs with 15V V_{DISP}

GENERAL DESCRIPTION

The ICM7281 LCD Dot Matrix Column Driver is designed to convert a serial data stream into drive signals for a multiplexed dot matrix LCD. Easily cascadable, up to 10 ICM7281's can be driven by one ICM7280 Intelligent Row Driver to make an 80 character dot matrix display. The ICM7281 also serves as both a Row Driver and Column Driver in LCD dot matrix graphics displays. The low output resistance and the 15V drive capability make it well suited for graphics displays with up to 256 x 256 dots (with 10pF/dot capacitance).

The ICM7281 consists of a 40 bit shift register, a 40 bit latch and 40 level-shifters/drivers. The 4 display drive voltages are generated externally, usually by a Row Driver. A serial data interface is used to minimize the number of pins needed for digital interfacing. Two data Carry Outputs are included for cascading several ICM7281's to drive large LCD displays.

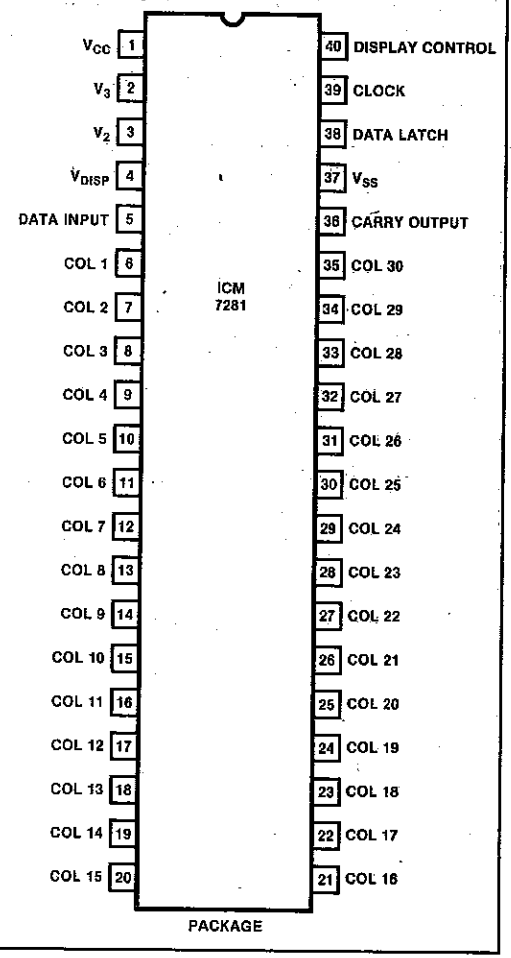
ORDERING INFORMATION

No. Of Columns	Package	Order Number
30	40 Pin Plastic	ICM7281IPL
40	Dice	ICM7281I/D
40	52-64 Pin Plastic Flatpack	—

TYPICAL APPLICATIONS

- Column Drivers for Dot Matrix Alpha-numeric Displays using ICM7280 Row Driver
- Row and Column Drivers for LCD Dot Matrix Graphics Displays
- Segment Driver for LCD Bargraphs and Annunciators
- Serial Input I/O Expander

PIN CONFIGURATIONS
(Outline dwg. PL)



6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} — V_{SS}) 6V

Display Voltage (V_{CC} — V_{DISP}) 18V

Input Voltage (Note 1) . . . . V_{CC} + 0.3V to V_{SS} − 0.3V

Power Dissipation (Note 2) . . . . . 0.3W @ + 85°C

Operating Temperature Range . . . . − 20°C to + 85°C

Storage Temperature Range . . . . . − 65°C to + 150°C

V_2, V_3 . . . . . V_{DISP} to V_{CC}

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in any junction isolated CMOS device, connecting an Input to any voltage greater than V_{CC} or less than ground may cause destructive device latch-up. If the input voltage can exceed the recommended range, the input should be limited to less than 1 mA to avoid latch-up.

NOTE 2: This limit refers to that of the package and will not occur during normal operation.

OPERATING CHARACTERISTICS

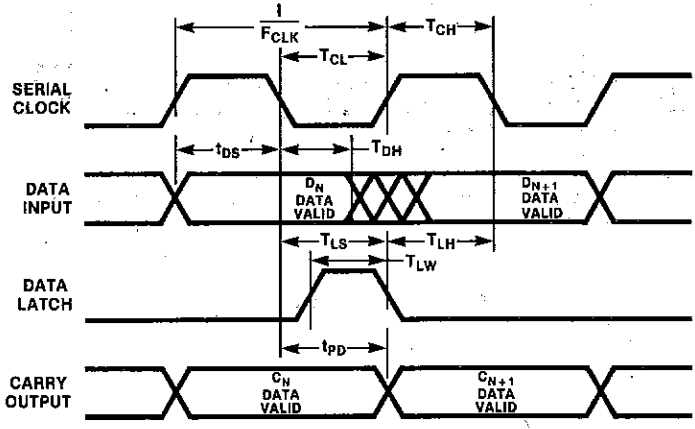
(V_{CC} = 5V ± 10%, V_{DISP} = − 10V, V_2 = 1/3 (V_{CC}-V_{DISP}), V_3 = 2/3 (V_{CC} - V_{DISP}), V_{SS} = 0V, T_A = − 20 to + 85°C) Unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SUPPLY CHARACTERISTICS						
Operating Supply Range	V_{SUPP}	V_{SS} = 0V	4.5	5.0	5.5	V
Display Voltage	V_{DISP}	V_{CC} = 5V, $V_{DISP} < (V2,V3) < V_{CC}$	− 10		V_{CC}	V
Supply Current Quiescent Dynamic	 I_{CC} I_{CC}	 F_{CLK} = 0 F_{CLK} = 500KHz		 .1 450	 10 1000	uA
INPUT CHARACTERISTICS						
Logic 1 Input Range	V_{IH}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	0.7V_{CC}		V_{CC}	V
Logic 0 Input Voltage	V_{IL}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	0		0.3V_{CC}	V
Input Current	I_{IN}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL $0 < V_{IN} < V_{CC}$	− 5	0.01	5	uA
Input Capacitance	C_{IN}	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL Dice Plastic Packaged Parts		 3 5		pF
OUTPUT CHARACTERISTICS, CARRY OUTPUTS						
Output High Voltage	V_{OH}	No Load I_{OH} = 400μA	V_{CC} − 0.05 2.4	V_{CC} 4.9		
Output Low Voltage	V_{OL}	No Load I_{OL} = 1.6mA		0 0.16	0.05 0.4	V

OPERATING CHARACTERISTICS (continued)

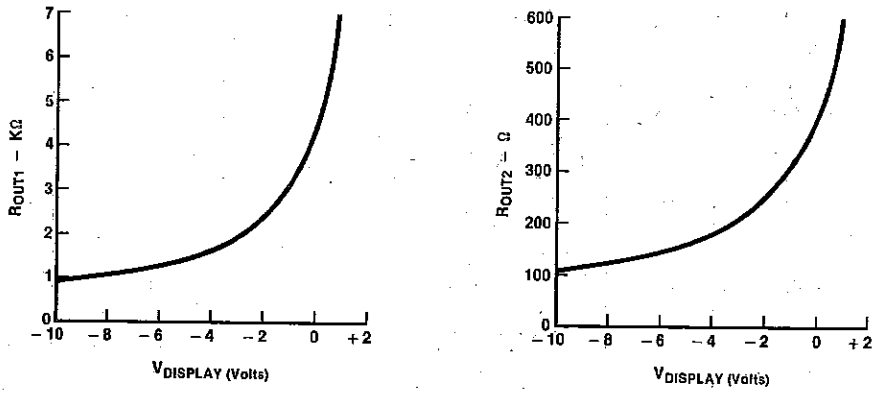
(V_{CC} = 5V ±10%, V_{DISP} = −10V, V_2 = 1/3 (V_{CC}-V_{DISP}), V_3 = 2/3 (V_{CC} - V_{DISP}), V_{SS} = 0V, T_A = −20 to +85°C) Unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
OUTPUT CHARACTERISTICS, COLUMN OUTPUTS						
Output Resistance	R_{OUT1}	V_{CC}-V_{DISP} = 10V, I_{OUT} = 0.1mA, V_{COL} = 0V, 1 Column ON		1	2	K Ohm
Output Resistance	R_{OUT2}	V_{CC}-V_{DISP} = 10V, V_{COL} = 0V I_{OUT} = 0.05mA per Column All Columns ON		150	250	Ohm
Column Rise Time	T_R	V_{CC}-V_{DISP} = 10V, C_L = 150pF per Column, 0-63% V3 to V_{CC} or 0-63% V2 to V_{DISP} One Column ON All Columns ON		0.3 1.5		µS
Column Fall Time	T_F	V_{CC}-V_{DISP} = 10V, C_L = 150pF per Column, 0-63% V_{CC} to V3 or 0-63% V_{DISP} to V2 One Column ON All Columns ON		0.3 1.5		µS
AC CHARACTERISTICS (See Timing Diagram)						
Data Setup	T_{ds}		150	90		ns
Data Hold	T_{dh}		0	−20		ns
Data Latch Width	T_{lw}		250	100		ns
Data Latch Setup	T_{ls}		625	250		ns
Data Latch Hold	T_{lh}		100			ns
Clock Frequency	F_{clk}		0	2	1	MHz
Clock High Period	T_{ch}		500			ns
Clock Low Period	T_{cl}		500			ns
Carry Prop Delay	T_{pd}	C_L = 15pF		200	350	ns

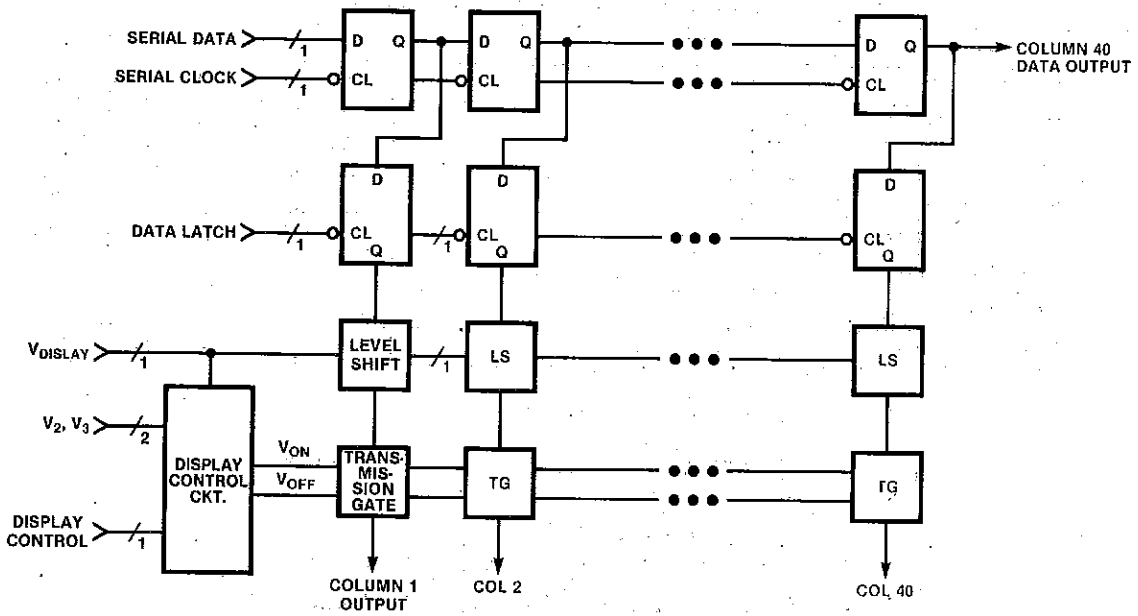


TIMING DIAGRAM

TYPICAL PERFORMANCE CURVES, 25°C



OUTPUT RESISTANCE vs. $V_{DISPLAY}$



ICM7281 COLUMN DRIVER BLOCK DIAGRAM

DETAILED DESCRIPTION

Data Interface

To reduce the pincount, the data interface is serial. The data on DATA INPUT is shifted into the shift register with each falling edge of CLOCK. The data in the shift register is also shifted one bit with each falling edge of CLOCK. The data in the 20th and 40th registers is available as COL 20 OUTPUT and COL 40 OUTPUT on the ICM7281 dice. The packaged part has only one CARRY OUTPUT, which is the 30th column. These outputs are normally used as the DATA INPUT for an adjacent ICM7281.

The DATA LATCH input is used to transfer data from the shift register to the 40 bit latch, which consists of 40 negative edge-triggered D flip-flops. The data in the shift register is stored by the falling edge of DATA LATCH and this latched data will be held until the next falling edge of DATA LATCH.

The DISPLAY CONTROL pin is used to convey multiplex timing information to the Column Drivers. This input is used as one of the two control inputs to the 1 of 4 analog multiplexer that drives each column output.

Figure 1 shows a typical interface between an array of ICM7281's and the ICM7280 Intelligent Row Driver. The Column Driver also readily interfaces with microprocessors, as shown in the block diagram of a graphics display, Figure 2.

LCD Interface

The ICM7281 uses a modified Alt and Pleshko multiplexing scheme, in which the Column Driver uses 4 voltages: V_{CC}, V2, V3, and V_{DISP}. These drive voltages are generated externally, usually by the ICM7280 Intelligent Row Driver. Each column output is driven by an analog multiplexer. The truth table and a schematic of this multiplexer are shown in Figure 3. The column data is the data that is serially loaded into the shift register, then parallel loaded into the data latch. The DISPLAY CONTROL signal, generated by the ICM7280 Row Driver, tells the ICM7281 which half of the mux cycle is occuring.

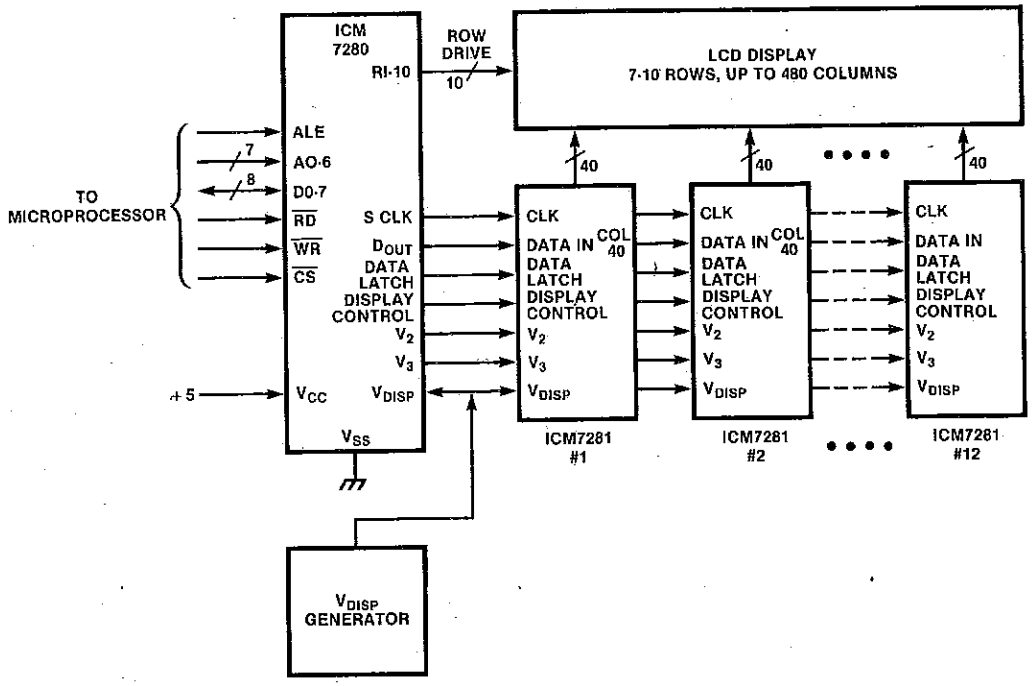


Figure 1. Alphanumeric LCD Display System

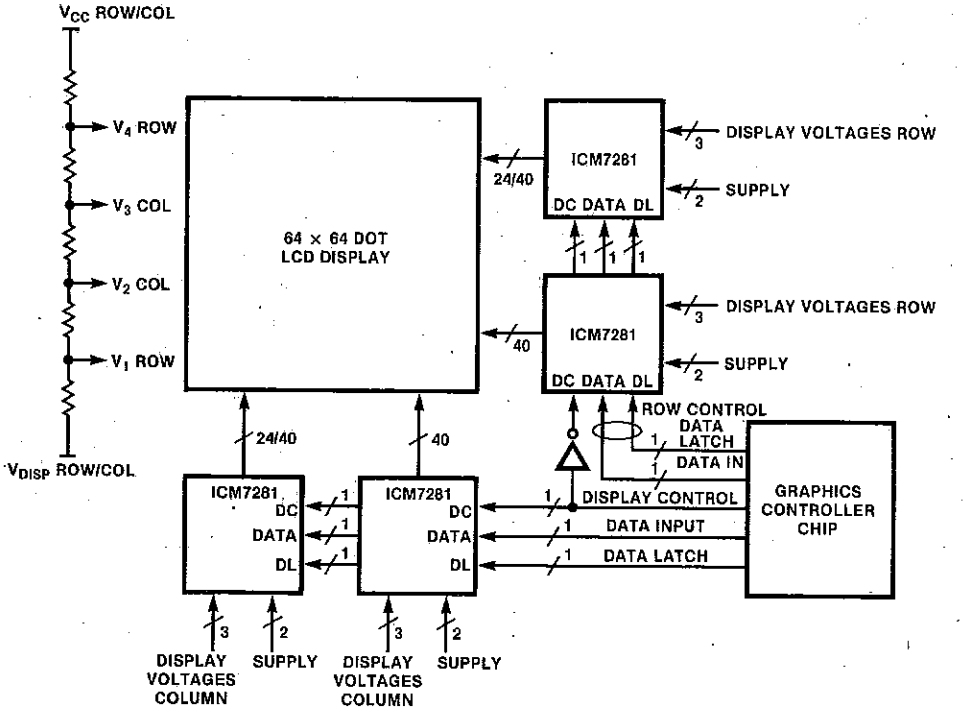
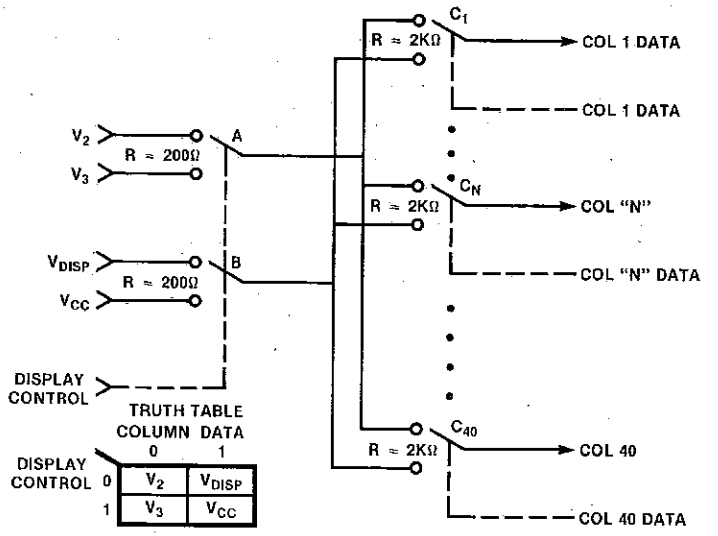


Figure 2. ICM7281 Column Driver Used in a Graphics Application



COLUMN OUTPUT MULTIPLEXER AND TRUTH TABLE

Figure 3. Column Output Multiplexer and Truth Table

LCD MULTIPLEXING

Multiplexing Schemes

The goal in LCD multiplexing is to increase the number of segments a given number of column lines can drive, while not unacceptably degrading the viewability of the LCD display. Increasing the number of rows driven by a column decreases the ratio between the voltage across an ON segment and the voltage across an OFF segment. This ON/OFF voltage ratio is critical since the contrast of an LCD segment is determined by the RMS voltage across that segment. Figure 4 shows a typical curve of RMS voltage vs. contrast. For an acceptable display, the RMS OFF voltage must be below the 10% contrast point and the RMS ON voltage must be above the 50% contrast point. The RMS on voltages for different multiplex ratios are also shown in figure 4. Note that as the number of rows or backplanes goes up, the RMS on voltage decreases.

The ICM7281 can drive either columns or rows using the modified Alt and Pleshko waveforms as shown in figure 5. The ON/OFF voltage ratio formula and the calculated values for common multiplex ratios are shown in table 1. Table II shows the optimum voltages for V1 to V5 for different multiplex ratios.

Temperature Effects and Temperature Compensation of V_{DISP}

The performance of LCD fluids is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures some displays may take several seconds to change to a new character after the new information appears at the LCD driver outputs. However, for most applications above 0°C this will not be a problem, and for low temperature applications, high-speed liquid crystal materials are available. High temperature operation is generally limited by long term degradation of the polarizer and the sealing materials above 70°C or 85°C.

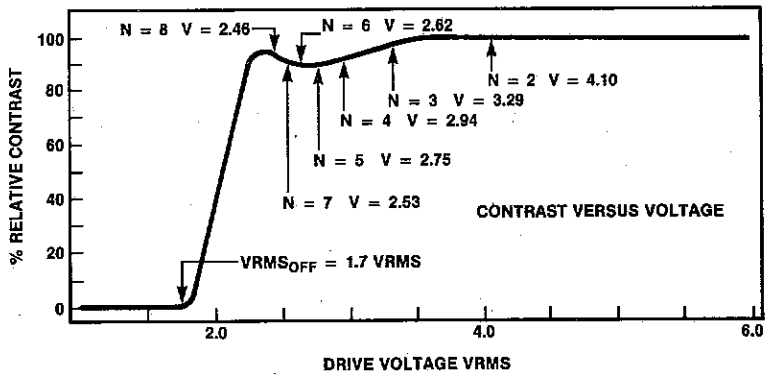
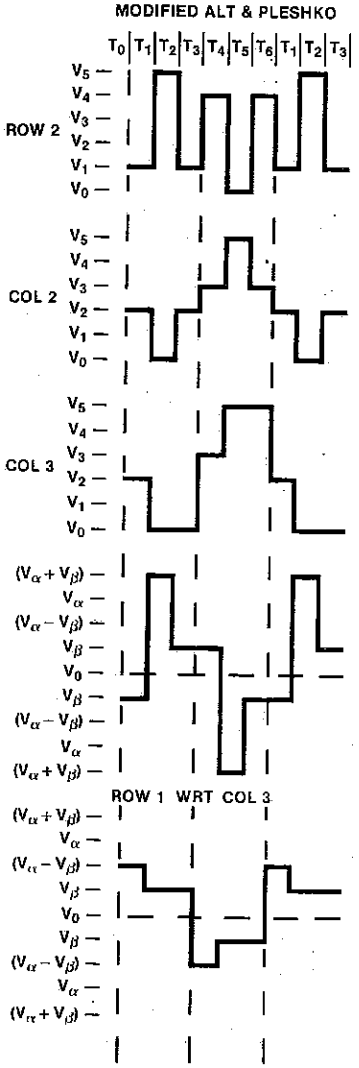
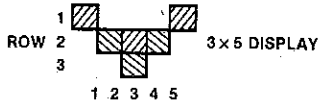


Figure 4.

Table 1. OPTIMUM MULTIPLEX DRIVE

Rows	$V_{ON/OFF}$	Alt and Pleshko V_{CC}-V Display/V_T	ICM7280/ICM7281 V_{CC}-V Display/V_T
4	1.73	4	3
7	1.488	4.74	3.27
8	1.447	4.97	3.37
9	1.414	5.20	3.46
10	1.387	5.41	3.56
12	1.346	5.81	3.74
14	1.315	6.18	3.917
16	1.290	6.532	4.08
32	1.196	8.817	5.19
64	1.134	12.01	6.804





WITH

$V_0 = 0$
$V_1 = V_\beta$
$V_2 = 2V_\beta$
$V_3 = V_\alpha - V_\beta$
$V_4 = V_\alpha$
$V_5 = V_{DISPLAY} = V_\alpha + V_\beta$

$$V_\alpha = \frac{\sqrt{(K+1)^3}}{2(K-1)} V_{TH} \quad , \quad V_\beta = \frac{\sqrt{K+1}}{2} V_{TH}$$

WHERE: $K = \dfrac{\sqrt{N}+1}{\sqrt{N}-1}$

V_{TH} = THRESHOLD VOLTAGE OF LCD

$$V_{ON\ RMS} = \sqrt{\frac{(V_\alpha + V_\beta)^2 + (N-1)V_\beta^2}{N}}$$

$$V_{OFF\ RMS} = \sqrt{\frac{(V_\alpha - V_\beta)^2 + (N-1)V_\beta^2}{N}}$$

$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{(M+1)^2 + (N-1)}{(M-1)^2 + (N-1)}}$$

$$M = \frac{V_\alpha}{V_\beta}$$

FOR OPTIMUM CONTRAST $M = \sqrt{N}$ $N \geq 4$

Figure 5.

Table II. Optimum Drive Voltages

N	V1	V2	V3	V4	V5	ON/OFF VOLTAGE RATIO
4	1.000	2.000	1.000	2.000	3.000	1.732
5	0.951	1.902	1.176	2.127	3.078	1.618
6	0.919	1.838	1.332	2.252	3.171	1.543
7	0.897	1.793	1.476	2.372	3.269	1.488
8	0.879	1.759	1.608	2.488	3.367	1.447
9	0.866	1.732	1.732	2.598	3.464	1.414
10	0.855	1.710	1.849	2.704	3.559	1.387
11	0.846	1.692	1.960	2.806	3.652	1.365
12	0.838	1.677	2.066	2.904	3.743	1.346
16	0.816	1.633	2.449	3.266	4.082	1.291
20	0.802	1.605	2.786	3.589	4.391	1.255
24	0.793	1.585	3.090	3.883	4.676	1.23
30	0.782	1.564	3.502	4.284	5.066	1.203
32	0.779	1.559	3.629	4.409	5.188	1.196
40	0.771	1.541	4.103	4.874	5.645	1.173
48	0.764	1.529	4.332	5.296	6.061	1.156
54	0.761	1.522	4.830	5.590	6.351	1.147
64	0.756	1.512	5.292	6.047	6.803	1.134

The temperature effect most important in the 0-70°C range is the variation of threshold voltage with temperature. For typical liquid crystal materials, the threshold voltage, V_{THRESH}, has temperature coefficient of -7 to -14mV/°C. Since the V_{DISP} is 3.27 times V_{THRESH} (for 7 row multiplex, see Table 1), the V_{DISP} has a tempco of about -25 to -50 mV/°C, depending on LCD fluid tempco. As can be seen in Figure 4, for optimum viewability and contrast ratio, the driving voltage must be accurately matched to the LCD threshold voltage. If a significant variation is temperature is expected, a method of adjusting the V_{DISP} must be provided. Figure 6 uses the ICL7663 voltage regulator to independently set V_{DISP} and the tempco of V_{DISP}. The Vbe multiplier circuit of Figure 7 can be used with some displays. Since the Vbe multiplier's voltage and tempco cannot be independently adjusted, the Vbe multiplier is suitable only for use over a limited temperature range or with a display whose V_{DISP} tempco matches the Vbe multiplier tempco.

With the fluids now available for 32 and 64 multiplex operation it is quite common to have a "Contrast" adjustment accessible to the user. This "Contrast" adjustment varies the V_{DISP} to compensate for both temperature variations and for variations in the viewing angle.

Multiplex Rate and Maximum Drive Capability

The minimum multiplex rate is determined by the response time of the LCD. To avoid flicker, the mux rate should be above 30Hz. The maximum multiplex rate is determined by power dissipation limits and the drive capability of the ICM7281.

The drive capability of the ICM7281 indirectly sets the upper limit of the mux rate. The absolute maximum limit of DC voltage across an LCD is usually specified as 50mV. As the multiplex rate increases, any asymmetry in the rise and fall times will cause a DC offset, in addition to any offset caused by V2 and V3 not being exactly symmetrical with respect to V_{DISP} and V_{CC}. The ICM7281 was designed to have equal rise and fall times, as well as low resistance drivers which make the rise and fall times short. This allows the ICM7281 to drive over 2000pF at mux rate of 100Hz. Normally an LCD dot matrix display will have less than 1000pF capacitance per 40 columns (each ICM7281 drive 40 columns).

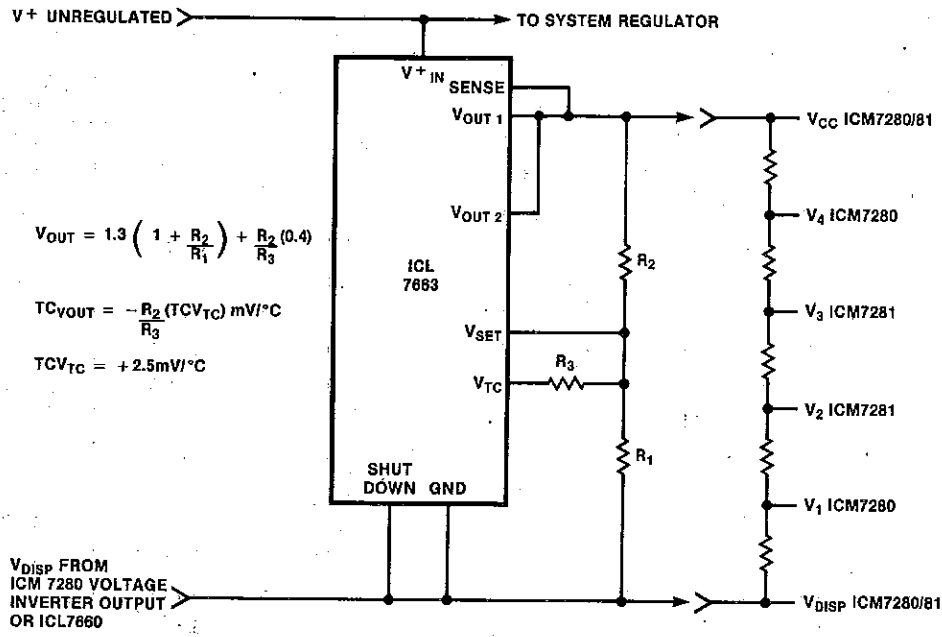


Figure 6. V_{DISP} Generator

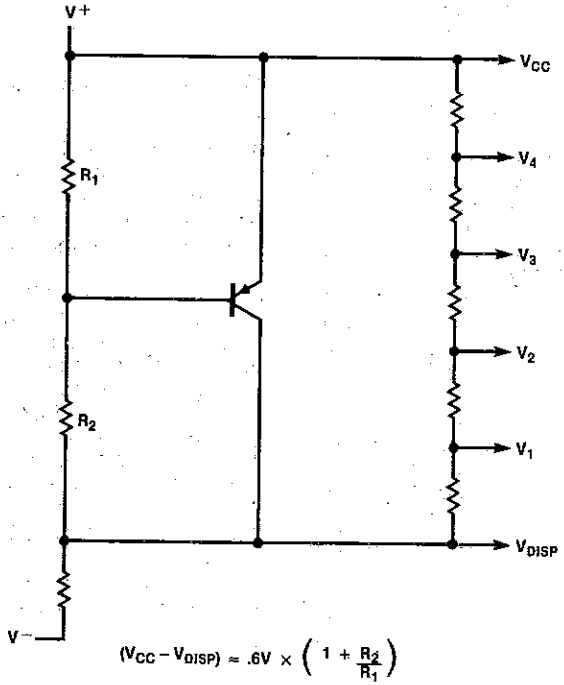


Figure 7. V_{BE} Multiplier

POWER DISSIPATION

The power dissipation of a display system driven by the ICM7281 has several components:

1) Quiescent or DC power dissipation of the ICM7281

2) Dynamic or AC power dissipation of the ICM7281

3) Power consumed in driving the LCD display.

ICM7281 Power Dissipation

The quiescent current of the ICM7281 is very low, typically less than 1μA, and can generally be ignored. The dynamic current is proportional to the clock frequency, with a typical value of 1.0 mA per MHz. This means that at a 500 KHz clock the dynamic current will be 0.5 mA.

LCD Display Drive Dissipation

Since the LCD has very low leakage currents, most of the power used to drive the LCD is used to charge and discharge the LCD capacitance. The power is

$$P_{LCD} = C V^2 F_{EFF}$$

Where:

P_{LCD} is the power dissipated in driving the display

C is the display capacitance

V is Voltage across the display

F is the effective multiplex frequency

The effective multiplex frequency ranges from F_{MUX} to N x F_{MUX}, where F_{MUX} is the multiplex rate and N is the number of rows. The actual effective multiplex frequency is dependent on which characters or bit pattern is being displayed and is typically about N/3 x F_{MUX}

Low Power Shutdown

If the data clock is stopped and the voltages across the LCD are not changing, the power consumption will drop to the 5 to 50 microwatt range. Set V_{DISP}, V2 and V3 equal to V_{CC} to prevent permanent damage to the LCD display by a DC bias. An easy way to shutdown the display voltages is to use the SHUTDOWN pin of an ICL7663, as shown in Figure 6.

APPLICATIONS

Alphanumeric Display Using ICM7280 Intelligent Row Driver

The ICM7280 Intelligent Row Driver is specifically designed to drive multiple ICM7281 LCD Column Drivers. Figure 1 shows a typical 80 character display. The ICM7280 and ICM7281's will drive either 7, 8, 9 or 10 row displays, with the characters having either 5 or 6 columns. The Row Driver receives ASCII data, converts that data to bit-by-bit column data for the ICM7281's and serially shifts data into the ICM7281's. This process is repeated for each phase of the multiplex cycle. The ICL7663 provides a temperature compensated V_{DISP} to the ICM7280 voltage divider, which generates the other voltage needed to drive the LCD display. For further details refer to the ICM7280 Intelligent LCD Row Driver data sheet.

LCD Graphics Display

In this circuit, ICM7281's are used to drive both the rows and columns of the LCD dot matrix. An external controller is used to generate the row and column data that is serially transferred into the ICM7281's.

The display drive voltages are generated in a resistor divider network, with the ICL7663 providing the temperature compensated V_{DISP}. The optimum voltages for V1 through V5 can be calculated using the equations of figure 5. Optimum voltages for common multiplex ratios are shown in Table II.

The LCD shown in Figure 2 is a 32 row display, divided into two sections of 16 rows to increase the ON/OFF RMS voltage ratio, thereby improving the contrast of the display. As LCD fluids improve it will become practical to use 32 or 64 row multiplexing, reducing the number of column drivers by a factor of 2 or 4.

As the number of rows increases, the V_{DISP} required by the ICM7281's modified Alt and Pleshko multiplex scheme increases less than the V_{DISP} required by a classic Alt and Pleshko multiplex scheme. For example: a 64 row display with a 1.45V threshold would require + 5V and − 12.4V supplies using standard Alt and Pleshko multiplexing. The ICM7281 would require only + 5V and − 4.9V to drive this same display with 64 row multiplexing. This means that the negative voltage could easily be generated using a charge pump such as the ICL7660 or the onboard charge pump of the ICM7280.

Serial Input I/O Expander

In addition to driving LCD's, the ICM7281 can be used as an I/O expander as shown in Figure 8. In this case, the data can be serially entered into the ICM7281 shift register using the 80C51 serial port. The 80C51 then transfers the data to the output latch by pulsing the DATA LATCH input with an I/O port line. Note that multiple ICM7281's can be cascaded to get more than 30 output lines. This cascading does not require any additional logic since the ICM7281 CARRY OUTPUTs are used.

DISPLAY CONTROL is tied to V+ so that the data on the column outputs is the same as the data that was entered. If DISPLAY CONTROL is grounded, the column outputs will be inverted data. With V_3 grounded, the logic level at the column outputs will be CMOS compatible, swinging from ground to V+. The output resistance of the column outputs is about 2K ohms.

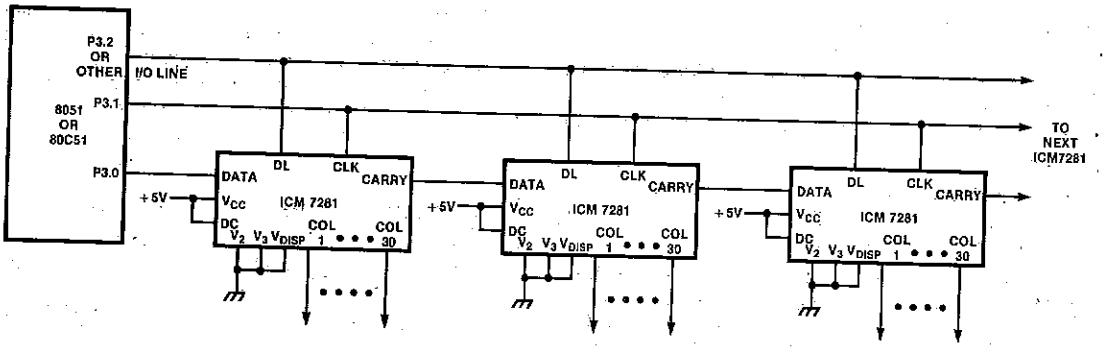
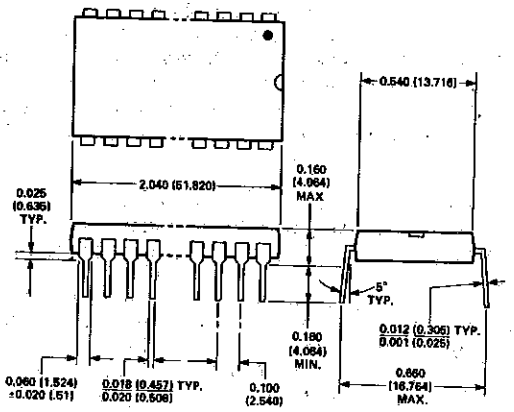


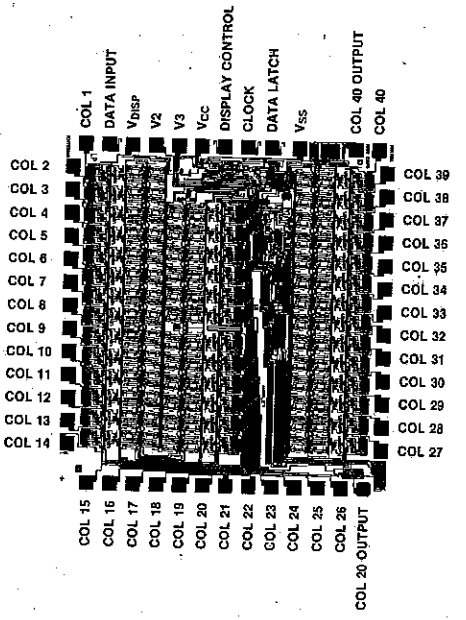
Figure 8. Serial I/O Expander 7281

PACKAGE OUTLINES

All dimensions given in inches and (millimeters).



40 LEAD PLASTIC (PL)



CHIP TOPOGRAPHY

ICM7555/7556
CMOS
General Purpose Timers

FEATURES

- **Exact equivalent in most cases for SE/NE555/556 or the 355.**
- **Low Supply Current — 80μA Typ. (ICM7555) 160μA Typ. (ICM7556)**
- **Extremely low trigger, threshold and reset currents - 20pA Typical**
- **High speed operation - 500 kHz guaranteed**
- **Wide operation supply voltage range guaranteed 2 to 18 volts**
- **Normal Reset function - No crowbarring of supply during output transition.**
- **Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005% per °C at 25°C**
- **Outputs have very low offsets, HI and LO**

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

6

APPLICATIONS

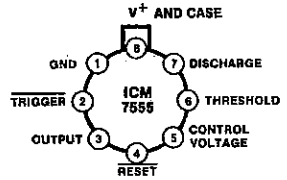
- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

ORDERING INFORMATION

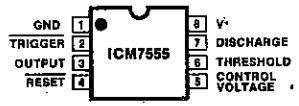
ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555IPA	−20 to +85°C	8 Lead MiniDip
ICM7555ITV	−20 to +85°C	TO-99 Can
ICM7555MTV	−55 to +125°C*	TO-99 Can
ICM7556IPD	−20 to +85°C	14 Lead Plastic DIP
ICM7556MJD	−55 to +125°C*	14 Lead CERDIP
ICM7555/D		DICE
ICM7556/D		DICE

*Add /883B to order number if 883B processing is desired.

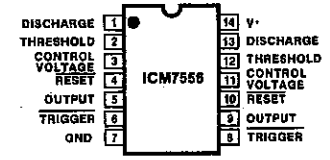
PIN CONFIGURATIONS (Top View)



(OUTLINE DRAWING TV)



(OUTLINE DRAWING PA)



(OUTLINE DRAWING JD, PD)

INTERSIL

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage ..... +18 Volts
Input Voltage
Control Voltage $\overline{\text{Trigger}}$, Threshold, $\overline{\text{Reset}}$ ..... $\leq V^+ + 0.3V$ to $\geq V^- - 0.3V$
Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Operating Temperature Range[2]
ICM7555IPA .....–20°C to +85°C
ICM7555ITV .....–20°C to +85°C
ICM7556IPD .....–20°C to +85°C
ICM7555MTV ..... –55°C to +125°C
ICM7556MJD ..... -55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 60 Seconds) ..... +300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS (T_A = 25°C, V^+ = +2 to +15 Volts unless other specified)

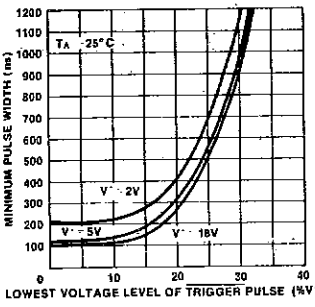
PARAMETER	SYMBOL	TEST CONDITIONS			VALUE MIN	VALUE TYP	VALUE MAX	UNITS
Supply Voltage	V^+	–20°C ≤ T_A ≤ +70°C –55°C ≤ T_A ≤ +125°C			2 3		18 16	V V
Supply Current[3]	I^+	ICM7555	V^+ = 2V V^+ = 18V			60 120	200 300	µA µA
		ICM7556	V^+ = 2V V^+ = 18V			120 240	400 600	µA µA
Timing Error		R_A, R_B = 1k to 100k, C = 0.1µF	5V ≤ V^+ ≤ 15V					
Initial Accuracy		Note 4				2.0	5.0	%
Drift with Temperature		Note 4	V^+ = 5V V^+ = 10V V^+ = 15V			50 75 100		ppm/°C
Drift with Supply Voltage		V^+ = 5V				1.0	3.0	%/V
Threshold Voltage	V_{TH}		V^+ = 5V		0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}		V^+ = 5V		0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	V^+ = 18V V^+ = 5V V^+ = 2V				50 10 1		pA pA pA
Threshold Current	I_{TH}	V^+ = 18V V^+ = 5V V^+ = 2V				50 10 1		pA pA pA
Reset Current	I_{RST}	V_{RESET} = Ground	V^+ = 18V V^+ = 5V V^+ = 2V			100 20 2		pA pA pA
Reset Voltage	V_{RST}	V^+ = 18V V^+ = 2V			0.4 0.4	0.7 0.7	1.0 1.0	V V
Control Voltage Lead	V_{CV}		V^+ = 5V		0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo	V^+ = 18V V^+ = 5V	I_{SINK} = 3.2mA I_{SINK} = 3.2mA		0.1 0.15	0.4 0.4	V V
		Output Hi	V^+ = 18V V^+ = 5V	I_{SOURCE} = 1.0mA I_{SOURCE} = 1.0mA	17.25 4.0	17.8 4.5		V V
Rise Time of Output	t_r	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Fall Time of Output	t_f	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Guaranteed Max Osc Freq	f_{max}	Astable Operation			500			kHz

NOTES:

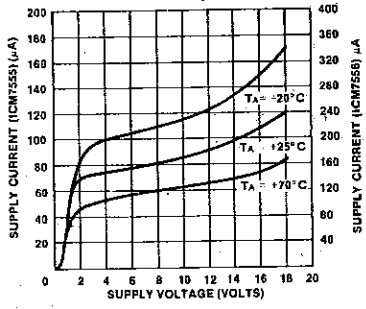
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- –0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
2. Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).
3. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD and $\overline{\text{RESET}}$ voltages.
4. Parameter is not 100% tested. Majority of all units meet this specification.

TYPICAL CHARACTERISTICS

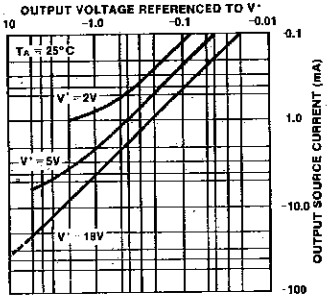
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



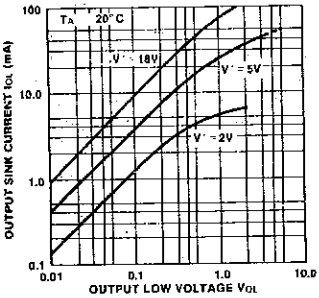
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



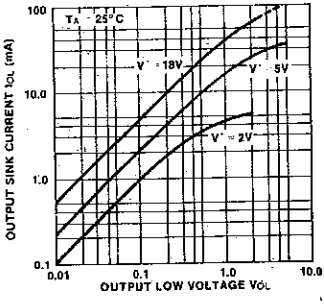
OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



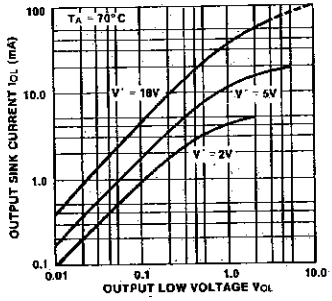
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



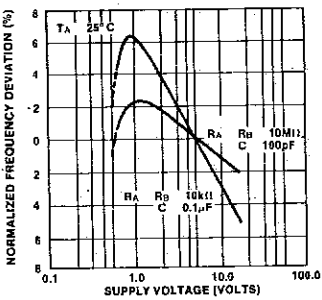
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



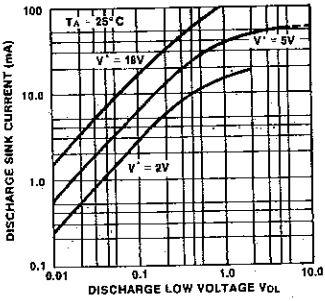
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



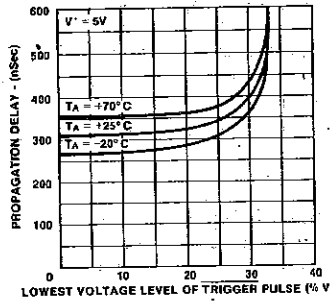
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



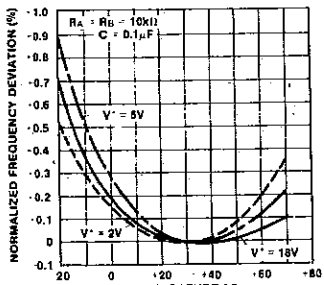
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



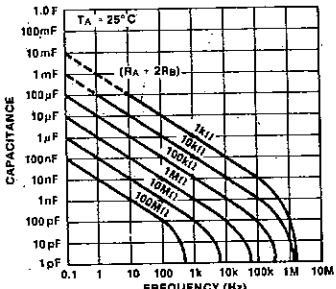
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



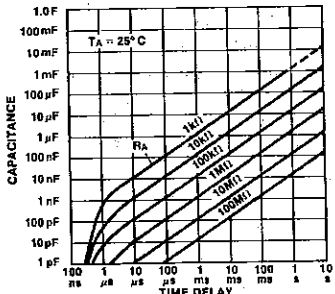
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



FREE RUNNING FREQUENCY AS A FUNCTION OF RA, RB and C



TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C



6

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 2.

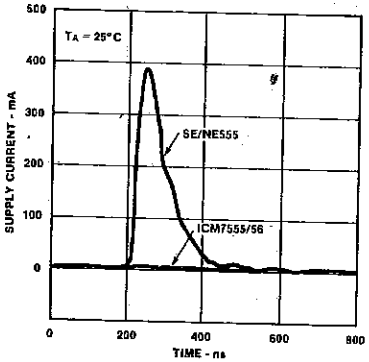


Figure 2. Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2-3 mA instead of 300-400 mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 3 and 4.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 3. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4\ RC}$$

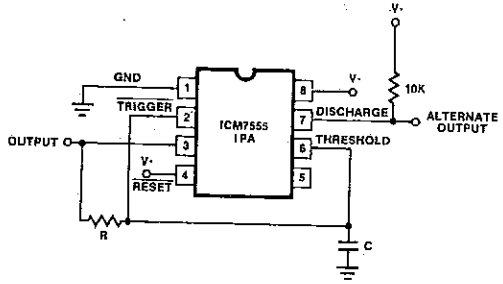


Figure 3: Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

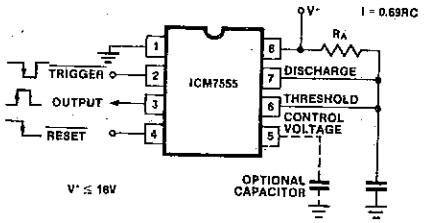


Figure 4: Monostable Operation

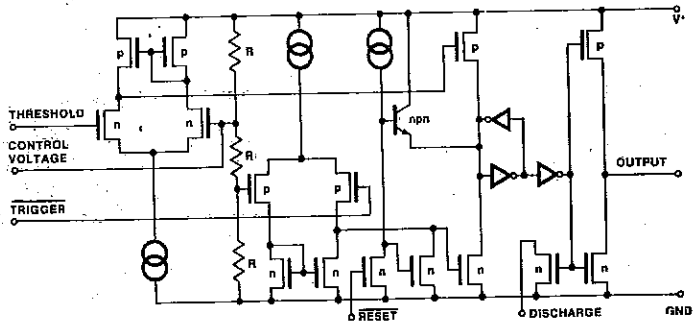
CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

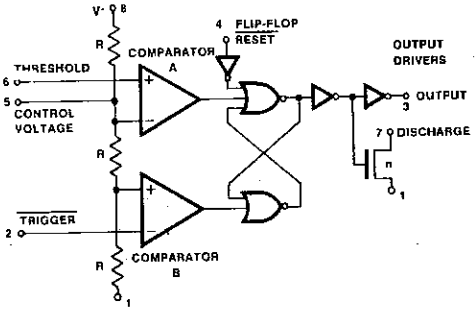
$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

EQUIVALENT CIRCUIT



BLOCK DIAGRAM



This block diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.
R = 100kΩ, ± 20% typ.

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V^+)	>1/3(V^+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V^+)	HIGH	HIGH	OFF

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

CHIP TOPOGRAPHIES

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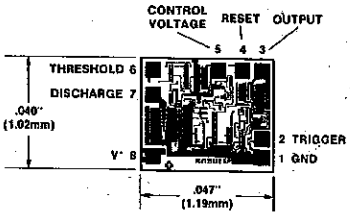

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