SECTION 8—PACKAGE INFORMATION

Package Thermal Characteristics

Package Designator	Package Type	Lead Material	$R\Theta_{JA}$† (°C/W)	$R\Theta_{JC}$† (°C/W)
A	14-Pin Plastic DIP	Copper	60	38
A	16-Pin Plastic DIP	Copper	60	38
A	18-Pin Plastic DIP	Copper	55	25
A	20-Pin Plastic DIP	Copper	55	25
A	22-Pin Plastic DIP	Copper	50	21
A	28-Pin Plastic DIP	Copper	40	16
A	40-Pin Plastic DIP	Copper	36	—
B	8-Pin Semi-Tab Plastic DIP	Copper	75	13*
B	14-Pin Semi-Tab Plastic DIP	Copper	45	13*
B	16-Pin Semi-Tab Plastic DIP	Copper	45	13*
B	22-Pin Semi-Tab Plastic DIP	Copper	40	13*
EK	20-Contact Sq. Hermetic LCC	N.A.	110	14-19
EK	28-Contact Sq. Hermetic LCC	N.A.	100	10-19
EK	44-Contact Sq. Hermetic LCC	N.A.	—	7.5-19
EL	18-Contact Rect. Hermetic LCC	N.A.	—	—
EP	20-Lead Square Plastic LCC	Copper	75	28
EP	28-Lead Square Plastic LCC	Copper	65	16
EP	44-Lead Square Plastic LCC	Copper	50	15
H	8-Pin Hermetic DIP	Kovar	120	40
H	14-Pin Hermetic DIP	Kovar	90	20
H	16-Pin Hermetic DIP	Kovar	90	20
H	18-Pin Hermetic DIP	Kovar	75	20
H	22-Pin Hermetic DIP	Kovar	65	20
L	8-Lead SOIC	Copper	165	45
L	14-Lead SOIC	Copper	118	29
L	16-Lead SOIC	Copper	110	27
LB	20-Lead Semi-Tab SOIC	Copper	46	7.9*
LW	16-Lead SOIC	Copper	97	—
LW	18-Lead SOIC	Copper	97	—
LW	20-Lead SOIC	Copper	87	17
M	8-Pin Mini DIP	Copper	80	55
R	14-Pin CerDIP	Kovar	75	—
R	16-Pin CerDIP	Kovar	75	—
R	18-Pin CerDIP	Kovar	65	—
W	12-Lead Power Tab SIP	Copper	24	3.0*
Z	5-Lead Power Tab SIP	Copper	40	4.5*

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specification takes precedence.

†$G\Theta_{JA} = 1/R\Theta_{JA}$ and $G\Theta_{JC} = 1/R\Theta_{JC}$

*$R\Theta_{JA}$

Interface and Linear ICs

For Surface-Mount Applications

The Sprague Semiconductor Group offers many of its peripheral power interface and linear integrated circuits in small-outline packages and leaded or leadless chip carriers for use in high-density surface-mount applications. Popular products presently available include industry-standard Series ULN-2000, ULN-2060/70, ULN-2800, UDN-2980, and Series UCN-5800 peripheral power drivers for printers, displays, motors, solenoids, relays, and other power interface; Series UDS-5790 PIN-diode drivers; and custom telecommunications circuits. Additional devices will become available as needs are developed.

SURFACE-MOUNT PACKAGE AVAILABILITY

Leads	Package Style	Industry Pkg. Outline	Tape & Reel Width × Pitch (mm)	Sprague P/N Suffix
8	SO-8	MS-012AA	12 × 8	L
14	SO-14	MS-012AB	16 × 8	L
16	SO-16	MS-012AC	16 × 8	L
	SOL-16	MS-013AA	16 × 12	LW
18	SOL-18	MS-013AB	—	LW
	LCC-18	M38510/C-9	24 × 12	EL
20	SOL-20	MS-013AC	24 × 12	LW
	SOL-20B	MS-013AC	24 × 12	LB
	LCC-20	M38510/C-3	16 × 12	EK
	PLCC-20	MO-047AA	16 × 12	EP
28	LCC-28	M38510/C-4	24 × 16	EK
	PLCC-28	MS-007AA	24 × 16	EP
44	LCC-44	M38510/C-5	32 × 44	EK
	PLCC-44	MS-007AB	32 × 44	EP

LCC = Hermetic Leadless Chip Carrier.
PLCC = Plastic Leaded Chip Carrier.
SO = Small Outline IC, 0.15" Gull-Wing.
SOL = Small Outline IC, 0.30" Gull-Wing.

The SOL-20B package is a miniature "bat wing" package (12 active connections plus eight tab/ground connections) for use in surface-mount, high package-power dissipation requirements. Similar designs are being addressed for use with plastic leaded-chip carriers to provide multi-pin packages with minimized board space requirements and with junction-to-tab thermal resistances of less than 5°C/W. The unique Sprague PLCC power package construction will be compatible with other PLCC products and will allow the easy attachment of external heat sinks for highest package power dissipation. Except for the SOL-18 package, all devices can be supplied in tape and reel to EIA 481A.

SURFACE-MOUNT PACKAGING FOR ICs

Part Number	Package	Description
ULN-2001 through 2005L	SO-16	7 Darlingtons, 50 V/350 mA
ULN-2021L through 2025L	SO-16	7 Darlingtons, 95 V/350 mA
ULS-2001EK through 2005EK	LCC-20	7 Darlingtons, 50 V/350 mA
ULN-2046L	SO-14	5 NPN Transistors
ULN-2061L	SO-8	2 Darlingtons, 50 V/1.25 A
ULN-2064/68/74LB	SOL-20B	4 Darlingtons, 50 V/1.25 A
ULN-2081L	SO-16	7 NPN Transistors, Common Emitter
ULN-2082L	SO-16	7 NPN Transistors, Common Emitter
ULN-2083L	SO-16	5 Independent NPN Transistors
ULN-2086L	SO-14	5 NPN Transistors
ULN-2204LW	SOL-16	AM/FM Radio System
UDN-2580EP	PLCC-20	8 Darlingtons, 50 V*/ – 350 mA
UDN-2580LW	SOL-18	8 Darlingtons, 50 V*/ – 350 mA
UDN-2585EP	PLCC-20	8 Drivers, 25 V/ – 120 mA
UDN-2585LW	SOL-18	8 Drivers, 25 V/ – 120 mA
UDN-2595EP	PLCC-20	8 Drivers, 20 V/100 mA
UDN-2595LW	SOL-18	8 Drivers, 20 V/100 mA
ULN-2801LW through 2804LW	SOL-18	8 Darlingtons, 50 V/350 mA
ULN-2821LW through 2825LW	SOL-18	8 Darlingtons, 95 V/350 mA
ULS-2803EK and 2804EK	LCC-20	8 Darlingtons, 50 V/350 mA
UDN-2933LB	SOL-20B	3-Channel Half-Bridge, 30 V/ ± 800 mA
UDS-2982EK	LCC-20	8 Darlingtons, 50 V/ – 350 mA
UDN-2982EP	PLCC-20	8 Darlingtons, 50 V/ – 350 mA
UDN-2982LW	SOL-18	8 Darlingtons, 50 V/ – 350 mA
UDS-2984EK	LCC-20	8 Darlingtons, 80 V/ – 350 mA
UDN-2984EP	PLCC-20	8 Darlingtons, 80 V/ – 350 mA
UDN-2984LW	SOL-18	8 Darlingtons, 80 V/ – 350 mA
UDN-2993LB	SOL-20B	Dual 40 V/500 mA H-Bridge
ULN-3781L	SO-8	Low-Voltage Audio Power Amplifier
ULN-3782L	SO-8	Dual Audio Power Amplifier
ULN-3820LW	SOL-20	C-QUAM® AM Stereo Decoder
ULN-3839LW	SOL-16	AM Radio System
ULN-3841LW	SOL-20	AM Signal Processor
ULN-3842LW	SOL-20	AM/FM Signal Processor
ULN-3859EP	PLCC-20	Low-Power, Narrow-Band FM IF

*Increased voltage ratings available.
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SURFACE-MOUNT PACKAGING FOR ICs

Part Number	Package	Description
ULN-3862LW	SOL-16	FM IF System
ULN-3883LW	SOL-18	FM Communications IF/Audio System
UCN-4807EP and 4808EP	PLCC-20	Addressable, 8-Channel Latched Drivers
UDN-5707EP	PLCC-20	Quad NAND Driver, 80 V/300 mA
UDN-5725L	SO-14	Dual Power Driver, 70 V/1 A
UCS-5791EK	LCC-18	Quad PIN Diode Driver, 120 V/300 mA
UCN-5800L	SO-14	4-Bit Latch, 50 V/350 mA
UCN-5801EP	PLCC-28	8-Bit Latch, 50 V/350 mA
UCN-5810EP	PLCC-20	10-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5810LW	SOL-18	10-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5812EP	PLCC-28	20-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5815EP	PLCC-28	8-Bit Latch, 60 V/ – 25 mA
UCN-5816EP	PLCC-28	4-Bit Decoder/Latch, 60 V/350 mA
UCN-5818EP	PLCC-44	32-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5821EP through 5823EP	PLCC-20	8-Bit SR/Latch, to 100 V/350 mA
UCN-5832EP	PLCC-44	32-Bit SR/Latch, 40 V/100 mA
UCN-5833EP	PLCC-44	32-Bit SR/Latch, 30 V/100 mA
UCN-5841EP through 5843EP	PLCC-20	8-Bit SR/Latch, to 100 V/350 mA
UCN-5851EP and 5852EP	PLCC-44	32-Bit Serial-In, 225 V/100 mA
UCN-5853EP and 5854EP	PLCC-44	32-Bit SR/Latch, 60 V*/ ± 20 mA
UCN-5881EP	PLCC-44	Dual 8-Bit Latch, 20 V/25 mA
UCN-5895EP	PLCC-20	8-Bit SR/Latch, 50 V/ – 120 mA
UCN-5895LW	SOL-18	8-Bit SR/Latch, 50 V/ – 120 mA
UDN-6118LW	SOL-18	8 Drivers, 80 V*/ – 25 mA
ULN-8130LW	SOL-18	Supervisory Systems Monitor
ULN-8131LW	SOL-20	Supervisory Systems Monitor
ULN-8163LW	SOL-16	SMPS Controller
NE5560D	SOL-16	SMPS Controller
NE5568D	SO-8	SMPS Controller
SG3525A	SOL-16	SMPS Controller
SG3526	SOL-18	SMPS Controller
SG3527A	SOL-16	SMPS Controller
TL594CDW	SOL-16	SMPS Controller
TL595CDW	SOL-18	SMPS Controller

*Increased voltage ratings available.

OPERATING AND HANDLING PRACTICES FOR MOS INTEGRATED CIRCUITS

Handling Practices — Packaged Devices

Sprague Electric incorporates input protection diodes in all of its MOS/CMOS devices. Because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.
2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.
3. Devices should not be inserted into or removed from test stations unless the power is off.
4. Neither should signals be applied to the inputs while the device power supply is in an off condition.
5. Unused input leads should be committed to either V_{SS} or V_{DD}.

Handling Practices — Die

A conductive carrier should be used in order to avoid differences in voltage potential.

Automatic Handling Equipment

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aid here and are available commercially. This method is very effective in eliminating static electricity problems.

Ambient Conditions

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

Alert Failure Modes

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.
2. Shorted or 'blown' open gates.
3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

MOUNTING POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. "Brute Force" mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

THERMAL DESIGN FOR PLASTIC INTEGRATED CIRCUITS

PROPER THERMAL DESIGN is essential for reliable operation of many electronic circuits. Under severe thermal stress, leakage currents increase, materials decompose, and components drift in value or fail. Present-day linear integrated circuits are capable of delivering 5 to 10 watts of continuous power. Previously, such power levels came only with discrete metal can power transistors. It was relatively easy to determine the thermal resistance of these devices and attach a massive heat sink. However, in many markets, economic factors now dictate the use of molded dual in-line plastic packaged monolithic circuits. The guidelines to be discussed will provide the circuit design engineer with information on maintaining junction temperature below a safe limit under worst case conditions.

Design Considerations

Four factors must be considered before the required heat-sinking can be determined. These are:

1. Maximum ambient temperature
2. Maximum allowable chip temperature
3. Junction-to-ambient thermal resistance
4. Continuous chip power dissipation

Maximum ambient temperature for the integrated circuit is normally between +70°C and +85°C and is usually dependent on the case material. In most applications, however, the limiting factor is the associated discrete components and a limit of about +50°C is specified. The maximum allowable chip temperature is usually +150°C for silicon.

Thermal resistance is the all-important design factor. It is composed of several individual elements, some of which are determined by the integrated circuits manufacturer, and some by the user.

Chip Power Dissipation

The chip power dissipation should be obtainable from the manufacturer's specifications. In most applications it is a variable and determined by the user when he specifies the circuit variables.

A typical example is a dual 2-watt audio power amplifier. Power dissipation is determined by the load impedance, the required peak output power, the acceptable amount of total harmonic distortion (THD), and the supply voltage (V_{cc}). This is illustrated in Figures 1-3. Note that for a given supply voltage, the chip dissipation may be greatest at some point below the peak output power rating and must be considered.

As shown in the figures, a peak output power of 2 watts per channel with 3% maximum THD would mean a chip power dissipation of about 2.7 W and a V_{cc} of 15 V with a load impedance of 4Ω, or 1.8 W and 15 V at 8Ω, or 1.4 W and 19 V at 16Ω. In general, the highest load impedance for a given output power is the most desirable (within the output voltage capability of the device).

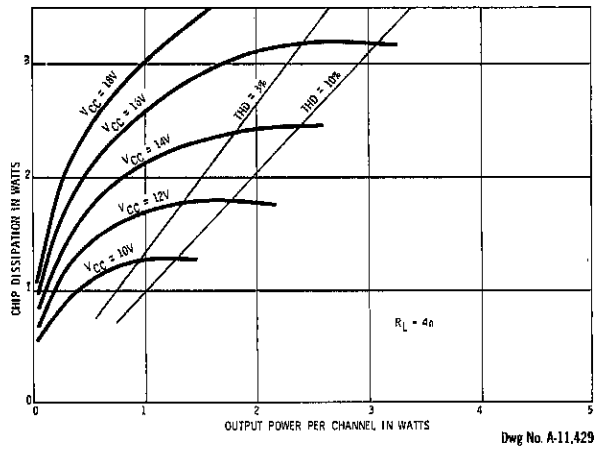

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Figure 1

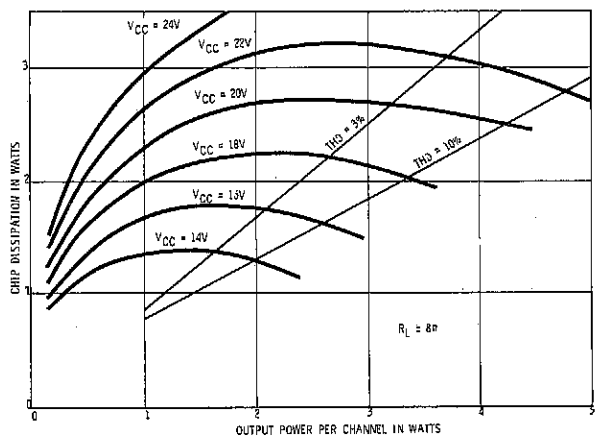

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Figure 2

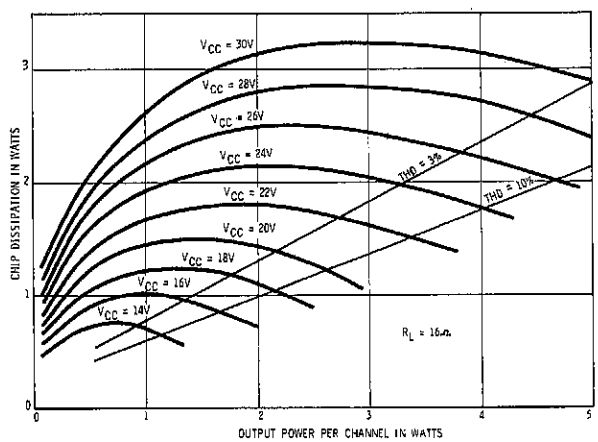

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Figure 3

Heat Dissipation

In any circuit involving power, a major design objective is to reduce the temperature of the components in order to improve reliability, reduce cost, or improve operation. The logical place to start is with the heat-producing component itself. First, keep the amount of heat generated to a minimum. Second, get rid of the heat that must be generated.

Heat generation can be minimized through proper circuit design. Heat dissipation is a function of thermal resistance.

With the typical discrete component, heat dissipation can be accomplished by fastening it directly to the chassis. Dual in-line plastic packaged integrated circuits, however, are quite a bit different. Their shape is not conducive to fastening directly to the chassis, they are normally installed in a plastic socket or on a printed wiring board, and the heat producing chip is not readily accessible.

Some users specify unusual packages so as to get the heat sink as close as possible to the chip and/or provide an attachment point for an external heat sink. A common factor in many of these special designs is that the lead frame is an integral part of the heat sink.

Since the plastic package may have a thermal resistance of between 50 and 100°C/W and the lead frame a thermal resistance of only 10 to 20°C/W, this would seem like the best route to go.

Standard Packages

The most common lead frame material has been Kovar (an iron-nickel-cobalt alloy). Its coefficient of expansion is close to that of silicon thereby minimizing mechanical stresses. However, Kovar has a relatively high thermal resistance and consequently is not suitable for standard lead frames in high power dissipation circuits. For these applications, copper or copper-alloy lead frames should be used. Additionally, some type of added heat sinking may be necessary. Thus lead frame configurations are being altered from the standard 14-pin or 16-pin designs.

Rapidly becoming an industry standard is the "bat-wing" package. This package is the same size as a 14-pin dual in-line package, but the center portion of the frame is left as tabs, measuring about ¼" square. These tabs can be soldered, welded, or bolted to a heat sink, or inserted directly into some sockets. The worst case thermal resistance of various lead frames (Θ_{JC}) is given below.

Lead Frame	Thermal Resistance
14-pin Kovar	47°C/W
14-pin copper	19°C/W
"Bat-wing"	11°C/W

Which Heat Sink?

If the integrated circuit manufacturer has done his job well, the chip-to-ambient thermal resistance will be minimized for maximum chip power dissipation. It would appear that even the Kovar lead frame would be adequate for most applications. However, the total thermal resistance (Θ_{JA}) is also dependent on a stagnant layer of air at the lead frame-ambient interface which will support a temperature gradient. The total thermal resistance of a non-heat sinked dual in-line plastic package is therefore much higher. Since air is a natural thermal insulator, maximum heat transfer is through convection and the total thermal resistance will decrease some at high power levels.

Lead Frame	Total Thermal Resistance	Max. Power Diss. (W) at 50°C T_A, 150°C T_J
14-Pin Kovar	120°C/W	0.83
14-Pin Copper	72°C/W	1.39
"Bat-Wing"	50°C/W	2.0

Ignoring any safety margin and device performance, even the "bat-wing" is now only barely adequate for most applications. The obvious solution is the use of an external heat sink.

Referring to Figures 4 and 5, the thermal resistance requirement of the heat sink is found at the junction of the specified chip power dissipation and maximum ambient temperature. These curves are typical of those furnished in many monolithic integrated circuit data sheets. Actual performance in a specific situation depends on factors such as the proximity of objects interfering with air flow, heat radiated or convected from other components, atmospheric pressure, and humidity. A good safety factor is therefore in order.

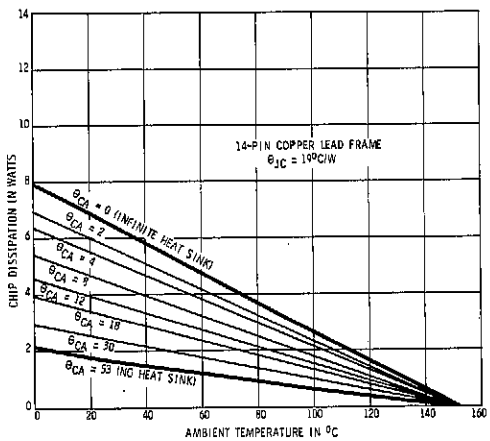

Figure 4

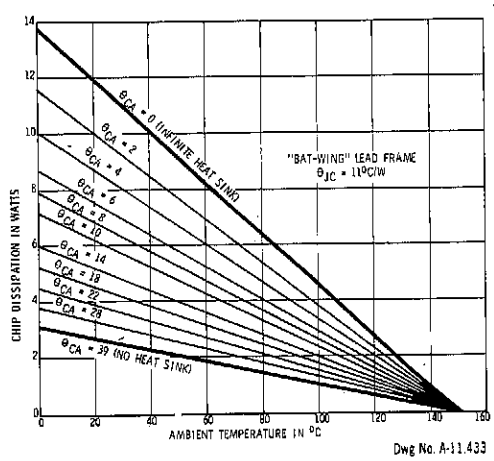

Figure 5

Heat sinks for plastic dual in-line packages can be of almost unlimited variety in design, material, and finish. Economics will normally play a very important role in the selection of any heat sink.

The least expensive and easiest to fabricate heat sink is the plain copper sheet. It is also very effective in reducing the total thermal resistance. The necessary dimensions can be obtained from Figure 6. These heat sinks are square in geometry, 0.015 inches thick, mounted vertically on each side of the lead frame, and with a dull or painted surface (Figure 7). The heat sinks should be soldered directly to the lead frame (approximately 0.3°C/W interface thermal resistance).

The plain copper sheet heat sink is also available commercially and may be less expensive than in-house manufacture. Two standard types are the Staver V7 and V8.

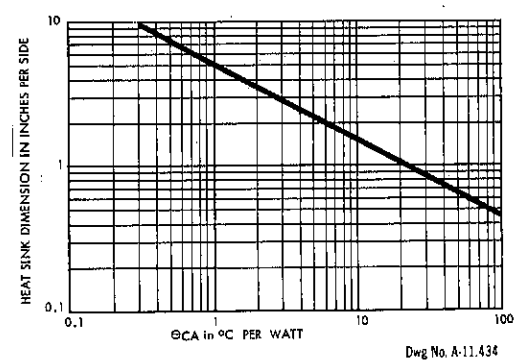

Figure 6

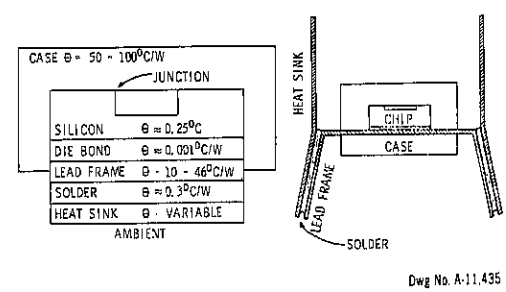

Figure 7

Heat Sink Finishes

Although plain copper is an effective heat sink, it is sometimes desirable to have something that is more appealing to the eye. For this reason, and others, many heat sinks are either painted or anodized.

The most common finish is probably black anodizing. It is economical and offers a good appearance. The black finish will also increase the performance of the heat sink, due to radiation, by as much as 25%. However, since anodizing is an electrical and thermal insulator, the heat sink should have an area free of anodize where the heat-generating device is attached.

Other popular finishes for heat sinks are irridite and chromic acid dips. They are economical and have negligible thermal and electrical resistances. These finishes, however, do not enjoy the 25% increase in performance that a dull black finish has.

Forced Air Cooling

The performance of many heat sinks can be increased by as much as 100% by forcing air over the fins. Where space is a problem, the cost of a small fan can often be justified. If a fan is required for other purposes, it is advantageous to place the semiconductor heat source in the air flow. A rule-of-thumb is that semiconductor failure rate is halved for each 10°C reduction in junction operating temperature.

Chip Design

Proper thermal design by the integrated circuit user can reduce the operating temperature of the semiconductor junction. However, the minimum chip temperature at any power level is determined solely by the device manufacturer. For this reason, care must be taken in choosing the manufacturer. "Exact equivalent" integrated circuits are not necessarily identical. Electrically and mechanically they may be the same, but thermal differences can mean that "identical" audio power amplifiers will not put out the same power without exceeding the rated junction temperature.

The circuit manufacturer must optimize his chip design so that component drift is minimized and/or equalized so that rated performance can actually be obtained under maximum thermal stress.

Note in Figures 8 and 9 that the Darlington input differential pairs are cross-connected so as to minimize differences in gain as a function of output transistor power dissipation. Transistor Q_4, being closest to the output power transistors, is naturally the hottest; Q_3 is a degree or two cooler; Q_1 and Q_2 are about equal and midway between Q_3 and Q_4. The gain of the Q_1-Q_2 Darlington pair is about equal to the gain of Q_3-Q_4 at all output power levels because of careful thermal design.

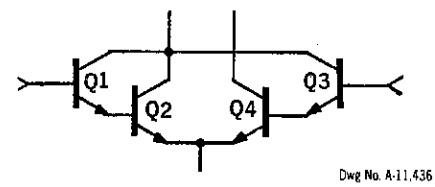

Figure 8

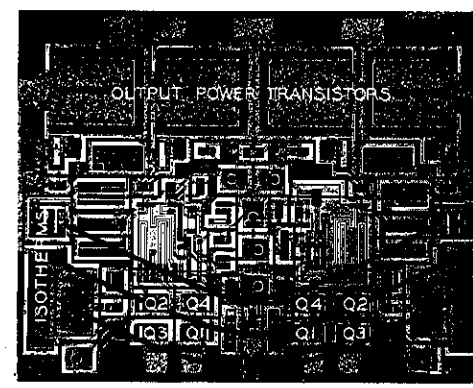

Figure 9

8

In certain specialized applications, thermal coupling can be used to a distinct advantage. Experimentally, thermal coupling has been used to provide a low-pass feedback network which otherwise could be obtained only with very large values of capacitance.

The foregoing discussion has covered the average thermal characteristics of today's dual in-line plastic integrated circuits. The specific devices will vary with the different packages and bonding techniques employed, but the concepts will remain the same.

APPENDIX

The following is intended to review terminology and compare thermal circuits with the more familiar electrical quantities.

The first law of thermodynamics states that energy cannot be created or destroyed but can be converted from one form to another. The second law of thermodynamics states that energy transfer will occur only in the direction of lower energy. In the semiconductor junction, the electrical energy is converted to thermal energy. Since no heat will be stored at the junction, the heat will flow to a lower temperature medium, air. The rate of heat flow is dependent on the resistance to that flow and the temperature difference between the source and the sink.

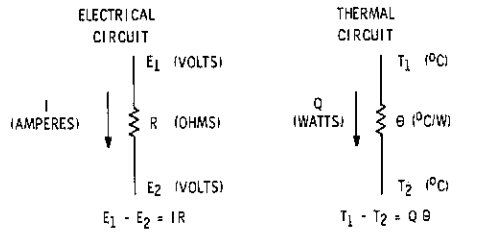

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Figure 10

This thermal electrical analogy is convenient only for conduction problems where heat flow and temperature obey linear equations. The analogy becomes much more complex for situations involving heat flow by convection and radiation. Where these two modes are not negligible, they can be approximated by an equivalent thermal resistance. If ignored, the error introduced will only improve the device reliability.

A simplified thermal flow diagram of a molded dual in-line package and heat sink is shown. The thermal resistance of the lead frame-heat sink-ambient is shown as a variable resistor, because this is under the control of the user and may be varied over a considerable range.

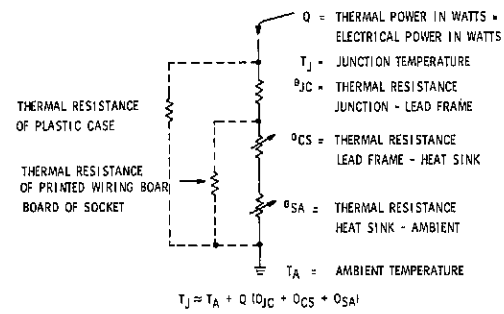

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Figure 11

Material	Thermal Resistance in °C/W for Unit Area/Unit Length
Silver	0.09
Copper, Annealed	0.10
Gold	0.12
Beryllia Ceramic	0.20
Aluminum	0.20
Brass (66 Cu, 34 Zn)	0.40
Silicon	0.50
Germanium	0.70
Steel, SAE 1045	0.80
Solder (60 Sn, 40 Pb)	1.5
Alumina Ceramic	2.0
Kovar (54 Fe, 29 Ni, 17 Co)	3.0
Glass	40
Epoxy	40
Mica	50
Teflon PTFE	200
Air	2000

Computing IC Temperature Rise

Heat is the enemy of integrated circuits—particularly power devices. Here's how to use thermal ratings to determine safe IC operation.

EXCESSIVE heat shortens the life of an IC and reduces its operating capability. Until recently, ICs were capable of operating only in low-power applications requiring perhaps a few milliwatts of power. But now, new ICs handle several hundred milliamperes and drive devices such as relays, solenoids, stepping motors, and incandescent lamps. These high power levels may increase IC temperatures substantially and are capable of destroying devices unless appropriate precautions are taken.

Thermal Characteristics

The thermal characteristics of any IC are determined by four parameters. Maximum allowable IC chip junction temperature T_J and thermal resistance R_θ are specified by the IC manufacturer. Ambient temperature T_A and the power dissipation P_D are determined by the user. Equation 1 expresses the relation of these parameters.

$$T_J = T_A + P_D R_\theta \quad (1)$$

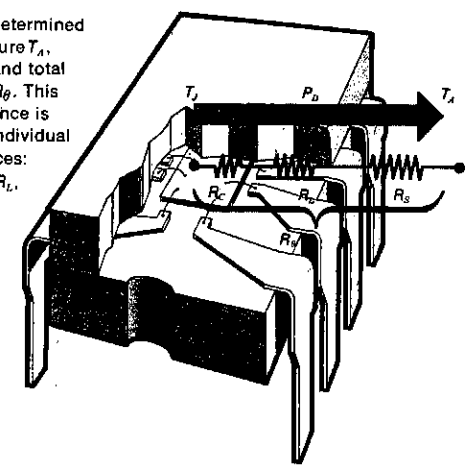
Junction temperature T_J usually is limited to 150°C for silicon ICs. Devices may operate momentarily at slightly higher temperatures, but device life expectancy decreases exponentially for extended high-temperature operation. Usually, the lower the junction operating temperature, the greater the anticipated life of the IC.

Ambient temperature T_A is traditionally limited either to 70°C or 85°C for plastic dual in-line packages (DIPs) or 125°C for hermetic devices. Again, the objective is to operate at as low a junction temperature as practical.

Thermal resistance R_θ is the basic thermal characteristic for ICs. It is usually expressed in terms of °C/W and represents the rise in junction temperature with a unit of power applied in still air. (The reciprocal of thermal resistance is thermal conductance, or derating factor,

Why IC Temperatures Rise

IC temperature T_J is determined by ambient temperature T_A, heat dissipated P_D, and total thermal resistance R_θ. This total thermal resistance is comprised of three individual component resistances: chip R_C, lead frame R_L, and heat sink R_S.



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G_θ expressed as W/°C.) Thermal resistance of an IC consists of several distinct components, the sum of which is the specified thermal resistance. For a typical IC, these components of thermal resistance are 0.5°C/W per unit thickness of the silicon chip, 0.1 to 3°C/W per unit length of the lead frame, and up to 2,000°C/W per unit thickness of still air surrounding the IC. DIPs are used more than any other type of packaging for ICs and newer copper-alloy lead frames provide a superior thermal rating over the standard iron-nickel-cobalt alloy (Kovar) lead frames. However, power ICs are also available in other packages such as flatpacks and TO-type cans.

The power P_D that an IC can safely dissipate usually depends on the size of the IC chip and the type of packaging. Most common copper-frame DIPs can dissipate about 1.5 W, although some special-purpose types have ratings as high as 5 W.

Total IC power to be dissipated depends on input current, output current, voltage drop, and duty cycle. Thus, for many industrial digital-control ICs, logic-gate power P_l (typically less than 0.1 W) and output power P_o must be determined to find the total power to be dissipated. Total power dissipation for these logic devices is the sum of P_l and P_o.

$$P_l = n(V_{CC}I_{CC}) \quad (2)$$

$$P_o = n(V_{CE(SAT)}I_C) \quad (3)$$

where V_{CC} = logic-gate supply voltage, I_{CC} = logic-gate ON current, $V_{CE(SAT)}$ = output saturation voltage, I_C = output

Finding Safe Operating Limits

Here's how to calculate the safe operating limits for an IC. The first two examples are simple calculations involving maximum allowable power and are straightforward. The third and fourth examples are more complex and involve logic power, output power, and duty cycle.

Problem: Determine the maximum allowable power dissipation that can be handled safely by a 16-lead Kovar DIP with an R_θ of 125°C/W in an ambient temperature of 70°C.

Solution: From Equation 1, the maximum allowable power dissipation P_D for this IC is

$$P_D = \frac{150°C - 70°C}{125°C/W}$$

$$= 0.64\ W$$

Problem: Determine the maximum allowable power dissipation that can be handled by a 14-lead copper DIP with a derating factor G_θ of 16.67 mW/°C in an ambient of 70°C.

Solution: Since the derating factor G_θ is the reciprocal of thermal resistance R_θ, the maximum allowable power dissipation P_D from Equation 1 is

$$P_D = (150°C - 70°C) \times (16.67\ mW/°C)$$

$$= 1.33\ W$$

Problem: Calculate the maximum junction temperature for a quad power driver with a thermal resistance of 60°C/W in an ambient of 70°C and which is controlling a 250 mA load on each of the four outputs.

Solution: To determine the maximum (worst case) junction temperature for this IC, the maximum total power dissipation must be determined from the data listed on the IC data sheet. The specifications are usually listed as typical and minimum or maximum values. It is important to use maximum voltage and current limits to insure an adequate design. Common maximum values for an

Measuring IC Temperature

Sometimes IC junction temperature cannot be calculated readily and instead must be measured. Measurement should be made when there is insufficient data with which to calculate, when the effects of external variables such as forced-air cooling or enclosure size must be determined, or as a check on the manufacturer's specifications regarding package thermal resistance.

The most popular technique for measuring IC temperature uses the characteristic of a diode to reduce its forward voltage with temperature. Many IC chips have some sort of accessible diode—parasitic, input protection, base-emitter junction, or output clamp. With this technique, a "sense" diode is calibrated so that forward voltage is a direct indicator of diode junction temperature. Then, current is applied to some other component on the chip to simulate operating conditions and to produce a temperature rise. Since the thermal resistance of the silicon chip is low, the temperature of the sense diode is assumed to be the same as the rest of the monolithic chip.

The sense diode should be calibrated over at least the expected junction operating temperature chamber. Apply an accurately measured, low current of about 1 mA through the sense diode and measure the forward voltage in 25°C increments after stabilization at each temperature. This calibration provides enough data for at least six points to construct a diode-forward-voltage versus junction-temperature graph at the specified forward current. A typical 25°C forward voltage is between 600 and 750 mV and decreases 1.6 to 2.0 mV/°C.

For power levels above 2 W, it may be necessary to use more than a single transistor if only the device saturation voltage and sink current are used. When higher power is desired, keep the output out of saturation.

Measuring the sense-diode forward voltage may require a considerable waiting period (10 to 15 minutes) for thermal equilibrium. In any event, at the instant of measurement, the heating power may have to be disconnected since erroneous readings may result from IR drop in circuit common leads. Various circuit connections (such as four-point Kelvin) may be arranged to reduce or eliminate this source of error.

The IC junction temperature can be determined by comparing the voltage measurement with the internal power source against the voltage measurement with the temperature chamber.

industrial power driver are $V_{CC} = 5.25$ V, $I_{CC} = 25$ mA, and $V_{CE(SAT)} = 0.7$V, and $I_c = 250$ mA. From Equations 2 and 3, worst case logic and output power dissipation are

$$P_l = 4(5.25\text{ V} \times 25\text{ mA}) = 525\text{ mW}$$

$$P_o = 4(0.7\text{ V} \times 250\text{ mA}) = 700\text{ mW}$$

Thus, the total worst case power dissipation P_D is 525 mW plus 700 mW, or 1.225 W. From Equation 1, maximum junction temperature T_J is

$$T_J = 70°\text{C} + (1.225\text{ W}) \times (16.67\text{ mW/°C}) = 143.5°\text{C}$$

Problem: Determine the acceptable duty cycle for a hermetic power driver with a thermal resistance of 100°C/W in an ambient of 85°C and which is controlling load currents of 250 mA on each of four outputs.

Solution: From Equation 1, the allowable average power dissipation P_D for this IC is

$$P_D = \frac{150°\text{C} - 85°\text{C}}{100°\text{C/W}} = 0.65\text{ W}$$

This means that there is 0.65 W limit on average power, but, not instantaneous power. If the duty cycle is low enough, and the ON time is not more than about 0.5 sec, the average power dissipation can be considerably lower than the peak power. The ON, or peak power, is determined from the data sheet maximum values of V_{CC}, I_{CC}, and $V_{CE(SAT)}$ at the specified load current of 250 mA. From Equations 2 and 3, logic-gate power P_l and output power P_o for the ON state are

$$P_l = 4(5.5\text{ V} \times 26.5\text{ mA}) = 583\text{ mW}$$

$$P_o = 4(0.7\text{ V} \times 250\text{ mA}) = 700\text{ mW}$$

Instantaneous ON power P_{ON} is the sum of P_l and P_o for the ON state, or 1.283 W. The OFF power is primarily the power dissipated by the logic in the OFF state, and is found by using the I_{CC} maximum rated current listed on the specification sheet. The power dissipated in the output stage can be calculated from the leakage current I_C and supply voltage V_{CE}. From Equations 2 and 3, logic-gate power P_l and output power P_o for the OFF state are

$$P_l = 4(5.5\text{ V} \times 7.5\text{ mA}) = 165\text{ mW}$$

$$P_o = 4(100\text{ V} \times 0.1\text{ mA}) = 40\text{ mW}$$

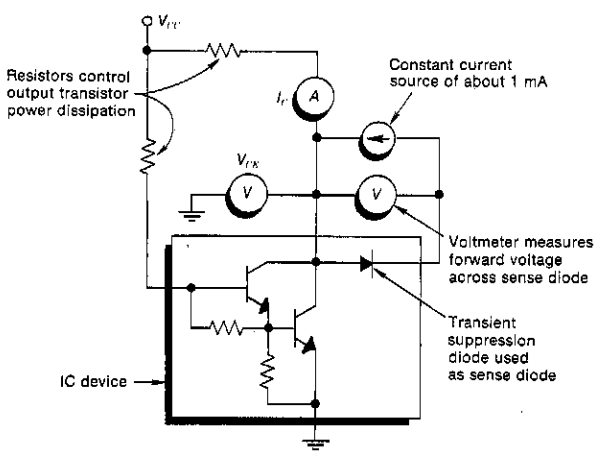
Instantaneous OFF power P_{OFF} is the sum of P_l and P_o for the OFF state, or 205 mW. From Equation 4, acceptable % duty cycle D is

$$D = \frac{P_D - P_{OFF}}{P_{ON} - P_{OFF}} = \frac{0.65\text{ W} - 0.205\text{ W}}{1.283\text{ W} - 0.205\text{ W}}$$

load current, and n = number of logic gates. Manufacturers usually list typical and maximum values for these voltages and currents. For thermal considerations it is best to use the maximum values so that worst-case power dissipation is determined.

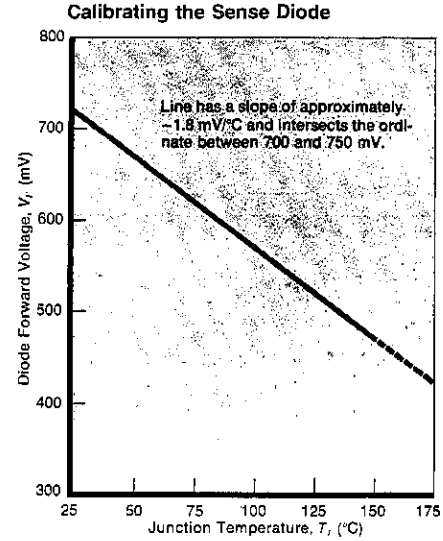
If the duty cycle of the device is longer than 0.5 sec, the peak power dissipation is the sum of the logic-gate power P_l and output power P_o for the logic ON state alone. If the ON time is less than 0.5 sec, however, average power dissipation must be calculated from instantaneous

Setting Up the Circuit



Input power is negligible compared to output power and is therefore not measured.

Calibrating the Sense Diode



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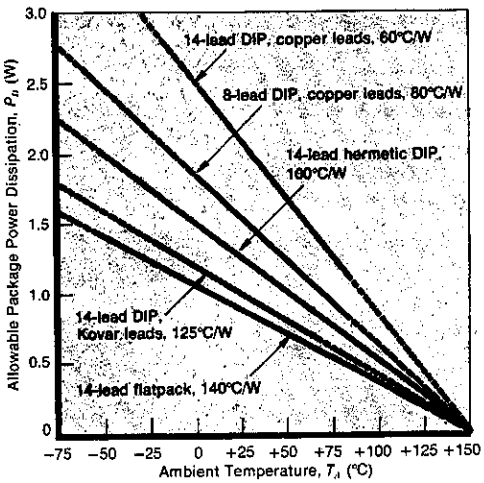
What the Curves Show

The junction temperature of an IC depends on several factors, including the thermal resistance of the IC and the operating duty cycle. Graphs showing the relationship of these factors are often useful in specifying an IC.

Thermal Ratings

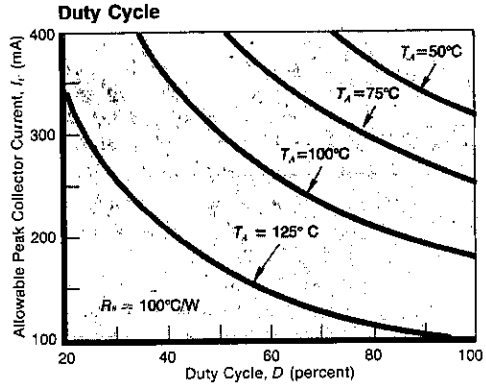


Typical thermal-resistance ratings for ICs in still air range from 60°C/W to 140°C/W. The slope of each curve on this graph is equal to the derating factor $G\theta$, which is the reciprocal of thermal resistance $R\theta$. For an ambient temperature of 50°C, a typical 14-lead flatpack with an $R\theta$ of 140°C/W can dissipate about 0.7 W. A typical DIP, however, with 14 copper-alloy leads can dissipate almost 1.7 W at 50°C.

The highest allowable package power dissipation shown here is 2.5 W. Other special-purpose DIP packages are available with power dissipation ratings as high as 3.3 W at 0°C ($R\theta$ = 45°C/W). If not for package limitations, IC chip dissipation might be greater than 9 W at an ambient temperature of up to 70°C.

Although the curve for plastic DIPs goes all the way to 150°C, they ordinarily are not used in ambients above 85°C because of traditional package limitations. Hermetic DIPs are specified to temperatures of 125°C, and at 150°C the device should be derated to 0 W. The higher specification limits for hermetic devices is the result of their design for use in rigorous, high-reliability military applications.

Duty Cycle



Duty cycle is important in calculating IC junction temperature because average power—not instantaneous power—is responsible for heating the IC. To convert from peak power to average power, multiply the peak power dissipation by the duty cycle. The average-power rating is then used with the thermal-resistance rating to calculate the IC junction temperature. Thus, short duty cycles allow peak power to be high without exceeding the 150°C junction-temperature limit. However, this consideration applies only to ON times of less than 0.5 sec.

ON and OFF power P_{ON} and P_{OFF} from

$$P_D = DP_{ON} + (1 - D)P_{OFF} \quad (4)$$

Corrective Actions

If the junction temperature or the required power dissipation of the IC is calculated to be greater than the maximum values specified by the manufacturer, device reliability and operating characteristics possibly will be reduced. Possible solutions are: 1. Modify or partition the circuit design so the IC is not required to dissipate as much power. 2. Reduce the thermal resistance of the IC by using a heat sink or forced-air cooling. 3. Reduce the ambient temperature by moving heat-producing components such as transformers and resistors away from the IC. 4. Specify a different IC with improved thermal or electrical characteristics (if available).

THERMAL RESISTANCE— A RELIABILITY CONSIDERATION

More and more the semiconductor component supplier and the ultimate system user are becoming aware of the need for reliable components. Most failure mechanisms responsible for reliability failures are temperature dependent and the kinetics of the failure reaction are normally described by an Arrhenius function. This dependence, therefore, demands the capability of measuring the mean temperature which an integrated circuit die will attain during operation to realistically assess the reliability of the part.

The problem addressed by this paper is the inconsistency of the measurement techniques and the results used by manufacturers and users to determine the thermal characteristics of packaged semiconductor components. Our objective is to provide insight into the considerations which must be applied when evaluating these thermal properties of the packaged component. These considerations are materials, geometry and environment.

Furthermore, we wish to instill uniformity in the method of determining thermal properties of packaged semiconductors through understanding of the variables involved which can lead to a useable industry standard.

Reliability—The Temperature Function

The recognition of the problems one encounters in measuring the mean temperature of a die has been directly related to our experiences at the Sprague Electric Co. in our Reliability Assurance Programs. The large number of device types manufactured require an equally large number of burn-in boards having different functions and geometry for the individual reliability studies. The variations in board density and thermal environment for a device under test have provided considerable junction temperature data from which we conclude that a "thermal resistance" measured in one oven with its set of conditions is not transferable to another oven with different boards, loading, etc. when the reference temperature for the measurement is the oven control temperature. Furthermore, it has become obvious that these same problems in measuring a mean die temperature exist in a system environment.

Most reactions which can cause a failure in an electrical parameter of an integrated circuit are chemical in nature and are influenced by temperature. The temperature dependence of these reactions has been described very well by S. Arrhenius in his treatment of reaction kinetics.[1] In his treatment, the reaction velocity or rate is given by the equation.

$$d\ln V_r/dT = E/RT^2$$

here V_r is the specific reaction rate, T is the absolute temperature, R is the Molar Gas Constant, and E is the energy difference between a mole of active molecules and a mole of normal molecules.

This equation integrates to

$$\ln V_r = E/RT + A$$

where A is a constant which is the value of $\ln V_r$ at $1/T = 0$, $(\ln V_r)$. A more familiar expression is

$$\ln V_r = \ln V_r^0 - \epsilon/kT$$

or

$$V_r = V_r^0 e^{-\epsilon/kT}$$

where ϵ is the activation energy per molecule $(= E/N)$, N = Avagado's number and k is the gas constant per molecule $(=R/N)$, which is generally known as the Boltzmann constant. It has the value 8.6×10^{-5} eV/°K.

V_E, the time rate of change of the electrical parameter is proportional to V_r, i.e., $V_E = BV_r$. The amount of change in the electrical parameter necessary to cause a normal device to fail, ΔP_f, is $V_E t_f$ where t_f is the time of failure.

Recalling that $V_E = BV_r$, then

$$\Delta P_f = BV_r t_f$$

For a given device ΔP_F is a constant, therefore,

$$t_f = \Delta P_f B^{-1}/V_r$$

but

$$V_r = V_r^0 e^{\epsilon/kT}$$

therefore

$$t_f = (B^{-1}\Delta P_f/V_r^0 e^{\epsilon/kT} = \delta e^{\epsilon/kT}$$

where

$$\delta = B^{-1}\Delta P_f/V_r^0$$

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The acceleration factor ($\overline{AF}$) between any two temperatures is derived from this equation, when the activation energy for the failure reaction is known:

$$\overline{AF} = t_{f_1}/t_{f_2} = e^{\phi/k(1/T_1 - 1/T_2)}$$

Activation energies of most reactions responsible for random failures in a normal operating period (beyond infant mortality) are nominally

$$(0.4 - 1.0)\,eV.$$

The importance of accurately determining the die temperature is now clear if one considers a not unrealistic situation where a device is thought to be operating with a die temperature of 120° and the actual temperature is 150°C. If the failure reaction has an activation energy of 0.7 eV, then the acceleration factor is 4.3 which means the device would fail in less than one quarter of the time it would have taken if the device actually operated at 120°C.

Thermal Resistance – θ_{JA}

Quite frequently applications engineers have made attempts to identify the temperature attained by a die when a steady state rate of heat is being generated by the die by applying the term called "Thermal Resistance." This "constant," designated $R\theta_{JA}$ or simply θ_{JA}, relates the temperature rise of a packaged integrated circuit die above an ambient temperature when a known constant power is generated in the die. This term is normally defined as

$$\theta_{JA} = (T_J - T_A)/P_D$$

where T_J is the mean junction or die temperature, T_A is an ambient temperature, and P_D is the power generated within the die which must be conducted from the die to the ambient. This is occasionally designated Q_T, the time rate of heat generation in the die. Thermal resistance data supplied by manufacturers may be referenced to a cubic foot of free or still air, flowing air at some velocity, or simply no reference. These are some of the definitions of "ambient" from which one must determine where to measure T_A.

Thermal resistance as defined by θ_{JA} is not constant. It is made up of a constant term (or terms) in series with a number of variable terms. The constant terms relate to the package materials and geometry, which we will designate θ_{JC_i} and the variable terms relate to the heat paths from the package boundary to some isothermal envelope in the system which has the temperature T_A. Even if the system for measuring θ_{JA} is defined, it is virtually impossible to reproduce that system in an application since the external thermal paths are determined by the method of mounting, the printed wiring board if used, other heat generating components on the board or in the vicinity, air flow patterns, etc. These are all variable for each application. We have measured values of θ_{JA} for the same device which vary by a factor of two when the mounting and environmental conditions are changed. The values in the θ_{JA} column in Tables 2 and 3 are indicative of the variation.

One is tempted to partition θ_{JA} into two thermal terms,

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{JC} is defined as the thermal resistance from the source of power at T_J to the boundary of the package not including the external legs, and θ_{CA} is the thermal resistance from the package boundary to that isothermal envelope at T_A. However, when one examines the thermal profile along the surface of a plastic dual-in-line package such as shown in Figure 1, it is immediately obvious that a definition of θ_{JC}

$$\theta_{JC} = (T_J - T_C)/P_D$$

cannot be applied because T_C varies with position. Similarly, the term θ_{CA} defined by

$$\theta_{CA} = (T_C - T_A)/P_D$$

suffers from the same variability in T_C. This being the case it is invalid to partition θ_{JA} when operating on the *total* power to be dissipated, P_D.

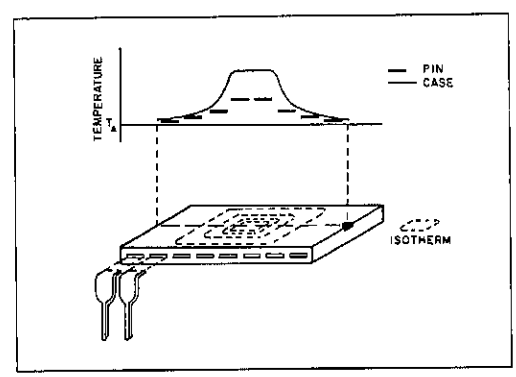


Figure 1

The Thermal Model

When one examines a plastic package supplied by an individual manufacturer it is found that the geometry of the lead frame, its position within the package boundary, its composition, the composition of the plastic and its filler, the internal wire bonding are very carefully controlled and constant in time. This being the case one can readily build a model of the package which can be as invariant as the package material properties. If one considers all possible heat flows, a very complex model emerges. However, if the thermal conductivities of the package materials and the orders of magnitude difference in the values of these conductivities are considered, a simplified workable model can be generated by neglecting heat paths where heat flows are minimal. The simplified model shown in Figure 2 has ignored the heat flow between leads and assumes that the large difference between the thermal conductivity of the loaded plastic and the metals in the package define the specified heat paths. For example, the heat flow between leads would be a shunting resistor between heat paths in the model. The thermal conductivity of most plastics range between 1.5 and 3 × 10^{-3} calories/cm − °C while copper based materials range between 0.5 and 0.82 calories/cm − °C and nickel based alloys are about 0.03 calories/cm − °C.

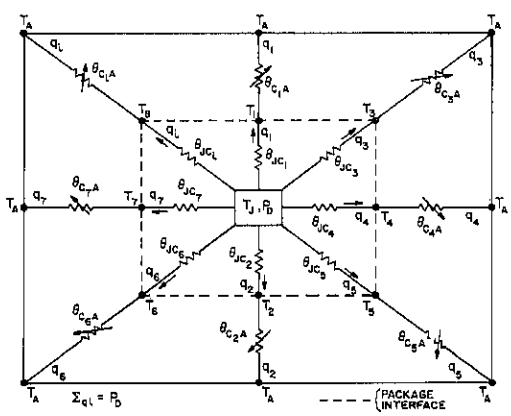


Figure 2

The heat paths defined by θ_{JC_i}, where i refers to a particular path, radiate from the chip to an area on the package periphery defined by the projected chip or pad area as well as the mean cross-sectional area of each of the leads within the plastic package boundary (see Figure 1). Because of package symmetry, a 16 lead isolated pad package may have seven different heat paths which can be characterized. The thermal resistance, θ_{JC_i}, can be calculated for each path from the geometry and material properties. For example θ_{JC_1} is the resistance from the top of the chip to the projected area on the package surface. The value of θ_{JC_1} is given by

$$\theta_{JC_1} = (T_J - T_{C_1})/q_1 = L/K_pA$$

where L is the length of the heat path (thickness of the plastic above the die), A is the cross-sectional area of the heat path (are of the die or the pad), K_p is the thermal conductivity of the loaded plastic and q_1 is the heat/second flowing in the path defined by A and L.

θ_{JC_2} is the thermal resistance from the top of the die through the silicon, through the pad and through the plastic to the bottom surface. The value of θ_{JC_2} is given by

$$\theta_{JC_2} = (T_J - T_{C_2})/q_2 = [1/A] \sum L_n/K_n \quad n = \text{Si, Metal, Plastic}$$

Similar expressions can be derived for each of the leads and they have the form

$$\theta_{JC_i} = (T_J - T_{C_i})/q_i = [1/t]\,[(L/K_PW_P) + (1/K_M) \sum L_n/W_n] \quad n = 1, 2 \ldots\ldots$$

where t is the thickness of the lead frame, K_p is the thermal conductivity of the loaded plastic, K_M is the thermal conductivity of the frame metal, L_n is the mean length of each connected portion of a leg segment having a mean width, W_n. In accord with the model, each internal path characterized by a thermal resistance, θ_{JC_i}, is in series with an external thermal resistance, θ_{CiA}, which completes the path to T_A. The value of θ_{CiA} can be calculated from the amount of heat, q_i, flowing through the internal package path and the temperature difference, $(T_{C_i} - T_A)$, with the equation

$$\theta_{CiA} = (T_{C_i} - T_A) / q_i.$$

Values of θ_{CiA} are variable and depend upon the specific environment.

We at Sprague Electric Company identify the heat paths in our calculations and data as follows: a) when i = 1 the path is from die to case surface directly above, b) when i = 2 the path is from die to the case surface directly below and c) when i = 3, 4, 5 . . . the path is from die through an identified metal lead to the intersection with the plastic surface.

Verification of Model

From the model one can derive the minimum thermal resistance which is characteristic of the package. This can be calculated for the condition when all case temperatures are equal and at T_A. This is equivalent to shorting all external thermal resistances so that $T_{C_i} = T_A$. When all T_{C_i} are equal, the reciprocal of the sum of the reciprocals of all θ_{JC_i} is the minimum thermal resistance for the package. This is realized experimentally by placing the unit in an infinite heat sink such as a rapidly stirred, low-viscosity controlled temperature bath. The case temperature is now forced to be the same over all surfaces and by definition it is T_A. θ_{JC} is the minimum limit of θ_{JA}. Table 1 shows the agreement between the values of θ_{JC} calculated from the model when the case temperatures are shorted together and the values experimentally measured in a controlled temperature liquid bath. The agreement between calculated and experimental values for packages constructed from different materials enhance the validity of the model.

Applying The Model To Measure T_J

Having verified the model, any one of the identified heat paths, which has a constant thermal resistance, o_{JC_i}, can now be used to determine quite accurately the die temperature, T_J. If one chooses to measure the case temperature directly above the die, the difference between die temperature and case temperature is related to the heat flow, q_i, through that path by the thermal conductivity equation:

$$q_i = K_p A (T_J - T_{C_i})/L_i.$$

Rearranging this equation to

$$(T_J - T_{C_i})/q_i = L_i/k_p A_i = \theta_{JC_i}$$

Then

$$T_J = T_{C_i} + q_i\theta_{JC_i}$$

If the fraction of total heat, P_D generated by the die which passes through path 1 is defined as k, then

$$q_1 = k_1 P_D$$

Substituting into the previous equation, T_J is now referenced to T_{C_1} by

$$T_J = T_{C_1} + k_1\theta_{JC_1}P_D$$

where T_J, T_{C_1}, and P_D are experimentally measureable quantities. Values of $k_1\theta_{JC_1}$ can be determined. This term can be used to determine T_J in any environment by measuring T_{C1} and the total heat generated by the die. This equation applies for any path, i., i, e.

$$T_J = T_{C_1} + k_i\theta_{JC_i}P_D$$

Experimental results are presented in Table 2 which establish that $k_i\theta_{JC_i}$ is a constant, the magnitude of which is determined by the heat path chosen.

In our notation, $k_4\theta_{JC_4}$ is the thermal resistance of the path determined by measuring the temperature of pin 4 at the point of intersection with the case body. Further data are presented in Table 3 for a copper tab package where the pad on which the die is mounted extends to the outside of the package. The values of $k_5\theta_{JC_5}$ remain constant over a large change in environment. When i = 5, the heat path is from the die through the heat tab to the intersection with the case surface.

Figure 3 shows the outline of the frame in the 16 pin isolated pad package which is designated the "A" package. The "B" package or tab package frame outline is also shown.

Measurement of $k_i\theta_{JC_i}$

Although the derived equations indicate that $k_i\theta_{JC_i}$ are determined by two temperature measurements at one power level, the values are more accurately determined from temperature versus power plots.

TABLE 1
COMPARISON OF CALCULATED AND EXPERIMENTAL VALUES OF $[\theta_{JC}]\ T_{C_i} = T_A$
(All measurements in °C/W)

Package Type	Frame Material	$[\theta_{JC}]\ T_{C_i} = T_A$ Experimental	Calculated
16 pin, isolated pad, Epoxy I	copper	41 ± 3	43
16 pin, isolated pad, Epoxy I	Kovar	100 ± 4	93
16 Pin Tab	copper	8.6 ± .7	8.5

TABLE 2
THERMAL RESISTANCE VALUES—ISOLATED PAD—EPOXY PACKAGE
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_4\theta_{C_4A}$	$k_1\theta_{C1A}$	$k_1\theta_{JC_1}$	$k_4\theta_{JC_4}$
ULN-2003A 16-Pin Copper Frame. "A" Package	1 ft.³ still air, socket mount	84.7	39.1	48.1	36.6	45.6
ULN-2003A 16-Pin Copper Frame. "A" Package	Oven #1 60 CFM, pin connectors	60.0	17.0	25.2	34.8	42.3
ULN-2003A 16-Pin Copper Frame. "A" Package	AAVID E type 5010 heat sink Oven #1 60 CFM	50.4	11.4	15.2	35.2	39
ULN-2003A 16-Pin Copper Frame. "A" Package	Fluorocarbon Bath, pin connectors	41.3	3.3	2.9	38.4	38

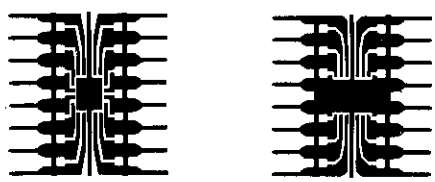


Figure 3
Plastic Package Frame Geometry

If one considers any one path, i, in the model, that path is described by:

$$T_J - T_A = q_i(\theta_{JC_i} + \theta_{C_iA})$$

Here again if k_i is the fraction of the total heat (P_D) which traverses path i then the previous equation can be written

$$T_J - T_A = k_iP_D(\theta_{JC_i} + \theta_{C_iA})$$

or rearranging terms

$$(T_J - T_A)/P_D = k_i\theta_{JC_i} + k_i\theta_{C_iA}$$

TABLE 3
THERMAL RESISTANCE VALUES—TAB PAD—EPOXY PACKAGE
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$K_5\theta_{C5}A$	K_5J_{C5}
Test Chip "B" Package	oven #1, T_A = 50°, 60 CFM	32.8	25.0	7.8
ULN-2068 "B" Package	oven #1, T_A = 50°, 60 CFM	34.9	26.4	8.5
ULN-2068 "B" Package	Socket mount, FC-40 Bath	23.2	13.5	9.7
ULN-2068 "B" Package	Socket mounted on board, FC-40 Bath	26.8	17.4	9.4
Test Die "B" Package	oven #1, soldered on test board, 60 CFM	31.2	22.8	8.4
Test Die "B" Package	oven #1, soldered in test board w/Staver heat sink	22.3	14.2	8.1

By definition $(T_J - T_A)/P_D = \theta_{JA}$, therefore by substitution and rearrangement

$$k_i\theta_{JC_i} = \theta_{JA} - k_i\theta_{C_iA}$$

where experimentally θ_{JA} is the slope of a plot of T_J versus P_D and $K_i\theta_{C_iA}$ is the slope of the plot of T_{C_i}, versus P_D. Figures 4, 5, and 6 are representative of the experimental plots for evaluation of $k_i\theta_{JC_i}$.

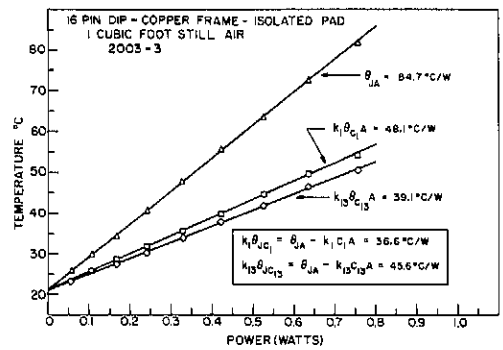


Figure 4

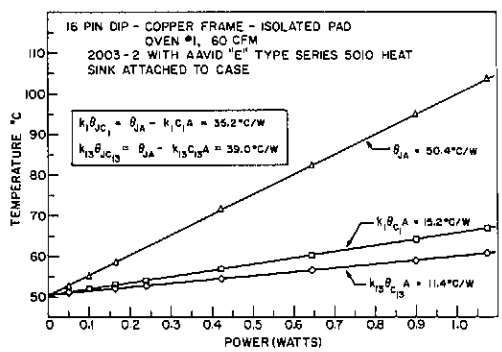


Figure 5

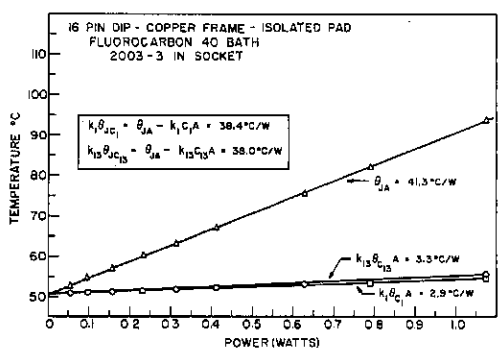


Figure 6

T_{C_i} Measurement

The numerical values of $k_i\theta_{JC_i}$ which we have shown experimentally to be constant over a large variation in environmental conditions are functions of the measuring system for determining the case or leg temperature, T_{C_i}. This can be shown by considering heat path 1 in the Model shown in Figure 2. In this case $q_1 = (T_J - T_A)/(\theta_{JC_1} + \theta_{C_1A})$. θ_{JC_1} is defined as L_1/k_pA_1 where A_1 is determined by the die area. When a thermocouple is attached to the surface directly over the die it also functions as a heat sink. This changes the effective area A of the internal heat path and also changes the external thermal resistance, θ_{C_1A}. The changes are functions of the thermocouple composition and size. The value of θ_{JC_1} is now determined by the effective area of contact of the thermocouple and its value remains constant when the attached thermocouple's size is held constant. k_1, $(= q_1/Q_t)$, also changes because q_1 is determined by the sum of θ_{JC_1} and θ_{C_1A}. The term $(T_J - T_A)$ is essentially constant within experimental error because q_1 is small compared to Q_t and the variations in q_1 do not measureably change the die temperature.

θ_{C_1A} decreases as the wire size of a copper-constantan thermocouple increases and it increases as the composition is changed from copper-constantan to iron constantan. The thermal conductivities of copper, iron, and constantan are respectively 0.9, 0.16, and 0.054 cal/°C-cm.

Data in Table 4 confirm the direction and change in $k_1\theta_{JC_1}$ with change in measuring system. Data were taken in the same oven ambient.

When the physical system for T_C measurement and the conditions for measurement are specified and held constant, values for $k_i\theta_{JC_1}$ are constants.

T_J Measurement For $k_i\theta_{JC_i}$ Determination

An accurate measurement of the value of $k_i\theta_{JC_i}$ requires a method of measuring the mean temperature of the die, T_J. Techniques to make this measurement have been discussed elsewhere. (See Ref. 2, 3, 4) They involve measurement of a temperature sensitive parameter of an element on the die. The forward voltage drop across a diode measured at constant current is a commonly used parameter. One must observe caution when applying the cali-

TABLE 4
VARIATIONS IN $k_i\theta_{JC_1}$ WITH MEASUREMENT SYSTEM
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_1\theta_{C_1A}$	$k_1\theta_{JC_1}$
Test device	.005" Type "J" thermocouple	127.6	52.2	75.4
Test device	.012" Type "J" thermocouple	123.5	31.5	92.0
2125-Linear TV Circuit	.005" Type "T" thermocouple	123.3	75.0	48.3

bration data for an element in an unpowered die to the measured values of that element when the die is powered. It is rather unique if a parasitic voltage or current from the powered portion of the die does not interact with the temperature measuring element. This interaction leads to an inaccurate indication of the true temperature.

A test chip with a number of temperature sensitive elements is valuable. Figure 7 is a photo micrograph of a test chip designed by personnel at the Sprague Electric Company to evaluate thermal resistance values for various packages as well as package-surface interactions. The die contains 3 heat generators, and 6 primary temperature sensors, which are either diodes or special resistors. Parasitics normally interact differently with different elements because of location or structure variations. Agreement in the value of temperatures measured simultaneously for different elements on the chip normally indicates a correct measurement.

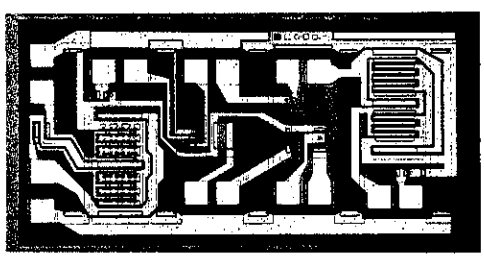


Figure 7

Figure 8 illustrates errors which can be introduced when making static steady state measurements of temperature during power application. Observe the plots of T_j (from V_{eb} calibration) versus P_D for three different diodes on the chip. Although the slopes of the plots after initial power agree within 10%, the initial portion of the curve indicates a negative thermal resistance and the offsets of the curves indicate a varying interaction at different power levels. Although calculation of thermal resistance by the slope method would introduce a similar error for all three diodes, the single power point method for calculating $k_i\theta_{JC_i}$, where $k_i\theta_{JC_i} = (T_J - T_{C_i})/P_D$, would introduce considerable and different levels of error in the calculated values for each diode measurement.

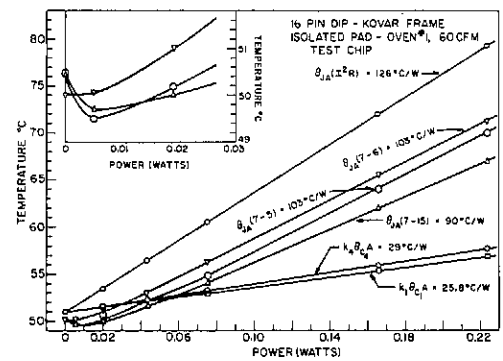


Figure 8

For example, if temperature measurements were made at a power level of 0.22 Watts, one would calculate a value of 44.6°C/W for $k_1\theta_{JC_1}$ using T_J from diode 7-15. 57.1°C/W using T_J from diode 7-5, and 63.8°C/W using T_J from diode 7-6. The true value which was verified by pulsed measurements was 97°C/W.

To eliminate interactions between the powered portion of a circuit and the temperature sensing element during measurement, the circuit shown in Figure 9 was developed. This circuit was designed for thermal evaluation of packages in which the function could be a linear circuit, a digital circuit, or the standard test chip which has a number of different power sources and temperature sensing elements.

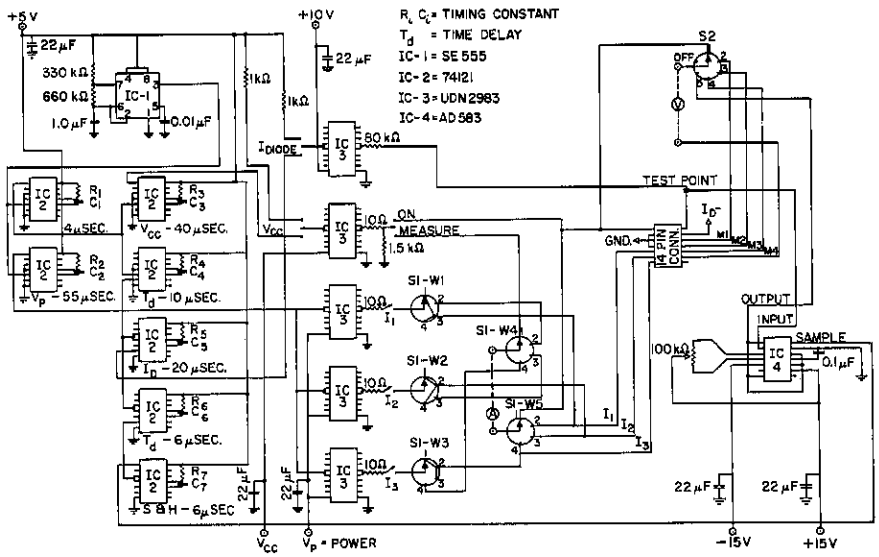


Figure 9

In operation, the circuit applies power at a measured level to the device under test for approximately one second, interrupts power for 40 microseconds, and continues this cycle throughout the test period. At the beginning of the 40-microsecond power off interval, a 10-microsecond delay allows circuit transients to decay before the diode current is activated. A 6-microsecond delay allows the current to settle before a sample and hold circuit samples the diode voltage to determine the chip temperature. This sequence allows the package under test to come to thermal equilibrium with the environment which approaches that for continuous power input. The power down sequence and temperature measurement interval are short enough to insure that the actual temperature drop when power is removed is less than the sensitivity of the temperature sensitive element.

The case temperature measurements, T_{C_1}, can be made by thermocouple or by infra-red measurements.[4] In theory the infra-red measurements would be preferred since a conductive contact is not made to the surface which is to be measured. In practice a number of difficulties with I.R. measurements are encountered. The emissivity of the surface to be measured must be controlled to give accurate measurements. This normally requires painting the surface with a "proprietary" film. When the emissivity is mastered, two larger difficulties must be overcome; a) physically placing the infra-red measuring instrument into the system to view a package surface when the unit may be buried in a maze of printed wiring boards and circuitry and b) the cost of available instrumentation.

The thermocouple technique to measure case temperature is a practical and reliable method when the composition of the thermocouples, its physical size, its location on the package, and the method of its attachment are defined. The method of measurement can be standardized and provides an accurate, inexpensive method for the applications engineer or the reliability engineer to determine a reference temperature to which the temperature rise across the package path, $(k_i\theta_{JC_1})P_D$, can be applied in order to determine a true T_J.

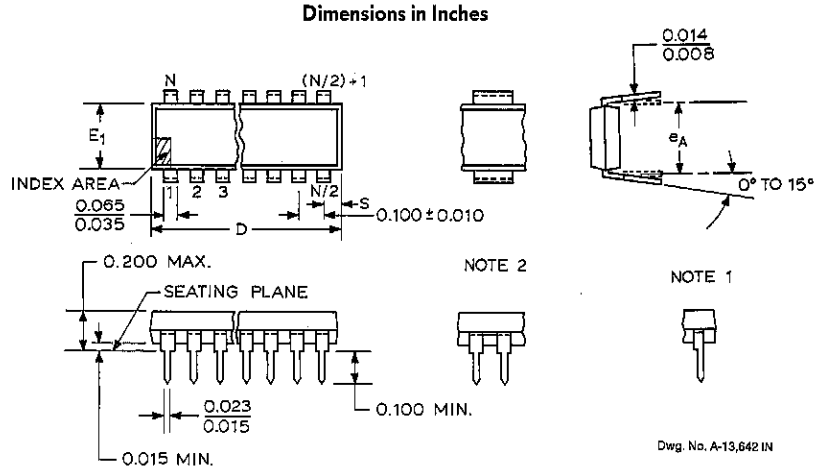
REFERENCES

1. S. Glasstone, *Textbook of Physical Chemistry,* 2nd Edition, D. Van Nostrand Co. Inc., New York, 1946
2. P. E. Roughan, *Thermal Resistance of Integrated Circuit Packages,* Technical Paper TP72-7, Sprague Electric Co., 1972
3. F. R. Dewey and P. R. Emerald, *Computing IC Temperature Rise,* Machine Design, pp 98-101, June 1977
4. C. A. Lidback, *Scanning I. R. Microscopy Techniques for Semiconductor Thermal Analysis.* 17th Annual Proceedings Reliability Physics 1979 IEEE Catalog No. 79CH1425-8 Phy.

PLASTIC DIP

SPRAGUE PACKAGE DESIGNATOR A, B, OR M

Dimensions in Inches



N	Leads Pkg. Designator	8 B	8 M	14 A	16 A	16 B	18 A
D	Body Length	0.360/0.390	0.360/0.390	0.735/0.785	0.735/0.785	0.735/0/785	0.885/0.915
E_1	Body Width	0.240/0.260	0.240/0.260	0.240/0.260	0.240/0.260	0.240/0.260	0.240/0.260
e_A	Row Spacing	0.300 BSC	0.300 BSC	0.300 BSC	0.300 BSC	0.300 BSC	0.300 BSC
S	Lead CL to End	0.040 REF	0.040 REF	0.075 REF	0.025 REF	0.025 REF	0.050 REF
Notes	(Leads Affected)	1 (1, 4, 5, 8) 2 (2, 3, 6, 7)	1 (1, 4, 5, 8) —	— —	1 (1, 8, 9, 16) —	1 (1, 8, 9, 16) 2 (4, 5, 12, 13)	— —

N	Leads Pkg. Designator	20 A	22 A	22 B	28 A	40 A
D	Body Length	0.990/1.040	1.050/1.120	1.050/1.120	1.380/1.460	1.980/2.060
E_1	Body Width	0.240/0.260	0.300/0.390	0.300/0.390	0.480/0.560	0.480/0.560
e_A	Row Spacing	0.300 BSC	0.400 BSC	0.400 BSC	0.600 BSC	0.600 BSC
S	Lead CL to End	0.060 REF	0.050 REF	0.050 REF	0.075 REF	0.075 REF
Notes	(Leads Affected)	— —	— —	2 (5, 6, 17, 18) —	— —	— —

NOTES:

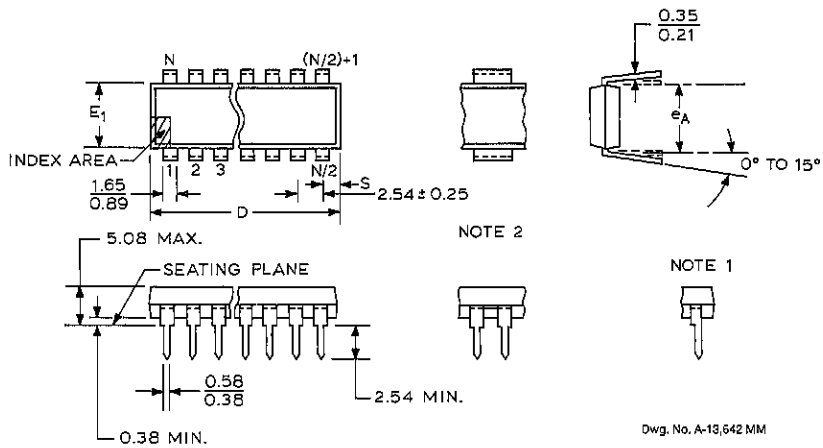
1. Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC DIP

SPRAGUE PACKAGE DESIGNATOR A, B, OR M

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,642 MM

N	Leads Pkg. Designator	8 B	8 M	14 A	16 A	16 B	18 A
D	Body Length	9.14/9.91	9.14/9.91	18.67/19.93	18.67/19.93	18.67/19.93	22.48/23.24
E_1	Body Width	6.10/6.60	6.10/6.60	6.10/6.60	6.10/6.60	6.10/6.60	6.10/6.60
e_A	Row Spacing	7.62 BSC	7.62 BSC	7.62 BSC	7.62 BSC	7.62 BSC	7.62 BSC
S	Lead CL to End	1.02 REF	1.02 REF	1.90 REF	0.64 REF	0.64 REF	1.27 REF
Notes	(Leads Affected)	1 (1, 4, 5, 8) 2 (2, 3, 6, 7)	1 (1, 4, 5, 8) —	— —	1 (1, 8, 9, 16) —	1 (1, 8, 9, 16) 2 (4, 5, 12, 13)	— —

N	Leads Pkg. Designator	20 A	22 A	22 B	28 A	40 A
D	Body Length	25.15/26.42	26.67/28.45	26.67/28.45	35.05/37.08	50.29/52.32
E_1	Body Width	6.10/6.60	7.62/9.91	7.62/9.91	12.19/14.22	12.19/14.22
e_A	Row Spacing	7.62 BSC	10.16 BSC	10.16 BSC	15.24 BSC	15.24 BSC
S	Lead CL to End	1.52 REF	1.27 REF	1.27 REF	1.90 REF	1.90 REF
Notes	(Leads Affected)	— —	— —	2 (5, 6, 17, 18) —	— —	— —

NOTES:
1. Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.

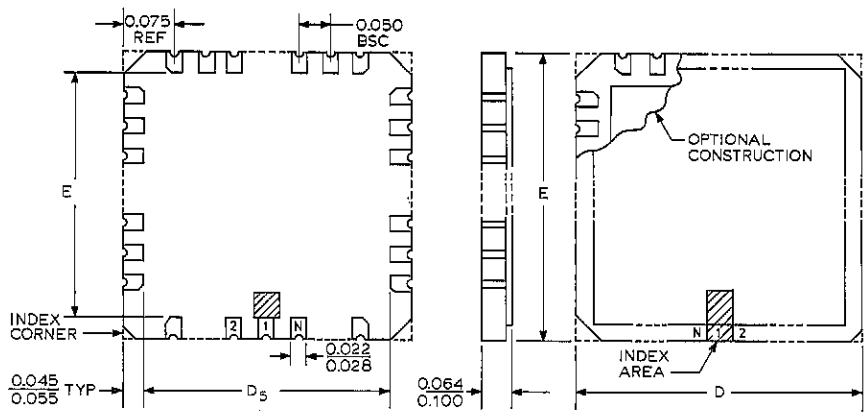
A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

8

CERAMIC LEADLESS CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EK OR EL

Dimensions in Inches



Dwg. No. A 14,156

N	Leads Pkg. Designator	18 EL	20 EK	24 EK	28 EK	32 EL	44 EK
N_D	Leads per Side	4	5	6	7	7	11
N_E	Leads per Side	5	5	6	7	9	11
D	Overall Length	0.280/0.290	0.342/0.358	0.395/0.410	0.442/0.460	0.442/0.458	0.640/0.662
D_S	Contact Spacing	0.185 REF	0.250 REF	0.300 REF	0.350 REF	0.350 REF	0.550 REF
E	Overall Width	0.345/0.365	0.342/0.358	0.395/0.410	0.442/0.460	0.540/0.560	0.640/0.662
E_S	Contact Spacing	0.250 REF	0.250 REF	0.300 REF	0.350 REF	0.450 REF	0.550 REF
M38510F Case Outline		C-9	C-2	C-3	C-4	C-12	C-5

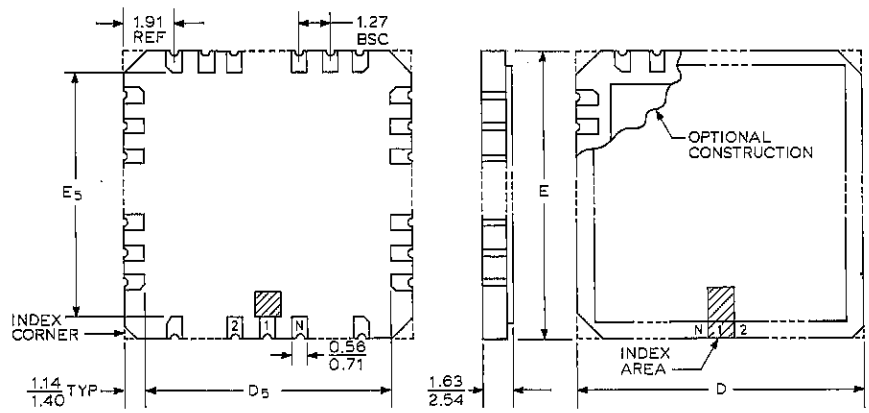
NOTE: Index is centered on D side. Corner shape (square, notch, radius) optional.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane..

CERAMIC LEADLESS CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EK OR EL

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-14,157

N	Leads / Pkg. Designator	18 EL	20 EK	24 EK	28 EK	32 EL	44 EK
N_D		4	5	6	7	7	11
N_E		5	5	6	7	9	11
D	Overall Length	7.11/7.37	8.69/9.09	10.03/10.41	11.23/11.68	11.23/11.63	16.26/16.81
D_5	Contact Spacing	4.70 REF	6.35 REF	7.62 REF	8.89 REF	8.90 REF	13.97 REF
E	Overall Width	8.76/9.27	8.69/9.09	10.03/10.41	11.23/11.68	13.72/14.22	16.26/16.81
E_5	Contact Spacing	6.35 REF	6.35 REF	7.62 REF	8.89 REF	11.43 REF	13.97 REF
M38510F Case Outline		C-9	C-2	C-3	C-4	C-12	C-5

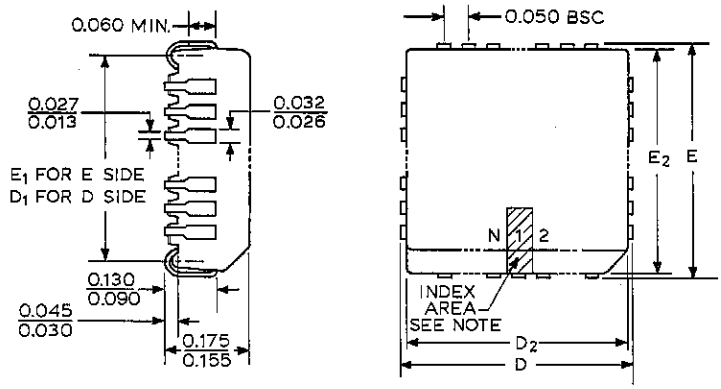
NOTE: Index is centered on D side. Corner shape (square, notch, radius) optional.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC LEADED CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EP

Dimensions in Inches



Dwg. No. A-13,644 IN

N	Leads Pkg. Designator	20 EP	24 EP	28 EP	44 EP
N_D	Leads per Side	5	6	7	11
N_E	Leads per Side	5	6	7	11
D	Overall Length	0.385/0.395	0.370/0.410	0.470/0.510	0.670/0.710
D_1	Row Spacing	0.290/0.330	0.332 REF	0.390/0.430	0.590/0.630
D_2	Body Length	0.350/0.356	0.360/0.380	0.440/0.460	0.640/0.660
E	Overall Width	0.385/0.395	0.370/0.410	0.470/0.510	0.670/0.710
E_1	Row Spacing	0.290/0.330	0.332 REF	0.390/0.430	0.590/0.630
E_2	Body Width	0.350/0.356	0.360/0.380	0.440/0.460	0.640/0.660
JEDEC Designation		MO-047AA	MS-006AA	MS-007AA	MS-007AB

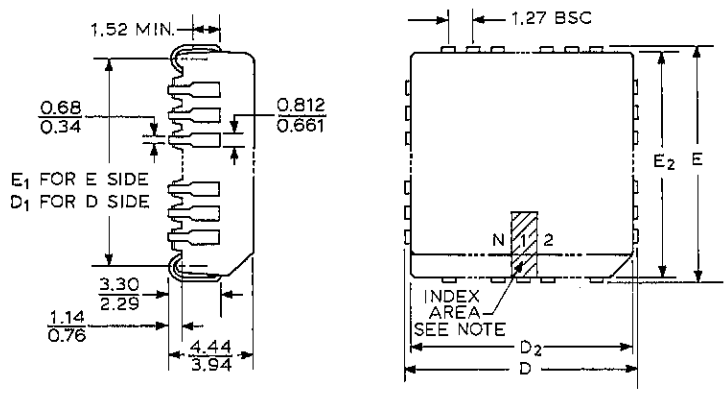
NOTE: Index is centered on "D" side.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC LEADED CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EP

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,644 MM

N	Leads Pkg. Designator	20 EP	24 EP	28 EP	44 EP
N_D	Leads per Side	5	6	7	11
N_E	Leads per Side	5	6	7	11
D	Overall Length	9.78/10.03	9.40/10.41	11.94/12.95	17.02/18.03
D_1	Row Spacing	7.37/8.38	8.43 REF	9.91/10.92	15.00/16.00
D_2	Body Length	8.89/9.042	9.15/9.65	11.18/11.68	16.26/16.76
E	Overall Width	9.78/10.03	9.40/10.41	11.94/12.95	17.02/18.03
E_1	Row Spacing	7.37/8.38	8.43 REF	9.91/10.92	15.00/16.00
E_2	Body Width	8.89/9.042	9.15/9.65	11.18/11.68	16.26/16.76
JEDEC Designation		MO-047AA	MS-006AA	MS-007AA	MS-007AB

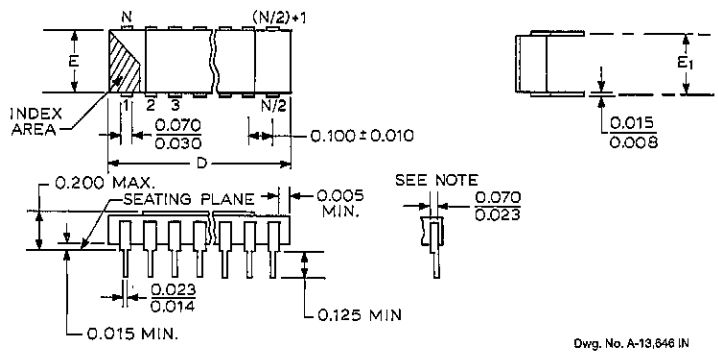
NOTE: Index is centered on "D" side.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

HERMETIC DIP

SPRAGUE PACKAGE DESIGNATOR H

Dimensions in Inches



Dwg. No. A-13,646 IN

N	Leads Pkg. Designator	8 H	14 H	16 H	18 H	22 H
D	Body Length	0.528 Max.	0.785 Max.	0.840 Max.	0.960 Max.	1.260 Max.
E	Body Width	0.220/0.310	0.220/0.310	0.220/0.310	0.220/0.310	0.350/0.390
E_1	Row Spacing	0.290/0.320	0.290/0.320	0.290/0.320	0.290/0.320	0.390/0.420
Notes	(Leads Affected)	—	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		—	D-1 Configuration 3	D-2 Configuration 3	D-6 Configuration 3	D-7 Configuration 3

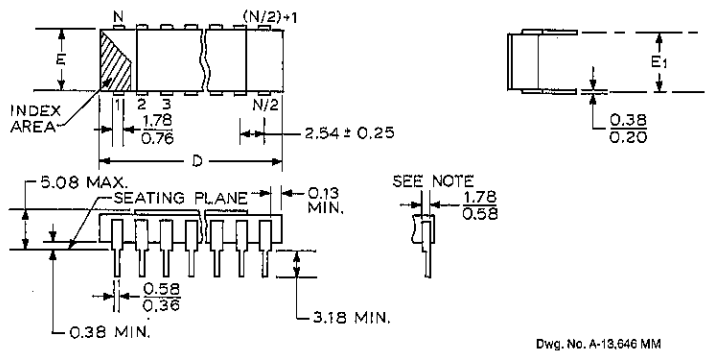
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

HERMETIC DIP

SPRAGUE PACKAGE DESIGNATOR H

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,646 MM

N	Leads Pkg. Designator	8 H	14 H	16 H	18 H	22 H
D	Body Length	13.41 Max.	19.94 Max.	21.34 Max.	24.38 Max.	32.00 Max.
E	Body Width	5.59/7.87	5.59/7.87	5.59/7.87	5.59/7.87	8.89/9.91
E_1	Row Spacing	7.37/8.13	7.37/8.13	7.37/8.13	7.37/8.13	9.91/10.67
Notes	(Leads Affected)	—	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		—	D-1 Configuration 3	D-2 Configuration 3	D-6 Configuration 3	D-7 Configuration 3

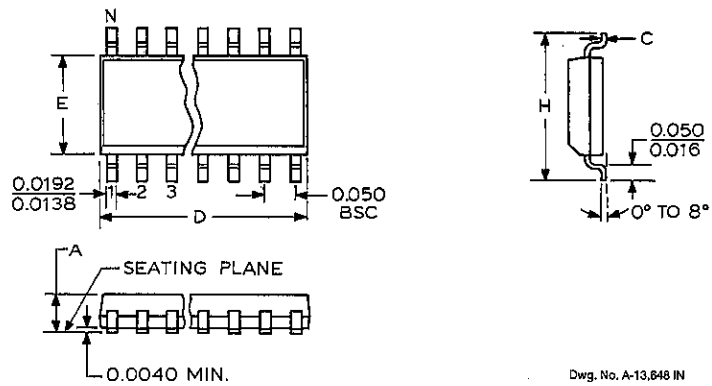
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC SOIC

SPRAGUE PACKAGE DESIGNATOR L, LB, OR LW

Dimensions in Inches
(Based on 1 mm = 0.03937")



Dwg. No. A-13,648 IN

N	Leads Pkg. Designator	8 L	14 L	16 L	16 LW	18 LW
A	Seated Height	0.0532/0.0688	0.0532/0.0688	0.0532/0.0688	0.0926/0.1043	0.0926/0.1043
C	Lead Thickness	0.0075/0.0098	0.0075/0.0098	0.0075/0.0098	0.0091/0.0125	0.0091/0.0125
D	Body Length	0.1890/0.1968	0.3367/0.3444	0.3859/0.3937	0.3977/0.4133	0.4469/0.4625
E	Body Width	0.1497/0.1574	0.1497/0.1574	0.1497/0.1574	0.2914/0.2992	0.2914/0.2992
H	Overall Width	0.2284/0.2440	0.2284/0.2440	0.2284/0.2440	0.394/0.419	0.394/0.419
Notes	(Leads Affected)	—	—	—	—	—
JEDEC Designation		MS-012AA	MS-012AB	MS-012AC	MS-013AA	MS-013AB

N	Leads Pkg. Designator	20 LB	20 LW
A	Seated Height	0.0926/0.1043	0.0926/0.1043
C	Lead Thickness	0.0091/0.0125	0.0091/0.0125
D	Body Length	0.4961/0.5118	0.4961/0.5118
E	Body Width	0.2914/0.2992	0.2914/0.2992
H	Overall Width	0.394/0.419	0.394/0.419
Notes	(Leads Affected)	(4-7, 14-17)	—
JEDEC Designation		MS-013AC	MS-013AC

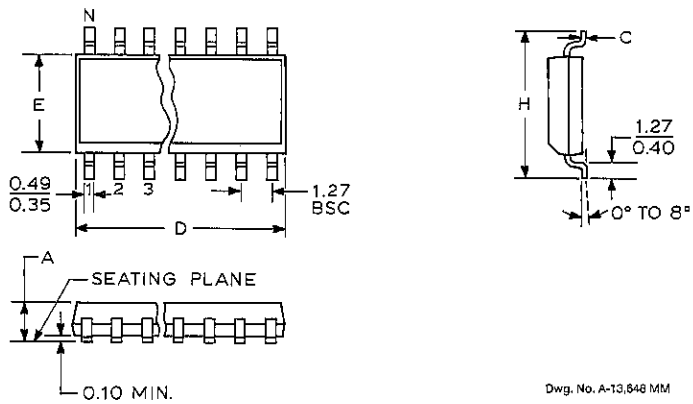
NOTE: Webbed lead frame. Leads indicated are internally one piece.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC SOIC

SPRAGUE PACKAGE DESIGNATOR L, LB, OR LW

Dimensions in Millimeters



Dwg. No. A-13,648 MM

N	Leads Pkg. Designator	8 L	14 L	16 L	16 LW	18 LW
A	Seated Height	1.35/1.75	1.35/1.75	1.35/1.75	2.35/2.65	2.35/2.65
C	Lead Thickness	0.19/0.25	0.19/0.25	0.19/0.25	0.23/0.32	0.23/0.32
D	Body Length	4.80/5.00	8.55/8.75	9.80/10.0	10.10/10.50	11.35/11.75
E	Body Width	3.80/4.00	3.80/4.00	3.80/4.00	7.40/7.60	7.40/7.60
H	Overall Width	5.80/6.20	5.80/6.20	5.80/6.20	10.0/10.65	10.0/10.65
Notes	(Leads Affected)	—	—	—	—	—
JEDEC Designation		MS-012AA	MS-012AB	MS-012AC	MS-013AA	MS-013AB

N	Leads Pkg. Designator	20 LB	20 LW
A	Seated Height	2.35/2.65	2.35/2.65
C	Lead Thickness	0.23/0.32	0.23/0.32
D	Body Length	12.60/13.00	12.60/13.00
E	Body Width	7.40/7.60	7.40/7.60
H	Overall Width	10.0/10.65	10.0/10.65
Notes	(Leads Affected)	(4-7, 14-17)	—
JEDEC Designation		MS-013AC	MS-013AC

NOTE: Webbed lead frame. Leads indicated are internally one piece.

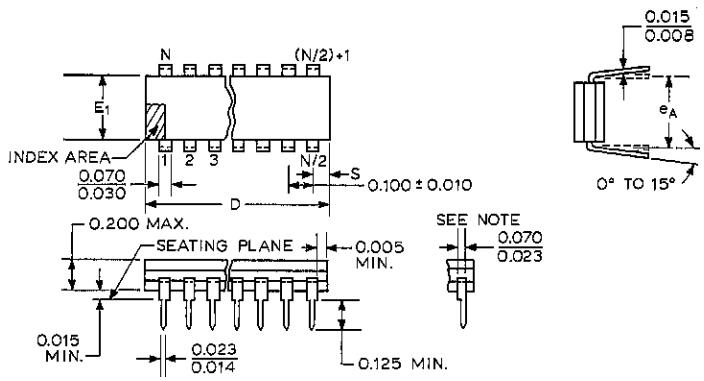
A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

8

HERMETIC CERDIP

SPRAGUE PACKAGE DESIGNATOR R

Dimensions in Inches



Dwg. No. A-13,650 IN

N	Leads Pkg. Designation	14 R	16 R	18 R	22 R
D	Body Length	0.785 Max.	0.840 Max.	0.960 Max.	1.260 Max.
E_1	Body Width	0.220/0.310	0.220/0.310	0.220/0.310	0.350/0.390
e_A	Row Spacing	0.300 BSC	0.300 BSC	0.300 BSC	0.400 BSC
S	Lead CL to End	0.075 Ref.	0.025 Ref.	0.050 Ref.	0.025 Ref.
Notes	(Leads Affected)	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		D-1 Configuration 1	D-2 Configuration 1	D-6 Configuration 1	D-7 Configuration 1

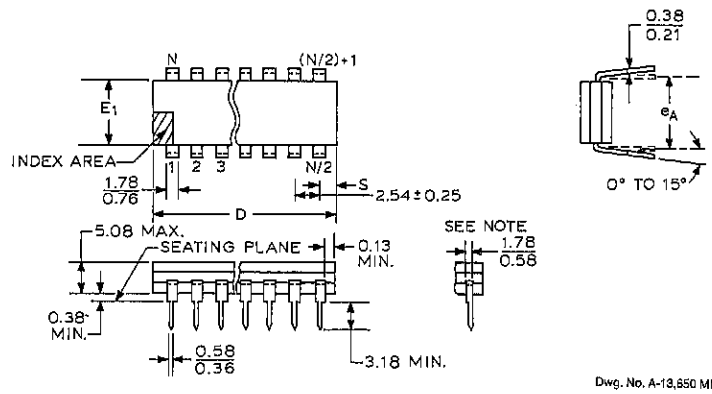
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/—— are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

HERMETIC CERDIP

SPRAGUE PACKAGE DESIGNATOR R

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,650 MM

N	Leads Pkg. Designation	14 R	16 R	18 R	22 R
D	Body Length	19.94 Max.	21.34 Max.	24.38 Max.	32.00 Max.
E_1	Body Width	5.59/7.87	5.59/7.87	5.59/7.87	8.89/9.91
e_A	Row Spacing	7.62 BSC	7.62 BSC	7.62 BSC	10.16 BSC
S	Lead Cl. to End	1.91 REF	0.64 REF	1.27 REF	1.27 REF
Notes	(Leads Affected)	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		D-1 Configuration 1	D-2 Configuration 1	D-6 Configuration 1	D-7 Configuration 1

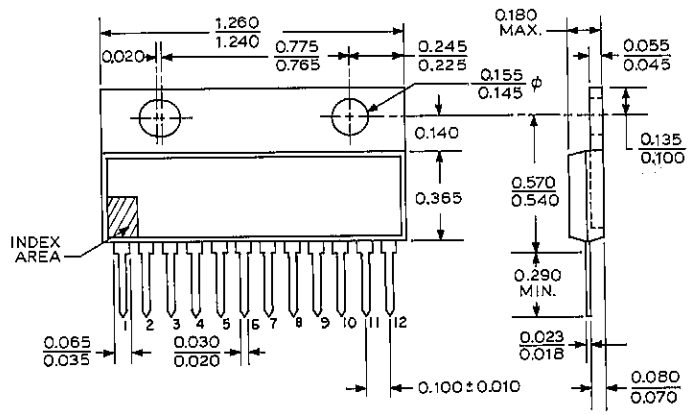
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall.also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR W

Dimensions in Inches



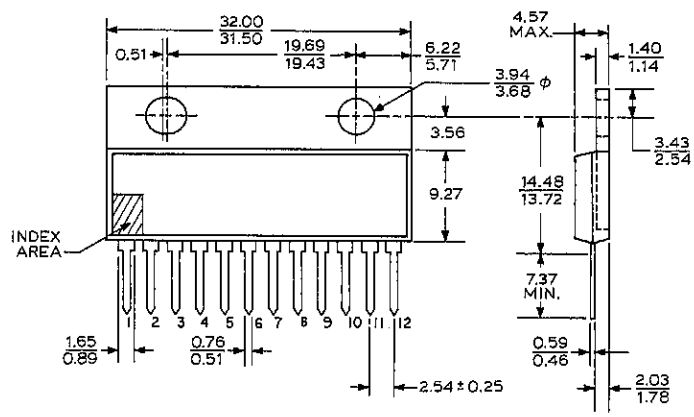
Dwg. No. A-13,652 IN

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR W

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,652 MM

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

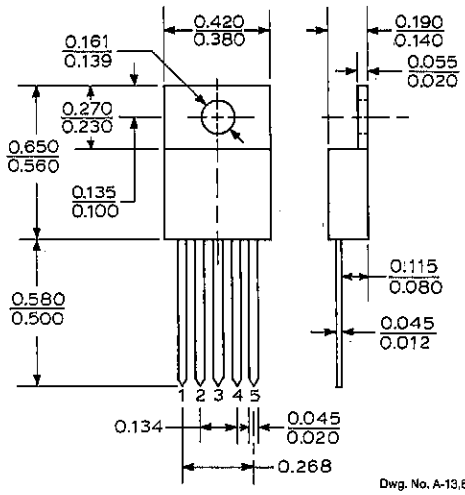
8

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR Z, ZH OR ZV

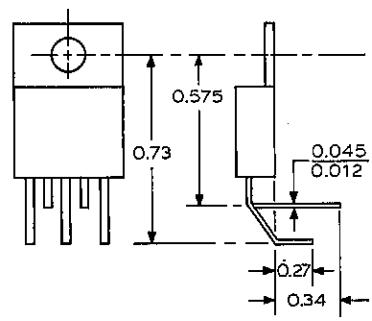
Dimensions in Inches

DESIGNATOR Z
(JEDEC Designation TO-220AB)



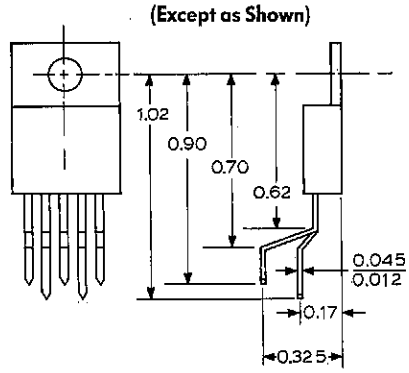
Dwg. No. A-13,654 IN

DESIGNATOR ZH
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,655 IN

DESIGNATOR ZV
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,656 IN

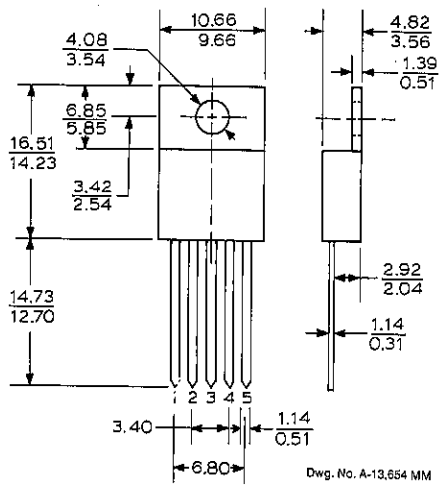
A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR Z, ZH OR ZV

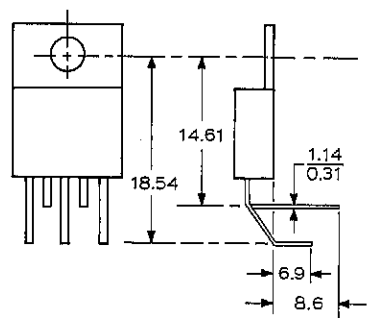
Dimensions in Millimeters
(Based on 1" = 25.40 mm)

DESIGNATOR Z
(JEDEC Designation TO-220AB)



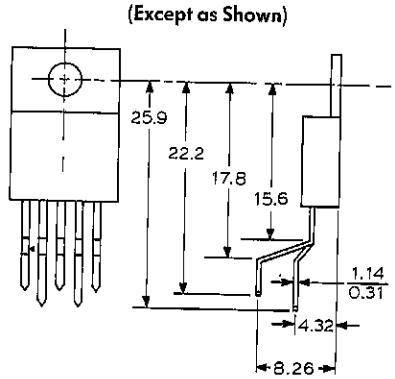
Dwg. No. A-13,654 MM

DESIGNATOR ZH
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,655 MM

DESIGNATOR ZV
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,656 MM

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.