Power Management Switch IC Series for PCs and Digital Consumer Product

1ch Small Current Output Power Managment Switch IC

BD6524HFV

No.09029EAT13

●Description

Power switch for memory card Slot (BD6524HFV) is a high side switch IC having one circuit of N-channel Power MOS FET. The switch realizes 200mΩ (Typ.) ON resistance. Operations from low input voltage (VIN ≥ 3.0V) can be made for use for various switch applications.
The switch turns on slowly by the built-in charge pump, therefore, it is possible to reduce inrush current at switch on. There is no parasitic diode between the drain and the source, reverse current flow at switch off is prevented. Further, it has a discharge circuit that discharges electric charge from capacitive load at switch off.
The BD6524HFV is available in a space-saving HVSOF6 package.

●Features

1) Low on resistance (200mΩ, Typ.) N-MOS switch built in
2) Maximum output current : 500mA
3) Soft start circuit
4) Under voltage lockout (UVLO) circuit
5) Discharge circuit built in : operations at switch off, UVLO
6) Reverse current flow blocking at switch off

●Applications

Memory card slots of notebook PC, digital still camera, portable music player, compact portable devices such as PDA and so forth

●Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	-0.3 to 6.0	V
Control input voltage	V_{EN}	-0.3 to V_{IN} + 0.3	V
Switch output voltage	V_{OUT}	-0.3 to 6.0	V
Storage temperature	T_{STG}	-55 to 150	℃
Power dissipation	Pd	510 *1	mW

*1 Derating : 4.08mW/℃ for operation above Ta = 25℃.
* This product is not designed for protection against radioactive rays.
* Operation is not guaranteed.

●Operation conditions

Parameter	Symbol	Limit	Unit
Supply voltage	V_{IN}	3.0 to 5.5	V
Operating Temperature	T_{OPR}	-25 to 75	℃
Switch current	I_{OUT}	500	mA

●Electrical characteristics

Unless otherwise specified, Ta = 25℃, V_{IN} = 5V,

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating current	I_{DD}	-	50	75	μA	V_{EN} = 5V, VOUT = Open
Standby current	I_{STB}	-	0.1	1	μA	V_{EN} = 0V, VOUT = Open
EN input voltage	V_{ENH}	-	-	2.5	V	High level input voltage
	V_{ENL}	0.7	-	-	V	Low level input voltage
EN input leak current	I_{EN}	-1	0.01	1	μA	
Switch on resistance	R_{ON}	-	200	255	mΩ	V_{IN} = 5V
		-	250	335	mΩ	V_{IN} = 3.3V
Switch leak current	I_{LEAK}	-	-	10	μA	At switch OFF
Switch rise time	T_{ON1}	-	0.4	0.8	ms	RL=10Ω. Refer to the timing diagram in Fig. 2.
Switch rise delay time	T_{ON2}	-	0.5	1.0	ms	RL=10Ω. Refer to the timing diagram in Fig. 2.
Switch fall time	T_{OFF1}	-	1	2	us	RL=10Ω. Refer to the timing diagram in Fig. 2.
Switch fall delay time	T_{OFF2}	-	2	4	us	RL=10Ω. Refer to the timing diagram in Fig. 2.
UVLO threshold voltage	V_{UVLO}	1.9	2.2	2.5	V	V_{IN} increasing
		1.8	2.1	2.4	V	V_{IN} decreasing
Discharge resistance	R_{DISC}	-	200	350	Ω	V_{EN} = 0V, I_L = 1mA
Discharge current	I_{DISC}	0.8	1.8	-	mA	V_{EN} = 0V,V_{IN} = V_{OUT} = 1.8V

●Measurement circuit

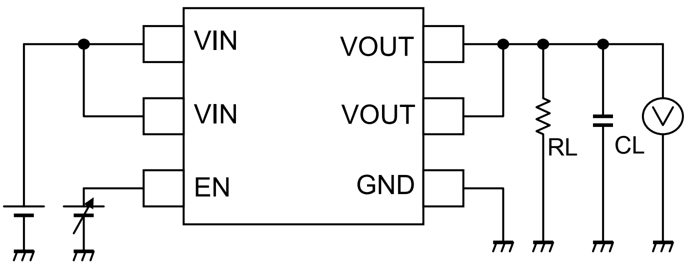


Fig.1 Measurement circuit

●Timing diagram

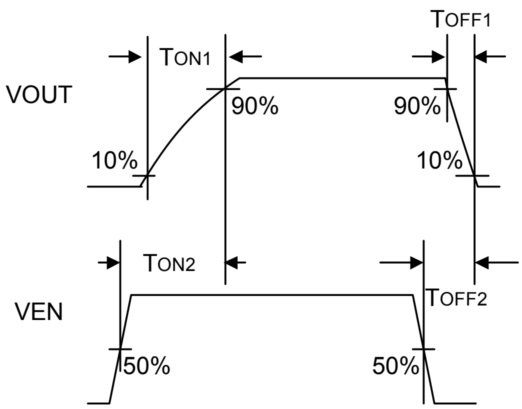


Fig.2 Timing diagram

●Typical characteristics

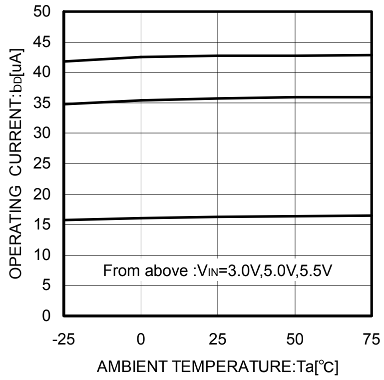


Fig.3 Operating current

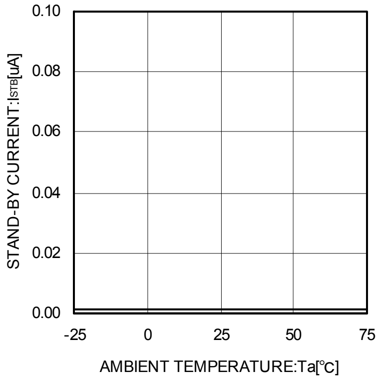


Fig.4 Standby current

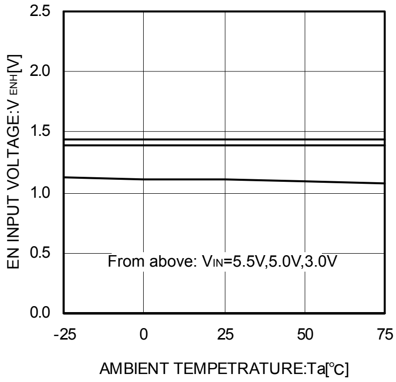


Fig.5 EN threshold voltage (High level input voltage)

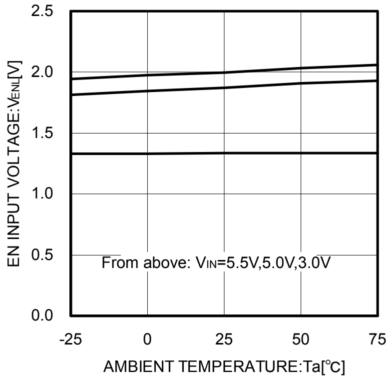


Fig.6 EN threshold voltage (Low level input voltage)

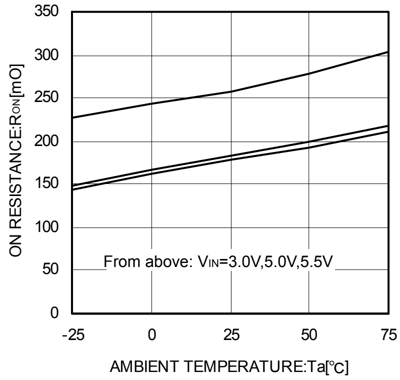


Fig.7 Switch on resistance

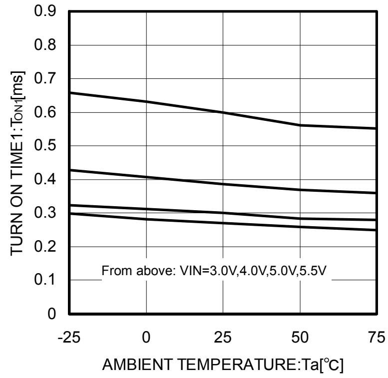


Fig.8 Switch rise time

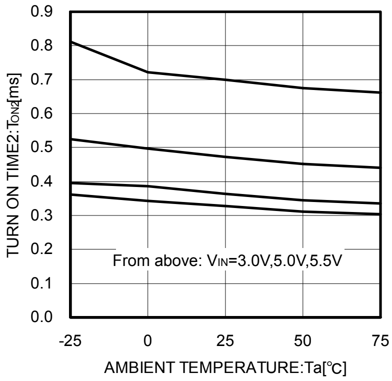


Fig.9 Switch rise delay time

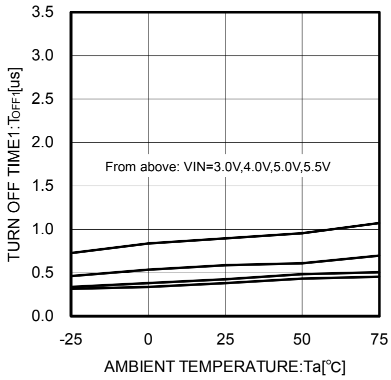


Fig.10 Switch fall time

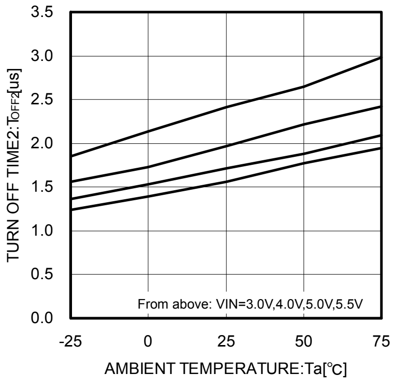


Fig.11 Switch fall delay time

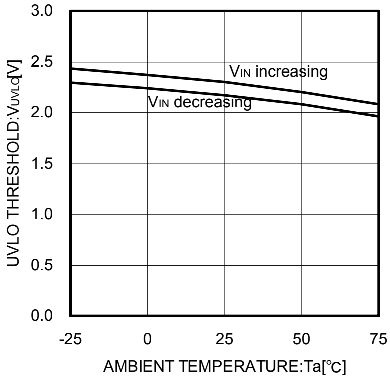


Fig.12 UVLO threshold voltage

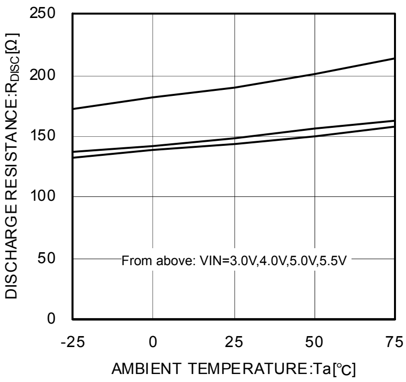


Fig.13 Discharge resistance

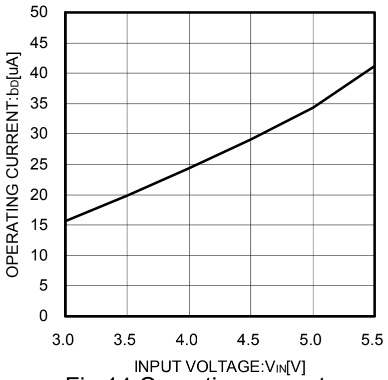


Fig.14 Operating current

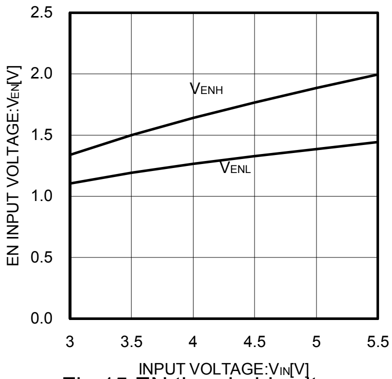


Fig.15 EN threshold voltage

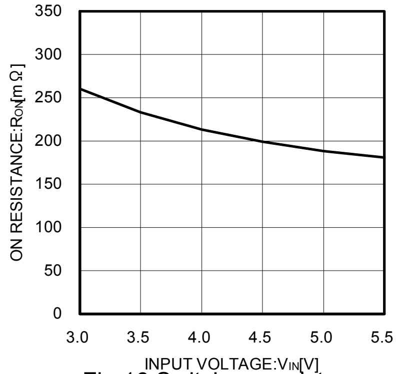


Fig.16 Switch on resistance

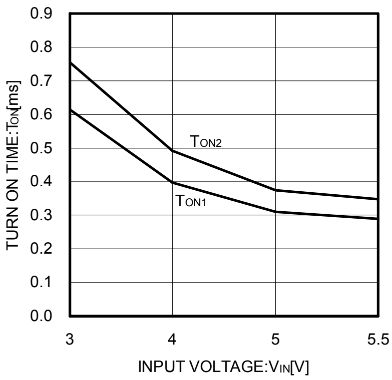


Fig.17 Switch rise time

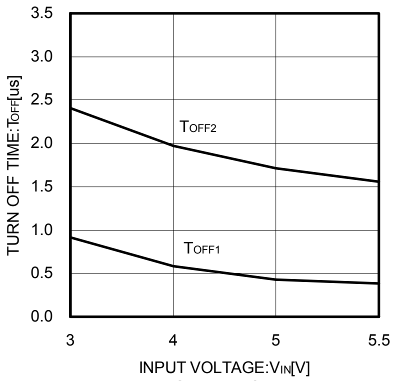


Fig.18 Switch fall time

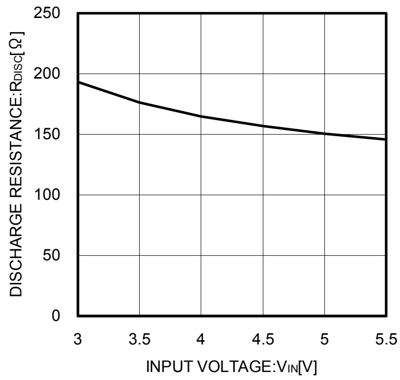


Fig.19 Discharge resistance

●Waveform data

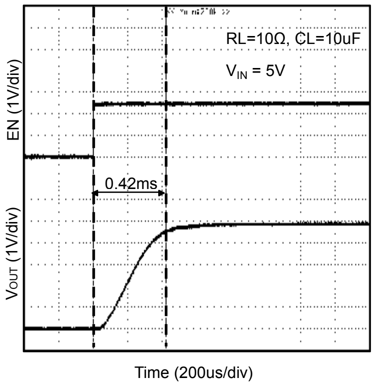


Fig.20 Switch rise time

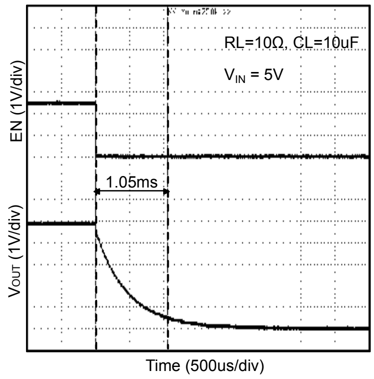


Fig.21 Switch fall time

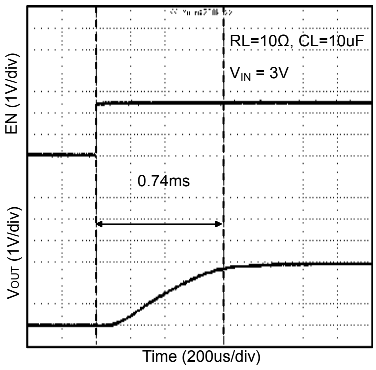


Fig.22 Switch rise time

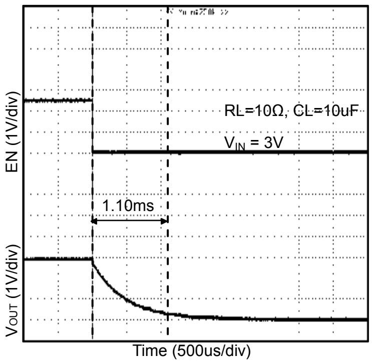


Fig.23 Switch fall time

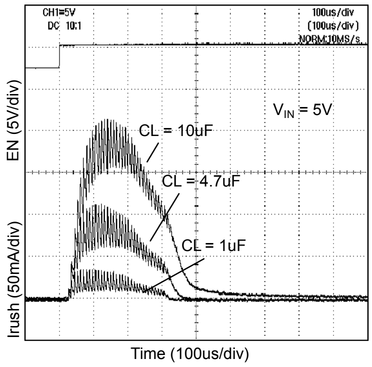


Fig.24 Inrush current

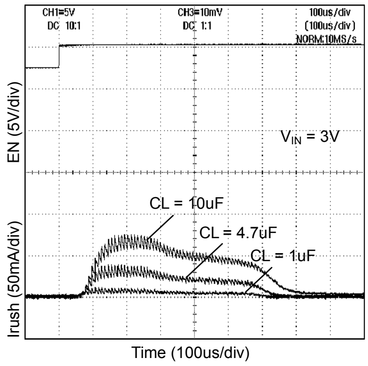


Fig.25 Inrush current

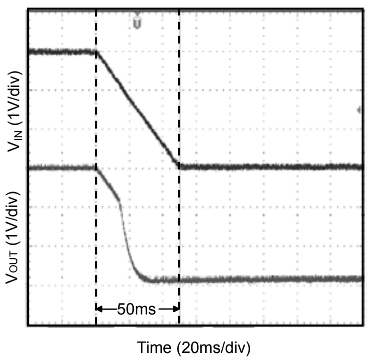


Fig.26 UVLO
CL = 10uF

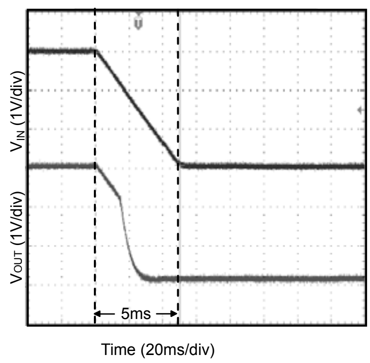


Fig.27 UVLO
CL = 1uF

● **Block diagram**

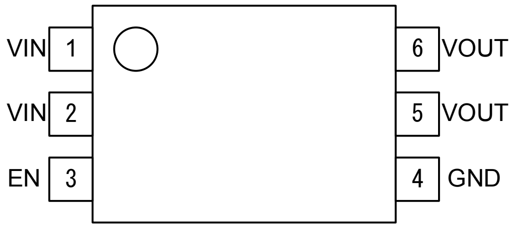


Fig.28 Pin configuration

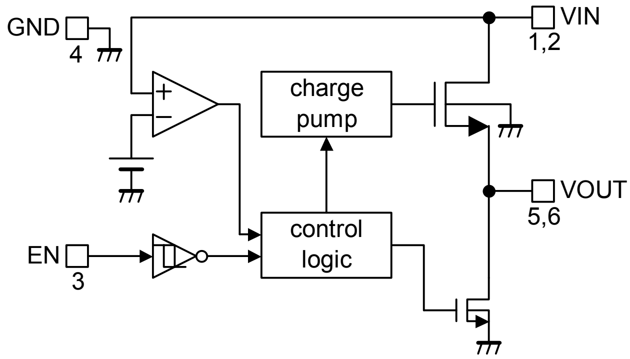


Fig.29 Block diagram

● **Pin description**

Pin No.	Symbol	Pin Function
1	VIN	Switch input pin. At use, connect each pin outside.
2		
3	EN	Switch control input pin (hysteresis input) Switch ON at High.
4	GND	Ground
5	VOUT	Switch output pin At use, connect each pin outside.
6		

● **I/O circuit**

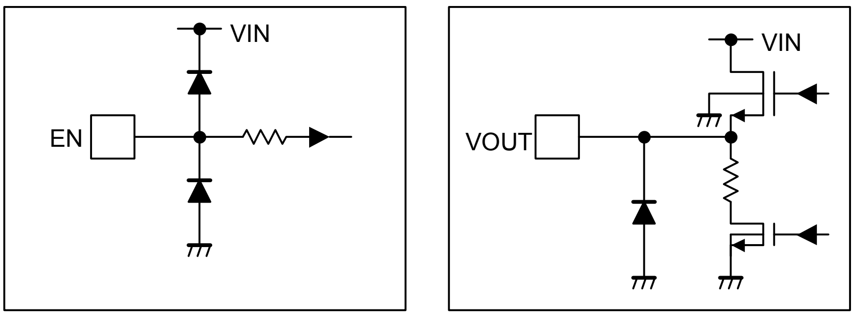


Fig.30 I/O circuit

●Functional description

1. Input / output

VIN pin and VOUT pin are connected to the drain and the source of N-MOS switch respectively. And the VIN pin is used also as power source input to internal control circuit.

When EN input is set to High level and the switch is turned on, VIN pin and VOUT pin are connected by a 200mΩ switch. In a normal condition, current flows from VIN to VOUT. If voltage of VOUT is higher than VIN, current flows from VOUT to VIN, since the switch is bidirectional. There is not a parasitic diode between the drain and the source, it is possible to prevent current from flowing reversely from VOUT pin to VIN pin when the switch is disabled.

2. Discharge circuit

When the switch between the VIN and the VOUT is OFF, the 200Ω(Typ.) discharge switch between VOUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged.

3. Under voltage lockout (UVLO)

The UVLO circuit monitors the voltage of the VIN pin, when the EN input is active. UVLO circuit prevents the switch from turning on until the V_{IN} exceeds 2.2V(Typ.). If the VIN drops below 2.1V(Typ.) while the switch turns on, then UVLO shuts off the switch.

While the switch between the VIN pin and VOUT pin is OFF owing to UVLO operations, the switch of the discharge circuit turns on. However, when the voltage of VIN declines extremely, then the VOUT pin becomes Hi-Z.

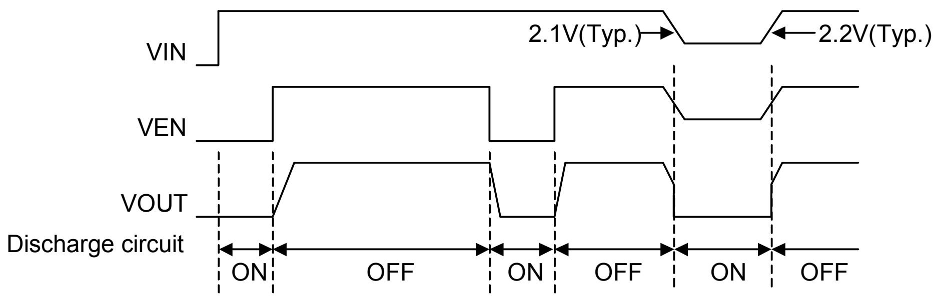


Fig.31 Operation timing

●Typical application circuit

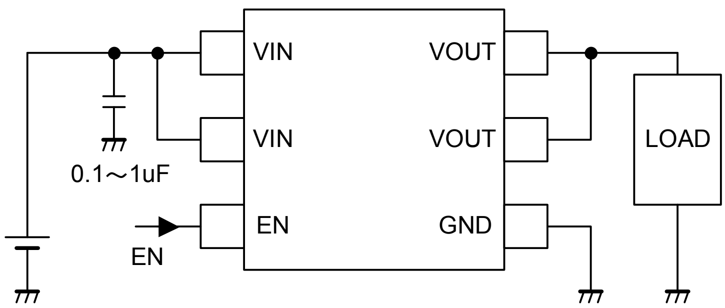


Fig.32 Typical application circuit

●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

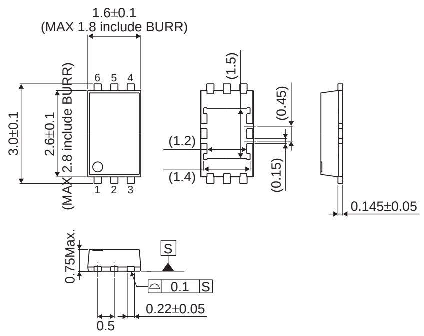
(12) Thermal design
Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

● Ordering part number

B	D		6	5	2	4		H	F	V	-	T	R

- Part No. (BD)
- Part No. 6524
- Package HFV: HVSOF6
- Packaging and forming specification TR: Embossed tape and reel (HVSOF6)

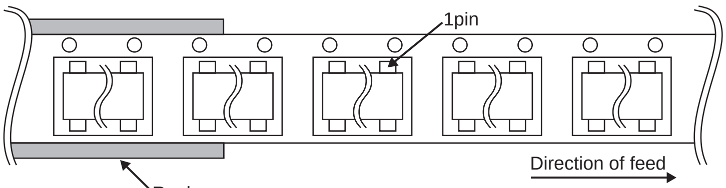
HVSOF6



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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