ROHM

STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT SERIES	1ch Piezo Driver built-in 15MHz Oscillator
TYPE	**BH6456GUL**
FEATURES	· Built-in 15MHz Oscillator
	· Built in 1ch H Bridge Driver
	· 2-wire serial interface (I2C-compatible)

●Absolute maximum ratings (Ta=+25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage	VCC	-0.3 to +4.5	V
Motor power supply voltage	VM	-0.3 to +5.5	V
Power save input voltage	VPS	-0.3 to VCC+0.3	V
Control input voltage	VIN	-0.3 to VCC+0.3	V
Power dissipation	Pd	530[*1]	mW
Operating temperature range	Topr	-25 to +85	°C
Junction temperature	Tjmax	+125	°C
Storage temperature range	Tstg	-55 to +125	°C
H-bridge output current	Iout	-500 to +500[*2]	mA

[*1]Conditions: mounted on a glass epoxy board (50mm × 58mm × 1.75mm; 8 layers).   In case of Ta>25°C, reduced by 5.3 mW/°C.
[*2]Must not exceed Pd, ASO, or Tjmax of 125°C.

●Operating Conditions (Ta= -25°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	2.3	3.0	3.6	V
Motor power supply voltage	VM	2.3	3.0	4.8	V
Power save input voltage	VPS	0	-	VCC	V
Control input voltage	VIN	0	-	VCC	V
2-wire serial interface transmission rate	SCL	-	-	400	kHz
H-bridge output current	Iout	-	-	±400[*3]	mA

[*3]Must not exceed Pd, ASO.

This product is not designed for protection against radioactive rays.
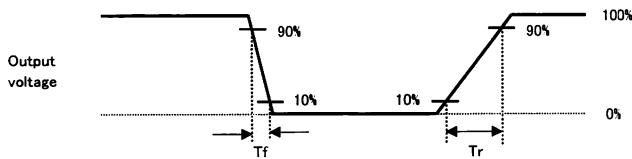Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

REV. A

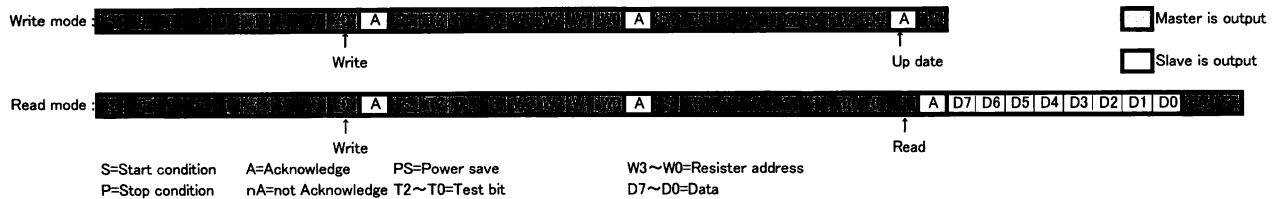○Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=VM=3.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current during standby operation	ICCST	-	0	1	μA	PS=L
Circuit current	ICC	-	3.2	6.4	mA	PS=H, SCL=400kHz, OSC active
UVLO						
UVLO voltage	VUVLO	1.8	-	2.2	V	
Power save input						
High level input voltage	VPSH	1.5	-	VCC	V	
Low level input voltage	VPSL	0	-	0.5	V	
High level input current	IPSH	15	30	60	μA	VINH=3.0V
Low level input current	IPSL	-3	0	-	μA	VINL=0V
Control input(SDA,SCL)						
High level input voltage	VINH	1.5	-	VCC	V	
Low level input voltage	VINL	0	-	0.5	V	
Low level output voltage	VOL	-	-	0.4	V	IIN=3.0mA (SDA)
High level input current	IINH	-10	-	10	μA	Input voltage=VCC
Low level input current	IINL	-10	-	10	μA	Input voltage=GND
H Bridge Drive						
Output ON-Resistance	RONP	-	0.7	1.0	Ω	
	RONN	-	0.7	1.0	Ω	
Cycle length of sequence drive	TMIN	10.35	10.67	11.00	μs	[*4] Built in CLK 160 count
Output rise time	Tr	-	0.1	0.8	μs	[*5] 7.5Ω load condition
Output fall time	Tf	-	0.02	0.4	μs	[*5] 7.5Ω load condition

[*4]   The time that 1 cycle of sequence drive at the below setting of 2-wire serial data
   ta[7:0]=8'h13, brake1[7:0]=8'h03, tb[7:0]=8'h1e, brake2[7:0]=8'h6b, osc[2:0]=3'h0

[*5]   Output switching wave

○2-wire serial interface specification (Fast mode : SCL=400kHz)

S=Start condition   A=Acknowledge   PS=Power save   W3~W0=Resister address
P=Stop condition   nA=not Acknowledge   T2~T0=Test bit   D7~D0=Data

REV. A

○Characteristics of the SDA and SCL bus lines for 2-wire serial interface.
(Unless otherwise specified, Ta=-25~+85°C, VCC=2.3~3.6V)

Parameter	Symbol	FAST-MODE[*6]			STANDARD-MODE[*6]			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	fSCL	-	-	400	-	-	100	kHz
High period of the SCL clock	tHIGH	0.6	-	-	4.0	-	-	μs
Low period of the SCL clock	tLOW	1.3	-	-	4.7	-	-	μs
Rise time of SDA signal	tR	-	-	0.3	-	-	1.0	μs
Fall time of SDA signal	tF	-	-	0.3	-	-	0.3	μs
Hold time (repeated) START condition	tHD:STA	0.6	-	-	4.0	-	-	μs
Set-up time (repeated) START condition	tSU:STA	0.6	-	-	4.7	-	-	μs
Data hold time	tHD:DAT	0	-	0.9	0	-	3.45	μs
Data set-up time	tSU:DAT	100	-	-	250	-	-	ns
Set-up time for STOP condition	tSU:STO	0.6	-	-	4.0	-	-	μs
Bus free time between a STOP and START condition	tBUF	1.3	-	-	4.7	-	-	μs
Pulse width of spikes which must be suppressed by the input filter	tI	0	-	50	0	-	50	ns

[*6] Standard-mode and Fast-mode 2-wire serial interface devices must be able to transmit or receive at that speed.

The maximum bit transfer rates of 100 kbit/s for Standard-mode devices and 400 kbit/s for Fast-mode devices

This transfer rates is provided the maximum transfer rates, for example it is able to drive 100 kbit/s of clocks with Fast-mode.

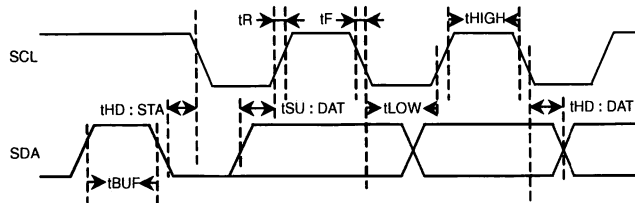○Definition of timing on the 2-wire serial interface
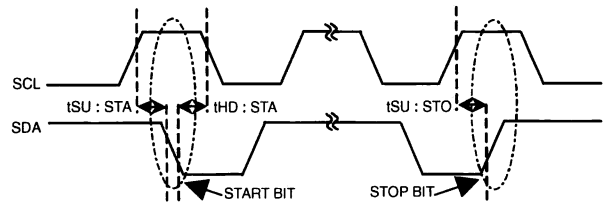

Fig.1 Definition of timing for serial data

Fig.2 Definition of timing for START and STOP bit
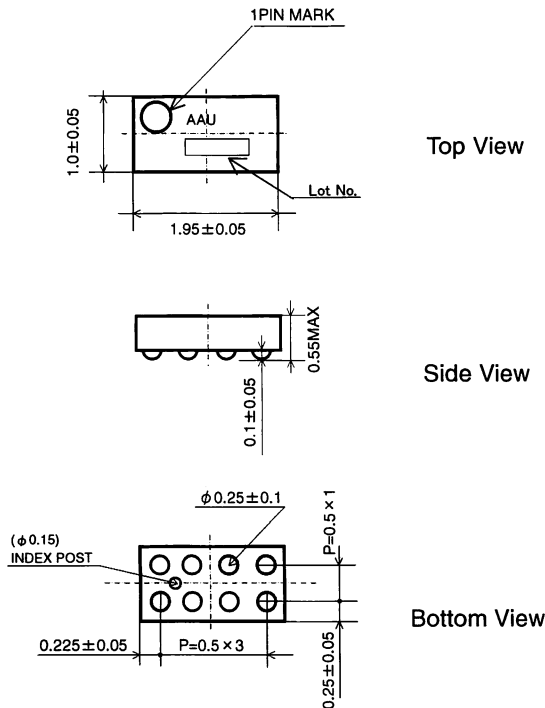
○Package outline

Top View

Side View

Bottom View

Fig3. VCSP50L1 Package (Unit;mm)

○Pin Arrangement (Top View)

	1	2	3	4
A	VM	OUTB	SCL	SDA
B	OUTA	GND	VCC	PS
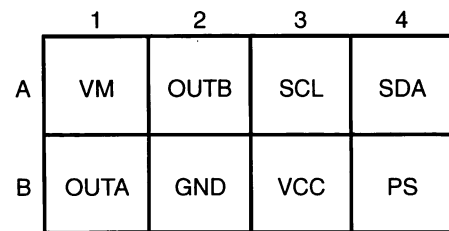
Fig4. BH6456GUL Pin Arrangement (Top View)

○Block Diagram
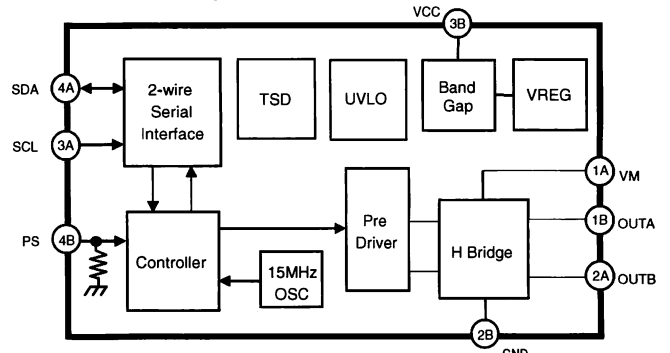
Fig5. BH6456GUL Block Diagram

REV. A

○Resister map

Address	W3	W2	W1	W0	D7	D6	D5	D4	D3	D2	D1	D0
0H	0	0	0	0	HiZE	initB[2]	initB[1]	InitB[0]	init	START	MODE	dir
1H	0	0	0	1	ta[7]	ta[6]	ta[5]	ta[4]	ta[3]	ta[2]	ta[1]	ta[0]
2H	0	0	1	0	brake1[7]	brake1[6]	brake1[5]	brake1[4]	brake1[3]	brake1[2]	brake1[1]	brake1[0]
3H	0	0	1	1	tb[7]	tb[6]	tb[5]	tb[4]	tb[3]	tb[2]	tb[1]	tb[0]
4H	0	1	0	0	brake2[7]	brake2[6]	brake2[5]	brake2[4]	brake2[3]	brake2[2]	brake2[1]	brake2[0]
5H	0	1	0	1	cnt[7]	cnt[6]	cnt[5]	cnt[4]	cnt[3]	cnt[2]	cnt[1]	cnt[0]
6H	0	1	1	0	cnt[15]	cnt[14]	cnt[13]	cnt[12]	cnt[11]	cnt[10]	cnt[9]	cnt[8]
7H	0	1	1	1	pa	pb	osc[2]	osc[1]	osc[0]	cntck[2]	cntck[1]	cntck[0]
8H	1	0	0	0	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST
9H	1	0	0	1	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST
AH	1	0	1	0	TEST	TEST	TEST	TEST	TEST	TEST	EXT	initEXT
BH	1	0	1	1	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST
CH	1	1	0	0	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST

* A low signal should be input to the TEST bit at all times

○Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the inductance of printed circuit board. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and ground pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a thermal shutdown circuit (TSD). If the temperature of the chip reaches the following temperature, the motor output will be opened. TSD is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD ON temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
150	20

(8) PS terminal

Release PS after rising VCC. PS works resetting logic as well. If keep connecting PS with VCC, resetting cannot be done cause misoperating or destroy

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